3D Design Activities at Fermilab – Opportunities for Physics

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*Operated by Fermi Research Alliance, LLC under contract No. DE-AC02-07CH11359

Abstract

Fermilab began exploring the technologies for vertically integrated circuits (also commonly known as 3D circuits) in 2006. These technologies include through silicon vias (TSV), circuit thinning, and bonding techniques to replace conventional bump bonds. Since then, the interest within the High Energy Physics community has grown considerably. This paper will present an overview of the activities at Fermilab over the last 3 years which have help spark this interest.

Keywords: vertical integration, 3D integration

1.0 Bonding technologies

Bonding along with precision alignment are critical components of 3D integration. Die to wafer bonding results in the highest circuit yield, while wafer to wafer bonding results in the lowest cost per mated circuit. Fermilab has worked with multiple vendors over the last 3 years. Copper tin eutectic bonding at RTI International and Direct Bond Interconnect at Ziptronix have been studied as replacements for conventional lead tin solder bumps. Oxide bonding at MIT Lincoln Laboratories and copper to copper bonding at Tezzaron have been studied for 3D circuit fabrication.

1.1 Bonding techniques to replace bump bonds

A study was completed with RTI International which compared bonding with copper tin (CuSn) pillars to conventional lead tin (PbSn) solder bumps [1]. Similar test structures were prepared for each bonding approach. The CuSn pillars and PbSn bumps were about 10 microns high. The goal was to determine if CuSn eutectic soldering was a better choice for bonding at a 20 micron pitch. It was found that CuSn bonding produced higher yields and stronger bonds than the PbSn bonding at the 20 micron pitch. The cost of CuSn bonding can be relatively low. If post bond thinning is necessary, a significant percentage of the chip surface area must be covered with CuSn to avoid circuit warping and die shear. This can unfortunately lead to a relatively high material budget. Figure 1 shows a cross section of a CuSn bond.

Another approach for bump bond replacement was tested with Ziptronix using their Direct Bond Interconnect (DBI) technology to bond 25 sensors to a wafer of readout chips as shown in figure 2. A small percentage of the mated surface area was covered with metal contacts. After bonding the sensor chips to the readout circuit wafer, the wafer was thinning to 100 microns. No warping or chip separation occurred and a reasonable bond yield was obtained. Future work will thin chips to 25 microns or less after DBI bonding. The DBI process begins with very small metal contacts imbedded in a smooth oxide surface. When the two oxide surfaces are brought together, an oxide bond is immediately formed. After the oxide bond reaches sufficient strength, the devices are heated and the metal contacts expand to compression bonds. Minimal mass is needed for the bonding, thus making this an excellent choice for applications such as the International Linear Collider vertex detector.

1.2 Bonding techniques for 3D chip fabrication

Fermilab began its 3D circuit design activities by using the MIT Lincoln Laboratory 0.18 micron SOI process with oxide bonding between the wafers. The MIT process is a "via last" process which means that vias between bonded wafers are added after the standard wafer fabrication is completed. The first circuits had three layers of electronics bonded together.

More recent design work at Fermilab has focused on the Tezzaron process using CMOS wafers with a copper to copper wafer bond interface. TSVs are added to the wafers at the foundry just after the fabrication of the transistors. This is commonly known as the "via first" process. Wafers with the TSV are fabricated in the Chartered 0.13 micron process. Although as many as five stacked layers have been demonstrated by Tezzaron, our designs only use two layers at the present time.

2.0 Consortium for 3D circuit design

Based on the success of the first 3D design at Fermilab and the opportunity to establish 3D multi project runs specifically for HEP, a number of institutions have come together and formed a consortium for 3D circuit design. The international consortium with 15 members from 5 different counties is completing work on its first 3D multi project run with Tezzaron. There are over 25 designs of complete circuits and test structures. The circuit designs are aimed at ATLAS pixels, CMS silicon strips, ILC pixels, B factory pixels, and X-ray imaging. The tests circuits are intended to study radiation tolerance, cryogenic operation, bond and via reliability, and SEU tolerance. To reduce costs, only a single set of masks are used for both the top and bottom layers of the 3D circuit. Because the frame is approximately 26 x 30 mm designs up to 5.5 x 6.3 mm have been accommodated.

3.0 Vertically integrated circuits by Fermilab

At the present time, Fermilab has completed design of five 3D integrated circuits. Two of the circuits were completed in the MIT LL silicon on insulator (SOI) process. These

circuits were full scale demonstrator chips for an ILC pixel detector. The first chip, VIP1, included many features: read out between ILC bunch trains, high speed data sparsification, analog output for improved resolution, 5 bit digital stamping for 30 usec resolution and 20 um pixels in a 4K array. The division of the circuit schematic into 3 tiers and the associated layout for one pixel is shown in figure 3 [2]. The VIP1 was found to be functional. The main problem was that the VIP1 yield was very low. Thus another version of the chip (VIP2a) was submitted to MIT LL with numerous changes including: improved power distribution, wider traces, redundant vias, and some circuit changes. VIP2b is still in fabrication.

After VIP2a, the focus at Fermilab shifted toward using a commercial CMOS process. The expected benefits include better yield and higher radiation tolerance. Thus the next three circuits were designed in CMOS using the Tezzaron 3D approach. The first circuit was a redesign of the VIP2a into the Chartered 130 nm process and a conversion from a 3 tier circuit to a 2 tier circuit. The new circuit called VIP2b has 8 bits of time stamping for better time resolution (3.9 usec), a larger pixel size of 24 um to accommodate the larger time stamp, and has a larger 192 x 192 array.

The next 3D chip is a demonstrator chip for CMS. Tracker occupancy at Super LHC will be extremely high and will require a Level 1 track trigger for data reduction since all data cannot be transferred at 40 MHz [3]. The track trigger must 1) identity hits associated with pt above 2 GeV for data transfer, 2) rapidly identify tracks with pt above 15-25 GeV, and 3) provide good Z vertex resolution of about 1 mm for tracks above 2 GeV. The overall goal is to reduce track hit data by a factor of 100-200. The approach taken is to construct detector modules with a pair of sensor planes separated by about 1 mm, and a single 3D chip to locally process signals from both sensors. The chip called VICTR (Vertically Integrated CMS TRacker) collect hits from both sensors, finds hit pairs with pt>2GeV by means of a coincidence circuit, and transfers data to a vector forming circuits. There the hit pairs>2GeV are collected, and track vectors are formed for identification of high pt tracks. Finally track vectors with low pt are rejected to further reduce the data before transferring data off the detector. A simplified block diagram of the top and bottom sensors and a portion of the VICTR chip are shown in figure 4. The top tier of the 3D chip processes sensor signals from the top sensor and sends the resultant signal to the bottom tier. The bottom tier processes signals from the bottom sensor and looks for a coincidence between 1 long strip the top sensor and the 5 short strips from the bottom sensor directly beneath. In the final circuit, the simple coincidence circuit will take into account neighbor strips. It is interesting to note that the 3D chip is thinned to 24 um and connections are made to both the top and bottom of the chip.

The last chip was designed for X-ray photon correlation spectroscopy to study the dynamics of equilibrium and non-equilibrium processes. The chip called VIPIC (Vertically Integrated Photon Imaging chip) is a 64 x 64 array of 80 um pixels. The array has a sparsified binary data output with a read out time of 10 usec for occupancies ~100 photons/cm2/s. It operates in a dead timeless, trigger less mode and is optimized for 8KeV photons. The chip is 5.5 x 6.3 mm and features two 5 bit counters for recoding of

multiple hits per time slice thus providing imaging information. The pixel address read out time is constant regardless of hit location due to use of a binary tree hit finder principle. The pixel array is read out on 16 parallel high speed LVDS output lines (figure 5). The design is adaptable to 4 side buttable X-ray detectors arrays.

4.0 Conclusion

Fermilab has used two different processes which can successfully replace conventional bump bonds at a 20 um pitch and below. Two other bonding processes have been used for fabrication of 3D integrated circuits. Based on the early design efforts at Fermilab, a large consortium of institutions has come together to develop 3D integrated circuits for physics applications. The five circuits designed by Fermilab suggest the wide range of applications that are possible with 3D integration.

5.0 Acknowledgements

The author wishes to thank the dedicated members of the ASIC group (G. Deptuch, J. Hoff, A. Shenai, M. Trimpl, and T. Zimmerman) who designed the circuits described in this paper. I would also like to acknowledge the many valuable discussions held with M. Demarteau, R. Lipton, and D. Christian.

6.0 References

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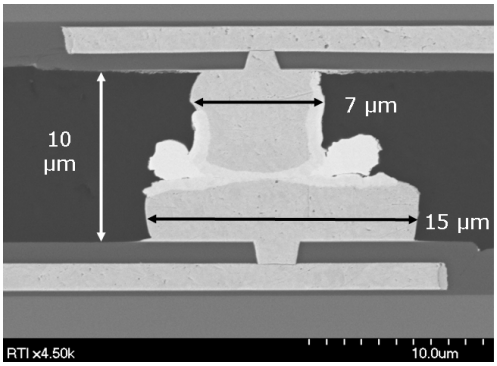

Figure 1 – Cross section of CuSn bond

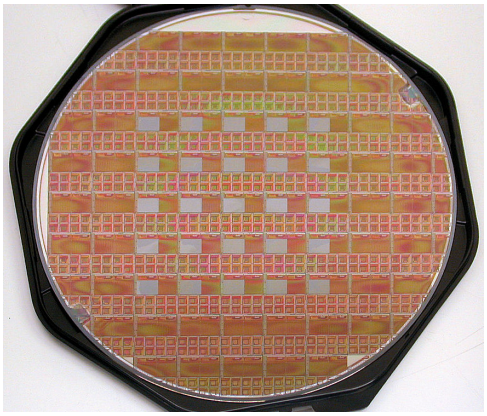

Figure 2 – 25 Sensors mounted with DBI

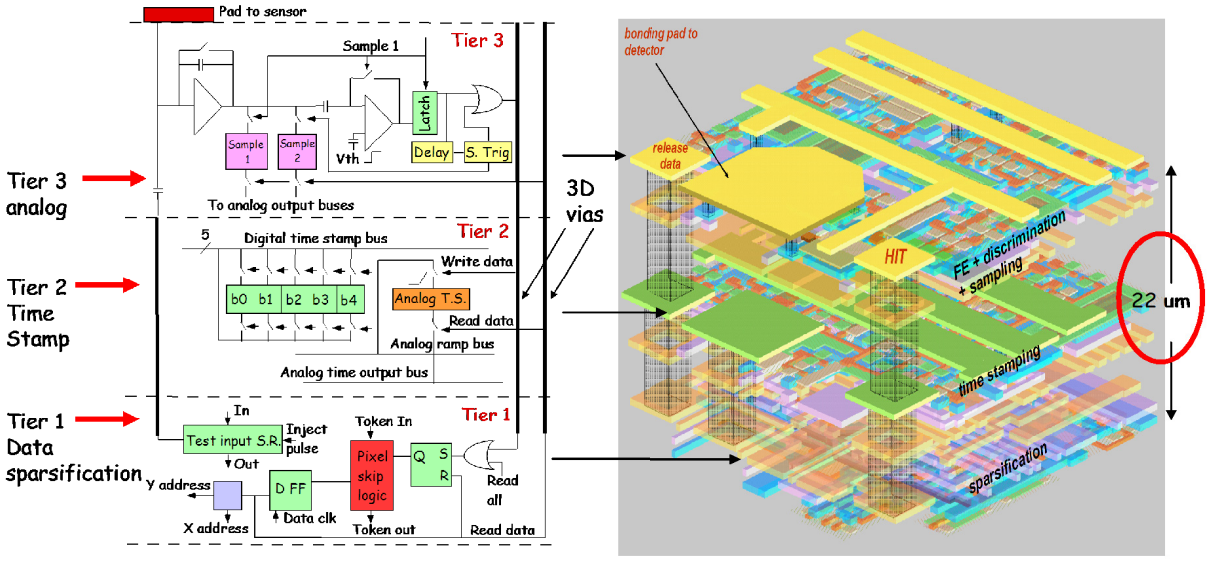

Figure 3 – 3D schematic and layout for one pixel VIP1 pixel cell

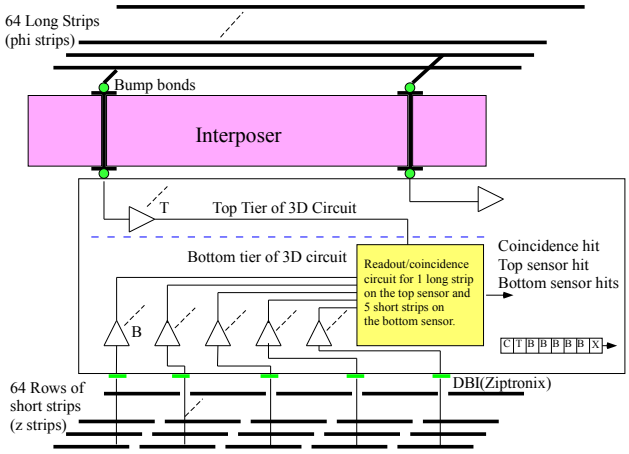

Figure 4 – Block diagram of a portion of the VICTR chip and the top and bottom sensors

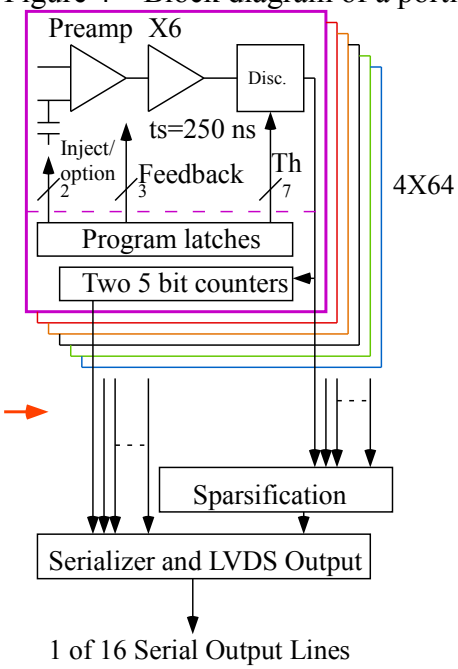

Figure 5- Block diagram of 256 VICTR pixels