The "Road Warrior" for the CDF Online Silicon Vertex Tracker

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Abstract—
The Online Silicon Vertex Tracker (SVT) is a new trigger processor dedicated to the 2-D reconstruction of charged particle trajectories at Level 2 of the CDF trigger. The SVT links the digitized pulse heights found within the Silicon Vertex detector to the tracks reconstructed in the Central Outer Tracker by the Level 1 Fast Track finder. The SVT was recently modified in order to increase its efficiency. The new configuration uses all the Silicon Vertex detector layers. On the other hand the processing time has increased. This can be a problem at higher luminosities of the Tevatron. The "Road Warrior" is a new board that eliminates redundant track candidates before Track Fitting. It is based on the principle of the Associative Memory. The algorithm used is described in the paper, as well as the hardware implementation.

I. Introduction

The core of the SVT is organized as 12 identical systems (sectors) running in parallel almost independently [1]. This architecture derives from the geometry of the Silicon Vertex detector (SVXII) which is divided into 12 identical wedges in azimuthal angle [2]. The main functional blocks of each SVT sector are the Hit Finders, the Associative Memory system, the Hit Buffer and the Track Fitter. Every time an event is accepted by the Level 1 trigger, the digitized pulse heights in the Silicon Vertex detector are sent to the Hit Finders which calculate hit positions. The hits found by the Hit Finders and the tracks found in the Central Outer Tracker (COT) are then fed simultaneously to the Associative Memory system and to the Hit Buffer. The Associative Memory system performs pattern recognition by selecting for further processing only combinations of COT tracks and SVXII hits that represent good track candidates. This is done by comparing the input data with a stored set of patterns in a completely parallel way, using a dedicated custom VLSI chip called AMchip [3]. The output of the Associative Memory system is a list of "Roads". Each Road is defined as a combination of five SuperStrips detected on five different detector layers. The five SuperStrips correspond to the hit positions on four silicon detector layers, while the fifth SuperStrip is a function of the curvature and azimuthal angle of the COT track reconstructed by the Level 1 Fast Track finder (XFT). To reduce the amount of required memory this pattern recognition process is performed at a coarser resolution than the full available detector resolution. The Roads found by the Associative Memory system are sent to the Hit Buffer, which retrieves the original full-resolution silicon hit coordinates and XFT track associated with each Road and delivers them to the Track Fitter (TF) for full precision computation of track parameters. Track reconstruction is performed by the SVT in the plane transverse to the beamline.

In the first implementation of the SVT [4] the definition of a Road used four of the five silicon detector layers only, ("4 out of 4" configuration), in addition to the XFT information treated as an additional layer. The four layers were chosen a priori. Therefore the overall SVT efficiency was largely affected by the hit inefficiency in each layer ($1-\epsilon \approx 5\%$). The total efficiency was roughly proportional to ϵ^4.

During the 2003 data taking, the definition of a Road was changed. In the new definition all five silicon layers are used, requiring the presence of hits on at least four of them, plus the XFT layer ("4 out of 5" configuration). In this case we observe an increase in the total efficiency of $4(1-\epsilon) \approx 20\%$. Another feature of the "4 out of 5" mode is that the track acceptance along the beam is larger by 10%, since tracks that cross different SVX longitudinal modules can be reconstructed.

The drawback of this new configuration is that the SVT timing increases from 23 μs to 30 μs. This can be a serious problem when the luminosity of the Tevatron increases to 10^{32} cm^{-2} s^{-1}, since a large dead time is introduced.

A large part of the increase in timing is due to duplicate ("ghost") Roads. In fact, for each real track it is possible to find a single "5 out of 5" road (one hit on each layer) and/or a number of "4 out of 5" roads (when a hit is missing on one layer). The four hits are the same for all these roads. When all these roads are sent to the Track Fitter, some processing time is wasted by repeatedly fitting the same hit combinations.

Eventually, duplicate tracks are eliminated by the "Ghostbuster" board, after the Track Fitter, but "ghosts" produce an increase of work for the SVT system which results in an increased processing time.

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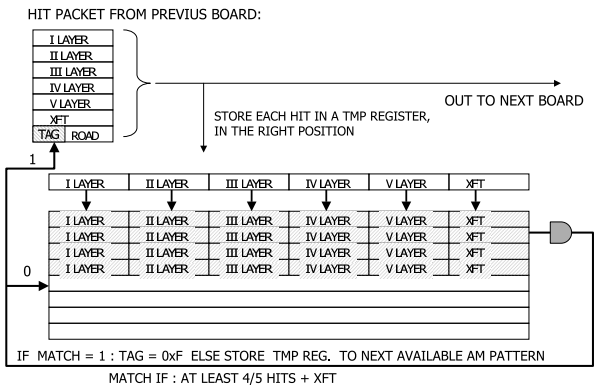

Fig. 1. Road Warrior algorithm

Quantitatively, "ghosts" are about 50% of the hit combinations input to the Track Fitter. The time needed to fit a hit combination is estimated to be about 300 ns, and a typical number of combination per event is about 30, depending on the Tevatron instantaneous luminosity.

The "Road Warrior" is a board that eliminates duplicate roads at the input to the Track Fitter.

II. The Algorithm

The Road Warrior algorithm is based on the principle of the associative memory, widely used in SVT, here implemented in an FPGA rather than in an ASIC. The associative memory stores up to 64 patterns. A pattern can be seen as a row of 6 locations, each one capable of storing a hit word. Each location is reserved for a definite layer (Figure 1).

The hits arrive on the board in a fixed order by layer, and the most recent hit in each layer is stored in a temporary location, again organized as a row of 6 locations. When this road word is complete, meaning that all the hits have been received, the temporary location is compared in parallel to all the stored patterns. The comparison is made using majority logic: it matches only if at least 5 out of 6 of the locations of a pattern match.

In case of a match, the packet received is a duplicate, so the road word is flagged and the track fitter will discard it. If there is no match, the temporary location is copied into the next available pattern in the associative memory, and the road word is not flagged.

At the end of the event the associative memory is cleared.

The firmware has been designed to not introduce any bottleneck, so it is organized as a straight pipeline, introducing only 3 cycles of latency. Each word that enters the board also exits from it, and only the road word is modified to instruct the Track Fitter to fit or discard the track.

Figure 2 shows a block diagram of how the pipeline is organized. In detail:

1. Hits arriving from the Hit Buffer board are written into a fifo. The fifo is read and hit words are immediately registered. From here on the dataflow will follow two independent paths.
2. Hits reach a 1 to 6 demultiplexer, switched by looking at the layer bits, which are part of the Hit word.
3. Through the multiplexer Hits are latched in a temporary register. Each Hit is written in the register corresponding to its own layer, and if more Hits belonging to the same layer are received, only the last one is recorded.
4. The content of the temporary register is compared to the associative memory logic (Figure 3).

In detail:

a : The hits coming from the temporary register are compared, in parallel, to the content of 64 registers for each layer, in which non-matching patterns from previous roads have been stored. More precisely only the registers that were written up to that moment are used for the comparison. The results are 6 groups of 64 match_layn signals.

b : 64 by 6 registers are used to store the patterns. If a pattern matches, a clock enable signal is generated to store the Hit in a register.

5. (Again Figure 2) the match_layn signals reach a combinatorial logic block that generates the Global Match signal. (Figure 4).

In detail:

a : The 6 match_layn signals, belonging to the same pattern, are sent to a majority logic that is set if at least 4 out of 5 of these signals are active, plus the XFT layer. This means that the incoming pattern is already stored in the bank, so it should be rejected by the Track Fitter board.

b : All the 64 pattern Match Signals are or-ed to form the Global Match signal.

c : The Global Match signal together with a 6-bit counter are used to form the Clock Enable signal to the pattern registers: if the incoming pattern doesn't match, it is stored in the next available pattern register.

6. (Again Figure 2) The hits coming out from the first register are delayed to be synchronous with the Global Match signal. This signal is used to set a specified bit that signifies to the Track fitter if the road should be rejected or processed. Logic then sends the hit, together with the data strobe signal, to the Track Fitter board.

Some error checking, like a parity calculation, is included in the firmware. Parameters that define the working mode of the Road Warrior can be changed through a VME interface.

III. Hardware implementation

To implement the Road Warrior, we have used a 9U VME board, recently developed by a group of physicists and engineers from Fermilab and the University of Chicago [5] and described at this conference (Figure 5).

This board, named Pulsar, was initially developed mainly for the upgrade of the CDF Level 2 trigger [6]. However the board design is flexible enough to be used in many other HEP applications within and outside CDF, and is fully compatible with the SVT architecture.

The Pulsar has three big Altera APEX20K400 Field Pro-

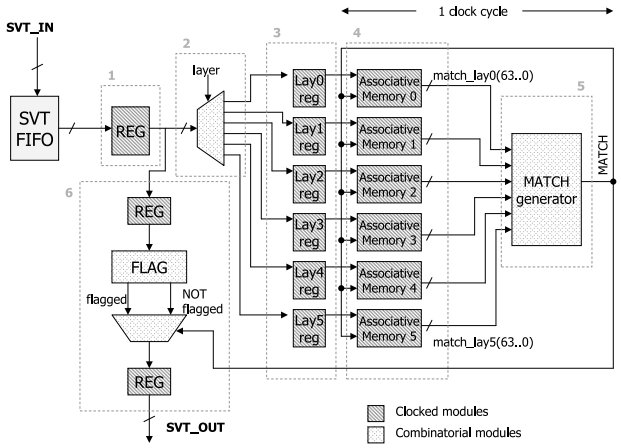

Fig. 2. Road Warrior firmware

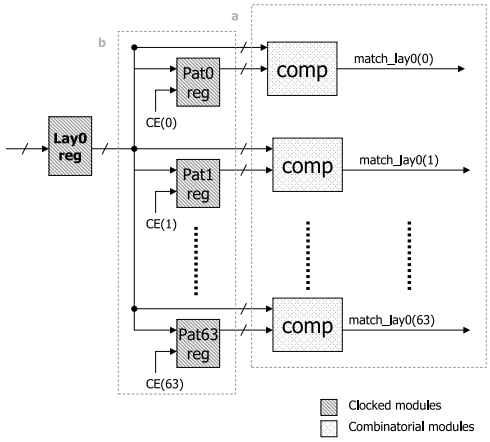

Fig. 3. Associative memory logic details

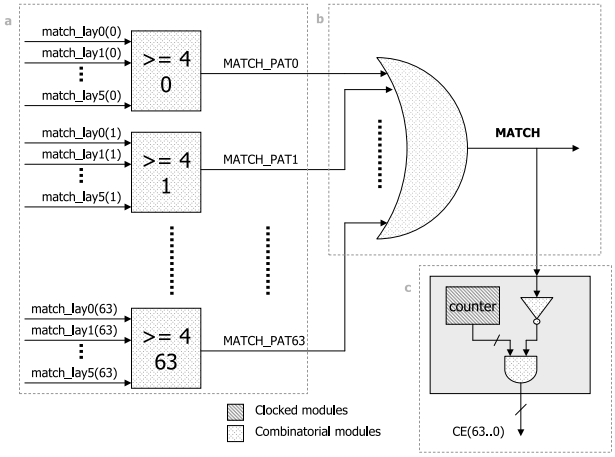

Fig. 4. Match logic details

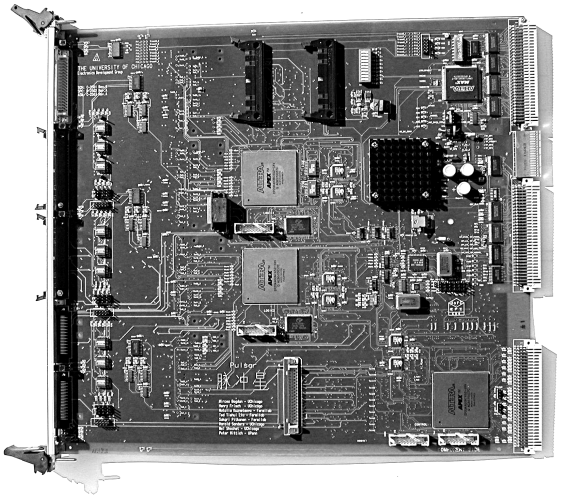

Fig. 5. Top view of the Pulsar board

grammable Gate Arrays (FPGAs) together with fast large SRAMs. Each FPGA can receive SVT input data, which makes it ideal to implement SVT-like functions in a quick and efficient way. For the Road Warrior application, we used only one FPGA and the resource usage on this FPGA is about 80%. It has been tested without problems at the SVT standard 30MHz frequency for this application even though the board itself typically runs at 80MHz for other Level 2 trigger upgrade applications.

The Road Warrior firmware has been successfully tested in the CDF detector. Twelve Road Warriors were installed in the SVT system in June 2004, and data have been taken with this configuration as default since then.

Figure 6 shows the average SVT processing time per event during data taking at different instantaneous luminosities of the Tevatron. Full dots show the processing time without the Road Warrior, and the open circles show the processing time when the Road Warrior was enabled. Since the first implementation of the "4 out of 5" configuration, the SVT timing was optimized in a number of ways, so that the timing at a luminosity of 20×10^{30} cm^{-2} s^{-1} was 26 μs instead of the original 30 μs. Luminosity has increased also, and the SVT timing again reached 30 μs in 2005. The Road Warrior allows an average reduction between 2 and 3 μs per event.

IV. Conclusions

By eliminating duplicate roads at an early stage, the Road Warrior reduces SVT processing time. Such a saving is useful for the whole CDF trigger system in order to cope with the increasing Tevatron luminosity

References

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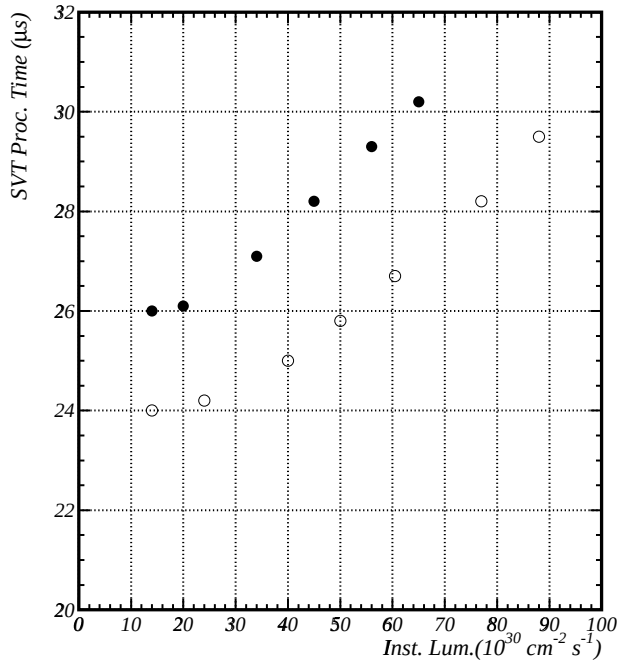

Fig. 6. SVT processing time (μs) vs. the Tevatron instantaneous luminosity (in units of 10^{30} cm^{-2} s^{-1}), without Road Warrior (full dots) and with Road Warrior (open circles).

[5] T. Liu et al., "Pulsar Design and Testing Methodology for CDF Level 2 Trigger Upgrade," Presented at the IEEE NSS Conference, Portland, Oregon, USA, October 22, 2003. More information about Pulsar project can be found at `http://hep.uchicago.edu/~thliu/projects/Pulsar/`.

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