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CDF Run IIb Silicon: Stave design and testing

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For the CDF collaboration

***Abstract*—The CDF Silicon Vertex Detectors (SVX) have been shown to be excellent tools for heavy flavor physics, with the secondary vertex detection and good vertex resolution. The CDF RunIIb Silicon Vertex Detector (SVXIIb) was designed to be a radiation tolerant replacement for the current SVXII which was not anticipated to survive the projected Run II luminosity dose. The outer five layers use identical structural elements, called staves, to support six silicon sensors on each side. The stave is composed of carbon fiber skins on a foam core with a built-in cooling tube. Copper on Kapton bus cable carries power and data/control signals underneath three silicon modules on each side of the stave. A Hybrid equipped with four new SVX4 chips are used to readout two silicon sensors on each module which can be readout and tested independently. This new design concept leads to a very compact mechanical and electrical detecting unit, allowing streamline production and ease of testing and installation. A description of the design and mechanical performance of the stave is given. We also present here results on the electrical performance obtained using prototype staves as well as results with the first pre-production parts.**

I. INTRODUCTION

THE CDF Run IIb silicon detector (SVXIIb) [1] is designed to be a radiation tolerant replacement for the current 5-layer SVXII and Beam-pipe layer (L00) detectors. The design of SVXIIb is optimized for Higgs and new particle searches while also being affordable, robust, and simple to construct and operate. To minimize the development time, the design of SVXIIb makes use of existing technologies to the largest extent possible.

The new detector is divided into two barrels covering a total of about 1.2 m along the beam direction (the CDF luminous region is about 35cm), with 6 active layers (full phi coverage for each layer) spanning radically from 2.1 cm up to 20 cm from the beam line. Staves populate layers 1 through 5 for a total of 180 while the innermost layer (layer 0) is totally different in concept and follows the design of the previous L00. The layouts of SVXIIb is shown in Fig. 1. Each stave has single-sided sensors on two sides of a carbon fiber foam core which has embedded cooling tubes.

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For the SVXIIb detector a new radiation hard SVX readout chip, called SVX4 chip, has been designed and fabricated on 0.25 micron CMOS technology by collaboration between LBNL, U. of Padova and Fermilab.

For the outer 5 layers SVXIIb uses two mask designs for the single-sided silicon sensors: axial and stereo. The strips on the stereo sensors have a 1.2 degree angle with respect to the axial direction. Layers 1 and 5 have axial sensors on both the top and bottom sides of the staves. Layers 2-4 have axial sensors on the top and stereo sensors on the bottom side. The combination of axial and stereo sensors provides three-dimensional tracking information up to pseudorapidity of 2.and the opportunity for stand alone track identification. Sensors are made at HPK on 320 μm thick 6 inch substrate with a strip pitch of 75 μm for the axial and 80 μm pitch for the stereo sensors. The depletion voltage is between 100V and 200V and the sensors good design and quality allows operation in excess of 500V. Studies on these sensors also after heavy irradiation confirm good quality and operability even after fluencies corresponding to ~20 fb^{-1} of data collected at the Tevatron.

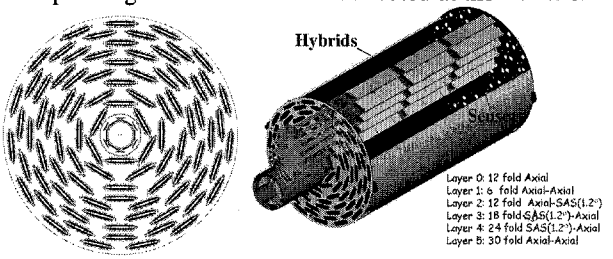


Fig. 1. The end-view (left) and a 3-D layout (right) of stave population of SVXIIb barrel volume.

II. STAVE DESIGN OVERVIEW

A stave is the basic building block of the SVXIIb detector. The new and unique aspects of the stave are that the readout cables and the cooling are completely contained within the stave structure. Using the same stave design for 92% of the detector volume has the advantage of very few types of components; fewer construction fixtures and streamlined production processes; reduce costs; fast construction. Another feature of this design is that the staves are essentially interchangeable.

Silicon sensors, bus cables, readout hybrids and Mini Port-card are all the electrically active components populating both sides (except for the Mini Port-card) of the stave mechanical support structure with built-in cooling channel. As already

mentioned, the stave is a self contained unit in terms of mechanics, cooling and DAQ. The material used on stave is low mass, with small effect on tracking and radiation hard so that SVXIIb can survive in the Run IIb tracking environment. Fig. 2 shows the components and structure of a stave. Six axial sensors are mounted on one side and 6 axial or stereo sensors are mounted on the other side. For improved connection to the inner most layer and the external tracking systems, layers 1 and 5 have axial sensors on both sides. Staves at layers 2 to 4 have axial sensors on one side and stereo sensors on the other to provide vertex information in the z (beamline) direction. 72 staves are double-axial and 108 are axial with 1.2 degree stereo sensors.

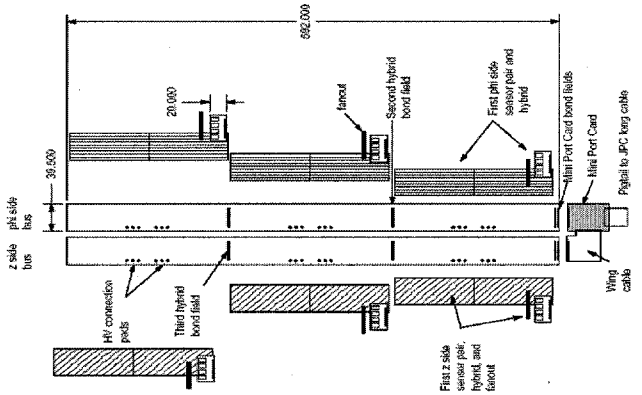


Fig. 2. The components and structure of a stave.

III. Mechanical Overview of Stave

The total length of a stave is 66 cm. The core of a stave is carbon fiber composite skins on a foam core with a built-in cooling tube. The design aims for a light and rigid structure. Two copper-kapton bus cables used for data and power distributions sandwich the stave core. Silicon sensors and readout electronics are glued and wire bonded to each other to form a module. Hybrids are wire bonded down to bus cables for both sides of stave.

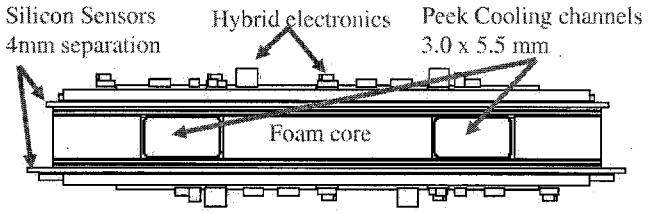


Fig. 3. A view of cross-section on stave structure and material.

A. Mechanical Support

The position of a stave is registered and aligned by precision holes at each end of the stave core. These fit onto precision pins which protrude from the inner and outer bulkheads. .

The low mass construction results in sag over the length of a stave which has support only at two ends. The maximum sag in the middle of a module on a stave is expected to be around 150 μm from simulation and is within the 160 μm specification of layer2 to 5. Test results from preproduction staves indicated gravitational sag less than 150 μm.

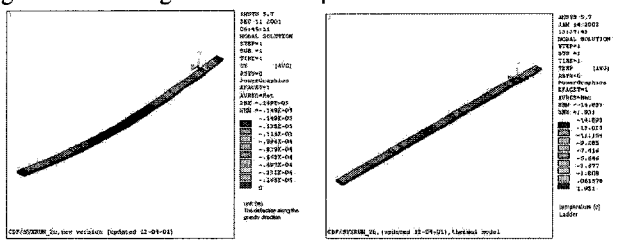


Fig. 4. (Left) Finite element analysis of stave structure under gravity. (Right) Stave temperature distribution assuming coolant temperature of -15 C.

B. Stave Cooling

To prolong the lifetime of the sensors in the high radiation environment the staves are required to operate at cold temperatures. The innermost layers receive the largest radiation dose and thus have the tightest temperature specification (-5C at the 2nd layer) while the outer layers could operate at 15C (6th layer). Good thermal coupling between the sensors and the cooling system is important to achieve these goals. The expected heat generated by a stave will be 17.9 Watt which includes 9.6W from 24 SVX4 readout chips, 4.2W from convection, 2.5W from the Mini Port-card, and 1.6W from leakage current of the silicon assuming after 30 fb^{-1} running.

The core of a stave contains a U shape built-in cooling tube. The tube is formed from 0.1mm wall polyetheretherketone (PEEK) plastic, which is selected for its radiation tolerant properties. A finite element thermal model has been developed to study the temperature trends on a stave. Assuming -15C coolant temperature running in the cooling system, the highest temperature spot is -2.9C on the silicon where right underneath the readout hybrid. And the integrated average strip temperature is lower than -10C on the axial side and -4C on the stereo side. The coolant will be mixture of water and 43% by weight of ethylene glycol with a freezing point of -25C. The cooling system will be operating below atmospheric pressure in the detector region. Therefore, if a leak occurs in the cooling system, the coolant will not leak into the detector volume. There will be a gas system providing a continuous gas flow of nitrogen to the detector volume. This dry gas keeps silicon volume slightly over atmospheric pressure and prevents condensation. The gas will be cooled before entering to the detector.

C. Stave Material

The material inside the tracking volume of a detector should be minimized to reduce multiple scattering which degrades the impact parameter resolution and tracking capabilities. The material of one stave is about 1.95% radiation length (X_0). The use of single-sided silicon on both sides of stave increases the silicon contribution to the material budget. This is compensated in part with a very small hybrid design and the positioning of the Mini Port-card at the end of the staves, outside the tracking volume. The expected material contributions for the whole SVXIIb detector are: ~37% from silicon, 16% from hybrids, 16% from bus cables, and 31% from support structure and

cooling. The stave design generally gives a smooth material distribution.

IV. Stave Readout Electronics

A stave is a single unit in the DAQ chain. A module is made up of two silicon sensors glued and wire bonded together with a hybrid that is glued on silicon. A hybrid carries 4 SVX4 readout chips for sensor signal readout. The three hybrids on each side of a stave are wire bonded down to the bus cable. The Mini Port-card at the end of stave connects bus cables on both side of stave for readout processing and bidirectional data control. The stave design of electronics should comply with the deadtime-less operation of SVX4 chips.

A. SVX4 chip

The SVX4 chip is designed and fabricated in the 0.25μm CMOS process on 300 μm thick silicon which gives radiation hard chips. It contains 128 parallel charge integration channels and 8-bit ADCs. The chip is designed to run in a deadtime-less mode: the front-end (analog) part can run in parallel with the back-end (digital) part. For each channel, there are 46 pipeline cells to store the data. These can hold at most 4 physics event for further digitizing and readout. The operation voltage of the chip is 2.5V instead of 5V in previous version of SVX3 chip.

The other features of SVX4 chips are

1) *Max interaction rate at 132 ns.*
2) *Optimized capacitance load between 10 to 35 pF.*
3) *Built-in charge injection for preamp calibration*
4) *Channel mask to exclude channels with excessive DC current input during operation*
5) *Readout in byte-serial mode with optional zero suppression (sparsification)*
6) *Real-time event-by-event pedestal subtraction (RTPS) which can suppress the common mode noise and compensate for any residual pickup effects.*
7) *Adjustable and loadable control parameters*

The noise of a SVX4 chip is around 400 electrons. The dynamic range of the amplifier is 200fC. The threshold and gain of the amplifier can be set to effectively readout a minimum ionizing particle (MIP) signal.

B. Hybrid

The hybrids are Beryllium Oxide (BeO) substrate circuit boards with gold conductors. A hybrid carries four SVX4 chips to readout the signal of the silicon sensors. The hybrids should be low material and reliable. The BeO substrate has the advantage of low mass and good thermal conductivity to spread the heat generated by chips. The 100/100 μm trace/space and 125 μm via technology help reduce the size of a hybrid. For each stave, there are 6 hybrids glued on silicon and wire bonded to bus cables. Ceramic pitch adapters are used to match the bond field of the hybrid to the sensors.

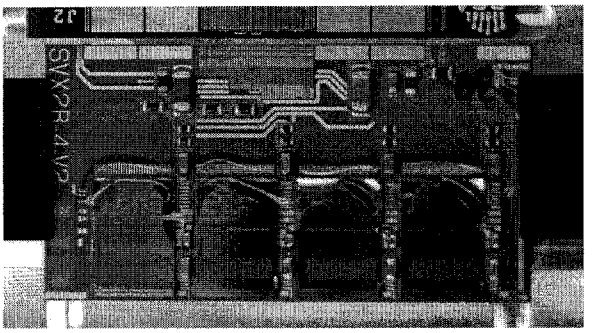


Fig. 5. A BeO hybrid carries 4 SVX4 chips. The wirebond between chips and hybrid pad are encapsulated.

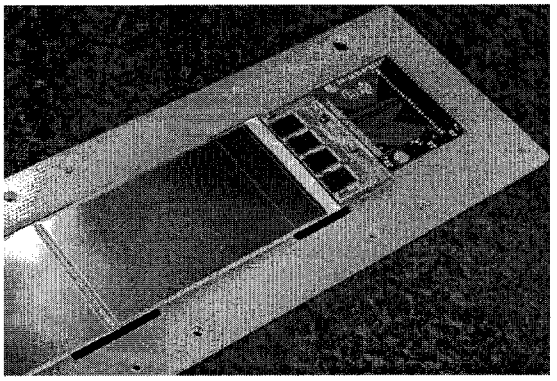
C. Mini Port-card

The Mini Port-card (MPC) also uses a BeO substrate. There are five transceiver chips and by-passing and termination components mounted on one side of the MPC. A pair of flex cables is used to connect to DAQ modules for data and power transition. An additional flex cable is bent around to the back side of the stave and glued on to the carbon fiber. This flex cable is used to connect MPC with the bus cable on the back side of the stave. All the communication, like clock and control signals, to the DAQ is LVDS (low voltage differential signal). The clock will be regenerated at the MPC and sent to the chips on the hybrids. Some signals will be transformed from LVDS to single ended signals for the chips. Some of the data bus lines are bi-directional, and the differential drivers on MPC regenerate the signal in both directions, from DAQ to hybrids and vice-versa.

D. Bus cable

The bus cable is a flexible etched laminate of kapton, copper and aluminum foil. The cables are laminated to the carbon fiber surface of the stave. The single-sided silicon sensors are glued on top of the cable. There are gaps, about 3mm wide, at the location between modules to allow wire bonds from the hybrids to the bus lines. Bus traces are 75 μm wide with 100 μm space and paired if they are used for differential signal transmission. Each pair is separated by a 150 μm cap. Power and ground traces are wider to avoid voltage drop.

The shield of aluminum foil above the bus traces is crucial to avoid pickup noise on back plane of silicon. The best solution was found to have the shield grounded to the closest analog ground which is on the hybrid. The connection should be solid to have small impedance and inductance. The impedance of the bus depends on the geometry and kapton thickness between bus lines and carbon fiber below and aluminum shield above. The measured value is at 75 ohms.



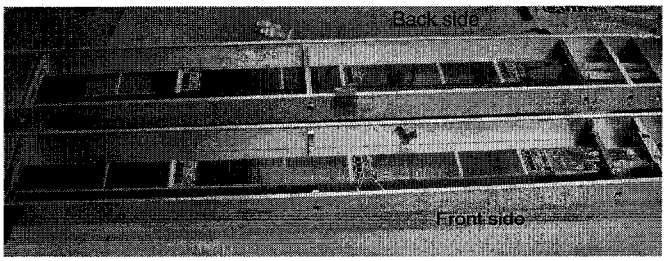


Fig. 6. Pictures of a module (upper) and staves (lower). Two silicon sensors are wire bonded and held by a G10 frame. One side of the sensor is bonded to a pitch adapter which connects to the SVX4 chips on hybrid. In the staves picture, both front and back sides of staves are shown.

IV. Stave Electrical Testing

All the components are tested and burned-in before hybrids / modules / stave assembling. SVX4 chips are probed on their wafer at Fermilab before dicing; hybrids are assembled and tested at LBNL and burned-in at U.C. Davis for at least three days before shipping to Fermilab.

A. Chips/Hybrids/Modules testing

The pedestal, noise, and differential noise (dnoise, i.e. common mode noise suppressed) distributions are used to study and determine if the chips, hybrids, or modules are working well. Fig. 7 shows pedestal and noise distributions for a single SVX4 chip with capacitors loaded for several preamp input values. The increase in capacitive load increases the noise.

Fig. 7 shows examples of data taken for a single SVX4 chip or prototype hybrid at Fermilab. By adding a capacitive load on the preamp, the noise/dnoise is seen to increase linearly with the capacitance. According to this, we can estimate the noise level for a module. The studies help us better understand the chip function as well as the module and stave performance. Other testing, such as gain scans, bandwidth scans and ramp pedestals will be performed on each hybrid and module to ensure the functioning of the components.

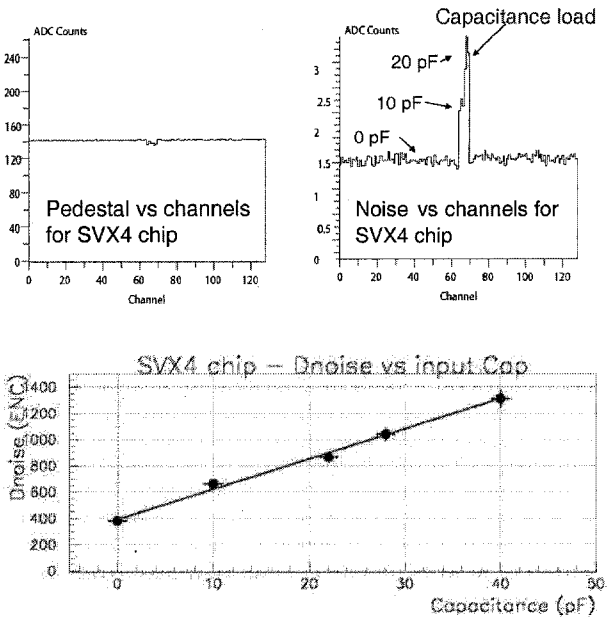


Fig. 7. The pedestal (upper-left) and noise (upper-right) distribution of a single SVX4 chip. The peak of the noise distribution is due to the increased capacitance on preamp channels. The lower plot is a study of dnoise dependence versus input capacitive load.

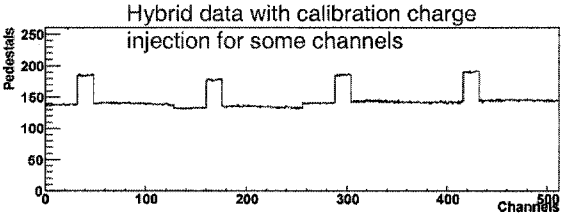


Fig. 8. The hybrid data with calibration charge injected for a bunch of channels of the chips on a hybrid.

B. Stave testing

The critical point of a stave is the noise performance. Since the bus cables which contain data buses and power traces are running beneath the silicon sensors, a layer of shielding is needed to avoid direct noise pickup from sensor backplane. Also the proper grounding and shielding of stave improve the noise performance. For example, the return ground of the bias of the sensor should go to the stave analog ground which is quiet; the carbon fiber structure of stave core is grounded to the closest analog ground which is on Mini Port-card side; also the aluminum box should be well shut and grounded.

The prototype stave has been used to study the performance. The noise/dnoise distributions give reasonably good results. The noise on the stave is around 1,100 electrons with typical gain of the preamps of 500 electrons per ADC count. The deadtime-less testing is a key issue for the stave [3]. The studies to date indicated close to acceptable performance in deadtime-less mode operation.

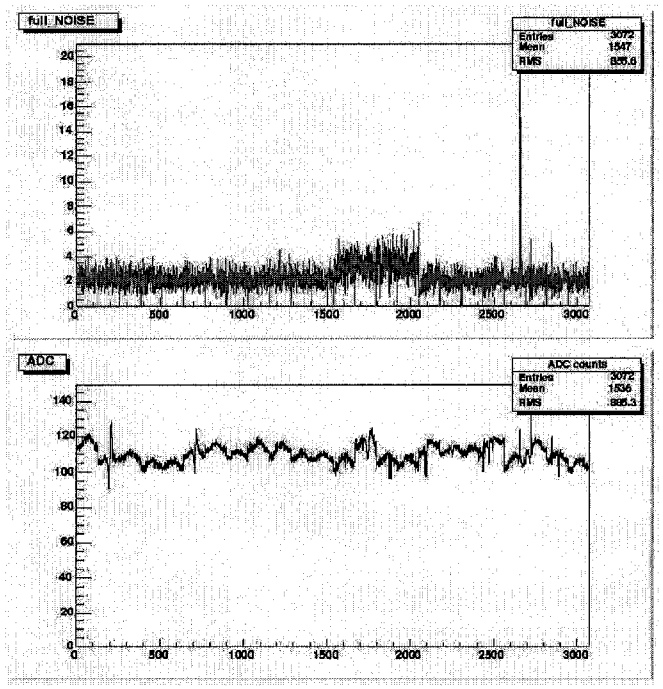


Fig. 9. The pedestal (lower), noise (upper blue), and dnoise (upper red) distribution for a full stave. Totally 3072 channels are readout and the noise of the stave is around 1,100 electrons. The Bow-shaped pedestal is corrected on the new SVX4 chip.

C. *Laser Run on Stave*

A laser run was performed to demonstrate that the stave is functioning. We shine the laser on silicon and readout the data. The offline pedestal subtracted data, as shown in the Figure 10, has a clear and clean laser signal which covers few strips of sensor. The laser spot covers around nine strips and sum of the ADC readout is around 175 counts.

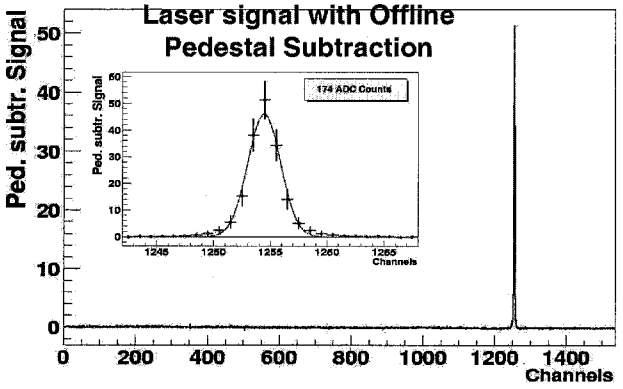


Fig.10. The offline pedestal subtracted laser data. A clear signal is seen at channel 1255 area and around 9 strips are illuminated by the laser.

V. SUMMARY AND PLAN

Although the SVXIIb project has been terminated and will be closed out in the coming year, we plan to build out a new setoff modules and staves. Most of the silicon sensors and SVX4 chips are ready and hybrids are being assembled at the time of this writing. At least 15 staves will be built and at least five staves will be mounted on the barrel structure and form a group with a few layer 0 modules. The system testing will be performed and cosmic ray data will be taken to demonstrate that SVXIIb and stave design is well understood and feasible.

VI. REFERENCE

[1] CDF Collaboration, the Run IIb Technical Design Report, CDFNOTE 6261.

[2] M. Aoki, *et al*, 'The CDF Run IIb Silicon Detector', CDFNOTE 6750, to be published in the proceeding of Frontier Detectors for Frontier Physics, Isola d'Elba, Italy, May 25-31, 2003.

[3] M. M. Weber, 'Electrical Performance and Dead-timeless Operation of "Staves" for the New CDF Silicon Detector', to be published in the proceeding of IEEE Nuclear Science Symposium 2003, Portland, Oregon, U.S.A. Oct. 19-25, 2003.