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Development of a High Density Pixel Multichip Module at Fermilab

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Abstract

At Fermilab, both pixel detector multichip module and sensor hybridization are being developed for the BTeV experiment. The module is composed of three layers. The lowest layer is formed by the readout integrated circuits (ICs). The back of the ICs is in thermal contact with the supporting structure, while the top is flip-chip bump-bonded to the pixel sensor. A low mass flex-circuit interconnect is glued on the top of this assembly, and the readout IC pads are wire-bounded to the circuit. The BTeV pixel detector is based on a design relying on a hybrid approach. This method offers maximum flexibility in the development process, choice of fabrication technologies, and the choice of sensor material. This paper presents strategies to handle the required data rate and performance characteristics of the pixel module prototypes.

Introduction

At Fermilab, the BTeV experiment has been approved for the C-Zero interaction region of the Tevatron [1]. The tracker detector for this experiment will be a pixel detector composed of 60 pixel planes of approximately 100x100 mm^2 each, assembled in 30 stations. The planes are located perpendicular to the colliding beam with pixels as close as 6 mm to the beam. Each plane is formed by an arrangement of multichip modules with three different lengths: 100 mm, 60 mm and 48 mm. The modules are formed by up to 9 pixel readout chips bump bonded to a single Silicon pixel sensor. The modules on opposite faces of the same pixel station are assembled perpendicularly in relation to each other (see Figure 1).

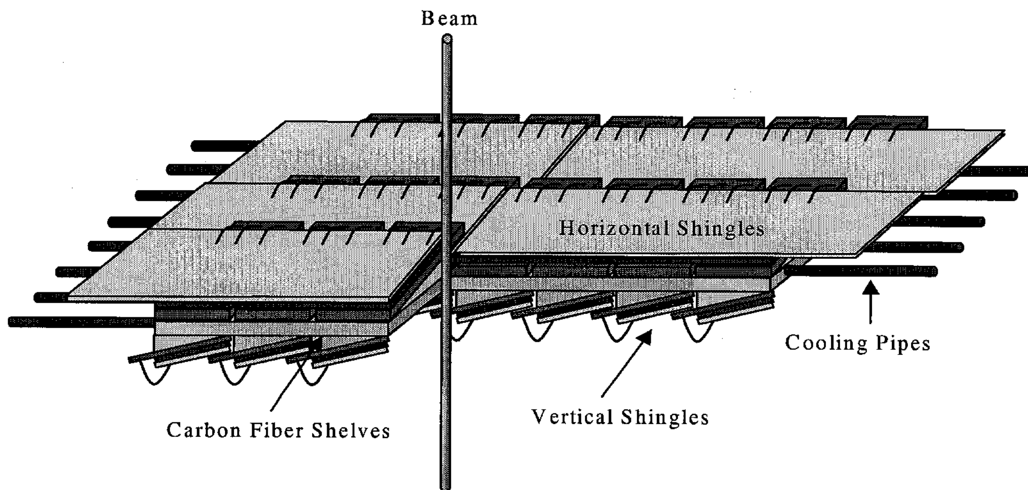

Figure 1 – Pixel Station

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A "hit" in the pixel sensor occurs when a charged particle (from the collision of a proton with an anti-proton) passes trought a pixel in the biased pixel sensor (Figure 2). The pixel cell is a n^+ implant in the n bulk of the sensor, isolated from each other with a p implant. The back of the sensor is biased with a negative voltage, so the passage of charged particle creates an ionezed channel in the sensor [2]. The charge deposited in the sensor from the particle is integrated in the pre-amplifier of the readout chips (connected with bump-bonds).

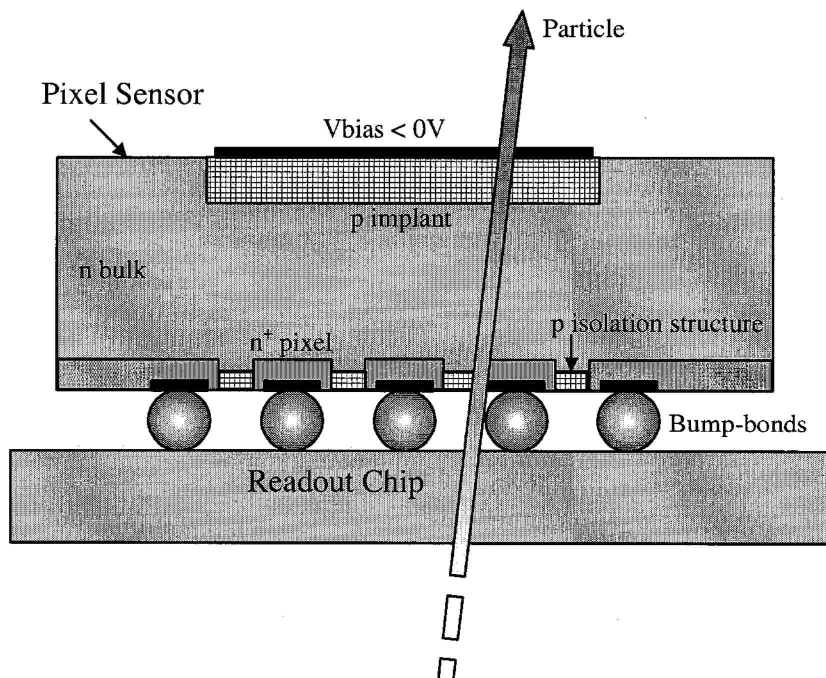

Figure 2 – Pixel Sensor

The multichip module packaging must conform to special requirements dictated by BTeV [1]: the pixel detector will be inside a strong magnetic field (1.6 Tesla in the central field), the flex circuit and the adhesives cannot be ferromagnetic, the pixel detector will also be placed inside a high vacuum environment, so the multichip module components cannot outgas, the radiation rates (around 3 Mrad per year) and temperature (-5° C) also impose severe constraints to the pixel multichip module packaging design. The flex circuit has a fine trace pitch (35 μm traces and 35 μm spacing), small via pad (200 μm), and 4 metal layers. Another challenge for this packaging is to find vendors willing to produce such fine pitch flex circuits for our production quantities (1500 flex circuits, small for industry standards).

The pixel detector will be employed for on-line track finding for the lowest level trigger system and, therefore, the pixel readout chips will have to read out all detected hits. This requirement imposes a severe constraint on the design of the readout chip, the hybridized module, and the data transmission to the data acquisition system. It also requires the collection of a large amount of data (~216 Gbit/s) that is going to be used to identify interesting tracks.

Several factors impact the amount of data that each readout chip needs to transfer: readout array size, distance from the beam, number of bits of pulse-height analog to digital converter (ADC) data format, etc. Presently, the most likely dimension of the pixel chip array will be 128 rows by 22 columns and 3 bits of ADC information.

Pixel Module Readout

The pixel module readout must allow the pixel detector to be used in the lowest level experiment trigger. Our present assumptions are based on simulations that describe the data pattern inside the pixel detector [3]. The parameters used for the simulations are: luminosity of 2×10^{32} $cm^{-2}s^{-1}$ (corresponds to an average of 2 hits per bunch crossing), pixel size of 400×50 μm^2, threshold of 2000 e^- and a magnetic field of 1.6 Tesla.

Figure 3 shows a sketch of the 40 chips that may compose a pixel half plane. The beam passes on the place represented by the black dot. These numbers assume the 23-bit data format shown in Figure 4. The rows in Figure 3 represent pixel multichip modules. For this discussion the modules are numbered from 1 to 5 from top to bottom. The chips are labeled from *a* to *i* from left to right. Module 4 is the busiest pixel module. The chip *e* in module 4 and chip *d* in module 5 are the busiest chips.

	a	*b*	*c*	*d*	*e*	*f*	*g*	*h*	*i*
Module 1 →	11	13	17	17	20	18	16	13	8
Module 2 →	11	18	26	31	39	33	25	18	12
Module 3 →	16	20	37	61	76	59	39	26	18
Module 4 →	17	35	63	141	234	130	65	36	16
Module 5 →	23	35	74	234	• ← Beam				

Figure 3 – Average Bit Data Rate at Middle Station, in Mbit/s

22			0
ADC	**Beam Crossing Number**	**Column**	**Row**

Figure 4 – Pixel Module Data Format (23 bits)

Table 1 presents the required bandwidth per module. From this table we see that each half pixel plane requires a bandwidth of approximately 1.8 Gbit/s.

	Req. Bandwidth
Module 1	133
Module 2	213
Module 3	352
Module 4	737
Module 5	366
Total	***1801***

Table 1 – Half Plane Required Bandwidth, in Mbit/s

We've used simulations of the readout architecture with a clock of 35MHz. This frequency can support a readout efficiency of approximately 98% when considering three times the nominal hit rate for the readout chip closest to the beam. Efficiency is lost either due to a pixel being hit more than once before the first hit can be read out, or due to bottlenecks in the core circuitry.

Proposed Readout Architecture

The readout architecture is a direct consequence of the BTeV detector layout. The BTeV detector covers the forward direction, 10-300 mrad, with respect to both colliding beams. Hence, the volume outside this angular range is outside the active area and can be used to house heavy readout and control cables without interfering with the experiment. The architecture takes advantage of this consideration.

The Data Combiner Board (DCB) located approximately 10 meters away from the detector remotely controls the pixel modules. All the controls, clocks and data are transmitted between the pixel module and the DCB by differential signals employing the Low-Voltage Differential Signaling (LVDS) standard. Common clocks and control signals are sent to each module and then bussed to each readout IC. All data signals are point to point connected to the DCB. Figure 5 shows a sketch of the proposed readout architecture. For more details refer to [4].

This readout technique requires the design of just one rad-hard chip: the pixel readout chip. The point-to-point data links minimize the risk of an entire module failure due to a single chip failure and eliminate the need for a chip ID to be embedded in the data stream. Simulations have shown that this readout scheme results in readout efficiencies that are sufficient for the BTeV experiment.

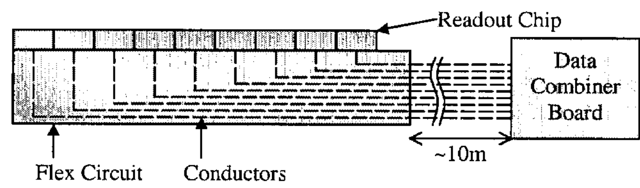

Figure 5 – Pixel Module Point-to-Point Connection

First Pixel Multichip Module Prototype Packaging

Figure 6 shows a picture of the first prototype of the pixel module. It is composed of a pixel sensor bump-bonded to five Fermilab Pixel (FPIX1) readout chips and a four layer high density flex circuit made by Fujitsu Computer Packaging Technologies (FCPT, San Diego). This flex circuit has line traces of 20 μm in a 40 μm pitch, copper line thickness of 5 μm, vias spaced by 200 μm, via cover pads of 100 μm and average via hole diameter of 26 μm.

In this prototype the flex interconnect is located on the side of the readout chips instead of on the top of the sensor (as in the baseline design). The pixel sensor used is oversized; it can be bump-bonded to a total of 16 readout chips.

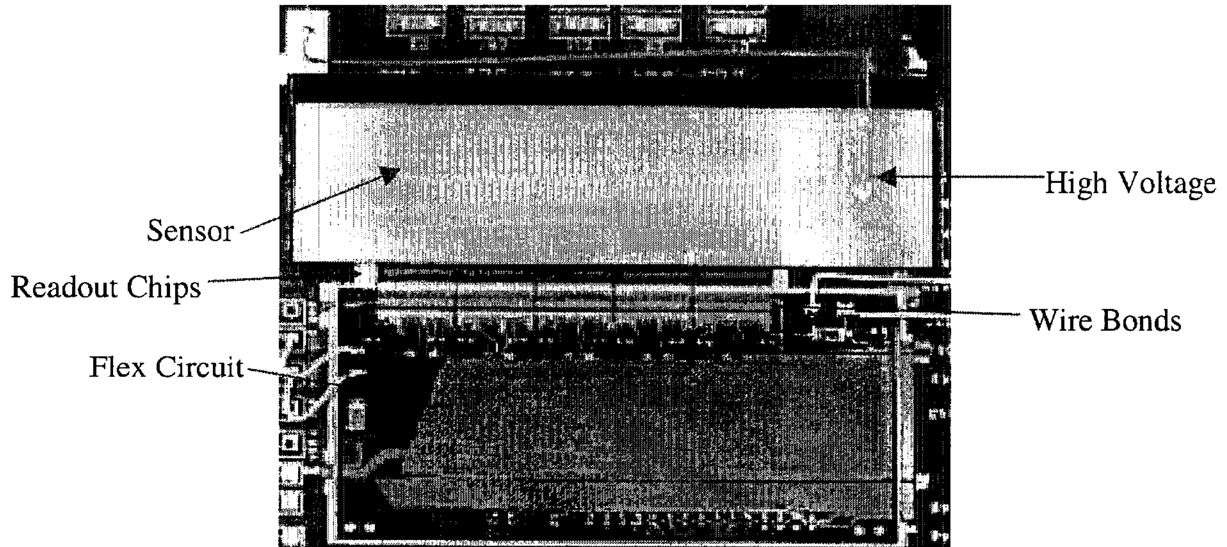

Figure 6 – Prototype Pixel Module

There are two ways to inject charge in the pre-amplifier of FPIX1. The first one is through the connection with the sensor that occurs when a particle hits a pixel. The second way is to inject an analog signal to a capacitor in the input of the chips pre-amplifier (Figure 7).

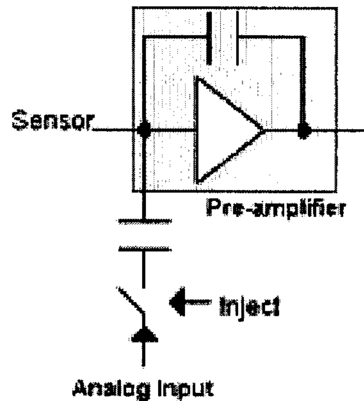

Figure 7 – FPIX1 Pre-amplifier Inputs

This pixel module has been characterized for noise (noise mean (μ_{Noise}) and noise variance (σ^2_{Noise})) and threshold dispersion (threshold mean (μ_{Th}) and threshold variance (σ^2_{Th})). These characteristics were measured by injecting charge in the analog front end of the readout chip with a pulse generator and reading out the hit data through a logic state analyzer.

Data of just four readout chips is available because one of the chips failed. The results for one specific threshold are summarized in Table 2. Results for three different thresholds are shown in Table 3.

Chip	1	2	3	4
μ_{Th}	1030	1250	1500	1400
σ^2_{Th}	400	350	370	420
μ_{Noise}	75	70	70	80
σ^2_{Noise}	26	25	20	24

Table 2 – Performance of the Five Chip Module (in e^-)

μ_{Th}	σ^2_{Th}	μ_{Noise}	σ^2_{Noise}
6360	380	70	20
2900	380	74	28
1030	400	75	26

Table 3 – Performance of One Chip in the Five Chip Module (in e^-)

The flex circuit has several digital lines (21 differential and 11 single ended lines) that can inject noise into the sensor underneath it. For this reason a solid ground plane was placed in the bottom layer of the flex circuit to avoid that the digital activity would interfere with the sensor charge collection. The comparison of these results with the results of a single FPIX1 chip shows no noticeable degradation in performance [5]. Figure 8 shows the hit map of a pixel chip in the 5-chip pixel module using a radioactive source (Sr 90). Furthermore, tests with a deadtimeless mode, where the charge injected into the front end is time-swept in relation to the readout clock also does not reveal any degradation in performance, indicating no crosstalk problems between the digital and analog sections of the FPIX1 and flex circuit.

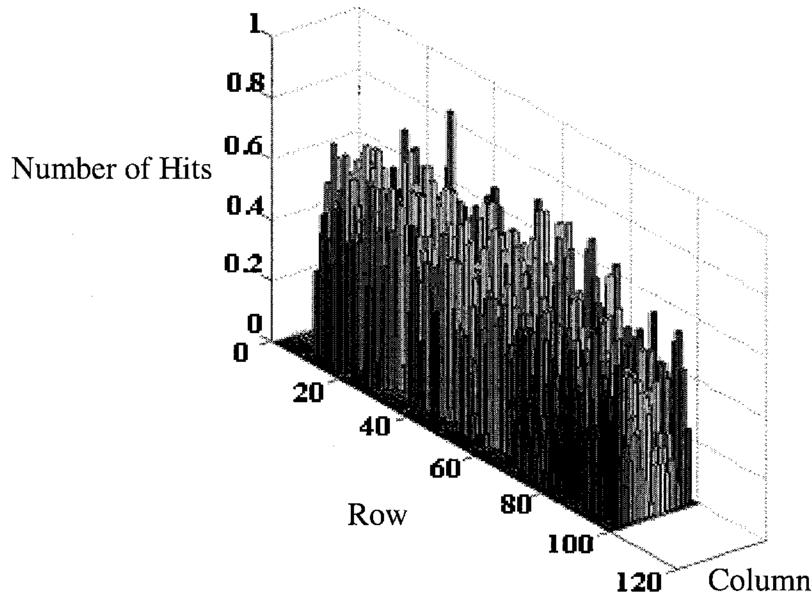

Figure 8 – Pixel Chip Hit Map

Second Pixel Multichip Module Prototype Packaging

Figure 9 shows a sketch of the second pixel multichip module prototype. This design uses the FPIX1 version of the Fermilab Pixel readout IC [3].

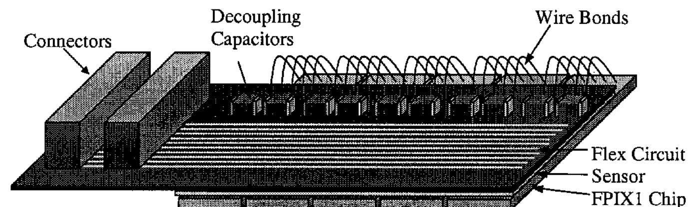

Figure 9 – Sketch of the Pixel Multichip Module

The pixel module is composed of three layers, as depicted in Figure 10. The pixel readout chips form the bottom layer. The back of the chips is in thermal contact with the station supporting structure, while the other side is flip-chip bump-bonded to the silicon pixel sensor. The clock, control, and power pad interfaces of FPIX1 extend beyond the edge of the sensor [6].

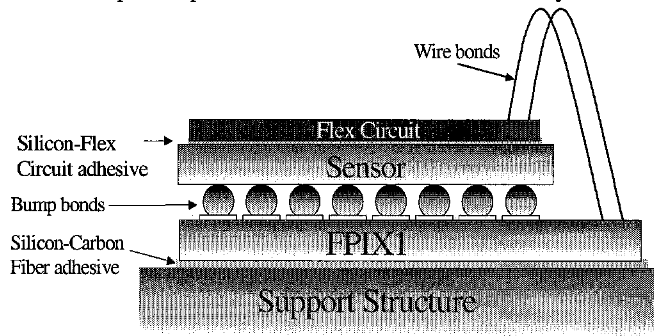

Figure 10 – Sketch of the Pixel Multichip Module "Stack"

The interconnect circuitry (flex circuit) is placed on the top of this assembly and the FPIX1 pad interface is wire-bonded to the flex circuit. The circuit then extends to one end of the module where low profile connectors interface the module to the data acquisition system. The large number of signals in this design imposes space constraints and requires aggressive design rules, such as 35 μm trace width and trace-to-trace clearance of 35 μm.

This packaging requires a flex circuit with four layers of copper traces (as sketched in Figure 11). The data, control and clock signals use the two top layers, power uses the third layer and ground and sensor high voltage bias use the bottom layer. The flex circuit has two power traces, one analog and one digital. These traces are wide enough to guarantee that the voltage drop from chip to chip is within the FPIX1 ±5% tolerance. The decoupling capacitors in the flex circuit are close to the pixel chips. The trace lengths and vias that connect the capacitors to the chips are minimized to reduce the interconnection inductance. A picture of the flex circuit made by CERN is shown in Figure 12.

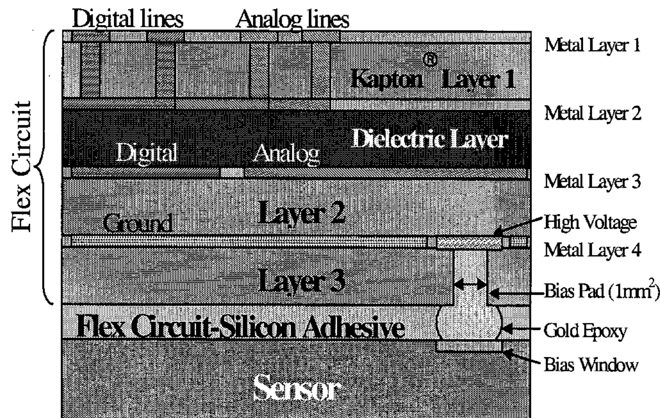

Figure 11 – Sketch of Flex Circuit Cross Section

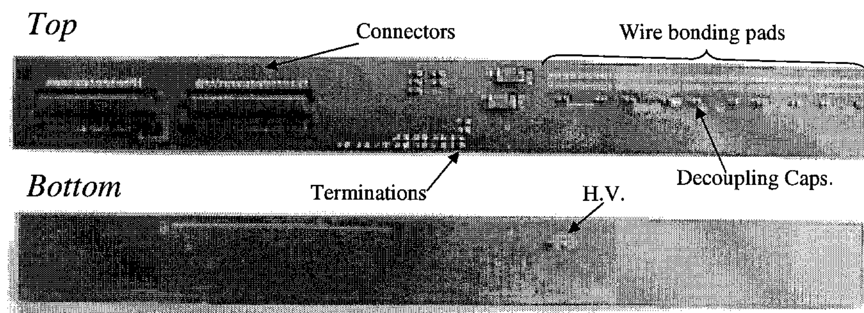

Figure 12 – Flex Circuit Picture

To minimize coupling between digital and analog elements, signals are grouped together into two different sets. The digital and analog traces are laid out on top of the digital and analog power supply traces, respectively. Furthermore, a ground trace runs between the analog set and the digital set of traces.

High Voltage Bias

The pixel sensor is biased with up to 1000 VDC through the flex circuit. The coupling between the digital traces and the bias trace has to be minimized to improve the sensor noise performance. To achieve this, the high voltage trace runs in the fourth metal layer (ground plane, see Figure 11) and bellow the analog power supply trace. The high voltage electrically connects to the sensor bias window through Gold epoxy. An insulator layer in the bottom of the flex circuit isolates the ground in the fourth metal layer of the flex circuit from the high voltage of the pixel sensor.

Assembly

The interface adhesive between the flex circuit and the pixel sensor has to compensate for mechanical stress due to the coefficient of thermal expansion mismatches between the flex circuit and the silicon pixel sensor. Two alternatives are being pursued. One is the 3M thermally conductive tape [7]. The other is the silicone-based adhesive used in [8].

The present pixel module prototypes were assembled using the 3M tape with a thickness of 0.05mm. Before mounting the flex circuit onto the sensor, a set of dummies with bump-bond structures where used to evaluate the assembly process. This assembly process led to no noticeable change in the resistance of the bumps. Figure 13 shows a picture of the dummy.

Figure 13 – Dummy Bump Bond Structure

Pixel Module Experimental Results

Two pixel module prototypes were characterized. One of these modules is a single readout IC (FPIX1) bump bonded to a SINTEF sensor (Figure 14) using Indium bumps. In the second pixel module the readout IC is not bump bonded to a sensor (Figure 15). In this prototype the flex interconnect is located on the top of the sensor (as in the baseline design).

The pixel modules have been characterized for noise and threshold dispersion. These characteristics were measured by injecting charge in the analog front end of the readout chip with a pulse generator and reading out the hit data through a PCI based test stand. The results for different thresholds are summarized in Table 4.

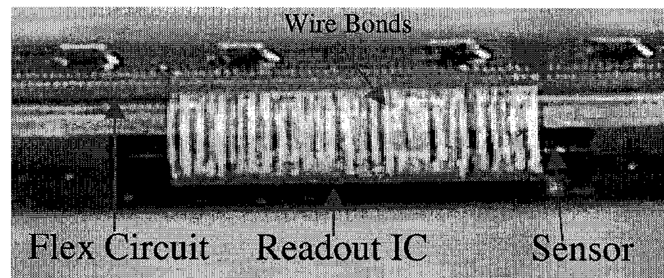

Figure 14 – Pixel Module with SINTEF Sensor

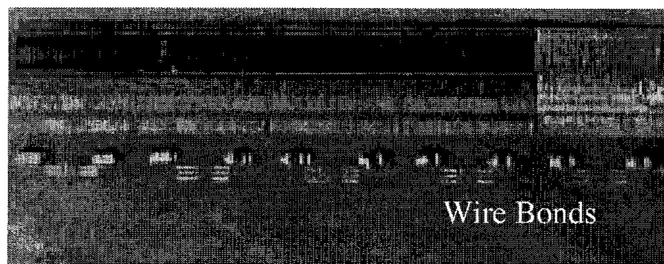

Figure 15 – Pixel Module without Sensor

Without Sensor				*With Sensor*			
μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}	μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}
7365	356	75	7	7820	408	94	7.5
6394	332	78	12	6529	386	111	11
5455	388	79	11	5500	377	113	13
4448	378	78	11	4410	380	107	15
3513	384	79	12	3338	390	116	20
2556	375	77	13	2289	391	117	21

Table 4 – Performance of the Pixel Prototype Modules (in e^-)

The comparison of these results with previous results (single readout IC without the flex circuit on top) shows no noticeable degradation in the electrical performance of the pixel module [9]. Figure 16 shows the hit map of the pixel module with sensor using a radioactive source (Sr 90), confirming that the bump bonds remain functional.

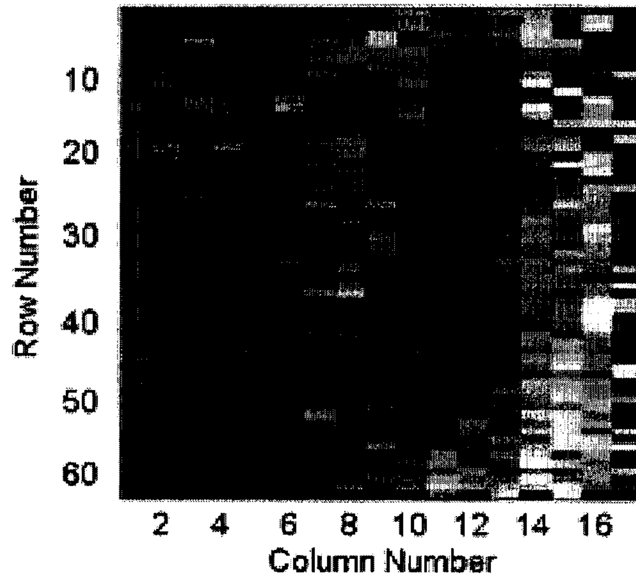

Figure 16 – Pixel Module Hit Map

Results of the Hybridization to Pixel Sensors

The hybridization approach pursued offers maximum flexibility. However, it requires the availability of highly reliable, reasonably low cost fine-pitch flip-chip mating technology. We have tested three bump bonding technologies: indium, fluxed solder, and fluxless solder. Real sensors and readout chips were indium bumped at both the single chip or wafer level by BOEING, NA. Inc (Anaheim, CA) and Advance Interconnect Technology Ltd. (Hong Kong) with satisfactory yield and performance.

We have recently received a new batch of single chip detectors and modules bumped bonded at AIT. Figure 17 is a Scanning Electron Micrograph (SEM) showing the indium bumps deposited on the readout chip. The bumps are about 10 μm high and 12 μm wide at the base. Figure 18 is a picture of our new 5-chip module.

We have also conducted tests on dummy detectors (see Figure 13) to evaluate eutectic Pb/Sn solder. The vendor, MCNC (Research Triangle Park, NC), together with UNITIVE Electronics (Research Triangle Park, NC), produced the dummy parts, and then carried on with the bumping process. The detectors are composed of channels that are a number of daisy-chained bumps at 50 μm pitch connected to probe pads at an edge of the dummy detector. We characterized the bump yield by measuring the resistance of each channel, and (to check for shorts) the resistance between neighboring channels.

Both fluxed and fluxless solder bumps have been studied. We found much better results using the fluxless process. The yield from the fluxed process is poor. For the fluxless assemblies, a process called Plasma Assisted Dry Soldering (PADS) [10] is used. The bumped chip wafer (top plates of the dummies) and un-bumped substrate wafer (bottom plates of the dummies with only under-bump metallization put on) were diced and tacked together (flip-chip assembly) before being treated in the PADS process. The solder was then reflowed at 250°C. After being reflowed, the detectors were rinsed with methanol and dried in air. The diameter of the bumps is approximately 40 μm, and the height is approximately 15 μm after mating. We estimate that the single solder bump resistance is less than 1 Ω.

In the fluxed process, flux was introduced to the bumped parts before the reflow. The purpose of the flux is to break through the oxide barrier that is formed on the surface of the bumps, with which a good connection is not formed. Due to the corrosive nature of the flux it has to be washed away with solvents after mating. Problems occurred when rinsing away the flux residue because the bumps are small (15 μm high) and the bump pitch is fine (50 μm).

We have previously reported [11] a bump yield of 99.95% or $4.5x10^{-4}$ failure/bump. The causes of the failures have been identified and solutions have been adopted to overcome these problems. This has led to changes in the bumping process.

One of the main problems identified was the oxidization of the Under Bump Metallization (UBM) before the solder bumps were put on the part. This thin oxide layer prevents the formation of a good joint until it is "broken" through by the application of an electrical voltage. To overcome this, the vendor has developed a process of gold plating the UBM which prevents the oxidization. Figure 19 shows an example of the gold plating process.

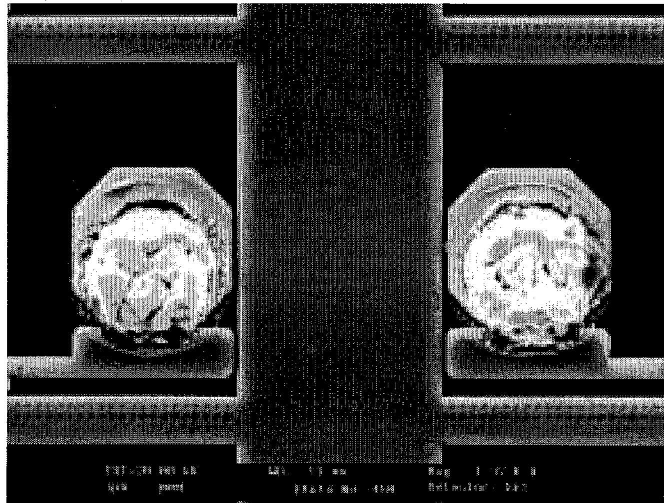

Figure 17 – Indium Bumps on the Readout Chip.

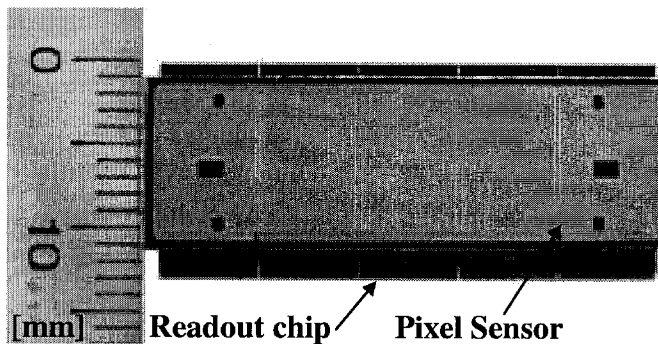

Figure 18 – 5-chip Pixel Module with Indium Bumps

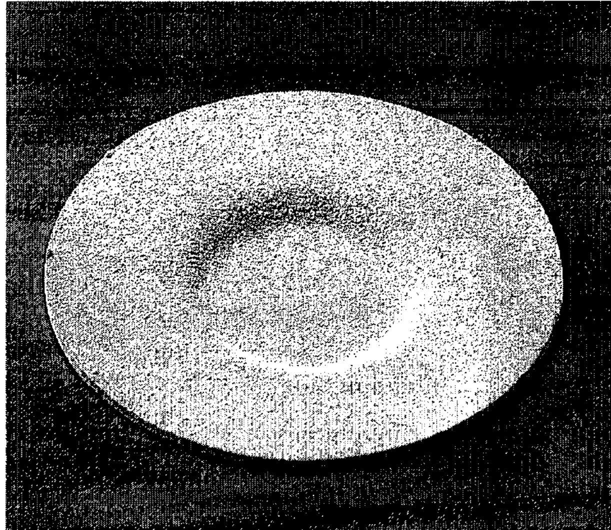

Figure 19 – Gold Plated Pad

Future Plans

A set of stack pixel modules will be mounted to form a pixel plane (see Figure 20). The mechanical support has to be as light as possible to reduce interactions with particles. The baseline design uses carbon composite structures that will include integrated cooling channels (tubes). Energy Science Laboratories, Inc. (San Diego, CA) will manufacture these structures by sandwiching nonporous carbon tubes between two sheets of carbon "flocking," which consists of many individual carbon fibers and looks like velvet material. Figure 21 shows a cooled carbon substrate prototype with two chips pasted on the structure. The "fuzzy carbon" surfaces of this structure will be machined to provide "shingled" surface on which the multichip assemblies will be mounted. This construction allows sensors on one side of the cooling support to overlap, and therefore allows two pixel measurement planes to be mounted on a single cooling support.

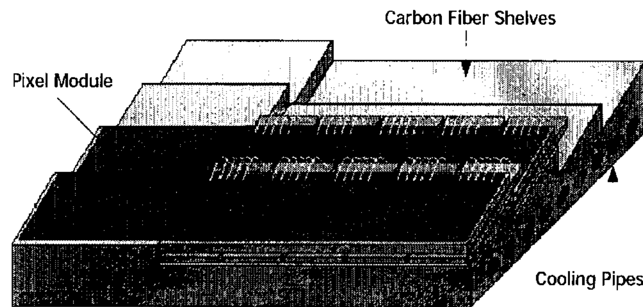

Figure 20 – Sketch of the Pixel Module "Shingled" Support Structure

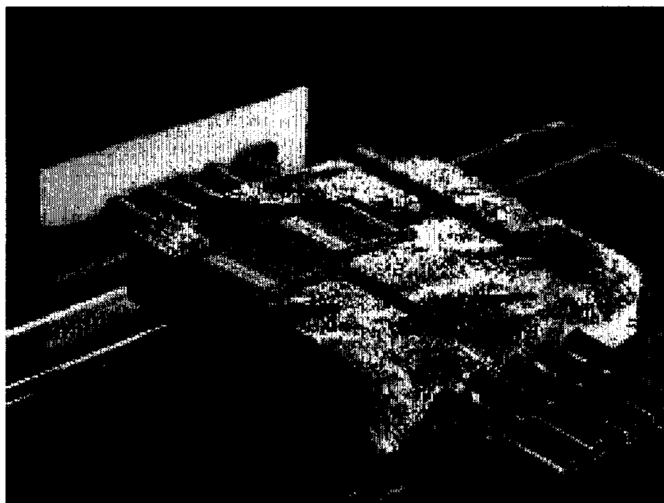

Figure 21 – Carbon Fiber Supporting Structure Prototype

Conclusions

We have described the baseline design pixel multichip module designed to handle the data rate required for the BTeV experiment at Fermilab. The assembly process of a single chip pixel module prototype was successful. A 5-chip pixel module prototype (Figure 18) will be assembled using the same process. The characterization of the two single-chip modules showed that there is no degradation in the electrical performance of the pixel module when compared with previous prototypes.

Indium bump bonding is proven to be capable of successful fabrication at 50 μm pitch on real detectors. For solder bumps at 50 μm pitch, good results have been obtained with the fluxless PADS processed detectors. The results are adequate for our needs and our tests have validated them as a viable technology. Inspection of the fluxed parts showed that the bumps are dirty, with stained marks, and a with flux residue spread around the part. The bad joints and connections are caused by the difficulty of removing the flux residues due to the small bump sizes and fine pitch. Incomplete removal of the flux residues leads to formation of dry joints. Furthermore, the flux residues may attack a good joint.

Reference

1. Kulyavtsev, A., et al., BTeV proposal, Fermilab, May 2000.
2. Seidel, S., "A Review of Design Considerations for the Sensor Matrix in Semiconductor Pixel Detectors for Tracking in Particle Physics Experiments," Nucl. Instr. and Meth., A 465, pp. 267-296, 2001.
3. Christian, D.C., et al., "Development of a pixel readout chip for BTeV," NIM A 435, pp.144-152, 1999.
4. Hall, B., et al., "Development of a Readout Technique for the High Data Rate BTeV Pixel Detector at Fermilab", to be presented in the 2001 Nuclear Science Symposium and Medical Imaging Conference, San Diego, November 2001.
5. Zimmermann, S., et al., "Development of High Data Readout Rate Pixel Module and Detector Hybridization at Fermilab," Pixel 2000 Conference, Genoa 2000.
6. Cardoso, G., et al., "Development of a high density pixel multichip module at Fermilab", 51st ECTC, Orlando, Florida, May 28-31, 2001.
7. Thermally Conductive Adhesive Transfer Tapes, Technical datasheet, 3M. April 1999.
8. Abt, I., et al., "Gluing Silicon with Silicone", Nucl. Instr. and Meth. A 411, pp. 191-196, 1998.
9. Mekkaoui, A., et al., "FPIX2: an advanced pixel readout chip," 5th Workshop on Elect. LHC Exp., Snowmass, pp. 98-102, Sept. 1999.
10. Koopman, N. et al., "Fluxless No-Clean Assembly of Solder Bumped Flip Chips," 46th ECTC, Orlando, Florida, May 28-31, 1996.
11. Cihangir, S., Kwan, S., "Characterization of Indium and Solder Bump Bonding for Pixel Detectors", 3rd Int. Conf. on Radiation Effects on Semiconductors Materials. Fermilab – Conf. 00/168-C. Florence, June 2000.