Fermilab FERMILAB-Conf-00/316-E December 2000

FPIX2: A Radiation-Hard Pixel Readout Chip for BTeV

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A radiation-hard pixel readout chip, FPIX2, is being developed at Fermilab for the recently approved BTeV experiment [1]. Although designed for BTeV, this chip should also be appropriate for use by CDF and DZero. A short review of this development effort is presented. Particular attention is given to the circuit redesign which was made necessary by the decision to implement FPIX2 using a standard deep-submicron CMOS process rather than an explicitly radiation-hard CMOS technology, as originally planned. The results of initial tests of prototype 0.25μ CMOS devices are presented, as are plans for the balance of the development effort.

1 Introduction

The most striking feature of BTeV, which is expected to begin running in 2006 in the new CZero region of the Fermilab Tevatron, is that the experiment will use data from a pixel vertex detector to reconstruct tracks and vertices *for every beam crossing*. The lowest level trigger will be an impact parameter trigger designed to identify events containing the reconstructable decays of charm and bottom particles [2]. An R&D program to develop a pixel readout chip for BTeV was started at Fermilab in 1997. The status of this program and its prospects are described in this paper.

2 FPIX Development History

In order to satisfy the needs of BTeV, the pixel readout chip must have an unusually high output bandwidth. It must also be radiation-hard. A series of prototype chips has been designed and tested. In 1997, it was assumed that the final chip would be fabricated using a radiation-hard 0.5μ SOI process. The plan was to develop the chip using radiation-soft CMOS technologies similar to

the target process. The final development step would be the translation of the design to the radiation-hard process. The first two generations of prototype devices (FPIX0 [3] and FPIX1 [4]) were designed using Hewlett Packard 0.8μ and 0.5μ CMOS, respectively. In December, 1998, the decision was made to try to use a standard commercial deep-submicron CMOS technology for the pixel readout chip instead of an explicitly radiation-hard process. This decision was made based on the results of RD49, which indicated that with proper design techniques, circuits realized in standard deep-submicron technologies might be at least as radiation-hard as circuits realized using explicitly radiation-hard CMOS technologies [5]. Commercial deep-submicron CMOS processes are more widely available than explicitly radiation-hard processes. Since they are used primarily for commodity electronics, they promise to be much less expensive than the radiation-hard processes. This not only reduces the cost of the final chip, it also makes it practical to design prototype devices using the same process that will be used for the final chip, thus eliminating a final development step.

3 Radiation Tolerant CMOS Design

The basic radiation damage mechanism in CMOS circuits is that ionizing radiation causes positive charge to be trapped in the oxide layers near the surface of the chip [6]. The magnitude of the charge increases with radiation dose. Charge trapped in the gate oxide is equivalent to a voltage applied to the gate of a transistor, and therefore causes a "threshold shift." CMOS processes with small feature size have thinner gate oxide layers than processes with larger feature size. In the very thin gate oxide layers of deep-submicron CMOS devices, some of the radiation-induced charge is able to tunnel out of the gate oxide into the gate or substrate, dramatically reducing the effect of the ionizing radiation. The resulting threshold shifts are often small enough to be inconsequential. However, the relatively thicker oxide used everywhere except over the transistor gates does still become charged. The charge trapped in the thicker oxides causes leakage currents in standard NFET's, and depending on circuit layout, also leads to currents between transistors. Currents between transistors are avoided by the use of guard rings, and leakage current is avoided by wrapping each NFET gate completely around the source or drain. However, the gate-all-around technique imposes constraints on NFET layout. As Fig. 1 illustrates for the case of a circular transistor, the gate-all-around technique introduces a correlation between the length and width of a transistor gate. Consequently, there is a minimum value of the ratio (W/L) of gate width to length [8]. NFET's with very small W/L are impossible to implement as single gate-all-around transistors.

The front end circuit designed for FPIX0 and FPIX1 (Fig. 2) was inspired by

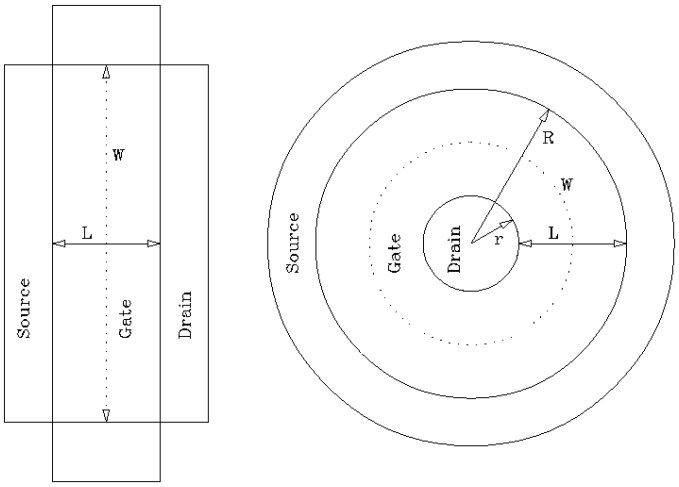

Fig. 1. A standard MOS transistor (left) can have any value of W/L. For a circular gate-all-around transistor (right), W/L $\approx \pi$(R+r)/(R-r). For this type of transistor, W/L may be arbitrarily large, but can not be less than W/L$\approx \pi$ (corresponding to R$\rightarrow$ infinity).

a design developed at CPPM for the ATLAS pixel detector [7]. The feedback element used in the first stage of the preamplifier consists of an explicit capacitor, and a transistor circuit. The transistor circuit acts like a large resistor for small input pulses and small leakage current. In the presence of a large pulse, or a large leakage current, the transistor circuit switches so that an externally-fixed current discharges the feedback capacitor. This simple circuit provides both fast and tunable return to baseline for large signals, and compensation for leakage currents as large as 100 nA. Unfortunately, both of the transistors in this circuit must be NFET's and must have W/L$\ll$1 [9]. This circuit can not be implemented in deep-submicron CMOS using the gate-all-around layout technique. Our decision to use deep-submicron CMOS meant that the FPIX front end needed to be significantly redesigned.

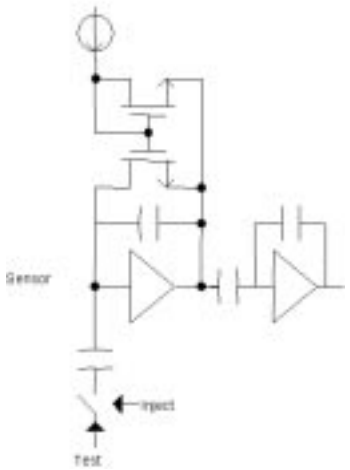

Fig. 2. FPIX0/FPIX1 front end.

4 FPIX2 Front End Design

In the redesigned FPIX front end, leakage current compensation and prompt return to baseline for large pulses are provided by two separate circuits. These circuits are described in detail in Ref. [9]. Leakage current compensation is provided by a differential amplifier which compares the input and output voltages of the first stage of the pixel amplifier and controls a current source, I_C, to directly offset the leakage current, I_L (see Fig. 3). Since this amplifier is placed in feedback of the first stage of the pixel amplifier, it must have *very low* bandwidth. In fact, a large fraction of the area of the FPIX2 front end is devoted to capacitors which kill the frequency response of this amplifier. The feedback element of the first stage of the pixel amplifier still contains a transistor which acts like a large resistor for small signals and provides a current to quickly return large signals to baseline. However, in the new design, this transistor is no longer required to carry the current which cancels the leakage current. This, together with the fact that it is biased by a single bias circuit (one per chip), means that a gate-all-around transistor with close to minimum W/L has adequate properties for use in the feedback circuit.

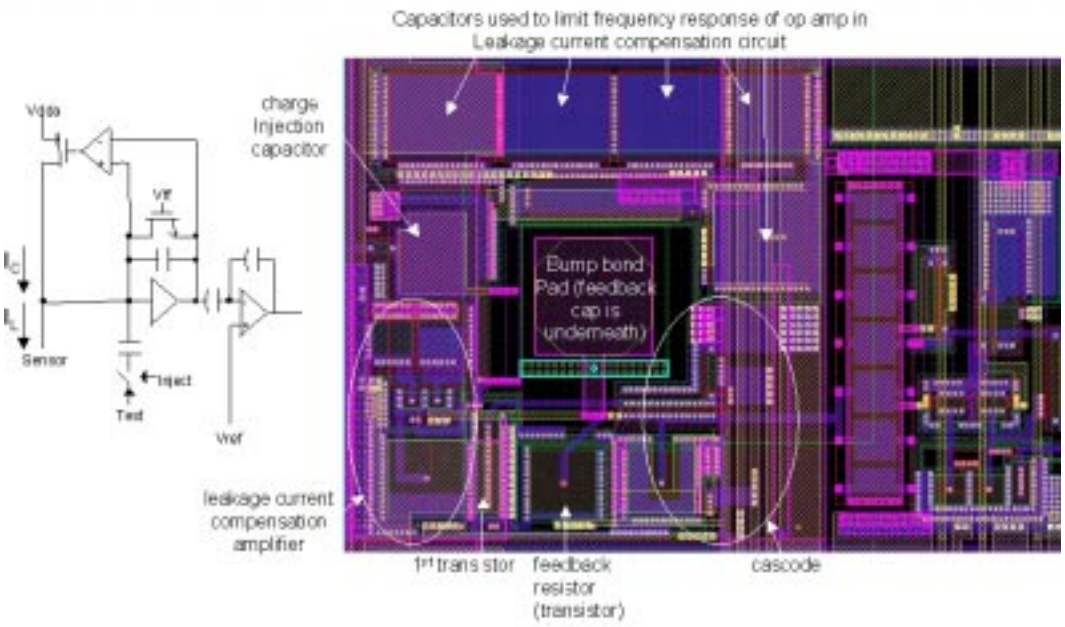

Fig. 3. FPIX2 front end layout.

Prototype "preFPIX2" circuits have been fabricated in two different 0.25μ CMOS processes [1] . The new feedback and leakage current compensation circuits have been tested and they perform as intended. Prototypes fabricated by

[1] FPIX2 is being designed so that it may be fabricated using either Tiawan Semiconductor Manufacturing Company 0.25μ CMOS or the 0.25μ CMOS process available to us through CERN.

TSMC have been exposed to ∼33 MRad of gamma irradiation using the ^{60}Co source at Argonne National Laboratory. Fig. 4 shows that amplifier noise and discriminator threshold dispersion were essentially unchanged by the irradiation. Fig. 5 shows the pulse response of the FPIX2 front end before and after irradiation. Exactly the same bias voltages and control currents were applied before and after irradiation.

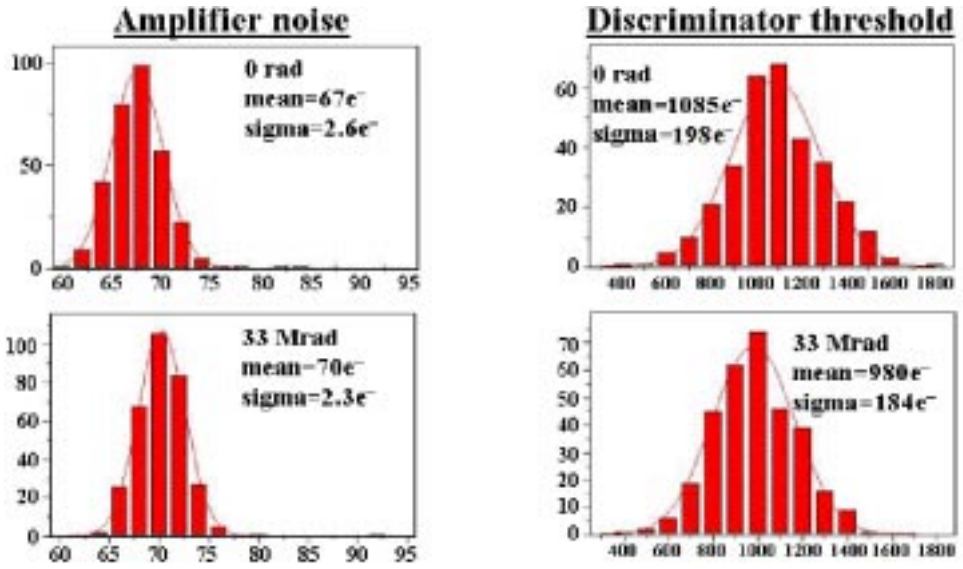

Fig. 4. PreFPIX2T radiation tolerance. The plots on the left show the measured amplifier noise for the 320 cells of a preFPIX2T chip, before and after irradiation. The plots on the right show the distribution of discriminator thresholds for the same 320 cells, before and after irradiation.

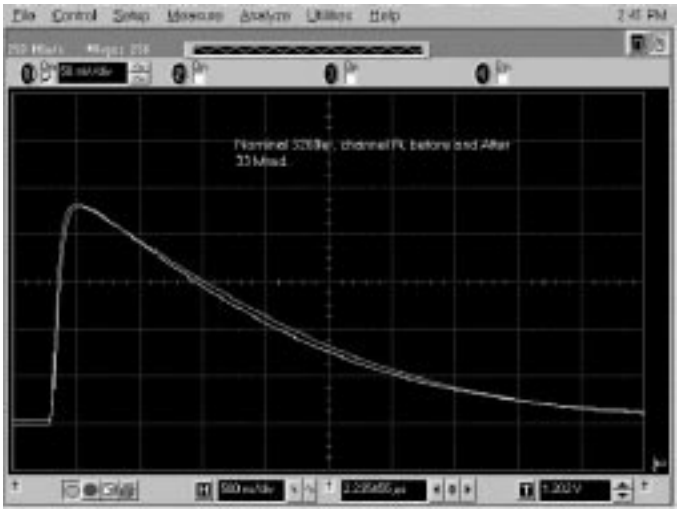

Fig. 5. PreFPIX2T pulse response: One trace was recorded before the irradiation; the other was recorded after irradiation.

5 FPIX2 Development Roadmap

As we have made the shift to a deep-submicron design, we have continued the evolutionary development of the fast FPIX readout architecture. The FPIX2 readout is simplified with respect to FPIX1. While the FPIX1 architecture allowed both externally triggered and self triggered operation, FPIX2 uses only self triggered readout. The simpler end-of-column logic in FPIX2 operates significantly more efficiently than FPIX1 [10]. We have also made progress towards a chip which will require a minimum of control connections. A second preFPIX2 circuit fabricated by TSMC is due in December 2000. This chip contains both a new programming interface and digital to analog converters to set discriminator threshold voltages, critical bias voltages and currents, and the return-to-baseline reference current.

In early December, 2000, preFPIX2 circuits manufactured in a joint submission with ALICE through CERN will be exposed to 200 MeV protons at the Indiana University Cyclotron Facility. This test will focus on the possibility that single event gate rupture may cause individual pixel amplifiers to become noisy, or cause individual pixel discriminators to change behavior. Early in 2001, the TSMC prototypes containing the new programming interface and DAC's will also be exposed at the Indiana University Cyclotron Facility and single event upset cross sections will be measured. Based on the results of these measurements, the design of the programming interface and its associated registers will be finalized.

During the first half of 2001, we will finalize the FPIX2 specifications. This includes a final specification of the number of $50\mu \times 400\mu$ pixels in the chip, and the output data format. We currently expect to use a differential point-to-point output protocol, but we have not yet determined the width of the output word or the output clock frequency. We expect a fully functional FPIX2 chip to be submitted before the end of 2001. If all goes well, this will be the final BTeV pixel readout chip.

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