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CHALLENGES ASSOCIATED WITH A LOW FREQUENCY CHARGE INTEGRATOR AND ENCODER FOR THE CDF II CALORIMETER

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The SMQIE is the newest member of the QIE family of integrated circuits. It has been developed specifically for the Shower Max Detector upgrade of the CDF Plug and Central Calorimeters at Fermilab. Like its predecessors, it converts charges over a wide dynamic range with a variable resolution. Unlike its predecessors it contains its own Flash, trigger delay pipeline and buffer area. Furthermore, it operates both at a lower frequency and with only a simple 5-volt power supply. The simultaneous requirements of low frequency and reduced voltage force the front end into a low current, high impedance regime. Specialized circuitry is necessary to prevent charge slopped-over into subsequent time slices. The considerable amount of digital circuitry monolithic with the analog front end makes for a noisy substrate. Specialized circuitry and layout techniques are necessary to keep this chip from being noise-limited. The final design is a two-channel single-ended Charge Integrator and Encoder (QIE) that operates at a frequency of 7.6MHz with a least significant bit resolution of 15 fC in its lowest range.

1 Introduction

QIEs or Charge Itegrator and Encoder ASICs are a family of integrated circuits developed at Fermilab specifically for High Energy Physics experiments [3]. They are particularly suited to Calorimetry experiments and have, in a very brief period of time, found homes in such experiments as CDF, KTeV and CMS. In a word, QIEs are analog-to-digital converters (ADCs) which convert into scientific notation. More specifically, they provide a broad dynamic range with a variable resolution by splitting input charges into eight binary-weighted ranges and integrating those signals onto eight capacitors (one per range). From these integrated signals, one range is selected. The chosen range and its capacitor voltage become the exponent and mantissa, respectively. This QIE process is illustrated in Figure 1.

The Shower Max Detector is a two-dimensional position sensitive device

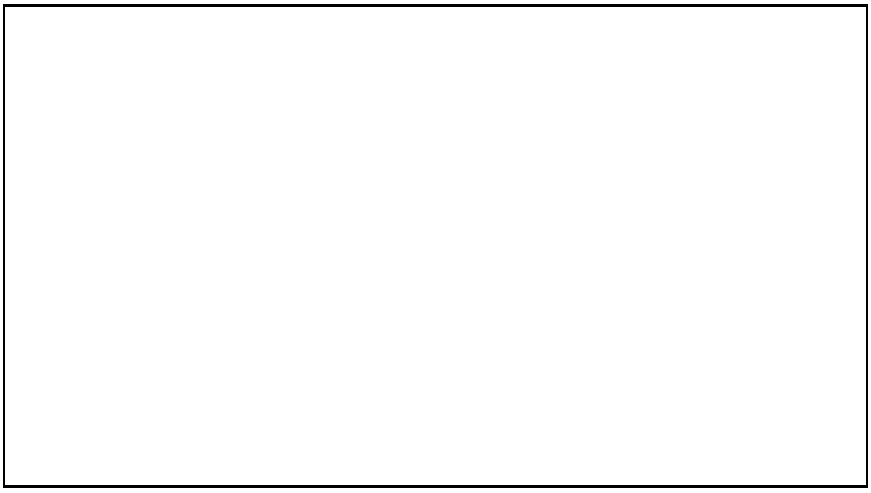

Figure 1. The QIE Process. The horizontal axis is the total input charge integrated over the 132ns time slice. The vertical axis are, from bottom to top, the range number of the selected capacitor, the encoded digital exponent resulting from the range selection, the Analog Output voltage resulting from the range selection, and the encoded digital output of the FADC resulting from the selected Analog Output.

sandwiched inside the electromagnetic calorimeter and placed at the shower maximum [1]. Its purpose is to aid in the identification of electrons and photons, to separate photons from π^0, and to help identify electromagnetic showers. Within the CDF detector, there are two calorimeters, the Plug and the Central, which are similar in function but very different in implementation. The CDF Technical Design Report calls for a ShowerMax detector in each calorimeter. The SMQIE is a QIE designed to fit the needs of the ShowerMax project.

The QIE Process of Figure 1 is accomplished in the SMQIE by the architecture shown in Figure 2. Charge is input into the emitters of an array of 128 bipolar transistors in a common base configuration. The collectors of these transistors are arranged in binary groups to provide the binary weighted splitting of the input. Above this Splitter are eight independent circuits, one per range. These independent circuits, known as the Range Circuitry, consist of the Cascode which regulates the voltage across the Splitter, the Dump circuit, which diverts overflow currents from the integrating capacitors and the Switch circuit whose primary function is to pipeline input charges into one of four integrating capacitors thus providing deadtime-less operation.

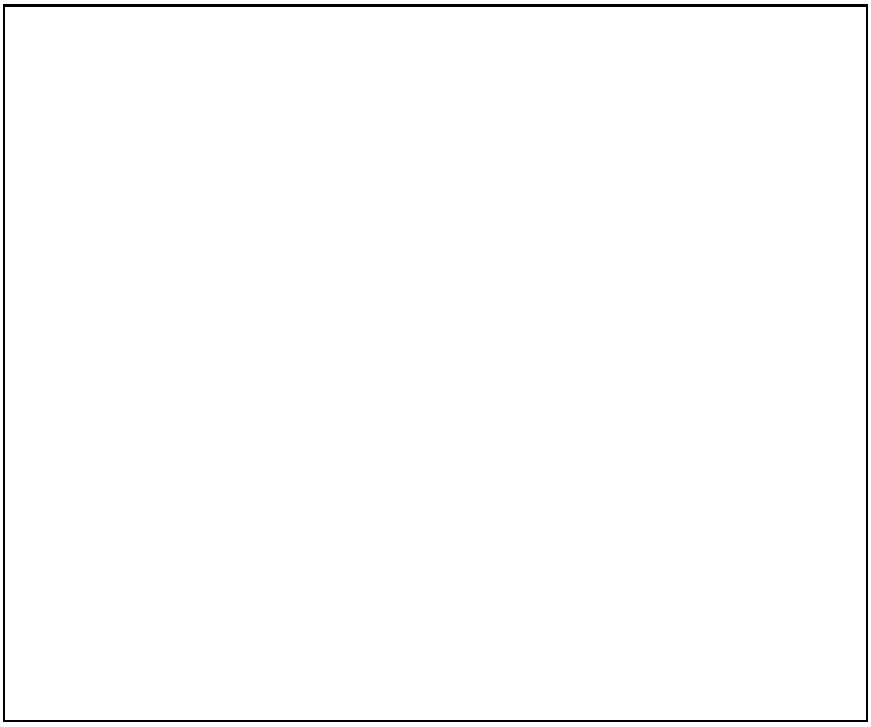

Figure 2. A Block Diagram of the SMQIE. The QIE is described herein. The Flash is a 5 bit CMOS FADC. The Delay is a 38 stage CMOS FIFO. The Buffer holds up to four triggered data words.

For a detailed description of the SMQIE, the reader is referred to [2].

2 Frequency Response

It is required that the Least Significant Bit resolution on Range0 be 12.5 fC [4]. With 32 counts per range (i.e. a 5-bit mantissa), this means that Range0 covers 400 fC. Given this, the calculation of capacitance of the integrating capacitors is very straightforward. $\Delta Q = C\Delta V$ where ΔQ is 400 fC and ΔV is 1 volt (see Figure 1). Clearly, C is 400 fF. From this, and from the fact that the integration time is 132 ns, the splitter bias current is constrained to be $6\mu A$. This bias current is smaller than that used in any other QIE by a factor of more than thirty. Moreover, this bias current forces the input impedance of

the SMQIE to almost 4.5kΩ for small inputs, and this is unacceptibly large. Control theory shows that the input impedance is reduced by a factor equal to the gain of the feedback amplifier shown in Figure 2. However, the gain of the feedback amplifier is itself constrained by necessities in size and bandwidth. Therefore, arbitrarily large feedback amplifier gains are not possible for the SMQIE. To make matters worse, this high impedance problem repeats itself more dramatically in the Range Circuitry at the interface between the Splitter and the Cascode.

To summarize, the long integration time and the required resolution of the lowest range together force the bias current to be very small ($6\mu A$). This, in turn, forces the SMQIE into a high-impedance regime at both the Splitter and the Cascode (in each range). In short, frequency response suffers dramatically.

The solution to this problem is to increase the current passing through the Splitter and Cascode. However, since the resolution of the SMQIE is defined by the amount of current reaching the integrating capacitors, any current added to the chip to improve its frequency response must be extracted before it reaches the integrating capacitors. To further complicate the problem, current must be added below the splitter, but it must be extracted in binary increments from each range circuit because the Splitter splits the bias current as well as the input current. To solve this problem, excess current is simultaneously added to the input of the Splitter and to the input of an "Excess" Splitter whose purpose is only to divide the excess current in a binary fashion. The split excess currents are extracted from each range above Cascode circuit via PMOS current mirrors.

A second problem related to frequency response occurs in the Dump Circuit. Once the Dump activates, all current, including bias, flows through the Dump. The Switch circuit gets current starved and it takes a very long time to restore nominal operating voltages. The net result is a "Dump Memory" in the SMQIE in which, if a range dumps in time slice X, then in time slice X+1, charge will be pulled from the integrating capacitor to restore proper operating voltages. This borrowing of charge appears as an erroneous signal in the X+1 time slice. In order to overcome this problem, an NMOS clamping transistor is added in parallel to each integrating capacitor. The clamping transistor works in conjunction with the Dump circuit and the Switch circuit. When the anode of the integrating capacitor falls low enough to turn the clamping transistor ON, the clamping transistor begins to divert current from the integrating capacitor. After the excess charge is dumped, current must still flow through the Switch circuit because of the clamping transistor. This allows the Switch circuit to restore the Range to its proper operating voltages before the next time slice.

3 Noise Reduction

The SMQIE contains more digital circuitry than any previous QIE. As a consequence, its sensitive analog front-end needs to be protected from a lot of noise. In modern mixed-mode VLSI, there are two principal means of noise coupling [7, 5, 6]. First, there is the mutual inductance and capacitance between any two bond wires and pins in a package. Second, there is coupling through the common substrate.

The primary factor in the reduction of coupling between bond wires is distance and the arrangement of pads. It is for this reason that all of the sensitive analog inputs and outputs are arranged on the bottom of the chip, 6.4mm from the digital outputs.

A second factor is the elimination of common impedances between references of two different circuits. To accomplish this, analog and digital power supplies and grounds are kept separate from one another. In fact, there are separate power supplies in each channel for the QIE, the Flash, and the digital backend. The substrate connection throughout the digital section has its own pins. Finally, the digital outputs have their own power supply.

The third factor is the choice of digital output driver. For the ShowerMax, Low-Voltage Differential Signaling (LVDS) is very desirable because of the reduction in output voltage swing and the consequent reduction in capacitive coupling and because it represents a constant current draw on the power supplies. However, standard LVDS is a point-to-point communications protocol and the SMQIE needs to be bussed. Therefore a custom LVDS-like driver was designed for the SMQIE. While obeying LVDS voltage and current conventions, the driver can be tri-stated and therefore bussed. Moreover, when the driver is tri-stated, a current path is opened within the chip which, rather than interrupting current flow, re-directs it through an internal resistor. This prevents large and noisy transients in the power supplies.

Coupling through the common substrate is controlled by distance, guard rings, and substrate contacts. Concentric rings of n+ and p+ guard rings surround every sensitive circuit in the SMQIE as well as every significant noise generator. The p+ guard rings act as current sinks that keep the current in their vicinity quiet. The n+ guard rings, on the other hand, act as barriers to substrate current flow. All of the substrate contacts in the digital section of the chip are run to independent pins on the periphery. In the QIE sections, the analog ground is connected directly to the substrate.

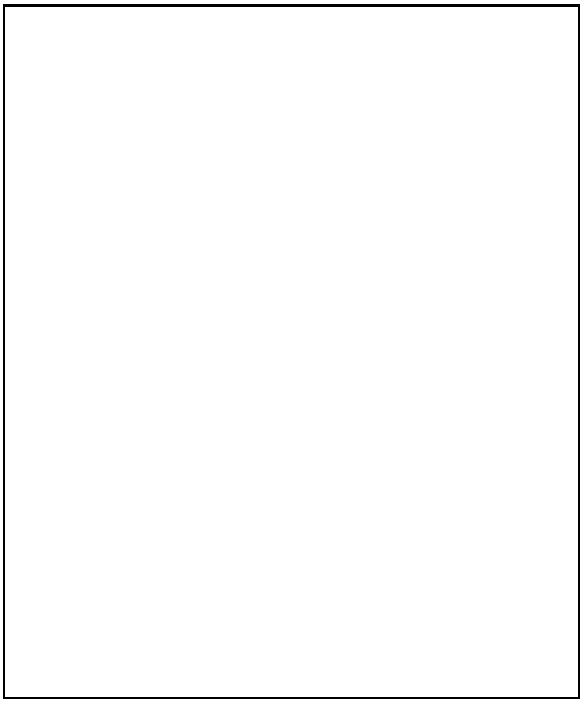

Figure 3. SMQIE Charge reconstruction and residuals.

4 Results and Conclusions

The SMQIE has passed through a number of prototyping steps, and the result is highly satisfactory. The SMQIE has been extensively bench tested under conditions similar to the expected operating environment. Moreover, additional groups at Argonne National Lab and at the Fermi National Accelerator Lab are using the SMQIE in calorimeter wedge tests in anticipation of the start of Run II.

Figure 3 shows an output charge reconstructed from Range and Mantissa values as a function of input charge. Also shown in Figure 3 is the fractional residual of the reconstituted charge. The vast majority of the residuals are well within the required 3 percent. However, at very low input charges, a few residuals are as high as 6 percent. For low input charges, there is some charge-loss into the next time slice. This loss is acceptible

In conclusion, the SMQIE is working and the results are excellent. However, significant problems arose due to the selection of integration time and resolution. Previous QIE chips which were operated at a higher frequency suffered from parasitic charge loss when the duration of the input signal was longer than the integration time. The SMQIE is evidence that reducing the clock frequency introduces its own set of problems to the QIE architecture, namely high-impedance and poor frequency response. Fortunately, these problems can be overcome with careful design and testing.

At the time of this writing, production runs of SMQIE chips have returned from the manufacturer and are being tested for implementation in Run II at CDF.

Acknowledgements

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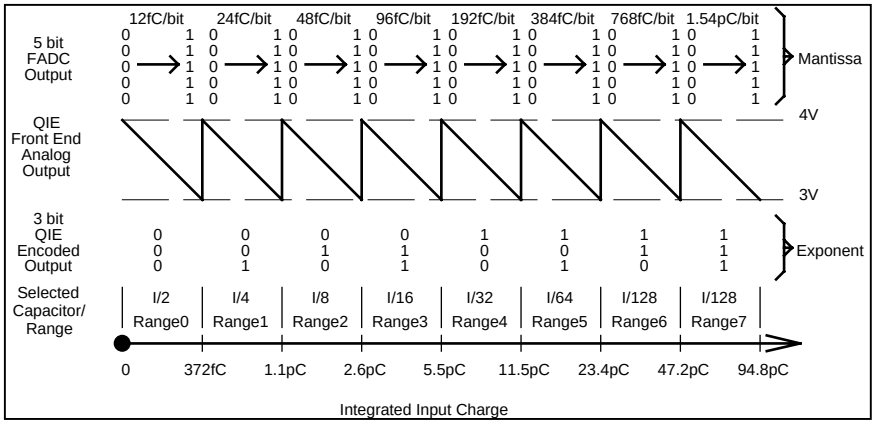
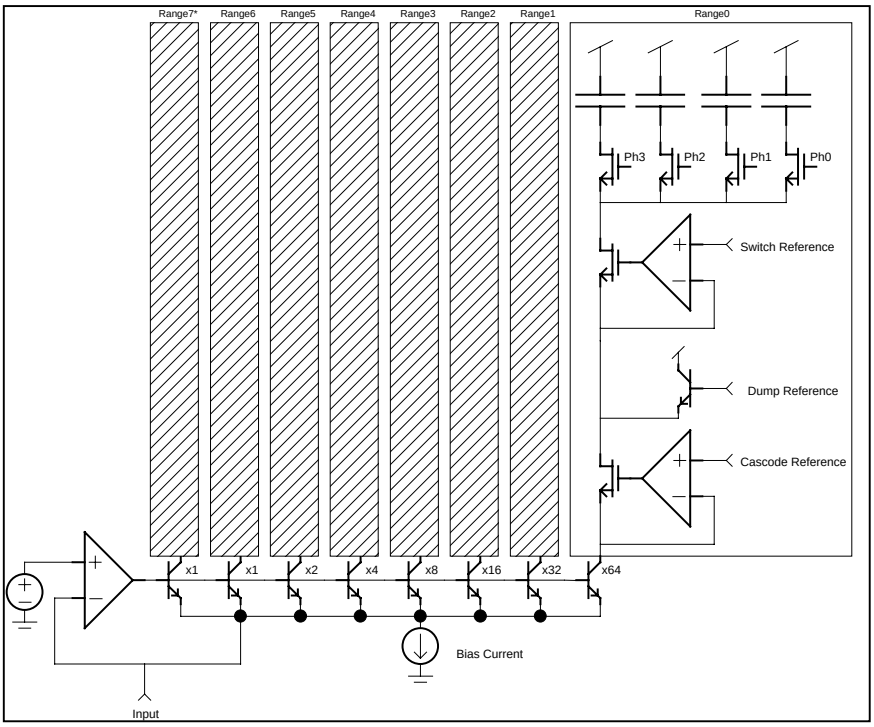
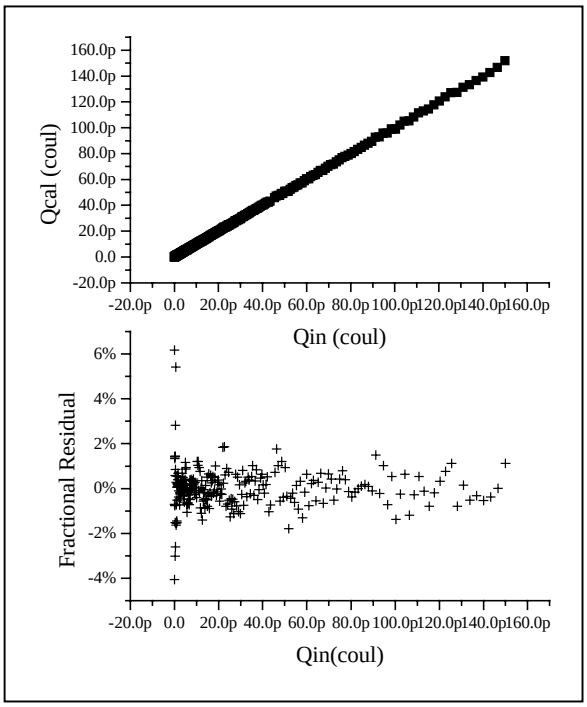

12fC/bit
24fC/bit
48fC/bit
96fC/bit
192fC/bit
384fC/bit
768fC/bit
1.54pC/bit
5 bit FADC Output
Mantissa
QIE Front End Analog Output
4V
3V
3 bit QIE Encoded Output
Exponent
Selected Capacitor/ Range
I/2
I/4
I/8
I/16
I/32
I/64
I/128
I/128
Range0
Range1
Range2
Range3
Range4
Range5
Range6
Range7
0
372fC
1.1pC
2.6pC
5.5pC
11.5pC
23.4pC
47.2pC
94.8pC
Integrated Input Charge


Range7*
Range6
Range5
Range4
Range3
Range2
Range1
Range0
Ph3
Ph2
Ph1
Ph0
Switch Reference
Dump Reference
Cascode Reference
x1
x1
x2
x4
x8
x16
x32
x64
Bias Current
Input


160.0p
140.0p
120.0p
100.0p
80.0p
60.0p
40.0p
20.0p
0.0
-20.0p
Qcal (coul)
-20.0p 0.0 20.0p 40.0p 60.0p 80.0p 100.0p120.0p140.0p160.0p
Qin (coul)
6%
4%
2%
0%
-2%
-4%
Fractional Residual
-20.0p 0.0 20.0p 40.0p 60.0p 80.0p 100.0p120.0p140.0p160.0p
Qin(coul)