



Fermi National Accelerator Laboratory

FERMILAB-Conf-97/427

SVX3: A Deadtimeless Readout Chip for Silicon Strip Detectors

T. Zimmerman et al.

*Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510*

December 1997

Published Proceedings of the *Frontier Detectors for Frontier Physics: 7th Pisa Meeting on Advanced Detectors*, La Biodola, Isola d'Elba, Italy, May 25-31, 1997

Operated by Universities Research Association Inc. under Contract No. DE-AC02-76CH03000 with the United States Department of Energy

Disclaimer

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, expressed or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Distribution

Approved for public release; further dissemination unlimited.

SVX3: A deadtimeless readout chip for silicon strip detectors

T. Zimmerman, , T. Huffman¹, J. Srage, R. Stroehmer², and R. Yarema

*Fermi National Accelerator Laboratory, P.O. Box 500, Batavia, IL 60510**

M. Garcia-Sciveras, L. Luo and O. Milgrome

Lawrence Berkeley Laboratory, University of California, Berkeley, CA 94720

A new silicon strip readout chip called the SVX3 has been designed for the 720,000 channel CDF silicon upgrade at Fermilab. SVX3 incorporates an integrator, analog delay pipeline, ADC, and data sparsification for each of 128 identical channels. Many of the operating parameters are programmable via a serial bit stream, which allows the chip to be used under a variety of conditions. Distinct features of SVX3 include use of a backside substrate contact for optimal ground referencing, and the capability of simultaneous signal acquisition and digital readout, allowing deadtimeless operation in the Fermilab Tevatron.

1. Introduction

The silicon upgrade for the Colliding Detector Facility (CDF) at Fermilab requires a custom IC solution for deadtimeless operation at a 132 ns beam crossing rate with integration, storage, digitization, and readout capabilities. Earlier chips designed for silicon strip detectors at Fermilab include the SVX and SVX2 [1, 2]. Although the SVX2 integrates detector current signals at a 132 ns beam crossing rate, and stores the results in a delay pipeline for digitization, the SVX2 pipeline cannot acquire and read out signals at the same time. The need for continuous data acquisition during digitization and readout led to the development of the SVX3 readout chip.

The integrator and digitize/readout sections in the SVX3 are similar to SVX2, with a few additions and modifications. The requirement of simultaneous read and write in the analog pipeline, however, forces a complete redesign of the pipeline section. Power distribution and isolation issues are more important in SVX3 since sensitive signal acquisition is concurrent with "noisy" digitization and readout. To improve noise immunity, SVX3 utilizes the grounding technique of substrate conduction with backside substrate contact [3, 4]. This technique, which has not previously been used with SVX-type readout systems, confers several important advantages and is crucial in obtaining the best performance and maximum isolation.

2. Architecture

The SVX3 is designed for fabrication in the Honeywell 0.8 micron radiation hard process. Since the earlier SVX2 was fabricated in a UTMIC 1.2 micron process, the move to Honeywell necessitated a completely new layout for all sections of SVX3, including those previously used in SVX2.

The SVX3 has been initially divided into two separate chip designs. A "front end" (SVX3FE) contains the integrator and pipeline sections, and a "back end" (SVX3BE) contains the digitization and readout circuitry. The division into two chips is a conservative approach to eliminate substrate coupling between the majority of the digital functions and the sensitive acquisition circuitry. Whether separate substrates are required to achieve sufficient isolation is being determined by testing. Since the SVX3 is the product of major efforts by two different institutions, Fermilab and LBL, the division of functions into two chips represents a natural division of labor, and simplifies chip testing. The two chip approach could also result in higher yields than a single large die.

The "FE" and "BE" chips are intended to be mounted directly next to each other, then wire bonded together. Disadvantages of the two chip system include making many wire bonds at fine pitch and a possible resultant decrease in reliability. To study the performance trade-offs of single vs. two chip architecture, the layouts on the prototype wafers have been arranged so that the SVX3FE and SVX3BE can be sawed into individual dice or as one large die with a common substrate.

A block diagram of a single SVX3 channel with simplified controls is shown in Fig. 1. Upon power up, the chip is initialized by downloading a serial bit stream to program the front end and back end sections. Parameters such as integrator bandwidth, pipeline delay, threshold level, chip ID, and channel test mask are set during initialization. Once the chip is initialized, the front end is switched to the Acquire Mode and the back end is switched to either the Digitize or Readout Mode as needed.

Fig. 1 shows that a detector signal is fed directly to a free running integrator without a feedback resistor. Double correlated sampling, performed each beam crossing by the pipeline, removes the integrator pedestal

¹ Visitor from University of Pittsburgh, Pittsburgh, PA

² Visitor from University of Munich, Munich, Germany

* Work supported by the U.S. Dept. of Energy under contract No. DE-AC02-CH03000.

and extracts the signal. The integrator has a dynamic range of about 300 fC. To prevent saturation, it is periodically reset during accelerator beam gaps. The integrator is optimized for detector capacitances of 10 pF to 30 pF, and its charge conversion gain is 5 mV/fC.

The output of the integrator is fed to an analog pipeline which is used to provide the delay required by the external Level 1 trigger system. The pipeline is dual ported for simultaneous write and read operation, and is comprised of a write amplifier, a read amplifier, and 47 identical storage cells. Writing to a given cell is performed by switching its capacitor into the write amplifier feedback loop, quickly resetting it before arrival of the signal, and then switching it out after the signal has settled. Reading a cell is performed by switching the desired capacitor into the feedback loop of the read amplifier. The write amplifier has a voltage gain of 3, which is set by the ratio of the input coupling capacitor and the total write amplifier feedback capacitance. The resultant front end gain is then 15 mV/fC, which helps to minimize the effects of offsets in the back end ADC.

An additional storage cell resides in the pipeline which is identical to all the others but is not normally addressed by the acquisition logic. This cell is reserved for write amplifier pedestal acquisition and is used in the analog to digital conversion process to reduce channel to channel offsets. Pedestal acquisition can be performed during beam gaps to avoid any deadtime.

The pipeline logic shown in Fig. 2, is used to control the operation of the analog pipeline. The pipeline uses a system of pointers and shift registers to control simultaneous writing and reading [5]. Skip logic removes storage cells from the pipeline which are flagged by triggers, and queues them for digitization. Up to 4 cells can be queued. After any cell is digitized, it is removed from the queue and returned to the pipeline. The maximum delay length of the pipeline is 42 cells, since up to 4 of the 47 cells can be in the queue, and one is reserved for pedestal acquisition.

The SVX3BE provides the digitization, sparsification, and readout/control functions. The design is very similar to the back end section of SVX2, with minor modifications and improvements. Each channel contains a Wilkinson type ADC, neighbor logic, and a register in a collapsing FIFO for data sparsification [2]. A simplified block diagram is shown in Fig. 1. The back end chip has three modes of operation: Initialize, Digitize, and Readout. An eight bit bidirectional data bus is used to provide control signals during Digitize, and to output digital data during Readout.

In Digitize mode, an autozero cycle is first performed in which the pipeline write amplifier pedestals are stored on the coupling capacitors to the ADC comparators. Then the desired stored signals are applied, effectively presenting signal minus pedestal to the comparators. All channels are digitized simultaneously using a common ramp voltage and digital counter.

In the Readout Mode, data is compressed and read out with the BE clock. As in the SVX2 chip, hit channels, hit channels plus neighbors, or all channels may be read out. Data transmission in a multichip

system is based on a common data bus with tri-stated SVX3 outputs and token passing between chips. Data from the active chip is output on each edge of the back end clock. Initially a chip presents its chip ID number, and then the address of the time slice being read out. Subsequently, the address and data for each pertinent channel is output. If there are no pertinent channels to read out, the token is passed to the next chip immediately after the chip ID and time slice have been read out.

3. Issues for Deadtimeless Operation

The SVX3 requirement of concurrent signal acquisition and triggered readout of stored signals establishes the need for separate write and read amplifiers in the pipeline along with additional storage capacitor switching circuitry and a set of read amplifier in/out buses. As shown in Fig. 1, three sets of switches instead of two are used in the SVX3 to place a given capacitor across one of the amplifiers. This allows the same set of switches (the "A" set) to be used for both sampling the write signal and placing the capacitor in the read amplifier. The "W" and "R" switches are used only for routing. This arrangement minimizes pedestal errors caused by switch mismatch.

The magnitude of substrate coupling depends on several factors: substrate resistivity, impedance from substrate to system ground, and physical distance between noise injector and noise receiver circuits. For high resistivity substrates, surface substrate current is prevalent and coupling is a weak function of the impedance between substrate and ground, and very sensitive to the distance between circuits. However, in low resistivity substrates with back side contacts, substrate currents are predominantly vertical and confined to a local region and coupling is a strong function of the impedance between substrate and ground [3].

SVX3 will be manufactured in the Honeywell 0.8 μ m process, which is an epitaxial process with a low resistivity substrate. By thinning and back plating the wafers, and attaching the chips with conductive epoxy directly to the system ground plane, the substrate to ground impedance is kept extremely low. This provides the best possible substrate isolation between circuits on the SVX3.

Use of the backside contact on the SVX3 is illustrated in Fig. 3. The die pad ground plane serves as the ground reference for the analog sections. Digital current transients flow primarily through the isolated loop of digital supply bond wires, digital circuitry on the chip, and the external digital bypass capacitor. Capacitively coupled currents from the digital sections to the substrate are conducted vertically (away from the analog sections) through the substrate to the low impedance die pad and returned to digital ground.

The ground return connections for circuits on chips are commonly through bond pads and wires to the system ground. However, with a low resistivity substrate, the conduction path can be directly through the substrate to the system ground [4]. This is done with the analog circuits in the SVX3FE as shown in Fig. 3. (Since digital ground can have large transients, it is

still brought out to a bondpad in the conventional manner.) Advantages to the substrate grounding method include: 1) removal of analog ground bond pads, 2) very low ground inductance, 3) elimination of large analog ground busses and voltage drop problems in ground busses, 4) reduced sensitivity to latchup.

Even if substrate coupling is completely eliminated, unwanted coupling can still occur through the power supplies. Therefore, separate supply voltages are required for the analog and digital portions of the circuit. In addition, the digital circuit which drives the pipeline capacitor switches must have quiet supplies to prevent transient voltages from coupling through the parasitic capacitance of the switches to the pipeline input. Thus the drivers for the switches have dedicated "quiet digital" supply pads which must be externally connected to the analog supply at a bypass capacitor.

4. Layout

A floorplan of the FE chip is shown in Fig. 4. The "left" border of the FE chip is reserved for bond connections to the detector. If the FE and BE designs are on separate substrates, the FE outputs and control signals are bonded across to the BE chip at a fine pitch. The BE data and control pads are all at the BE right chip border, for bonding to a hybrid. The channel pitch on the FE chip must be smaller than the detector channel pitch to allow area for on-chip peripheral functions (pipeline logic, supply bussing, biasing, etc.). The use of a low resistivity substrate with backside substrate contact obviates the need for numerous top side contacts in many of the digital areas, reducing the layout area. The pipeline logic section, shown in Figure 2, requires 600 μm of the 6250 μm chip height.

The I/O philosophy and power routing on the SVX3 have been significantly altered from SVX2. Whereas SVX2 used CMOS single ended levels for all digital inputs and outputs, SVX3 has been designed using low level differential signals for the clock and control inputs, and the digital outputs. This requires more pads, but minimizes digital to analog coupling. Since SVX3 has more control pads than SVX2 due to the differential nature of the digital signals, there is little room for power pads at the right end of the chip. Thus the power pads are placed on the top and bottom of the chip, close to the circuits they supply. These pads must be bonded down into the small gap (50 mils) that exists between neighboring chips. IR drops in the power busses are greatly reduced and less chip space is required using this method.

The circuit size of the SVX3FE is 6258 x 8060 μm , and the SVX3BE is 6258 x 4970 μm . If a common substrate implementation is adopted, the interchip bond pads and routing can be removed and the chip size would be reduced to approximately 6258 x 12000 μm .

5. SVX3 Test Results

SVX3 dice with a common substrate (single die form) and two chip die sets fabricated in the Hewlett Packard 0.8 micron radiation soft process have been received and tested. Radiation hard parts being

fabricated in the Honeywell 0.8 micron RICMOS process have not been received yet.

The HP parts are completely functional. Performance issues are being investigated. At the present time, no significant differences have been observed in the performance of the common substrate and the 2 chip set SVX3 design. Tests will continue to verify that a single chip implementation does not compromise the SVX3 performance.

Gain through the complete chip is measured to be 14 mv/fc. The dynamic range is greater than 40 fc. Linearity has been measured from 0 to 40 fc: $\text{INL} < 1/2 \text{LSB}$, $\text{DNL} < 1/5 \text{LSB}$. The noise has been measured at the output of the pipeline (analog measurement) and at the digitized output. The result is essentially the same with either technique. The equivalent noise charge (ENC) can be characterized as $500 + 60 \text{ e/pf rms}$. Power dissipation is about 3 mw/ch.

Pipeline cell uniformity and the effect of digital activity on the pedestal are good measures of success for a device of this type. The pedestal variation across the cells in any SVX3 channel is found to be $< 0.5 \text{ mv rms}$. A systematic pedestal variation of up to 8 mv has been observed across the channels in a given time slice under some conditions. This affect is understood and is expected to be removed in the final design. Pedestal variations in a cell depending on digital activity (digitization and readout) in the back end chip is on the order of a few mv and is still being evaluated. Testing is continuing to fully characterize the performance of the SVX3.

6. Conclusions

A deadtimeless silicon readout chip using a backside contact to reduce substrate coupling has been designed for CDF. A rad soft version of the SVX3 has been tested and found to be completely functional. The design operates in a deadtimeless mode. The SVX3 has been tested as a single die and as a two die set where the major analog and digital features are separated. Current results indicate that acceptable performance is achievable with the single chip design, including operation in the deadtimeless mode.

Acknowledgments

The authors would like to thank Al Clark, Al Dyer, and Bob Ely for their contributions to the development of the SVX3.

References

- [1] S. Kleinfelder, et al., A flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout, IEEE Trans. Nucl. Sc. NS 35 (1) (1988), 171.
- [2] T. Zimmerman, et al., The SVX2 Readout Chip, IEEE Trans. Nucl. Sc. NS42 (4)(1995), 803.
- [3] R. Gharpurey, et al., Modeling and Analysis of Substrate Coupling in Integrated Circuits, IEEE JSSC SC31 (3), 344.

[4] T. Gabara, Reduced Ground Bounce and Improved Latch-up Suppression through Substrate Conduction, IEEE JSSC SC23 (5)(1988), 1224.

[5] K. Borer, et al., APC3-A Charge Sampling, Storage & Readout Chip for Silicon Detector Readout, IEEE NSS (1993) 877.

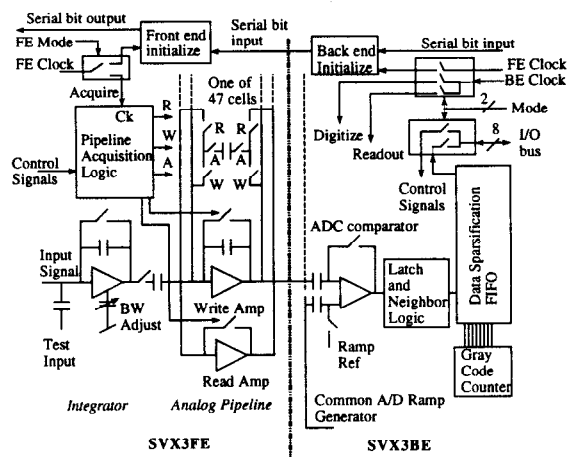


Fig. 1 SVX3 single channel block diagram with simplified controls

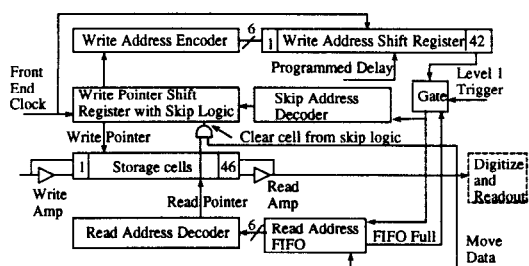


Fig. 2 SVX3 pipeline control logic

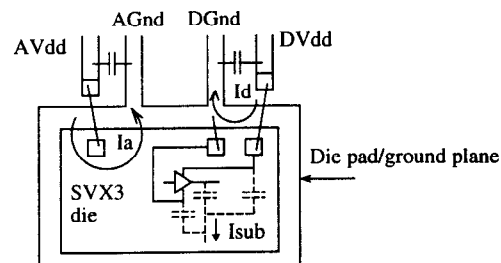


Fig. 3 SVX3 power and substrate connections for substrate isolation

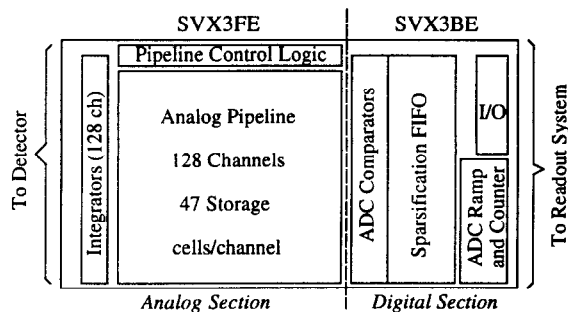


Fig. 4 SVX3 floorplan showing SVX3FE and SVX3BE