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# A High Speed Digitizing Photomultiplier Tube Base for the KTeV CsI Calorimeter

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# A HIGH SPEED DIGITIZING PHOTOMULTIPLIER TUBE BASE FOR THE KTEV CsI CALORIMETER

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ABSTRACT

A circuit has been designed to digitize PMT signals over an 18-bit dynamic range with 8-bits of resolution.[1,2,3] The crucial element of the circuit is the custom charge integrating and encoding (QIE) ASIC. This chip is designed to operate at rates up to 53 MHz, and, in conjunction with an 8-bit FADC, generates 12-bit floating point output. Bench tests of a 17-bit version of the digital base demonstrated excellent noise performance, linearity and pedestal and gain stability. Twenty-five channels of digitizing PMT bases have been built and used for readout of a CsI array in a test beam at CERN. Performance of these devices in a beam environment is discussed.

## 1. Introduction

A high speed digitizing base has been developed for readout of the pure CsI calorimeter in KTeV*, a Fermilab fixed target experiment. The major focus of the KTeV experiment is a precision measurement of the direct CP violating parameter $\epsilon'/\epsilon$.[4] To achieve this goal, the CsI calorimeter must have an energy resolution of 1% for 15 GeV photons and be extremely linear over a wide dynamic range. The digitizing circuit must be compatable with these stringent requirements. A detailed description of the KTeV calorimeter can be found in reference 5.

The required performance of the KTeV calorimeter has serious implications on the CsI crystals, photomultiplier tubes, and the readout electronics. Linearity specifications limit the peak current in the phototube to 30 mA, setting the high end of the dynamic range at 64 GeV. In addition, longitudinal crystal response needs to be monitored. Muons transverse to the crystal axis deposit 16 MeV of energy. A 5% measurement on these events necessitates 0.5 MeV resolution at the low end of the dynamic range. The result is a requirement of 17-bits to cover KTeV's full operating range. The ADC is allowed to contribute no more than 0.2% to the energy resolution between 1 GeV and 64 GeV. Digitization error from an 8-bit ADC meets this specification and is much less than the 0.5-1% CsI intrinsic resolution. In addition, the energy resolution is sensitive to pile-up problems† and to accidental energy deposits in the calorimeter. A detailed time profile will allow monitoring of these effects. The digital base circuit features the low input noise, wide dynamic range, and high frequency operation required for the KTeV calorimeter.

*A collaboration of Chicago, Colorado, Elmhurst, Fermilab, Osaka, Rice, Rutgers, UCLA, UCSD, Virginia and Wisconsin.

†The tail of a CsI pulse has a 25 ns fast and a 1 $\mu$s slow time component.

## 2. Overview of Digital Base Operation

The three fundamental components of the digital PMT base (DPMT) are the charge integrator and encoder (QIE) custom designed ASIC, a commercial FADC and a custom buffer/cable driver chip. Figure 1 shows a schematic of the primary functions of the digital base. The QIE receives signals from a PMT, splits the current

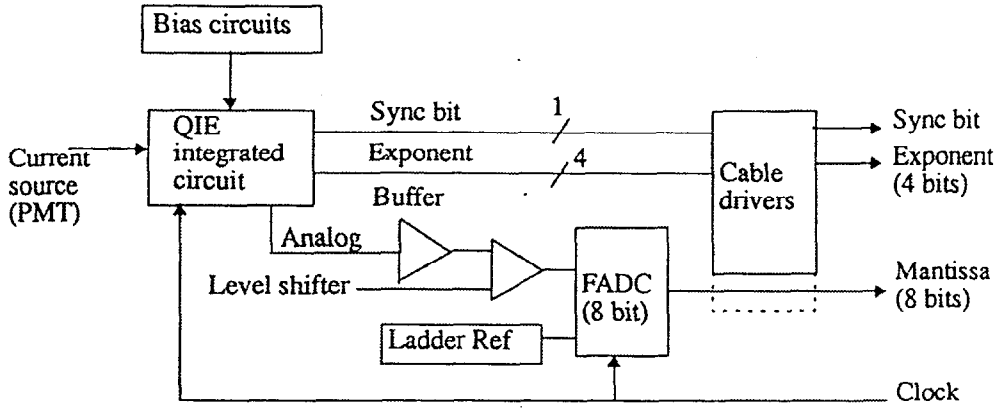


Figure 1: The KTeV multi-range digital PMT base block diagram.

into binary weighted ranges and integrates the divided signal on capacitors for each range. The QIE selects the integrated signal in the appropriate range of interest and presents the analog signal for digitization by the 8-bit FADC. Simultaneously, the QIE generates 4 bits of exponent data, identifying the range of the input signal. The 12-bit floating point data is buffered (to eliminate phase differences between mantissa and exponent data) and then piped to a FIFO using a custom cable driver circuit.

In order to better understand the performance of the QIE, a detailed description of the operating principles is useful. The QIE performs 4 distinct functions. It first adds the PMT signal current to a bias current, divides the total current into 10 binary weighted ranges (I,I/2,...,I/512), and simultaneously integrates the charge on 10 1pF capacitors. The capacitor voltages are then applied to a bank of comparators having a common reference voltage. The comparators are latched, and the latched output is encoded into a 4-bit Gray code number which represents the exponent[‡] Because of the binary weighting, only one capacitor voltage will be within the required -1V to -2V range. The voltage from this capacitor is output and mapped into the input range of the FADC. The capacitors are then reset. Fig. 2 depicts the device behavior over 4 clock cycles. A bank of four capacitors in each range is necessary for deadtimeless operation of the circuit. Each capacitor performs one operation per clock cycle with capacitors switching in round-robin fashion. Fig. 3 shows a schematic of the DPMT

[‡]The exponent lines from the QIE are differential, reducing pickup on the analog section of the device.

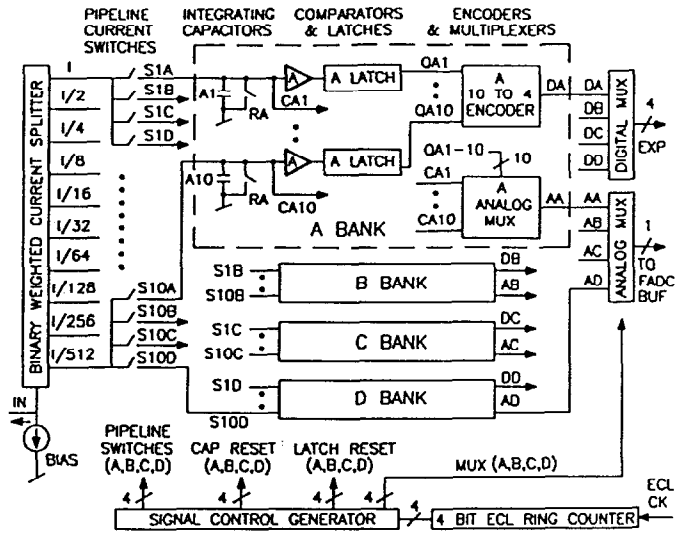


Figure 2: A schematic of the pipelined operations of the QIE ASIC.

analog and digital response versus input charge. The QIE generates a synchronization bit every fourth clock cycle to label the first capacitor in the pipeline.

The DPMT base incorporates both the PMT high voltage divider and the digital readout section. The circuit board dimensions are 0.94" x 9.75", with approximately 2.75" of the length designated for the HV divider. It is designed to fit directly behind a PMT in the dense array of phototubes in the KTeV calorimeter. The PMT anode signal is sent to the DPMT via a 6" coaxial cable. A 50 pin low profile header connector transmits low voltage power to and digital data from the board.

Because of space constraints, the QIE, FADC and buffer/driver chip are wire-bonded directly to the DPMT boards. Thermal vias located on the die pads conduct heat to the back of the card. A 1/32" copper plate is attached to the back of the board as a heat sink. The power dissipation for the digital part of the base is 3.5 Watts; the HV divider adds an additional 0.5 Watt.

## 3. Bench Tests of the DPMT

Measurements have been made using a 9-range (I/2 → I/512) QIE device and an 8-bit Analog Devices AD9002 FADC. Bench tests have been performed using a 16-bit DAC programmable charge pulser. To contain the pulse within a single time sample, the pulse was shaped to have a 15 ns tail and the DPMT was clocked at 10 MHz.[§] To simulate a PMT, the pulser output was fed through a current buffer to the AC coupled input of the DPMT.

[§]This device has been run at 53 MHz. However, parasitic capacitance differences between ranges result in slightly different pulse shapes in each range. This is not a problem if the charge is deposited in a single time sample, but it effectively leads to charge loss for a pulse which straddles multiple integration periods and switches ranges. Newer versions of QIE have addressed this problem.

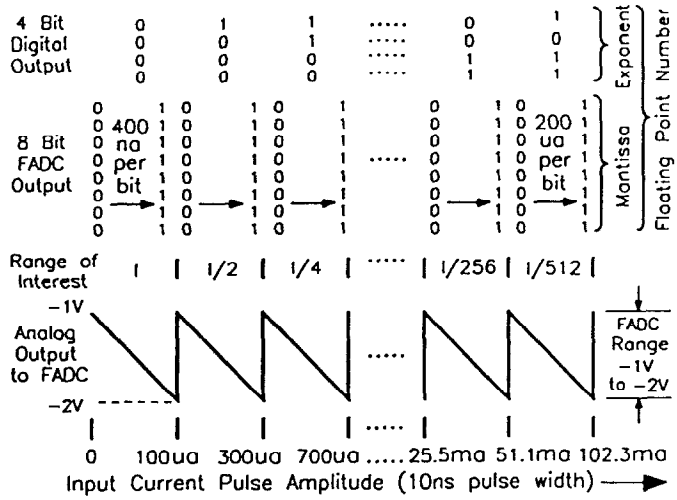


Figure 3: The analog and digital reponse of the QIE ASIC versus input charge. Also depicted is the digitization of the analog signal by an 8-bit FADC.

Tests of noise performance, capacitor gain and pedestal variation, and constants stability were made. DPMT output response for a single time sample versus input charge is shown in Fig. 4. The LSB for the DPMT in the I/2 range was 8 fC per count. The charge limit of the pulser system restricts the ranges probed to the lower six (I/2→I/64). Pedestal noise of 3-4 counts rms was primarily due to the pulser circuit. Similar measurements using a PMT input showed a pedestal noise of 0.3 count rms (2.4 fC). The four capacitors in a range had gain variations of 0.1-0.3% and mean pedestal variations of $\pm$ 2 counts. Differences in FADC switch points arise from the 20% variation in range comparator voltages within the QIE.

To study the stability of the correction constants, gains and offsets were derived and applied to data taken 1 week later. Fig. 5 shows the DPMT data after linearization using the "stale" constants. Also shown is the percent difference between corrected data and linear fit. The constants appear to be quite stable over a period of 1 week. The figures are nearly identical to ones made with current constants. The average mean residual is 0.2-0.3%. The remaining structure is common to all ranges (probably due to the FADC) and could be correctable. The resolution versus input charge is plotted in Fig. 6. The dominant contribution to the resolution at the low end is noise from the pulser circuit. The high end resolution is 0.1-0.3%, comparable to the resolution expected from digitization.

## 4. Performance of the DPMT in a Beam Environment

A test-array consisting of 25 CsI crystals has been instrumented using the DPMT cards described in Sec. 3 and tested in the X1 beam line at CERN. The PMT anode signals were DC coupled to the DPMTs, which were operated at 10 MHz. The 17-bit

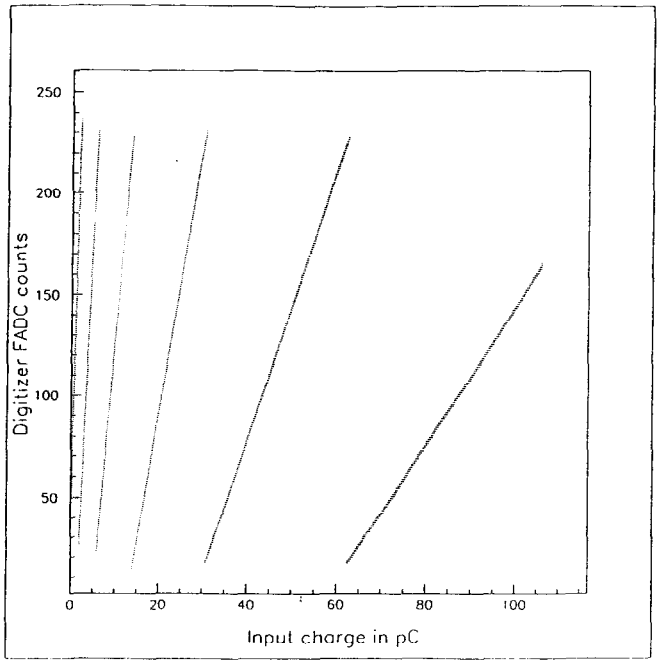


Figure 4: DPMT output in FADC counts versus input charge.

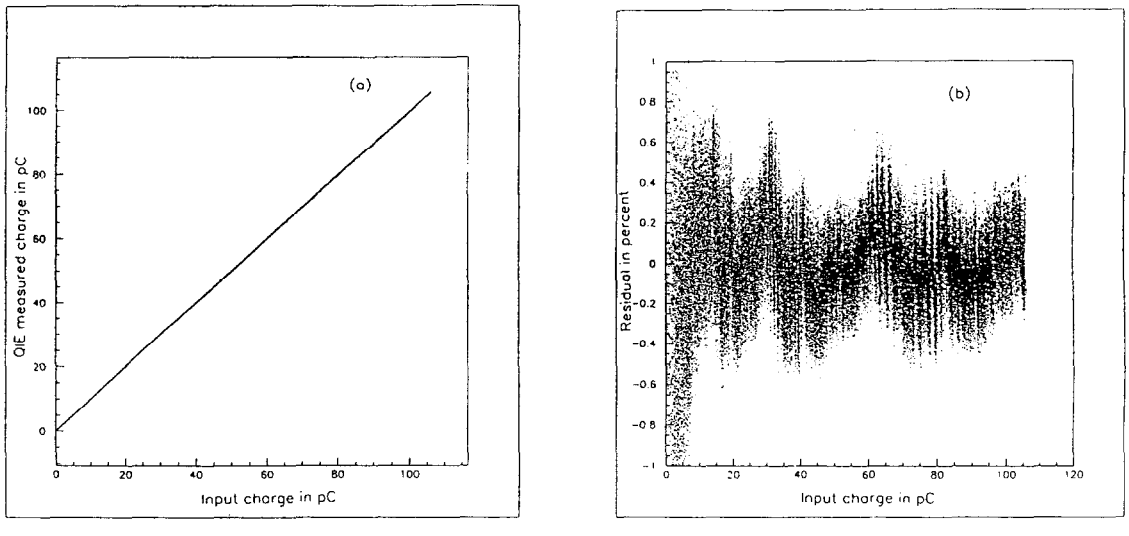


Figure 5: (a) Linearized DPMT output in pC versus input charge, (b) Percent residual from a straight line versus input charge.

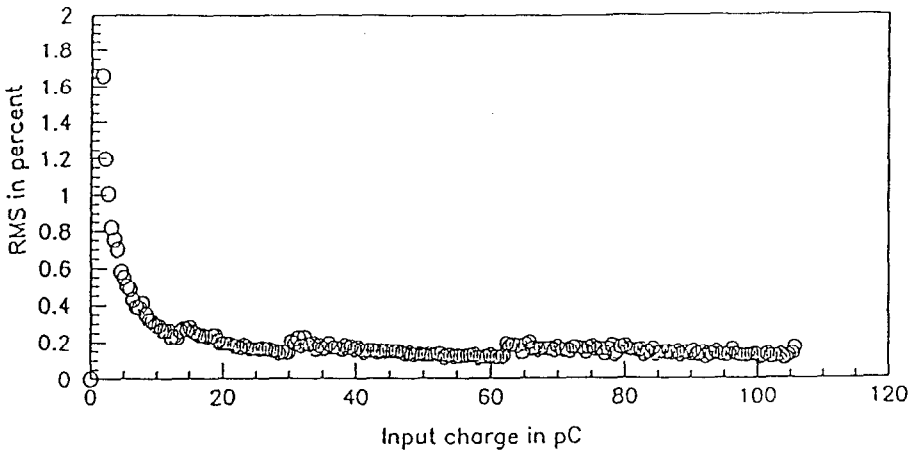


Figure 6: DPMT resolution in percent versus input charge. Breaks in the smooth function arise from switching from a higher sensitivity range to a lower sensitivity range.

dynamic range of the DPMT was tuned to have a lowest range (I/2) LSB of 13 fC, corresponding to 1 MeV, and a full scale energy of 102 GeV. A KTeV prototype laser system[7] was used to calibrate the DPMTs *in situ* over the full dynamic range. A detailed description of this mini-KTeV calorimeter and its performance in the test beam can be found in reference 6.

Beam data covered most of the dynamic range of the digitizer. Typical DPMT pedestal noise for a channel was less than 1 count rms. Pedestals summed over all 25 channels had a 5 count (5 MeV) rms. Data included 60 GeV electrons, 40 GeV pions and transverse muon data which was taken with the calorimeter rotated by $90^0$ with respect to the beam. Transverse muons deposit 30 MeV of energy in the 5 cm crystals which were used in the array. The dynamic range of the digitizers is illustrated in Fig. 7. CsI calorimeter $E/p$ resolutions of better than 1% were achieved for electrons between 5→60 GeV energies.

## 5. Conclusions

A 17-bit dynamic range digitizer circuit has been built and tested. Bench tests of the device show very low noise floors (2.4 fC), good linearity, and stable gains and pedestals over a period of 1 week. A 25 channel CsI array has been successfully instrumented with DPMTs and tested in a beam environment with excellent resolution.

## 6. Acknowledgements

The author would like to thank the Fermilab Research Division Electrical Engineering Department for their development of the digitizer circuit and the Fermilab Physics Department Electronics Group for their work on the clock modules, power

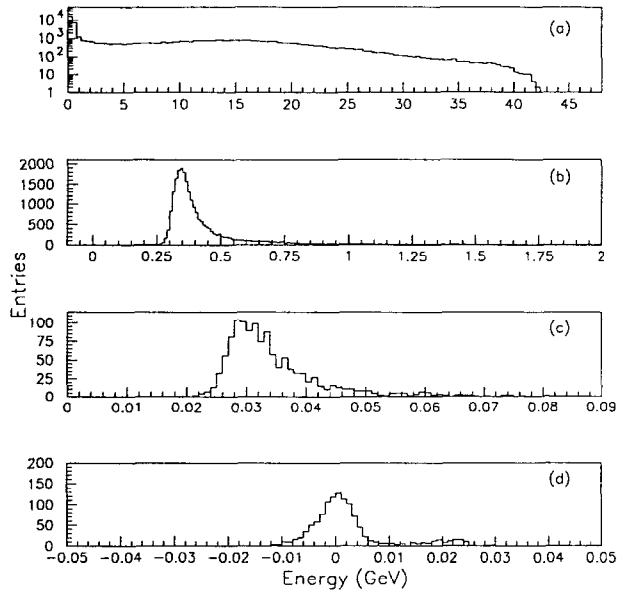


Figure 7: Energy distributions derived from summing 25 channels for data using one 100 ns time sample from a) 40 GeV pions, b) same spectrum for the pion MIP peak, c) 30 MeV transverse muons, and d) pedestals.

sequencers, ribs and CAMAC FIFOs.

## 7. References


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