OG.4.5.14

Development of Front-End Electronics for the Telescope Array Project

Y. Arai[1], T. Aoki[2], M. Fukutomi[3], K. Hashimoto[4], K. Honda[5], F. Ishikawa[2], N. Manago[2], M. Sasaki[2], K. Satake[3], M. Takeda[2], Y. Tanaka[3]

[1] *KEK, High Energy Accelerator Research Organization, Institute of Particle and Nuclear Studies, Tsukuba, Japan*

[2] *Institute for Cosmic Ray Research, University of Tokyo, Tokyo, Japan*

[3] *Department of Electrical Engineering, Nagasaki Institute of Applied Science, Nagasaki, Japan*

[4] *Faculty of Education and Human Science, Yamanashi University, Kofu, Japan*

[5] *Faculty of Engineering, Yamanashi University, Kofu, Japan*

Abstract

In the Telescope Array experiment, real time processing of finding small signals buried in a large background signal is highly required. To improve the signal processing power, a new front-end electronics system is designed. A prototype signal finder module which implements pipelined 5MHz, 12-bit ADCs and 100 MIPS DSPs for all 16 channels was developed. A custom LSI for the charge successive integration is also under development and described.

1 Introduction:

Front-end electronics for the Telescope Array detector (Sasaki, 1997) is one of most critical elements to achieve a large aperture of the telescope. In the pioneering work of the Fly's Eye detector, analog sample & hold circuit with a slow AD converter (Baltrusaitis, 1985) was used in conjunction with a relatively simple trigger. In the subsequent HiRes detector, 8-bit flash ADC was introduced with additional analog sum measurements to circumvent the effect of over range (Boyer, 1995).

A new pipelined ADC technology and a wide spread of digital video system enable us to use a fast and wide dynamic-range ADC for all channels. The pipelined ADC is fabricated in a CMOS process, and it has superior characteristics of low power, low cost and high speed. A 12-bit, 5-Msample/sec ADC is commercially available in less than $7.

While the fast ADC system could give us more information on air shower, it increases data size almost 100 times. Thus a large bandwidth is required in data acquisition system. Furthermore, to maximize the merit of the fast digitization, it is indispensable to process the data in real time to increase signal to noise ratio. This is particularly important in the fluorescence measurement since the signal waveform varies greatly depend on the zenith angle and the impact parameter.

To process the digital data in real time, a large processing power is required. Fortunately, recent progress in digital products introduces high-performance, low-cost DSPs (Digital Signal Processors). There are several DSPs, which performances are more than 100 MIPS and the price is less than $10. By using these DSPs we will be able to search optimal gate width for fluorescence signal in real time.

To realize the new approach described above, we have developed a signal finder module which implements high-speed ADCs and DSPs. Furthermore, to have a wide-dynamic range charge integrator, a custom LSI is being developed. The design of the module and the LSI are presented in following sections.

2 Front-end Electronics System:

Figure 1 shows the proposed block diagram of the Telescope Array electronics. There are 10,240 channels in each station (256 ch x 40 telescopes) and 8 stations in total (Takeda 1999). Required signal range is summarized in Table 1. To cover the large dynamic range, two-range scheme will be implemented in a front-end chip. Night background rate is estimated about 100 MHz, or 20 p.e. in 200 ns integration time.

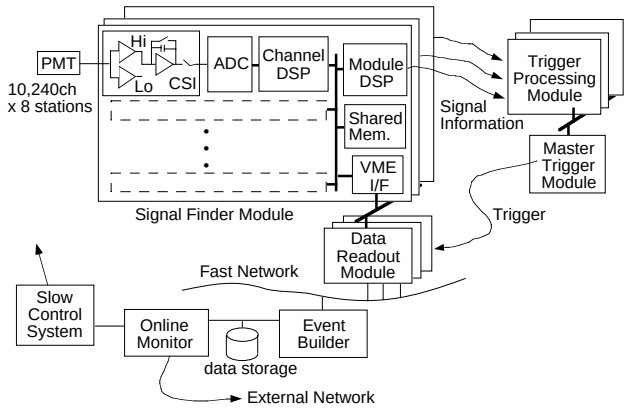

Figure 1: Block diagram of the Telescope Array electronics system.

Table 1: Required signal range and rough estimate of signal levels. Phototube gain of 10,000 is assumed.

Least count sensitivity	1 p.e. = 10,000 electrons = 1.6 fC = 1 mV on a 26 pF integration Capacitor (use Low Range: x16 amp)
Full scale sensitivity	50,000 p.e. = 80 pC = 3 V on a 26 pF (use High Range: x1 amp)

Charge Integration

In a calorimetric detector a charge integration stage is important. While a charge amplifier is normally employed, its dynamic range is limited under high background rate due to the output pileup.

To avoid the pulse pile-up in the charge amplifier, we are developing a Charge Successive Integrator (CSI) LSI (Figure 2). In the CSI three charge integrators are used for a channel. Each integrator is in one of three steps (Integrate, Read and Reset) and circulate in each clock. Since the integration capacitor is cleared in each cycle, there is no pile-up problem.

The CSI will be fabricated in a CMOS technology. In this technology the value of the capacitor matches in 0.1% level. Thus the uniformity of the integrators will be good enough. In addition, any non-uniformity can be corrected by a DSP if necessary. Instead of using three independent integrators, it is also possible to switch three integration capacitors to one amplifier. Although this will reduce Si area but may add parasitic capacitances, thus it might increase system non-linearity.

A test CSI chip using a 0.6 μm single-poly, triple-metal CMOS process was fabricated (Figure 3) at Rohm Co. through VDEC (VLSI Design and Education Center, The Univ. of Tokyo) multi project wafer service. While the prototype CSI includes only one range of circuit, final chip will be implemented in two-range scheme.

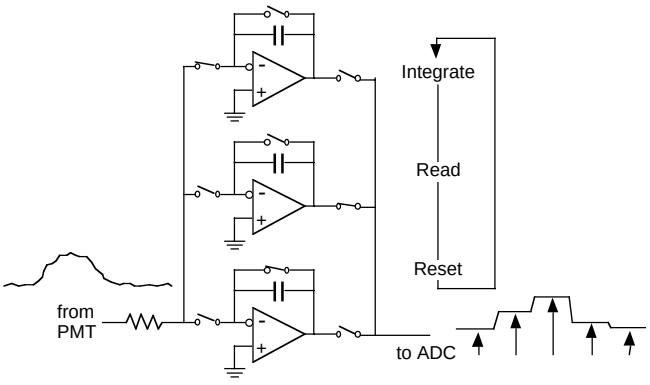

Figure 2: Simplified schematic of the Charge Successive Integrator.

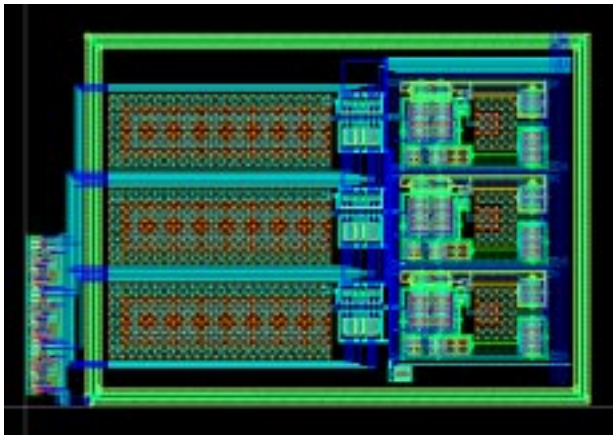

Figure 3: Layout of the test CSI cell designed in 0.6 μm CMOS technology. In this particular cell, 12 pF integration capacitors were used.

Pipelined ADC

Recent progress in digital video system brings a new high-speed, large dynamic-range, low-power, low-cost ADC. Technique used here is called pipelined ADC. The ADC has many pipelined stages, and digitization of only one or two bit is done in each stage. This ADC is fabricated in similar process used in CMOS digital LSIs and there are very little analog elements in the chip. A digital error correction technique is usually employed to achieve a high precision.

We are presently using Burr-Brown ADS803 of which power consumption is only 115 mW. The ADC has 12-bit dynamic range and 5MHz-conversion rate.

DSP

To process the ADC data in real time we need high-performance DSP. We are now using a Texas Instruments TMS320C549 DSP. This DSP runs at 100MHz, and most operations can be completed in one cycle. The C549 has 3 internal data bus and one program bus, and consists of 6 stage pipelines. It contains 32 k word internal memory that is enough for our application. The DSP consumes only 100 mW/chip.

Since the ADC generate 12-bit data in every 200 ns, there are 20 cycles for one data in average. From the viewpoint of signal finding algorithm (Sasaki 1999), we will set 30 μsec window for finding a signal and the window has 10 μsec overlap with next window, so there are 2,000 cycles for 150 data words.

This is very tight limitation, but we still expect enough calculation can be done with an optimized program that extracts full DSP power. Most calculation required in the signal finding such as the least mean square, the square distance, and the finite impulse response calculations can be done in one cycle. Furthermore, as usual in this field, higher performance DSPs may be available before fixing final design.

3 Signal Finder module

A prototype Signal Finder Module was developed in a 6U VME module (Figure 4). It includes 16 channels of inputs and the block diagram of the module is shown in Figure 5.

Each channel contains a hybrid version of the CSI, an ADC, and a DSP. The hybrid CSI is not yet implemented in the two-range scheme. Data transfer between the ADC and the DSP internal memory will be done through an 8-bit host port interface of the DSP. This operation is completed without DSP intervention (Figure 6). The internal memory is addressed in a circular-addressing mode. The size of the circular memory is 2 k word, thus the data can be stored in the memory up to 400 μsec (200 ns x 2 kW). If we need longer latency than 400 μsec, a data copy operation is required.

Between the ADC and the host port, 12-bit data and an overflow bit are connected. Two 8-bit data transfer cycles are used for an ADC data. In addition to the 13 bits from the ADC, 2 bits are connected to a 2-bit counter, which is used to check the data sequence. Last one bit is reserved for data flow control which is used in DSP software. The gain and signal offset of the amplification stage before the charge integration are programmable channel by channel with two 16 ch 8-bit DACs.

We have paid much attention to the analog and digital circuit separation. In addition to power and ground separation, signal between these two circuits are separated by LVDS (Low Voltage Differential Signaling) drivers/receivers to reduce interference from digital to analog circuit.

In addition to the channel DSPs, there is a module DSP which control channel DSPs and send processed information to the trigger module through its serial lines (50 Mbps). A JTAG boundary scan port is used to debug and monitor the DSPs. Easy-to-use PC tools are available in commercial. A dual port memory of 16 kB is used to exchange the data between the module and a VME master module. A Flash memory of 256 kB is included to store programs and parameters. The whole system can be synchronized by using an external system clock (5 MHz).

While the prototype signal finder module is lager than single-width VME module, we expect final design will be fit within the single-width module.

Figure 4: Photograph of the prototype signal finder module. The height of the module is 6U but the depth of the module was extended to 26 cm.

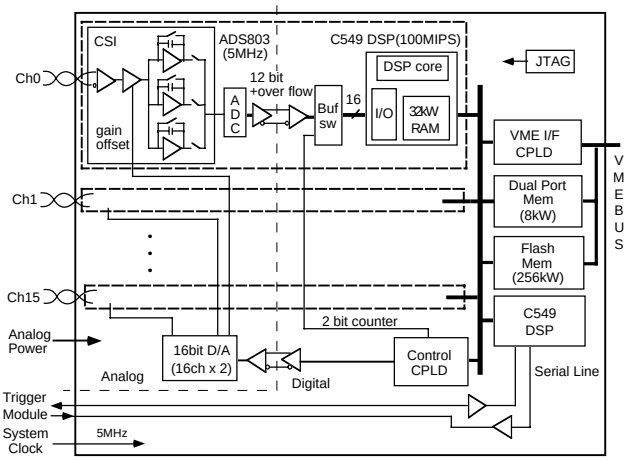

Figure 5: Block diagram of the 16-ch prototype Signal Finder module. The module is implemented in a 6U VME board.

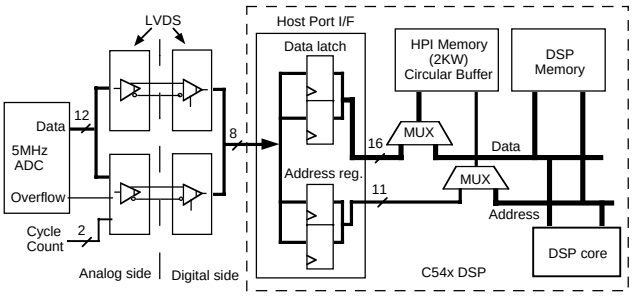

Figure 6: ADC to DSP interface. ADC and DSP are connected through 8-bit host port which maximum speed is 20 MB/sec. ADC data are automatically transferred to internal circular buffer of 2 k word. Analog side and digital side are separated by LVDS (Low Voltage Differential Signaling) drivers/receivers. 16 bit data are consists of 12 bit ADC data, an overflow bit, read/write flag and 2 bit cyclic count.

4 Summary

A new front-end electronics system for the Telescope Array project was designed. To realize the new system, a prototype signal finder module which implements 5MHz, 12-bit ADC and 100 MIPS DSP was developed. Development of DSP software and fine tuning is being done. A design of a custom CSI LSI is also proceeding. Test with a real telescope is being scheduled.

References

Baltrusaitis, R.M. et al., Nucl. Instr. And Meth. A240(1985)410.
Boyer, J. et al., Proc. 24th ICRC, 3, 492 (1995).
Sasaki, M. et al., Proc. 25th ICRC, 5, 369 (1997).
Sasaki, M. et al., Proc. 26th ICRC OG 4.5.15 (1999).
Takeda, M.,et al, Proc. 26th ICRC, OG 4.5.16 (1999)