High Speed Electronics for Atmospheric Cherenkov Detectors

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Abstract

We describe two of the electronic subsystems to be used in the VERITAS experiment: the signal digitizers and the front-end discriminators. A prototype containing a 500 MSPS flash analog to digital converter (FADC) and constant fraction discriminator has been tested on the Whipple 10m telescope and shows promise for reducing the event reconstruction threshold by a factor of $\sim \sqrt{2}$ compared with the charge ADC electronics. The prototype includes a novel autoranging circuit which provides an effective dynamic range of $>$2000 with a single 8 bit FADC. A memory depth of $> 8\mu$sec will provide for a high level trigger and will permit single telescope trigger rates in excess of 1 MHz.

1 Introduction:

Imaging atmospheric Cherenkov telescopes (IACTs) use large optical reflectors and fast photomultiplier tube (PMT) cameras to register the faint flashes of Cherekov light produced by γ-ray showers in the atmosphere. The effective area for detecting a γ-ray shower is comparable to the area of the Cherenkov light pool on the ground, providing a huge effective area $\sim 10^5$ m^2 compared with satellite experiments. However, these flashes of light are very faint and even with large reflectors, the energy thresholds of IACTs are large.

The Cherenkov flashes are detectable against the night sky background (NSB) because of the very short duration (3-5 ns) of the Cherenkov pulse at ground level. The use of shower imaging in atmospheric Cherenkov telescopes has provided a powerful method for rejecting events of hadronic origin (Weekes et al. 1989); however this can only be achieved if there is sufficient light detected to provide meaningful image reconstruction. Detection of these faint flashes against the Poissonian variations in the NSB noise (from stars, airglow, etc.) is the primary technical challenge in reducing the threshold of IACTs.

The energy threshold of a detector depends on: (1) the minimum discriminator threshold at which acquisition can be triggered with an acceptable rate of accidental triggers and system deadtime (trigger threshold), (2) the minimum amount of Cherenkov light required to produce a meaningful shower image (reconstruction threshold). In either case, the ratio of the Cherenkov light signal to the level of fluctuations in the NSB determines the threshold. The energy threshold for event reconstruction is inversely proportional to this signal to noise ratio (SNR): $E_{\rm th} \propto {\rm SNR}^{-1} \propto A^{-1/2}(B\tau)^{1/2}$ where A is the mirror area, B is the NSB level, and τ is the signal integration time. Thus the signal digitization electronics should be designed to minimize τ.

The electronics of the 10 m telescope are typical of those used in other ACTs. Each PMT signal is amplified and fed both to a discriminator, and through a coaxial delay cable to a gated charge analog-to-digital converter (qADC). The discriminator outputs are combined to form a low level (L0) trigger using coincidence logic (e.g., 2 adjacent pixels above threshold) which is designed to minimize the accidental trigger rate and reduce the threshold (e.g., Bradbury et al. 1997). This trigger is used to gate the qADCs, which integrate the PMT signal over the gate time τ_G. This mode of operation requires that the signal input to the qADC be delayed by a time greater than the development time of the trigger to ensure that the ADC gate precedes the analog signal. Such a delay can result in significant dispersion. Near the base of a Whipple PMT, a single photoelectron (p.e.) pulse has a rise time of $t_r = 2.9$ nsec, fall time of $t_f = 9.7$ nsec and width of $w = 6.4$ nsec. After 150 ft (230 nsec) of RG-58 delay cable, $t_r = 4$ nsec, $t_f = 16.5$ nsec and $w = 10$ nsec requiring an increase in τ_G to contain the broadened pulse. Time jitter in the trigger electronics also requires an increase in τ_G to ensure that the signal pulse is contained within the gate. Changes in PMT high voltages result in variations in the delay between photoelectic emission at the cathode and the arrival of a signal at the qADC. These uncertainties again necessitate widening the qADC gate. Thus, even though a Cherenkov signal from the Whipple telescope typically has a width of ∼8 nsec at the PMT, the ADC gates can not reliably be reduced below 25nsec.

Use of an array of telescopes provides a dramatic improvement in hadronic rejection (Daum et al. 1997) and a reduction in the trigger threshold. A high level array trigger (L1) formed from coincidences of signals from the individual telescopes reduces the accidental trigger rate at a given threshold allowing the threshold to be reduced. Using gated qADCs it is not possible to delay the signal by a sufficient time to develop the array trigger ($t_{\rm L1} \sim 1\,\mu$sec). In this mode of operation, digital conversion is initiated by the L0 trigger, but is vetoed if no array trigger is forthcoming resulting in a deadtime $> t_{\rm L1}$. For the VERITAS trigger configuration, this would result in a deadtime $t_{\rm DEAD} > t_{\rm L1} \sim 1\mu$sec, and a maximum single telescope trigger rate of ∼30 kHz.

The VERITAS experiment consists of an array of 7 10m ACTs (Weekes et al. 1999). For VERITAS we will use a high speed FADC on each channel to eliminate these problems. In this system digitized output samples from the FADC are continuously written into a circulating memory of depth $> 8\,\mu s$. When an L1 trigger arrives, writing ceases and the memory contents are examined for the presence of a signal. A programmable readout threshold set at a level $\sim 2\sigma$ above the pedestal fluctuations is used to provide zero-suppression for noise pulses. The FADC effectively has a method for looking backward in time up to 8μs to locate the stored digitized signal to the nearest 2 nsec sample. This eliminates the need for long delay cables, such as are typical for a system based on a simple gated charge integrator, and provides ample time for a trigger decision. Use of these devices allows operation of the individual telescopes well into the night sky background down to single telescope trigger rates in excess of ∼1 MHz. The exact pulse location for each channel can be 're-tuned' in later analysis using calibration pulses from the optical pulser and using the event data itself, allowing real-time calibration of the PMT and signal cable propagation times.

2 Description of the Prototype Electronics:

A prototype electronics channel for VERITAS has been constructed (Figure 2). The PMT signal is input to a fast shaping amplifier then fanned-out to the analog (FADC) and discriminator (CFD) logic. In order to increase the dynamic range, a novel autoranging circuit is used: The analog signal is split and is fed to two different amplifiers one with a $\times 10$ gain, the other with a $\times 1$ gain. The low gain signal is delayed and combined with the high gain signal after passing through a pair of high bandwidth switches. These switches, controlled by a discriminator, are normally closed for the high gain pulse and open for the low gain pulse; the low level signals are fed directly through to the FADC input. If the signal exceeds a threshold corresponding to the end of the 8 bit dynamic range, the low gain delayed input is switched in and the high gain input switched out. A status bit records the state of the discriminator. An 8-bit 500 MSPS FADC integrated circuit digitizes the input pulse

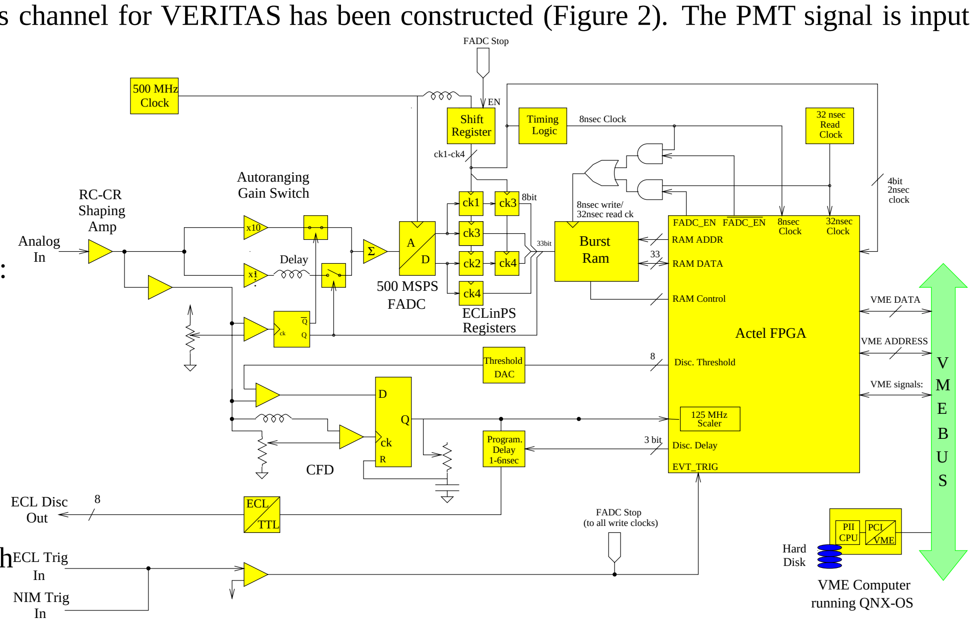

Figure 1: Schematic block diagram showing the prototype FADC/CFD. .

every 2 nsec to 8 bits resolution. The maximum slew rate at the input of the FADC will be 1 volt per 3 ns resulting in minimal aperture jitter and giving a nominal SNR of about 47 dB corresponding to 7.5 effective bits. Use of the autoranging circuit results in an extension of this dynamic range from 256 to 2560 and a slight increase in deadtime only for large (infrequent) pulses. The 8-bit resolution of this system is adequate for IACTs. The outputs of the FADC are strobed sequentially into a set of 4 8-bit ECLinPS registers every 8 nsec, with the first two registers buffered into a second level of registers on the third and forth clock cycles. This effectively converts the data stream from one 8 bit sample every 2 nsec to one 32 bit word every 8 nsec which can be strobed into a burst RAM within a 6 nsec window.

Also on the prototype is a constant fraction discriminator, implemented in fast ECL logic. The output of the discriminator is presented as a differential ECL signal on a front panel header. The discriminator has an adjustable threshold, delay and fraction, and uses a one-shot for control of the output pulse width. Use of a CFD minimizes jitter in the trigger and use of an adjustable delay on each channel allows the pulses to be aligned closely in time minimizing the coincidence resolving time of the system. This system also provides a very low time jitter signal with which to latch the 2nsec clock on the FADC, providing precise localization of the signal in the FADC memory.

The FPGA has a number of functions including control of readout of the RAM, VME interface logic, as well as a 32 bit singles rate scaler.

3 Performance of the Prototype Electronics:

The prototype electronics channel was connected through a 100 ft RG-58 cable directly to one PMT channel of the Whipple 10m camera with no external amplification. The VME crate containing the FADC and computer was mounted in an enclosure at the center of the mirror support structure. Data were taken in two modes: using the CFD to self trigger the system; and using the 2/331 channel trigger produced by the current Whipple electronics. The system was used in parallel with normal data taking.

Linearity and Charge Resolution: A pulse generator was used to provide 10 nsec pulses of adjustable amplitude both to the FADC (self triggered) and to a 1.5 GHz, 8GSPS scope. The integral of the FADC pulse is plotted as a function of the integral measured with the oscilloscope (charge) in Figure 3. This measurement reveals no significant deviation from linearity over the range of the measurement. The discontinuity above a charge value of $\sim$1500 corresponds to a change in state of the automatic gain switch for large pulses. The conversion factor from the units of FADC area (digital counts $\times$ nsec) to p.e. on the current Whipple telescope is 0.137 giving a range of 45 p.e. (below the current Whipple threshold) to 1715 p.e. (well above the end of the dynamic range of the 10 bit Whipple qADCs) for this measurement. While the trigger threshold was not set low enough to detect a single p.e. pulse, for this gain setting the total number of d.c. under a single p.e. pulse would be 7.3. Error bars indicate the rms error from repeated measurements. Using a simple trapezoidal integration algorithm, the charge resolution of the digitized pulse is better than 3% for all of the measurements shown.

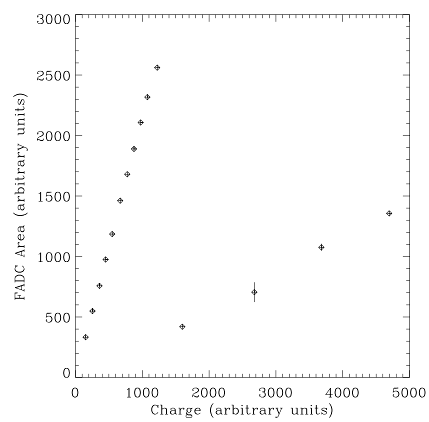

Figure 2: FADC charge measurement vs. charge measurement made with a digital oscilloscope.

Signal to Noise Ratio: The improvement in the SNR of the FADC system compared with the Whipple qADC system was determined from data taken using signals generated with a pulsed nitrogen arc lamp. These pulses have a FWHM $\approx$ 10 nsec, similar to Cherenkov light pulses. The FADC data were used to determine the average signal level for the nitrogen pulser data $S_{\rm FADC} = 2070 \pm 26$ d.c$\times$nsec and the pedestal variance $\sigma_{\rm FADC} \approx 16.6 \pm 2.5$, by integrating signals and background over a time interval of 10 nsec. The ratio of these give a measure of the SNR of the FADC: $\mathrm{SNR}_{\rm FADC} = 125 \pm 19$. For the same data set, for the other (gain-matched) PMTs the qADC electronics gave $S_{\rm qADC} = 278$, $\sigma_{\rm qADC} = 4.4$ giving $\mathrm{SNR}_{\rm qADC} = 63.3$.

The qADCs used a gate $\tau_G = 25\ nsec$, while the FADC measurement used an effective gate of 10 nsec; one would expect that the FADCs would improve the SNR by a factor of $\sqrt{25/10} = 1.6$. The measured result is statistically consistent with this ratio.

We have also investigated the utility of deconvolution of the single p.e. pulse (impulse response function) from the measured signal (e.g., Gadomski et al. 1992). The output signal $v(t)$ registered with the FADC is given by the convolution of the true Cherenkov light signal $s(t)$ and the impulse response $h(t)$. In the frequency domain $V(\omega) = S(\omega)H(\omega)$ and ideally one could deconvolve by taking the inverse Fourier transform $\mathcal{F}^{-1}[V(\omega)/H(\omega)]$. The presence of electronic and digitization noise means that $V(\omega)$ can be finite at high frequencies where $H(\omega)$ goes to zero. Thus the deconvolution will blow up the high frequency components unless an additional low pass filter $F(\omega, \omega_c)$ is applied. The deconvolution can then be written as a convolution integral: $s(t) = \left[\mathcal{F}^{-1}\left(\frac{F(\omega)}{H(\omega)}\right)\right] \otimes f(t)$ We measured the single p.e. profile using a Whipple PMT and 100 ft of RG-58 cable and found that the impulse response function was well described by $h(t) = t^2 e^{-t/2.5}$ where t is the time in nsec. We then derived the optimal low-pass filter by performing the deconvolution for a number of different cutoff frequencies ω_c, then measuring the SNR at each ω_c. The SNR was calculated from the ratio of the area under the signal pulse to the pedestal variance calculated over the same time interval. As ω_c was increased the deconvolved pulse width decreased but the pedestal variance increased. We find that while the deconvolution reduced the FWHM of the pulse (e.g., from 9.2 to 6.5) there was no statistically significant improvement in the SNR. If future work results in a useful technique, the forward convolution can be implemented as an integer matrix multiplication in the gate array.

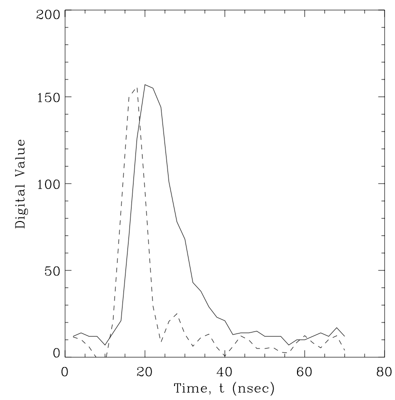

Figure 3: Solid line: a Cherenkov pulse recorded with the prototype FADC from a PMT of the Whipple telescope (FWHM = $\sim$11 ns). Dashed line: the same event after low-pass filtering and deconvolution (rescaled). .

4 Application of the Current Design to VERITAS:

For VERITAS, the single channel design will be incorporated into an 8 channel 9U VME card. 63 cards distributed in 4 VME crates will be used to read out the 499 PMT camera on each telescope. Assuming that we read 16 bytes of data for each channel above the zero-suppression threshold, with an array trigger rate of $\sim$1 kHz the total data rate will be about 300 kB/sec for each VME crate. Data will be read out from the cards using block transfers to the VME computer. This type of transfer should, in principle, permit a burst transfer rate of $>$40 MB/sec. Preliminary tests of the one-channel prototype on the Whipple telescope indicate that the current design has all of the necessary parameters for application to VERITAS.

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