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Progress in Detector Development for the All-sky X-ray & Gamma-ray Astronomy Monitor (AXGAM)

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Abstract

We are developing high resolution pixel detectors for the All-sky X-ray & Gamma-ray Astronomy Monitor (AXGAM) (Figure 1), an instrument combining Silicon (Si) and Cadmium Zinc Telluride (CdZnTe) pixel detectors with coded masks, to image the sky with arcminute accuracy in the 0.5 - 200 keV range (Tümer et al., 1997a-c; and Sushkov et al., 1999). AXGAM's wide field of view makes it well adapted to the study and monitoring of variable point sources and rapid transients such as gamma-ray bursts (GRBs) and soft gamma repeaters. Its large spectral range (3 decades), and exceptional energy and angular resolution will be important for monitoring the x-ray and gamma ray sky simultaneously. We envision AXGAM as being flown as a SMEX or a MIDEX mission to carry out an x-ray and gamma-ray full-sky survey, and to serve as an x-ray and gamma-ray monitor for future narrow field of view x-ray instruments such as Chandra. AXGAM will complement narrow-field, high-sensitivity instruments by providing notification of unusual source activity, and establishing the long-term context needed to interpret short-term, high-sensitivity observations.

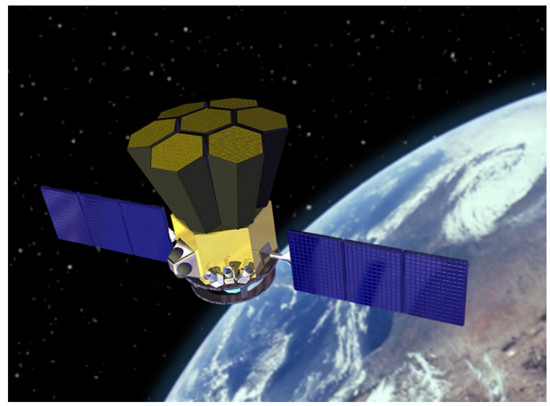

Figure 1: The AXGAM telescope in space showing the seven modules forming a SMEX size instrument.

1 Pixel Detectors:

We are developing both Si and CdZnTe pixel detectors for high energy and high spatial resolution x-ray and gamma-ray astronomy. The preliminary results obtained from testing the mixed signal ASIC readout chip developed for the pixel detectors and also results obtained from the first version silicon pixel detectors are presented below. Similar Si and CdZnTe pixel detectors for astrophysics and for application in other fields are under development (Beuville, et al., 1997; Barber et al., 1992; and Cook et al, 1998).

1.1 Two-Dimensional Silicon and CdZnTe Pixel Detectors: X-ray detection and imaging using solid-state devices has been a long sought aim of scientists and engineers. Lithium drifted silicon and germanium detectors were very successful for x-ray and gamma-ray spectrometry. The cryogenic requirement for using these devices has led investigators to search for alternative material systems that might allow room-temperature operation. Si and CdZnTe have been among the most promising because of their advantageous absorption coefficients, band-gaps, resistivities, and relatively good mobility-lifetime products. Si and CdZnTe are direct conversion detectors. The x ray or gamma ray is absorbed in the material by photoelectric process. The emitted photoelectron creates a number of electron-hole pairs (Figure 2) that is proportional to the energy of the incident photon. One electron-hole (e-h) pair is produced on the average for every 3.6 eV and 4.5 eV of energy deposited in Si and CdZnTe, respectively. The direct conversion detectors have many advantages over the indirect detectors where light photons are produced in a scintillating medium, which in turn produce electrons in a second detector. A major advantage of direct conversion is no losses during the intermediate conversion stage, giving the maximum possible signal-to-noise ratio. The electrons and holes are separated by the electric field as shown in Figure 2. With adequate bias potential, the lateral spread of the created charges is negligible and allows the detector to be made sufficiently thick to achieve high quantum efficiency without loss of spatial resolution.

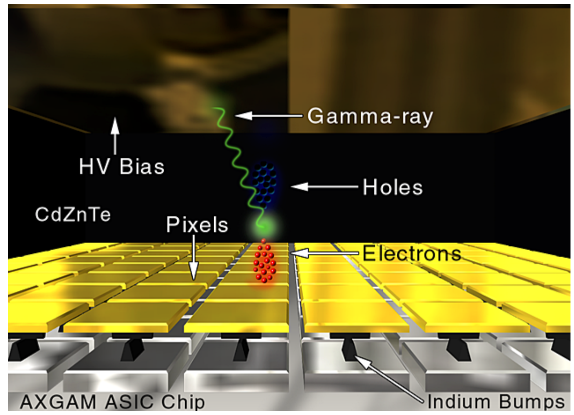

Figure 2: The concept drawing of a solid state direct conversion CdZnTe pixel detector. Inside the CdZnTe detector material is shown. The cloud of electrons and holes move in opposite directions under the influence of the applied electric field. This allows fabrication of thick detectors as the charge injections into adjacent pixels are minimal. The same diagram also applies to silicon pixel detectors. The detector pixels are indium bump bonded onto a VLSI ASIC readout chip with matching pixel pitch. The chip has a charge sensitive amplifier, shaper and peak/hold circuit under each detector pixel. A sparse readout system allows the read out of only the pixels that have data which reduces data readout times significantly.

2 Development of a VLSI ASIC Readout Chip:

The initial pixel detector developed has 16 x 16 pixel array of fine spatial resolution, 300 x 300 micron pitch (256 pixels). To read out such an array of pixels with conventional electronics is not practical. Another difficulty is routing the pixel to the perimeter of the detector. The best solution to read out such high position-resolution solid state detectors is to read each pixel directly by a VLSI (Very Large Scale Integrated) ASIC (Application Specific Integrated Circuit) with readout electronics that exactly match the pixel detector array. This allows the placement of 256 charge sensitive amplifiers, shapers and peak/hold circuits onto the same size area as the detector array. Fitting this circuitry inside a 300 x 300 micron pitch area is a challenge. Secondly, the detector pixel has to be connected to the input of the charge sensitive amplifier. This is done by indium bump bonding, which is a cold solder process. This type of detector fabrication and mounting process minimizes the input capacitance (< 100 fF), which improves the energy resolution.

A photograph of the low-noise VLSI AXGAM ASIC chip developed is shown in Figure 3. The individual pixel processor consists of a low-noise charge-sensitive amplifier, a polarity-switching amplifier, a variable shaping time amplifier/shaper, a peak detector, a peak/hold circuit, and the pixel readout logic (Figure 4). The adjustable shaping time and externally selectable polarity switch make the chip very versatile. The chip can be used with different detectors without modification by adjusting the shaping time for that detector and detecting either polarity of input signal such as electrons from CdZnTe and holes from Si. The chip readout logic has several built in modes for flexible testing, operation and calibration. The most important features are the self-trigger output and the sparse readout mode, which allows detection of an event and the reading out of only the pixels that contain the event. This will allow fast data throughput and high duty cycle. The readout of the pixel is event-driven. When a pixel reads a signal from the detector diode, the signal is shaped for low-noise performance (≈ 0.2 to 12 μs), applied to the peak detector and connected to outside through a buffer. The peak detector triggers the Comparator and produces a trigger signal. A digital circuit controls the AXGAM chip setup, operation, reset and different modes of data readout.

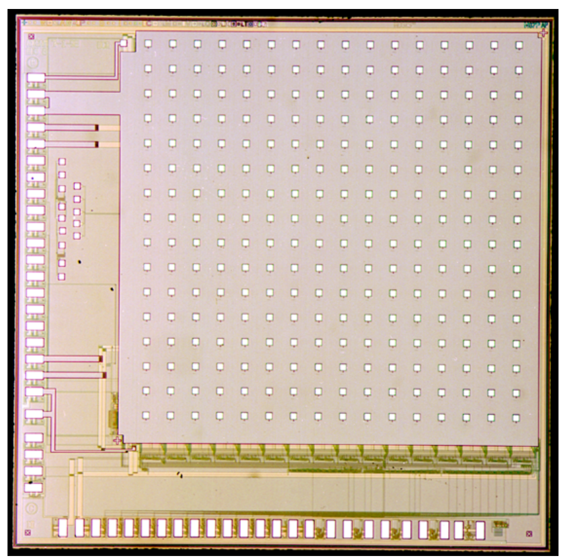

Figure 3: The photograph of the AXGAM ASIC chip. It shows the indium bump pads for the 16 by 16 array of 300 micron pitch square pixels. The circuit cannot be seen as it is covered by an aluminum layer to shield against noise

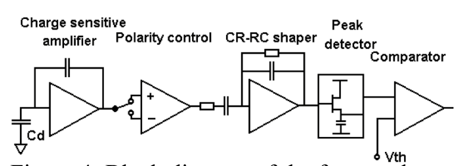

Figure 4: Block diagram of the front-end analog signal processing chain for one pixel. The detector is also shown as a capacitance, C_d.

Two of the 25 dies received from the foundry have just been tested. Both dies worked well. The preliminary results obtained show that the noise for each pixel is 28 e rms with 0 pf detector input capacitance (Figure 5) between 2 and 3 μs shaping time.

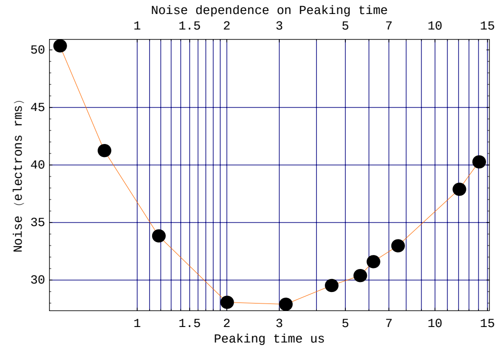

Figure 5: AXGAM ASIC pixel detector readout chip noise measurements vs. the shaping time. The optimum noise is about 28 e rms with 0 pF input capacitance at room temperature between 2 and 3 μs shaping time.

3 The Performance of AXGAM Pixel Detector:

Figure 6 shows a two-dimensional hybrid CdZnTe pixel detector. A Si pixel detector is very similar as a two-dimensional silicon PIN photo diode array replaces the CdZnTe pixel array. The detector arrays and the mixed signal ASIC readout chip described above are combined to form a "hybrid" assembly. An ultra high precision instrument forms this assembly by aligning the two sections and squeezing together the detector chip and the readout chip, each containing a matching indium bump per pixel. External electronics, connected by wire-bonds, provide the voltage biases and clock signals necessary to drive the chip and the signal pathways to multiplex out the analog signal from each detected photon.

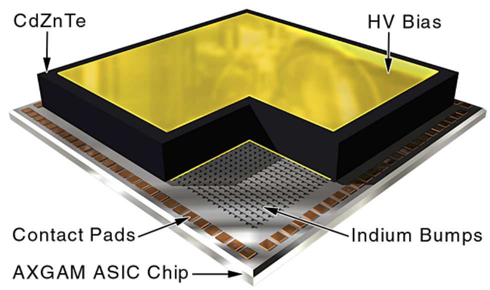

Figure 6: Hybrid CdZnTe pixel detector with CdZnTe pixel array indium bump bonded onto the AXGAM ASIC chip. The silicon pixel detectors are made similarly, by replacing CdZnTe pixel array with a silicon PIN photodiode array.

3.1 Energy Resolution Expected with Pixel Detectors: Spectroscopy is an important part of the AXGAM mission. Both the Si and the CdZnTe pixel detectors have FWHM energy resolution that will meet the needs of all of the AXGAM goals. In fact, the pixel size was chosen to optimize the resolution at the pixel level by minimizing the inter-pixel "cross-talk" caused by charge spreading in the energy range of interest. Both Si and CdZnTe have the properties required for high quantum efficiency detection of hard photon radiation, good spectral resolution, good time resolution, and the ability to provide digitally quantitative images. The properties of Si are excellent for application to x-ray imaging from about 0.2 eV to 20 keV and the CdZnTe is especially well suited for detection of x rays and gamma rays from about 2 keV to 200 keV.

3.2 Test Results of the Silicon Pixel detectors: We have built four silicon pixel detectors by indium bump bonding off-the-shelf silicon PIN photodiode arrays with the AXGAM ASIC (Figure 7). The off-the-shelf Si PIN diode array had a 151-micron pitch that was about half of the pixel size for the AXGAM chip. We have observed larger than normal leakage current from these detectors (30 μA @ Room Temp. and 3 μA @ 6 °C for the detector, and 300 nA @ 6 °C for the guard ring). Surface generation may have been the reason for the the large leakage current. Each pixel size was 130 micron and the gap between pixels was 20 micron. The thickness of the silicon PIN array was 300 microns. The active area of the PIN array was also about nine times larger than the AXGAM chip size (Figure 7).

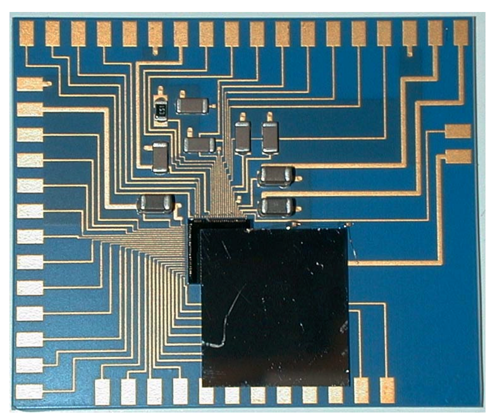
Figure 7: UCR's first SiPD, manufactured using off-the-shelf PIN diode array with 151 x 151 micron pitch and about 9 times the active area onto the AXGAM ASIC chip. The top surface of the PIN diode array is in fact a shiny aluminum coating which looks black here due to reflection. The ceramic carrier with bypass capacitors for the detector assembly is also shown.

All four of these detectors have been tested recently. Excellent results were obtained although the leakage current for these detectors was much larger than expected. The large leakage current affects the data acquisition because the chip is DC coupled. The preliminary pulses obtained from the first SiPD using a 50 V bias at 6 °C and an Fe-55 source are shown in Figure 8. The temperature is lowered to reduce the leakage current of the PIN diode array. The 11 collected oscilloscope traces for the 5.9 and 6.5 keV nuclear line pulses are well above noise. The noise with the PIN diode array mounted and biased is measured to be 58 e rms using high accuracy test pulses. Signals from the Fe-55 x-rays have been observed from all the four Si pixel detectors.

3.3 Spectra Obtained from the Si Pixel Detectors: We have obtained several spectra using radiation sources from a pixel selected at random of one of the Si pixel detectors developed. The spectra took a long time to accumulate due to the small pixel size, 0.0228 mm^2. Although the number of x-ray photons detected is not high the peaks are well defined. We lowered the detector temperature to reduce the leakage current. The improvement in the energy spectra was not significant below about -10 °C. All tested pixels and Si pixel detectors produced similar spectra and have uniform response. Several spectra from different sources were taken and two representative spectra are shown in Figures 9 and 10. The energy spectrum of the ^{57}Co source is shown in Figure 9. The 6.4-7.1 keV Fe K x-rays (54.7%) and the 14 keV peak (9.54%) are seen. The strong signal at low energies such as 6.4 keV shows that the aluminum layer deposited at the back of Si PIN diode array to apply the bias voltage did not cause significant attenuation. The thickness of this layer is important for imaging lower energy x-rays.

The ^{241}Am energy spectrum is shown in Figure 10. The lower energy peaks are clearly defined. The tiny 60 keV peak is due to the small thickness of the detector, 300 microns, and Compton scattering which dominates above ≈ 50 keV. An indication of the Compton edge is also visible. The lowest threshold is about 1 keV. We plan to use custom designed low leakage current Si pixel detectors (Ludewigt et. al., 1994) to lower the energy threshold and improve the energy resolution.

3.4 Progress in CdZnTe pixel array development: The design of the CdZnTe pixel array has been completed. High purity gold has been deposited onto the CdZnTe substrate to form the pixel structure . A photograph of 16 x 16 array of 300 x 300 micron pitch gold pixels are shown in Figure 11. The square gold ring on the perimeter is the guard ring structure. The marks on the four corners are the alignment marks specially designed for the indium bump bonding process. Several CdZnTe pixel detector arrays are in fabrication. Preliminary test results from the CdZnTe pixel detectors will be available soon.

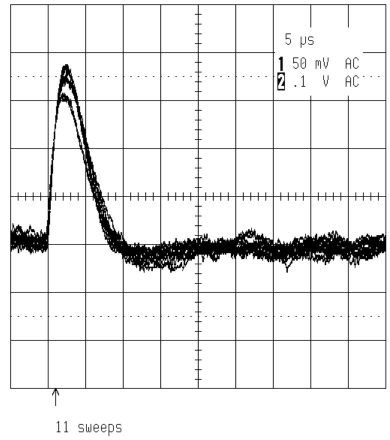

Figure 8: Preliminary pulses obtained from the first SiPD at 6 °C using 50 V bias using a Fe-55 source. This source has two very close peaks at 5.9 and 6.5 keV. Eleven sweeps are shown here.

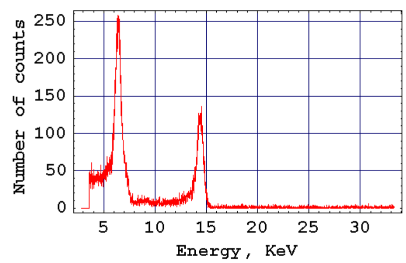

Figure 9: The ^{57}Co energy spectrum obtained from a single pixel of the Si pixel detector selected at random.

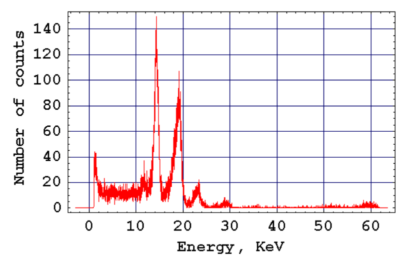

Figure 10: The ^{241}Am energy spectrum obtained from a single pixel of the Si pixel detector selected at random.

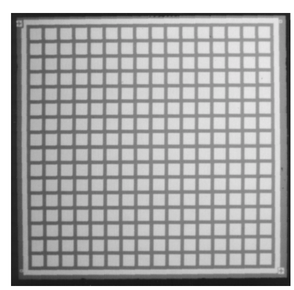

Figure 11. Photograph of the 16 x 16 array of 300 x 300 micron pitch gold pixels deposited onto CdZnTe substrate.

4 Acknowledgments:

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