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The CR-1 Chip: Custom VLSI Circuitry for Cosmic Rays

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Abstract

This paper describes a custom VLSI chip developed for use with large arrays of silicon detectors in cosmic ray experiments. It provides 16 channels of front-end electronics for integrating the charge pulse from silicon detectors and present the result as a held DC level. The outputs are multiplexed onto a common output line. The chip also has circuitry for calibration pulse injection into each channel. The noise is low enough to clearly distinguish minimum ionizing proton signals while the dynamic range of 1:4000 allows all charges from H to Fe to be measured even at large angles. The nominal power consumption is < 5.4 mW/channel.

1 Introduction:

Fully-depleted silicon detectors are used for measuring the ionization rate of charged particles in many cosmic ray instruments like the Advanced Thin Ionization Calorimeter (ATIC) experiment (Guzik et al., 1999) and PAMELA: An Antiproton, Positron Experiment on a Polar Orbit Satellite (Adriani et al., 1997). These experiments use large numbers of detectors and require the development of a custom VLSI chip to obtain low power and lightweight readout electronics. The CR-1 chip is designed for use with silicon detectors of up to 150 pF capacitance with leakage currents as high as 100 nA. It measures charges from 2.2 fC to 9 pC. When used with 380 μm thick detectors, this dynamic range is sufficient to measure charges from H to Fe even at large incidence angles. When used with silicon strip detectors in the PAMELA calorimeter it measures deposited energy over a dynamic range of 1:4000.

2 Chip Design:

The CR-1 chip is derived from the SICAL chip (Bederede et al., 1995) and the STAR chip (Beuville et al., 1996). It contains 16 channels of nuclear front-end electronics. Each channel has a charge-sensitive amplifier (CSA) followed by a shaping (SA) amplifier and a track-and-hold (T/H) circuit. The outputs of the T/H circuits are multiplexed to a common output buffer that is capable of driving a load of 1 kΩ and 100 pF. The output must settle fast enough to allow accurate readout at a multiplexing rate of 1.5 μs/channel. Multiplexing is accomplished by shifting a 'token' bit though a serial register. The register has both an input and an output allowing CR-1 chips to be daisy-chained. The output buffer is designed to be powered down when the chip is not being read. The buffer puts no load to the common output line when powered down so that 'daisy-chained' chips can be connected to a common output line.

There is a calibration circuit that uses CMOS switches to generate charge pulses from an external DC level and multiplex them into the CSA inputs. TTL logic is used for all multiplexers. The calibration circuit is designed to operate over the full range of the chip with ±5% linearity. To achieve this performance the chip is made in 2.4 μm MIETEC CMOS technology allowing a 7 V output swing. The chip is supplied with ±5 V and it nominally consumes < 5.4 mW/channel.

2.1 Charge Sensitive Amplifier: The CSA has a conversion gain of 125 μV/fC. This improves its speed, dynamic range, charge collection and pileup rejection. The CSA uses a folded cascode amplifier with a

double cascode output stage achieving a high open loop gain to get good charge collection even from 150 pF detectors. The CSA uses an 8 pF feedback capacitor which is reset with a MOSFET 'resistor' allowing the reset time to be adjustable. It can be set short enough to accept an event rate up to 30 kHz.

2.2 Shaping Amplifier: Because of the low gain in the CSA, the SA provide an additional gain of X4.4. The SA is capacitively coupled to the CSA and uses RC-CR shaping to achieve low noise, good linearity, small pedestals and low power consumption. The shaper also uses a MOSFET 'resistor' allowing the shaping time to be adjustable from 800 ns to 2 μs. To observe the outputs of the CSA, SA and T/H, special source-followers were added on channel 15 to drive these signals off-chip. Figure 1 shows the response of the SA to a charge pulse injected into the CSA on channel 15. This figure shows observed the shape of the SA output. Careful design of the SA makes it possible to restore the baseline to within 5-6% even at a peak event rate of 30 kHz as can be seen in the figure. The maximum output swing of the SA is 3V.

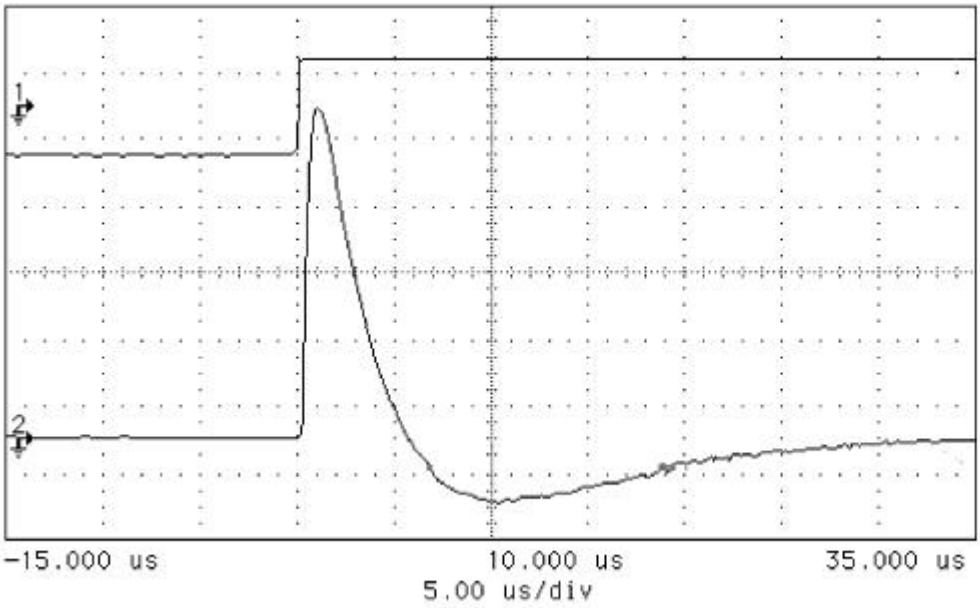

Figure 1: Shaping Amplifier Output, Trace 1 is the charge injection signal and trace 2 is the SA output.

2.3 T/H Circuit: The T/H circuit uses a 2 pF storage capacitor and dummy CMOS switches to reduce charge injection. Differential signaling is used to switch from track to hold so as to minimize the digital noise at this critical time.

3 Performance Tests:

A special test board was constructed to test the performance of the chip against all the design specifications. Using this board, chips were tested in Moscow, Trieste and Washington. Tests of the latest revision of the chip are just beginning as of this writing so results cannot be presented here. We expect to present them at the conference. The results presented below are from an earlier version and are not expected to change in the new version.

3.1 Power: The power consumption of the chip was measured with the test buffer biased and the output buffer on but not loaded. The results were 101 mW/ chip. With the test buffer not biased (which is the usual condition) the power dropped to 94.5 mW. With the output buffer off (also its usual state) the power dropped to 85 mW. If the self-trigger was turned off (as would be the case if it were not used) the power

dropped to 83.5 mW. This is the typical operating mode for ATIC so the power consumption will be 5.2 mW/ channel normally.

3.2 Calibration Circuit: The value of the calibration capacitor is designed to be 2 pF. It was measured to be 1.92 pF.

3.3 Output Stages: The chip has two buffers following the T/H circuit. The first has a gain of 1.7 to bring the maximum output voltage swing to 7V. This is followed by a push-pull output buffer to drive the design load. The output buffer was found to be capable of driving 1 kΩ and 100 pF.

3.3 Track and Hold Circuit: The T/H circuit was found to hold the signal to an accuracy of better than 1% at least 6 ms. Since the delay between switching from track to hold and multiplexing the signal onto the common line is usually the same for every event, any small change in the held signal is removed by calibration.

3.4 Crosstalk: The cross talk between channels was measured to be 1%. If one channel on a chip has a signal near the maximum of 9 pC then its nearest neighbors will see a signal of about 90 fC, about 41 times the minimum signal. This would be a problem in an experiment that must see signals near the minimum size in the channels nearest the one that receives a signal near the largest value. Fortunately, this is not a problem for the ATIC and PAMELA experiments.

3.5 Pedistals: The maximum pedestal spread within a chip was measured to be 100 mV. The maximum spread between chips was 160 mV.

3.6 Gain: The total spread in gain was 2% over all the channels in the 10 chips tested. The gain depends weakly on detector capacitance, decreasing 0.04%/pF. This is because of the large open-loop gain designed into the CSA.

3.7 Linearity: The integral non-linearity was found to be <2%. The non-linearity was measured to be <1.5% at the outputs of both the CSA and the SA.

3.8 Noise: The noise was measured at the outputs of the CSA, the SA, the T/H and the chip. At the output of the shaper the rms noise is 4600 electrons at 90 pF detector capacitance. Measurements of the noise from the CSA using a laboratory SA indicate that the noise comes almost equally from the SA and the CSA. The noise increases with detector capacitance at a rate of 8 electrons/pF.

4 Conclusions:

We have developed a chip for use with silicon detectors in cosmic ray experiments. The chip has been shown to have low enough noise to detect minimum ionizing protons at normal incidence with 100% efficiency while producing few noise signals above the discriminator threshold. With a dynamic range of 1:4000, the chip can measure cosmic ray charges up to Fe in 380 μm of silicon even at large incidence angles. The nominal power consumption is < 5.4 mW/channel.

References

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