The ANTARES digital electronics scheme

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Abstract

The ANTARES neutrino telescope will consist of an array of mooring lines carrying clusters of digital optical modules. Lines are connected through a junction box to an electro-optical cable going to the shore station. Other network nodes are the super control module at the bottom of each line, the local control module which controls a cluster of optical modules, and the optical module. Each optical module is read out using an ASIC which samples the optical module pulse at a 1 GHz rate and stores it in analogue memories. The information is digitized when a majority trigger condition is fulfilled. The digital data is then multiplexed and transferred to the shore station. On shore, a higher level software trigger is used to perform online data reduction.

1 The ANTARES detector layout

The ANTARES detector (Hubbard, 1999 and Moscoso, 1999) is aimed at the observation of neutrinos from astrophysical sources and at the study of neutrino oscillations. An array of photo-multiplier tubes detects the Cherenkov light emitted in the sea water from the muons produced by the neutrinos in the surrounding medium. The detector will consist of about 1000 optical modules on several lines read out via a single optical cable to shore. Each line is equipped with up to 48 storeys of three photo-multiplier tubes.

The electro-optical cable ends at the junction box from which the lines are connected. The next network nodes are the super control module at the bottom of the line, the local control module which controls a set of nearby optical modules and the optical module which contains the photo-multiplier tube and its associated electronics. Given the length of the line (about 300 m equipped), we envisage dividing it in eight sectors thus leading to an intermediary node between the super control module and the local control module, named master local control module.

Several possible connection schemes are being evaluated, from the star topology where one cable goes from the junction box to each super control module to the daisy chain topology where only one cable goes from the junction box to the first super control module, then from the first super control module to the second one, etc. Robustness against single point failure, easiness of deployment and recovery and cost will have to be correctly balanced in the final choice.

Offshore electronics are being developed based on front-end digitization and digital data transmission which allow the required multiplexing of the data. The loss of information is minimized and a digital link is more robust than an analogue one against pick-up noise, cross-talk, bandwidth limitation and amplitude attenuation, all problems to be faced when propagating signals over several hundreds of metres. The design is strongly inspired by the pioneering work exposed in (Chaloupka, 1996).

2 Trigger levels

Trigger level 0 is fired when the output of any photomultiplier tube exceeds a threshold corresponding to 1/4 to 1/3 of the most probable amplitude for a single photo-electron. In order to accommodate the photomultiplier tube counting rate in the sea (Palanque-Delabrouille, 1999), time coincidences of the order of 20 ns between neighbouring optical modules are used. This constitutes the level 1 trigger. A level 2 majority trigger can be built out of looser time coincidences of level 1 triggers, the time being of the order of that needed for a particle to pass through the whole detector. The level 2 condition could be at least two level 1 on the same line which will be referred as the “line trigger” or at least three level 1 triggers on three different lines which will be referred as the “array trigger”. When either the line or the array trigger condition is satisfied, a readout request

is sent back through the whole detector array. It is received in each individual optical module which starts the digitization of all the information which is in the time window corresponding to the maximum allowed time of flight.

The level 1 trigger logic will be installed in each Local Control Module. The level 2 trigger logic has to be linked to all the LCMs which may participate in the majority trigger. The line trigger could be installed at the bottom of each line, the array trigger in the junction box. However, as the distribution of readout request will originate from the junction box, the line triggers will be sent to the junction box as well.

In total, a level 2 trigger rate of a few kHz in expected. In order to cope with bioluminescence bursts, the storeys affected by a burst are removed from the trigger logic in real time.

3 Digital optical module

The use of an Application Specific Integrated Circuit (ASIC) in a digital optical module has been first suggested in (Chaloupka, 1996). It is indeed very appealing for our application as it features the following advantages:

- it needs very little physical space (a few cm^3);
- power consumption is minimal (about 200 mW);
- it suffers almost no ageing, and is therefore very reliable (MTBF $>$ 10 y);
- mass production makes it very cheap (about 100 FF/chip);
- the specifications can be tailored to our needs;

At the end of 1996 development started on an ASIC, called the Analogue Ring Sampler (ARS). The chip constantly samples the photomultiplier tube signal at a selectable frequency between 300 MHz and 1.5 GHz and holds the analogue information on 128 switched capacitors on obtaining a level 0 trigger request. The information is then digitized by an external 8 bit ADC. Figure 1 shows the resulting histogram. The effective

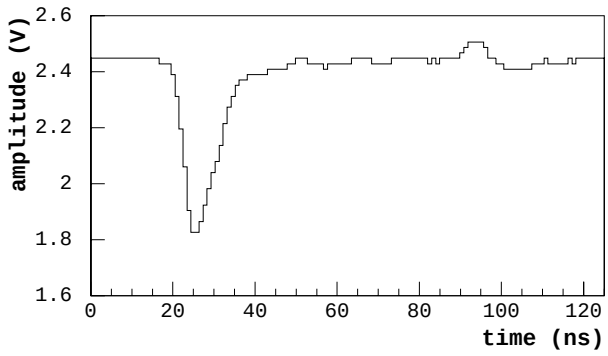

Figure 1: Charge measured in the 128 switched capacitors of the ARS memory after the capture of an analogue signal from a photomultiplier tube

sampling frequency is 1.024 GHz in this case. The reflection of the signal arises from an impedence mismatch on the test board.

Each chip contains five such channels, four of which are typically in use, the fifth being held in reserve. These capacitors have an effective dynamic range of 9 bits. In addition, the reading out of one or two dynode

outputs as well as the anode is under consideration to increase the effective dynamic range to about 18 bits. In order to achieve a relative timing of the signals to better than 1 ns, a 20 MHz reference clock is sampled on a fourth channel. A time stamp of each event can be obtained by counting the reference clock cycles. A reset command sent through the clock stream will allow all the counters of the array to be restarted synchronously.

In order to reduce the dead time and the data flow, another ASIC dedicated to the treatment of single photo-electron pulses, has been developed. The first part of the ASIC performs pulse shape discrimination (PSD). It identifies three conditions:

- large pulse if a threshold corresponding to several photo-electrons is exceeded;
- wide pulse if the time over a low threshold is longer than about 15 ns;
- multiple pulse if the first pulse is followed by a second less than 60 ns later;

If none of these conditions are satisfied, only the pulse charge and time of arrival are measured, this is referred to as single photo-electron mode. The level of the high threshold, the time over threshold and the time window for multiple pulse indicated here can be adjusted. About 99% of the event classes are represented by these three conditions. In the remaining 1% of events, the ARS is used to precisely measure the pulse shape for offline analysis.

The next version of the Analogue Ring Sampler (ARS1) is currently under development. This will integrate all these functions on the same chip, together with the ADCs, DACs and slow control interface (figure 2). A pipeline memory will be implemented to store the single photo-electron information for sufficient time to allow the level 2 trigger propagation and formation time which will be around 10 μs for a 1/10 km^2. It will be possible to use up to four memories in the token ring per digital optical module. This will permit the chip to be used with photomultiplier tubes bigger than 25 cm diameter for which the counting rate may exceed 60 kHz and for a km-scale detector where the trigger formation and propagation time may reach 30 μs. The dead-time of the front-end electronics is estimated to be limited to less than 5% when exposed to the noise rates and patterns measured in situ.

The ARS1 prototype is expected to be available for testing in September 1999.

4 Data handling and transmission to the shore

A number of electronic functions must be developed in order to process and transmit the digital data coming from the optical modules. These functions take place at each storey on the line (LCM container), at the base of the line (SCM), or in the junction box (JB). The specific functions are outlined below:

- Organizing data coming from the optical modules and transferring them to the base of the line (SCM). Segmentation of the line into eight sectors would permit the use of a 100-Mbit/s Ethernet protocol for data transfer to the base of the line. A proprietary protocol has been developed for data transfer between the levels of the segment and the collection point for the segment.
- Handling of the trigger at each storey (LCM trigger), triggering for all the storeys of a single line (SCM trigger), and triggering involving all of the lines.
- Slow control and monitoring. Involves establishing and maintaining the configuration of all of the electronic functions at each storey of the detector and at the SCM and JB electronics modules. Slow control commands will use the same data link as the data from the LCM and optical modules up to the sector controllers, where the slow control commands will be separated from the data. Through the slow control it is possible to test every electronic function from the shore.
- Clock distribution from the shore to the LCM containers and on to the optical modules, in order to timestamp all digitized events. At each level of the line the clock module will permit a shore-based

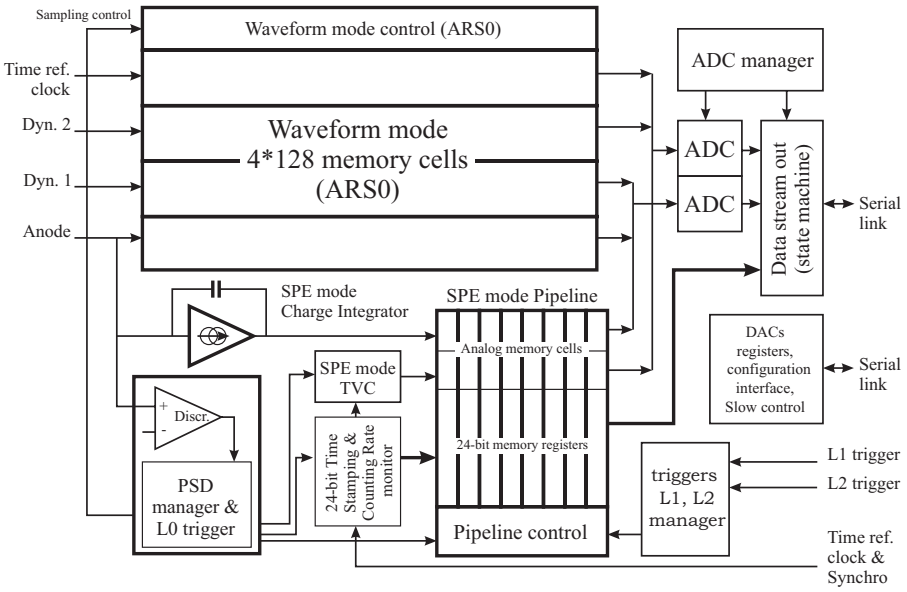

Figure 2: ARS1 block diagram

measurement of the clock propagation time, permitting an absolute calibration of the event time stamp. This measurement, and thus the time stamping of events, should be carried out with sub-nanosecond precision, under the control of a master timing station on shore.

- Handling of the acoustic positioning electronics for each line, distributed over certain levels throughout the length of the line, performed at the LCM level.
- Acquisition of mechanical positioning information used to produce an accurate description of the deformation of the lines, attitude sensors and magnetic compasses are incorporated in the LCMs.
- Transmission of data and slow control commands among the lines, the junction box and the shore.

5 Conclusion

A series of two ASICs have been developed to allow for front-end digitization and data compression of the photo-multiplier signals used in ANTARES. The development of a second generation of ASIC is currently achieved, which will allow for a compact and robust design of the ANTARES digital optical module. The use of an analogue pipeline together with a loose, adjustable offshore trigger limits the dead time of the electronics to less than 5%. Several functions are being studied to finalize the network architecture of the ANTARES detector.

References

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