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The OWL-AIRWATCH Experiment: Fluorescence Image Read-out Electronics (trigger and read out system to detect faint fluorescence signals).

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Abstract

A basic problem for the OWL-AIRWATCH (hereafter designated OA) experiment is the development of suitable trigger, read-out and data handling techniques. The very wide field of view of optics requires a large numbers of image-sensors (pixels). The complexity of the electronics, demanding a huge amount of channels, makes conventional solutions not generally suitable for mission based on space vehicles, where stringent limitations are present for power , weight and telemetry. One way to deal with such a problem, in the assumption of using a fast detector capable of detecting single photoelectrons, is to reduce the number of position and timing channels without significant loss of information. We present an On-board Unit System Trigger (OUST) and a modular Fluorescence Image Read-out Electronics (FIRE) system that are appropriate for such experiment. The modular hierarchical organization of FIRE, assisted by OUST, allows to register X-Y position and arrival time at level of the single photoelectron detection.

1 Introduction:

The OA instrument consists of three main parts: optics, focal plane detector and system electronics. An overview of the OA instrument is presented by O. Catalano (this conference 1999) whereas the focal plane detector is described by R. Stalio (this conference 1999). The purpose of this contribution is to present a general description of the proposed electronics system for the OA instrument.

In order to design a system which is reliable, it is firstly necessary to provide an architecture which is capable of being reliable for space application and then produce a detailed design which supports this architecture. A new approach has been considered for the pixel front−end, trigger and read−out electronic modules governing the ≈ 500000 pixels constituting the focal plane detector of the OA instrument. The method proposed is based on the single photoelectron counting technique that requires a fast detector response (≈ 10 ns resolving time). This suggests the use of digitized signals, which makes possible to design a simpler, low power and modular electronics system. The architectural modularity is at the base of the design. A simplified block diagram of the electronics system is shown in fig. 1. The block diagram summarizes the design concept

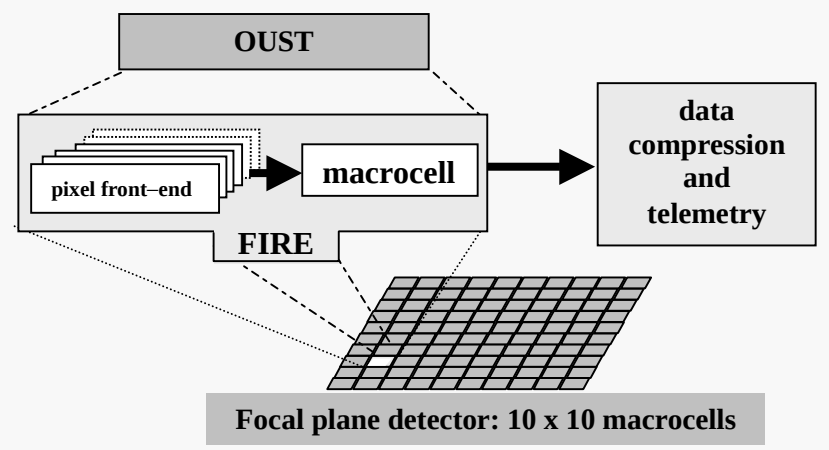

Figure 1: Focal plane detector and electronics system is schematically represented. Modularity is evident in the block diagram with one to one correspondences between focal plane macrocell and the FIRE system module.

showing the main modules. Pixels detector front–end and macrocell units constitute the **FIRE** system whereas control and trigger module forms the **OUST** module.

2 The OA electronics system modules:

As specified in the introduction, the electronics system is constituted by the two main modules that orchestrate the major functions of the system as binary readout of the detector signals, data handling, trigger decision and data validation and compression (O. Catalano, 1998).

2.1 The FIRE system: A primary objective in the design of the FIRE system is the reduction of the total number of read–out channels to minimize the power budget. This objective has been accomplished using a simple but effective design that manages the connections with adjacent pixels (respectively by rows and by columns) OR–ing them together. This function is accomplished by the pixel detector front-end module, schematically shown in fig. 2. The module functions are:

- Convert the analog detector signal into a digital signal.
- Count the digitized pulses and enable the output at a programmable digital threshold.
- Split the digitized signals for the X and Y positions and for the macrocell timing channel.

Moreover, the characteristic of this design is to reduce the pixel background rate by enhancing the signal to

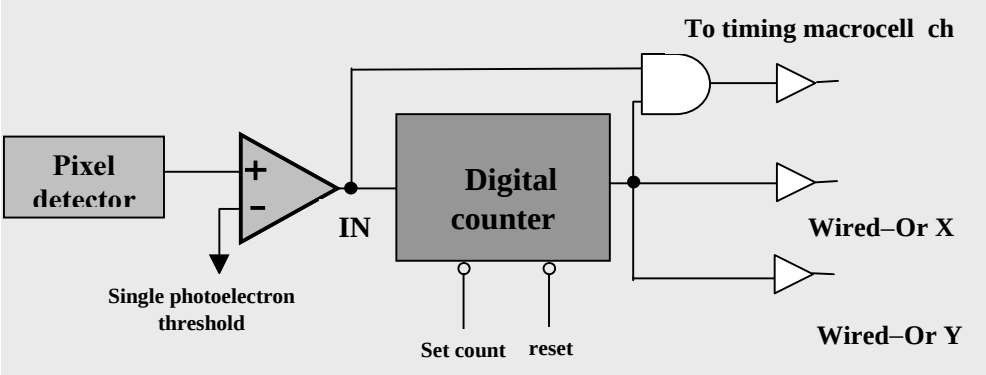

Figure 2: Block diagram of the pixel front–end electronics. Wired–Or signals of n x n pixels are connected to the correspondent macrocell.

noise ratio. In fact, setting the "set count" input of the programmable counter at an integer value **b**, corresponding to the Poissonian probability P_b to find in one pixel at least **b** photoelectrons in one GTU (Gate Time Unit), the signal to noise ratio becomes $\mathbf{(S-b+1)/\sqrt{b}}$ where **S** is the total number of photoelectrons in one pixel per GTU. The principle of operation of the pixel detector front-end is illustrated in fig. 3. Due the simplicity of the electronics parts constituting the circuit, the pixel front-end electronics is suitable for large–scale integration using ASIC (Application Specific Integrated Circuit) technology.

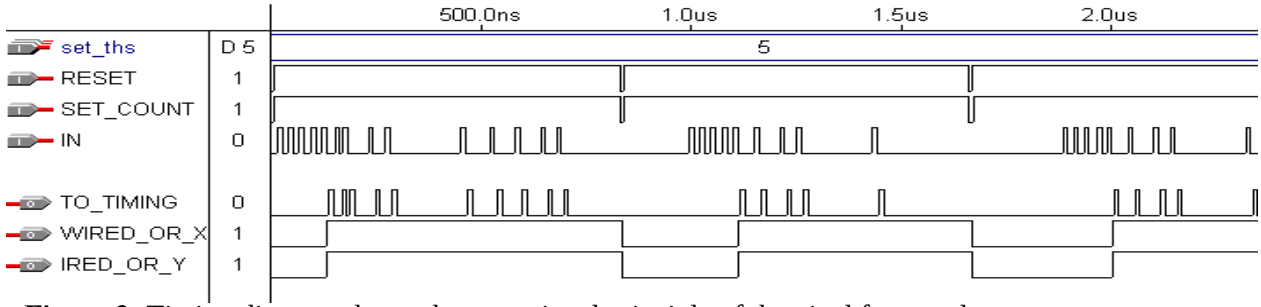

Figure 3: Timing diagram shows the operational principle of the pixel front end.

Split signals coming from the pixel front-end are routed to the macrocell. The X and Y ring–memories, reflecting the status of rows and columns, are written sequentially every GTU. The ring–memories are written continuously updating the information in the memory up to when a trigger condition is met. Finally, memories are read backward for an appropriate length given by a gate time unit counter. Fig. 4 shows

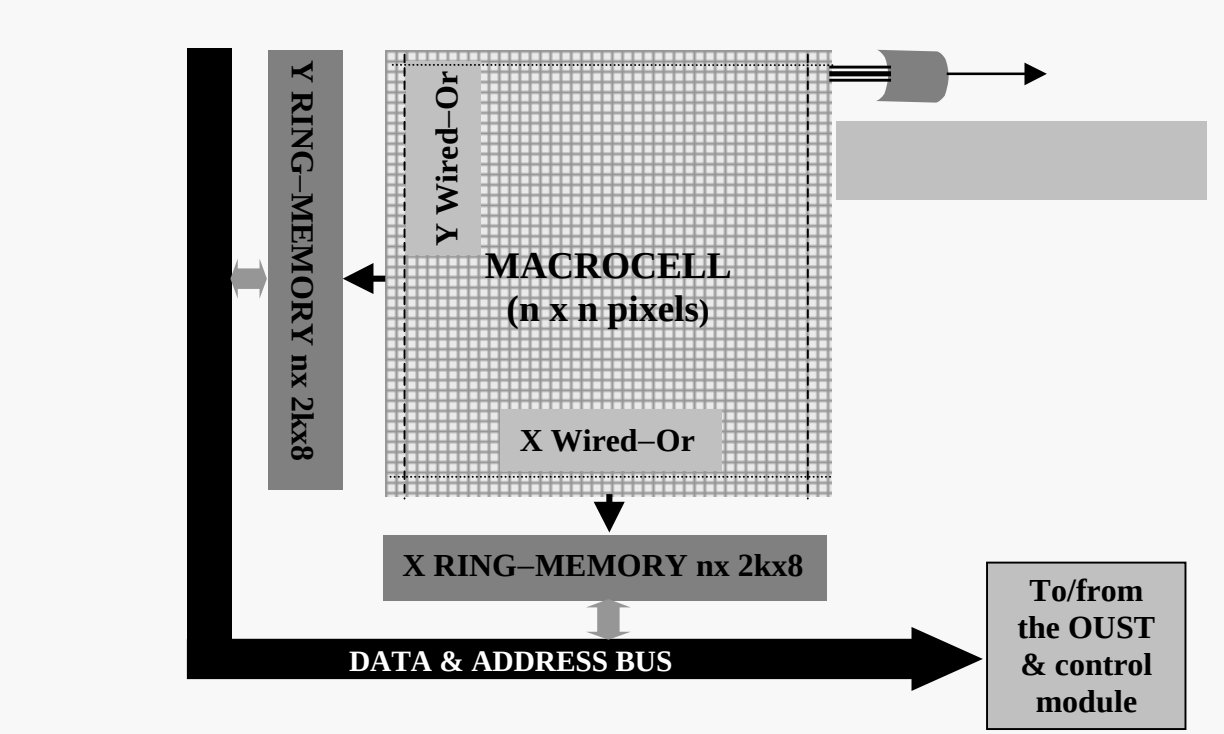

Figure 4: This particular macrocell architecture permits to reduce the number of read–out channels. In fact instead of n^2 channels, only 2 x n channels per macrocell have to be read.

schematically the macrocell architecture. In the presence of **single track** events, the ambiguity introduced by Or–ing X and Y signals, does not interfere with the reconstruction of a track, since the signals belonging to the track are coherent in space and time, whereas those that make up the background are incoherent. Fig. 5 shows the contents of the ring–memories for a simulated shower track. The X and Y projections show the track as memorized respectively in the X and Y memories. Dots represent the pixel background related to the time (GTUs) involved in the shower–event developing process. The track direction, using the X and Y projections, is derived noting that:

$$\text{tang}(\varphi) = \Delta Y/\Delta X \text{ and } \text{tang}(\theta/2)=\sqrt{\Delta X^2+\Delta Y^2}/(c\cdot t)$$

which takes into account the particle's kinematics; c the light velocity (M. C. Maccarone, this conference 1999).

A timing channel for each macrocell is foreseen in the final FIRE design. The contents of the timing channel (a specialized memory) are the digitized pulses coming from

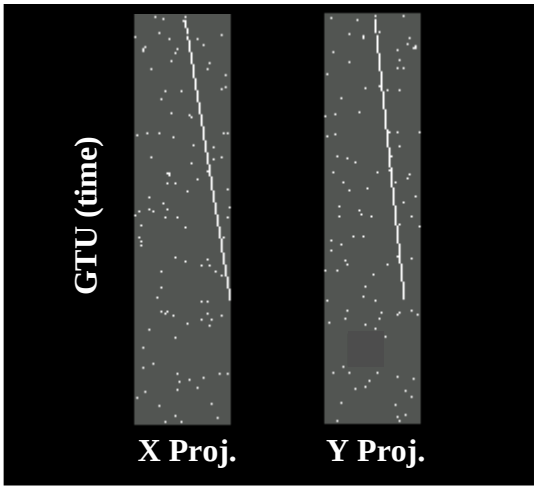

Figure 5: The track as selected and recorded, after triggering, in the ring–memories. The X and Y projections graphically shown the ring-memories content in terms of binary digital information.

the macrocell Wired-ored pixel front-end. The timing-memory give the relative arrival time as well as the number of photoelectrons detected in the corresponding macrocell using a technique developed in our Institute in Palermo.

2.2 The OUST and control module: The On–board Unit System Trigger and the control module consist of a number of programmable counters (one per macrocell), a GTUs counter, a pattern–latched register, a microprocessor. The control module contains dedicated logic for driving control signals to the macrocells. The control signals include clock, clear, set count and others auxiliary signals needed for the specific functionality required. Multiple trigger levels are supported by the OUST module by means of fast algorithms implemented in firmware and handled by the on-board microprocessor. The simpler algorithm makes use of the latch pattern register (one bit per macrocell) set, correspondingly for each macrocell, above a programmed counting threshold. The information of the pattern register is processed comparing the previous pattern with the current one (pipeline mode). The event trigger is generated if an imposed length, in terms of GTU, condition is met. The read-out of the ring-memories will be performed at that time. The flow diagram in fig. 6 illustrates the trigger performance. Due to the iterative characteristic of the process, it is possible to process statistically the information from the pattern register and to use it to set the programmable counters in the pixel front-end at a threshold level obtained from the background itself.

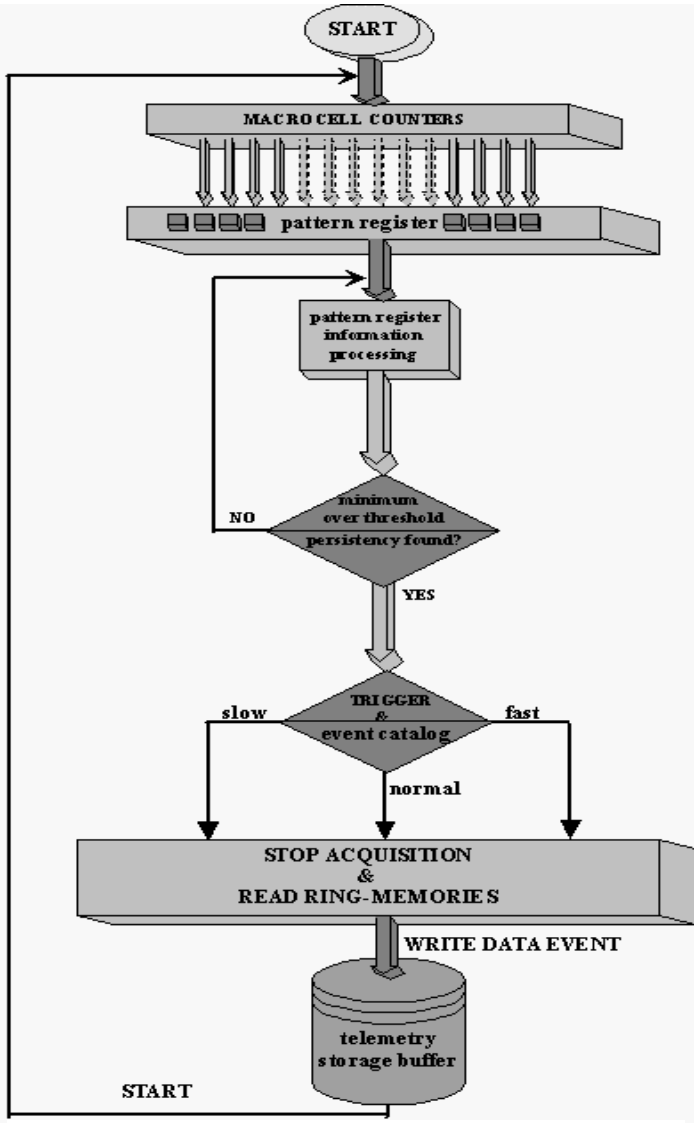

Figure 6: Flow diagram of the event trigger.

2 Conclusions:

The electronics system described here is suitable to meet the OA requirements. The detailed design is in progress and a prototyping activities will start at the end of this year.

References

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