FAST TRIGGER PROCESSOR FOR VENUS DETECTOR OF TRISTAN EXPERIMENT

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Summary

Fast look-up table processors of track finding and of the first level trigger decision have been developed for the VENUS detector. Both of them are key components of the VENUS trigger to achieve deadtimeless trigger. Even for the SSC experiment, the fast look-up table processor could be a quite powerful tool for the first and the second level trigger. It will be indispensable particularly for prompt track recognition.

Introduction

TRISTAN beam will come next fall, and we are working hard to make every part of the VENUS detector ready for data taking before beam. Most of the components of the data acquisition and trigger system have been developed and performance tests of them are ongoing. In the TRISTAN experiments, the beam-beam collision rate is expected to be very small, less than 0.01. Thus for the beam economy, any kind of event which may have useful physics must be triggered, read out, and stored in a storage device for later off-line analysis. For the same reason, the VENUS detector is designed to be a 4π, general purpose detector. Then the trigger system has to grasp every kind of useful event and reduce the trigger rate down to about 5 Hz because of limitations of data acquisition speed and of data storage capacity.

Useful signals for trigger are as follows[1]:

1) energy deposit in electromagnetic calorimeter, barrel lead glass (BLG) and end-cap liquid argon chamber;
2) track recognition on tracking devices, central drift chamber (CDC) and inner drift chamber (IDC);
3) fast timing signal of scintillation counter, T.O.F. counter.

The reasons why we are going to implement both R-ϕ track finder with CDC and R-Z track finder with IDC are:

1) to reduce cosmic ray background as well as beam-gas interaction and beam-beam pipe interaction background,
2) for redundancy of charged track trigger and for trigger efficiency check.

We are very much concerned about backgrounds originated by higher energy operation of the TRISTAN accelerator compared with its rather small radius. That makes us decide on implementation of an inner chamber having cathode pads for track finding on the R-Z plane in addition to an R-ϕ track finder. The circumference of the TRISTAN accelerator is 3 Km, and four bunch mode operation is scheduled. That turns out to be a 2.5 μs beam crossing interval, which provides a fairly long time for trigger processing. We, thus, try to form a single level, and deadtimeless trigger instead of the familiar multi-level trigger scheme. Trigger decision has to be made till certain time (0.8 μs necessary for fast clear or initialization) before next beam crossing, and we

have to reduce trigger rate to a level acceptable for data acquisition system with single-level decision. Usually a track finding processor has been implemented in the second level trigger because it takes a longer time to find tracks. Experiences of PETRA and PEP experiments teach us that taking a combination of track signals and energy deposited on the calorimeter is effective to reduce the trigger rate to several Hz. Energy-sum signal from electromagnetic calorimeters is fast enough to implement to the first level. So the key component to achieve deadtimeless trigger would be a fast track finder and a fast decision processor which has the capability of checking the correlation of a certain number of input signals. Then the first question is: how fast is the tracking chamber's signal? The central drift chamber (CDC) of the VENUS detector has a rather small cell size. Diameter of CDC cell is about 2 cm, which results in $<$ 300 ns drift time of liberated electron under 5 K Gauss axial field. Electron drift time of inner chamber is also short enough, since inner chamber has 1 cm cell size. These facts give us great hope to implement a track finder to the fist level (deadtimeless) trigger. The next questions are: what is a fast processor for track finding, and how to examine the correlation between the calorimeter signals and the track signals and make a fast decision? Intrinsic signal-formation time in the CDC and cable delay is estimated to be less than 0.7 μs, resulting in one microsecond remaining for track finding and for trigger decision using all available information. If we can develop the track finder and the decision processor with less

than 200 ns of each processing time, we can implement all available signal for trigger to the first level taking account of some contingency. The look-up table method, using high speed static RAM is the right selection to develop them. The plan of the deadtimeless VENUS trigger is shown in Fig. 1.

Track Finder

A track signal from the interaction point is a clear indication of the beam-beam interaction of and electron-positron colliding experiment. Particularly for the event like $\mu^+\mu^-$ final state, a track recognition coming from the vertex point is the only available information for the trigger. Thus the fast track finder is one of the indispensable trigger devices. Many ideas for a fast track finding method have been proposed and utilized[2] for the experiments in SPARE, PETRA, and PEP, but only a few have been implemented in the first level trigger, because most of the devices needed rather long processing times to find tracks.

We have developed a fast track finding device with look-up table method by using a high speed static RAM. This device will be implemented in the VENUS detector of the TRISTAN experiment. Since the look-up table method is a totally parallel processing system, we may expect the highest processing speed. Usually the look-up table for the trigger was made with FPLA (Field Programmable Logic Array) mainly due to its high speed. We need a more flexible track finder concerning its trigger conditions, because it is not easy to completely fix the program of trigger conditions before the start of the experiment. We can imagine situa-

tions that require us to change the trigger pattern in a short period of time according to the change of experimental conditions happening just before the start of the experiment or during the experiment. Therefore a rewritable look-up table is more convenient to the track finder. It can be produced by high speed static RAM. The static RAM access speed compatible to FPLA becomes available in these 2 to 3 years.

Look-Up Table Method

The principle of the look-up table is very simple as shown in Fig. 2. One has to prepare a large enough memory, which works as a look-up table, corresponding to the number of signal inputs. Input signals are fed to the address lines of the memory, then the data written at the address comes out with one action, just memory read-out. If one wants to implement such a naive look-up table, one has to prepare an enormous amount of memory area, for example, processing of 64 signal inputs requires a 2^{64} bit table, which is obviously impossible to implement. Most of the area of the naive look-up table is empty space. Some special combinations of the input signals are only realized and other combinations never come up in practical experiment. Such specific combinations may be estimated analytically or by the simulation. We may classify the input signals to the specific group in which the correlation is exclusively included. Then all input signals may be grouped into a certain small size of cluster. If such cluster size (size is presented by number of input signals) is less than the number of address line of the available LSI memory

chip, a look-up table corresponding to the assembly of input signals can be made up with the LSI memory chip. Thus, how to group input signals is the most critical point in the design of a look-up table.

Basic Idea of Track Findings on R-ϕ Plane

The central drift chamber of the VENUS detector has 20 layers of axial sense wire and 10 layers of stereo wire. Signals from inside 14 layers of axial wires are used for trigger. In order to form a trigger signal, signals from two staggered cells are taken AND as shown in Fig. 3. A charged particle passing through the chamber generates signals in both of the staggered cells. On the other hand, synchrotron radiation noise gives a randomly distributed hit signal, most of which turns out to be rejected by taking AND of adjacent cell signal. Taking AND of signals from the staggered layer makes 7 tracking layers for the trigger. Signals from each layer for trigger are ORed to form a basic trigger cell of which size is 1/64, shown in Fig. 3. Thus, track element will be found with these cell resolutions. A total of $64 \times 7 = 448$ signals are fed to track finding processors. To find a track element, a fan-shaped sector is formed to cover 1/64 of R- plane which is shown by the black solid line in Fig. 3. This sector can detect a track which has more than 200 MeV transverse momentum. The fan-shaped sector is decomposed to four 12 bit subsectors in order to fit a 4 K bit, high speed static RAM. Cell structures of four subsectors are shown in Fig. 4. The whole R-ϕ plane can be covered by 256 of 4 K bit RAM. Any

combination of these 12 bit can be programmed. One typical example of how to make trigger pattern follows. A simulated track generated basic hit patterns of the subsector. Taking account of an inefficiency of the drift chamber, a pattern in which any one or two cells missed should be counted as a basic pattern. If you think about track overlap and noise overlap, all patterns which include any of the basic patterns should be the trigger pattern. As shown in Fig. 3, many of the overlaps are between adjacent basic sectors. If you allow the inner-most cell missing to identify a track, both of two adjacent sectors may generate track signals by one real track. But this kind of problem can be solved by track counting with, so to speak, cluster counting technique. Each memory chip generates an on/off signal corresponding to track recognition or not. A total of 256 bit information is generated by 8 modules which cover the whole R-ϕ plane. This information can be readout via FASTBUS, which is expected to be very helpful in reconstructing tracks at off-line analysis. Four signals which correspond to one basic fan-shaped sector are ORed, resulting in 64 signals fed to the track counting logic.

Track Finder Module

One FASTBUS module can cover 1/8 of the R-ϕ plane, in other words, eight of the fan-shaped sectors are installed on one FASTBUS slave module. FASTBUS specifications are well matched to a large-size memory table, because of its large size of addressing capability and large board size. Also, a large number of pins of the auxiliary connector are open to the user, which is

essential to a large number of inputs to the large size look-up table for track finder. Functions of FASTBUS standard implementation in this module satisfies the minimum requirements of slave module, i.e., geographical addressing, secondary addressing and the control-status-register No.0 are installed.

Figure 5 shows a schematic diagram of track finder logic for CDC. The 76 input signals via auxiliary connector are latched by the timing signal made from the beam crossing signal. They are rearranged to 32 sets of 12 bit address and are immediately fed to address lines of 4K bit RAM chips which make up a look-up table. At the same moment, a read-out pulse ignites read-out action. We have used CMOS static RAM, HM6147HLP-35 (HITACHI), of which 35 ns access time is guaranteed. In practice, most RAM chips have put out signals within 20ns. RAM outputs are summed over 4 RAM corresponding to one basic fan-shaped sector. The resulting 8 outputs are supplied to the next track counting logic. Patterns in the look-up table are written via FASTBUS. Input pattern and output pattern can be readout via FASTBUS.

Processing Time of Track Finder

Time from latch-timing signal to output signal of track information is (85 $\pm$ 10)ns. A variation of readout time of used RAM was measured to be less than 5ns without selection. Output signals from the look-up table (track information) are ECL differential pulse of which width is set at about 100ns. Signal level of input is TTL and the recommended duration is more than 100ns. Since time jitter of output signal is less than 10ns, after 110ns from the latch timing pulse of input-signal, track

status can be read-in safely. Most of the processing time consumed is the timing circuit, not the RAM readout, because all timing circuits were made with standard LS-TTL and standard TTL programmable array logic. If you make a more sophisticated design of the timing circuit with advanced schottky TTL, it will be easy to achieve 50-60ns processing time for a track finder with the standard technology of a printed circuit board.

Decision Processor

The decision processor has also been developed on the basis of the look-up table method. The number of input signals to the look-up table is 16, and 8-channel additional input independent of the look-up table is prepared for an independent trigger. A block diagram of the decision processor circuit is shown in Fig. 6. Two tables are implemented. Each of them can be independently programmed. Both tables have a parity bit for security against table destruction by unexpected strong disturbance on the signal lines. The independent trigger inputs are controlled by a mask register maintained via FASTBUS. Input signal level is balanced ECL and output trigger signal is issued as an SR signal of a FASTBUS or TTL level signal via front panel connector. High speed CMOS RAM, 64K bit HM6287p-55, is used for the look-up table. Processing time of the look-up table has been measured to be 130ns.

Discussions and Conclusions

The track finder module and the first decision processor with RAM look-up table have been developed for the VENUS detector

of the TRISTAN experiment. Cosmic ray tests of the track finder and decision processor have been performed successfully by connecting with the central drift chamber. Since processing speed and stability of the track finder and the decision processor was well satisfied with the design value, we will build deadtimeless trigger for VENUS detector.

A very fast look-up table for SSC may be developed with the standard cell chip which is a standardized custom LSI including both analogue and digital circuit on one chip. For the application of track finder, for example, receiver amplifier, discriminator with threshold controller and look-up table can be implemented on the same LSI chip. Processing time of 30ns will be achieved by the on-chip look-up table. This look-up table will well match with the muon track finder of the SSC detector, even as the first level trigger. Figure 7 shows a possible scheme of an on-chip look-up table processor for a track finder. The first level processor must be installed on the detector or placed as close as the corresponding detector part to minimize signal propagation time. The maintenance of the look-up table and threshold set of the discriminator will be performed by a microprocessor installed beside the look-up table, which is linked with the host computer via optical fiber.

References

1) Proposal for study of e^+e^- reactions with a large aperture spectrometer, VENUS collaboration (TRISTAN-EXP-001, KEK), Jan. 1983.

2) See for example: H. Brafman, et al., IEEE Trans. Nucl.

Sci., Vol. NS-25, No. 1(1978), P. Waloschek, Physica Scripta, Vol. 23, 480(1981), J. J. Thaler, et al., IEEE Trans. Nucl. Sci., Vol. NS-30, No. 1(1983), A. J. Lankford, SLAC-PUB-3377, July 1984.

Figure captions:

Fig. 1 Plan of the deadtimeless VENUS trigger.

Fig. 2 Principle of the look-up table.

Fig. 3 Signal formation method of VENUS central drift chamber for track finder.

Fig. 4 Four subsectors corresponding to the RAM chip making the fan-shaped sector.

Fig. 5 Schematic diagram of the track finder circuit.

Fig. 6 Schematic diagram of the decision processor circuit.

Fig. 7 Possible scheme of on-chip look-up table processor for track finding.

Deadtimeless trigger scheme (VENUS)

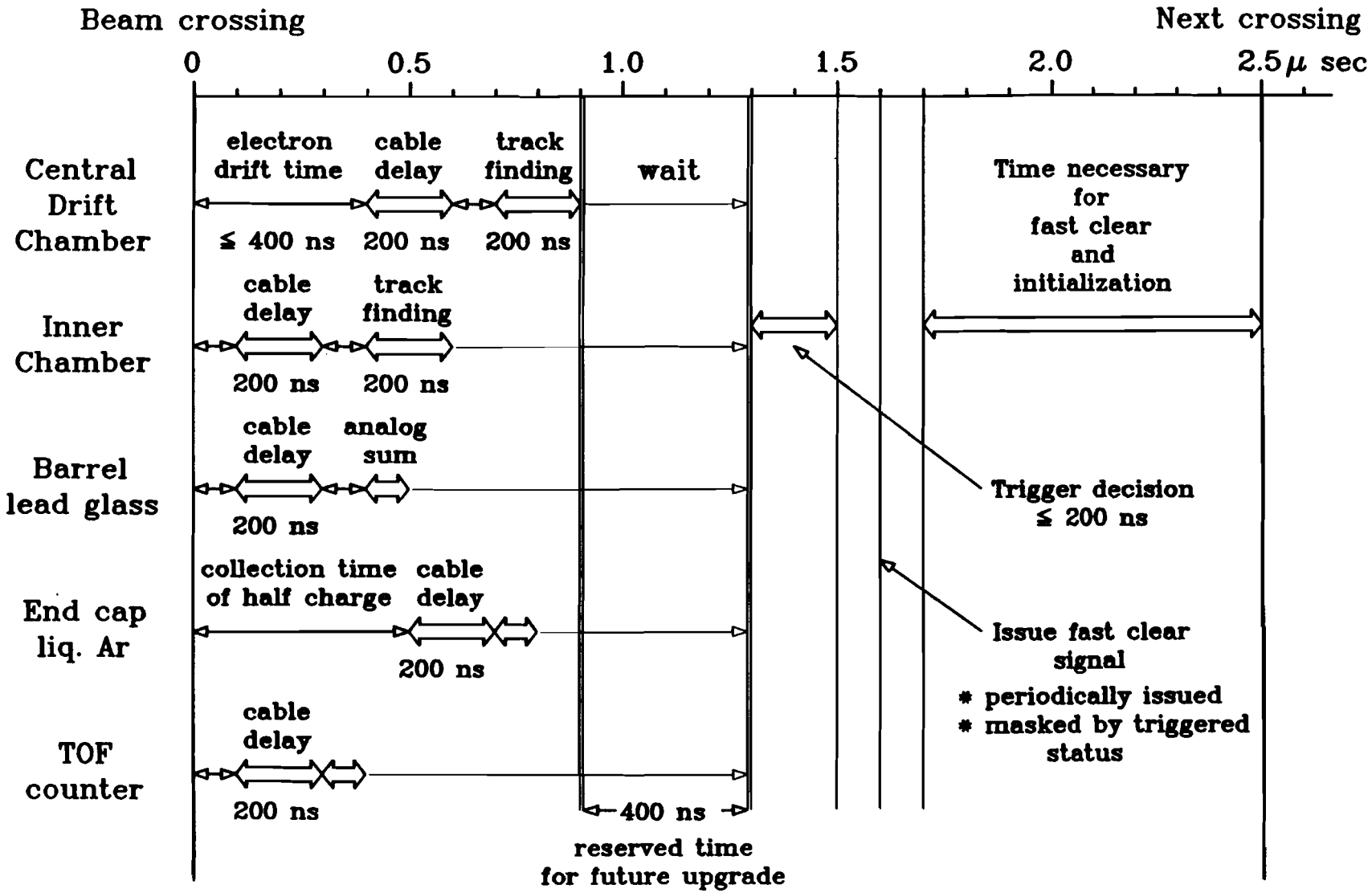

Fig. 1

Principle of Look-up Table

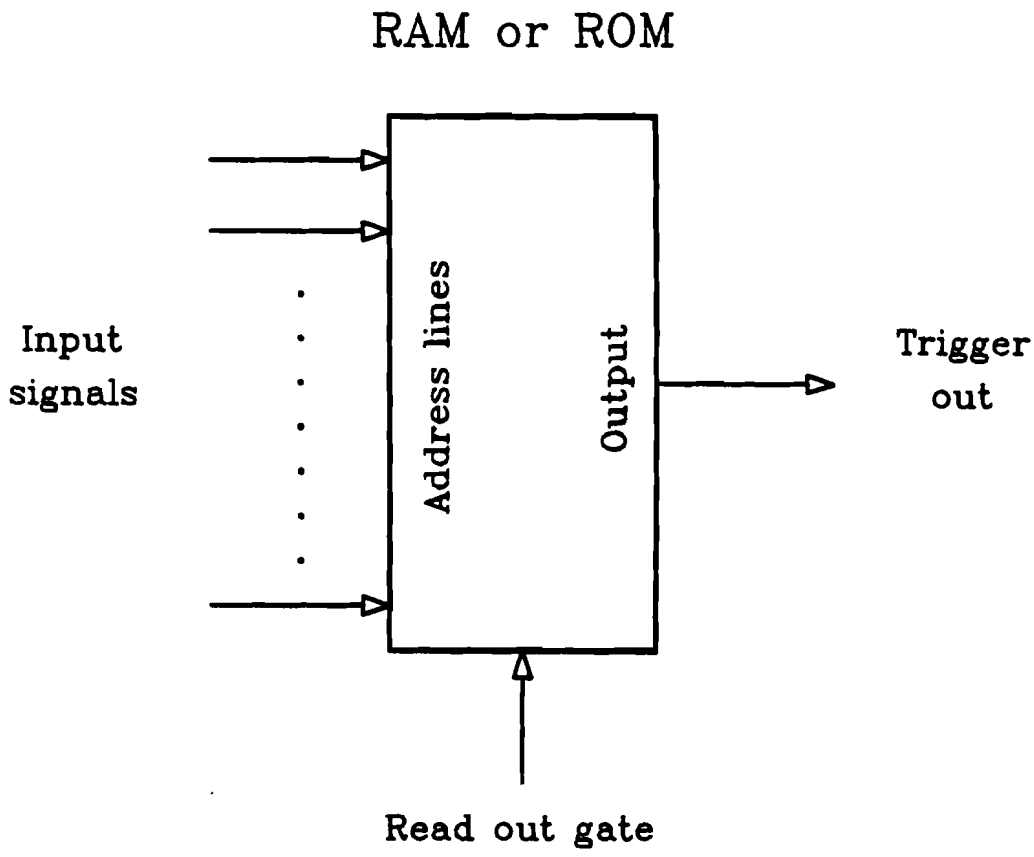

Fig. 2

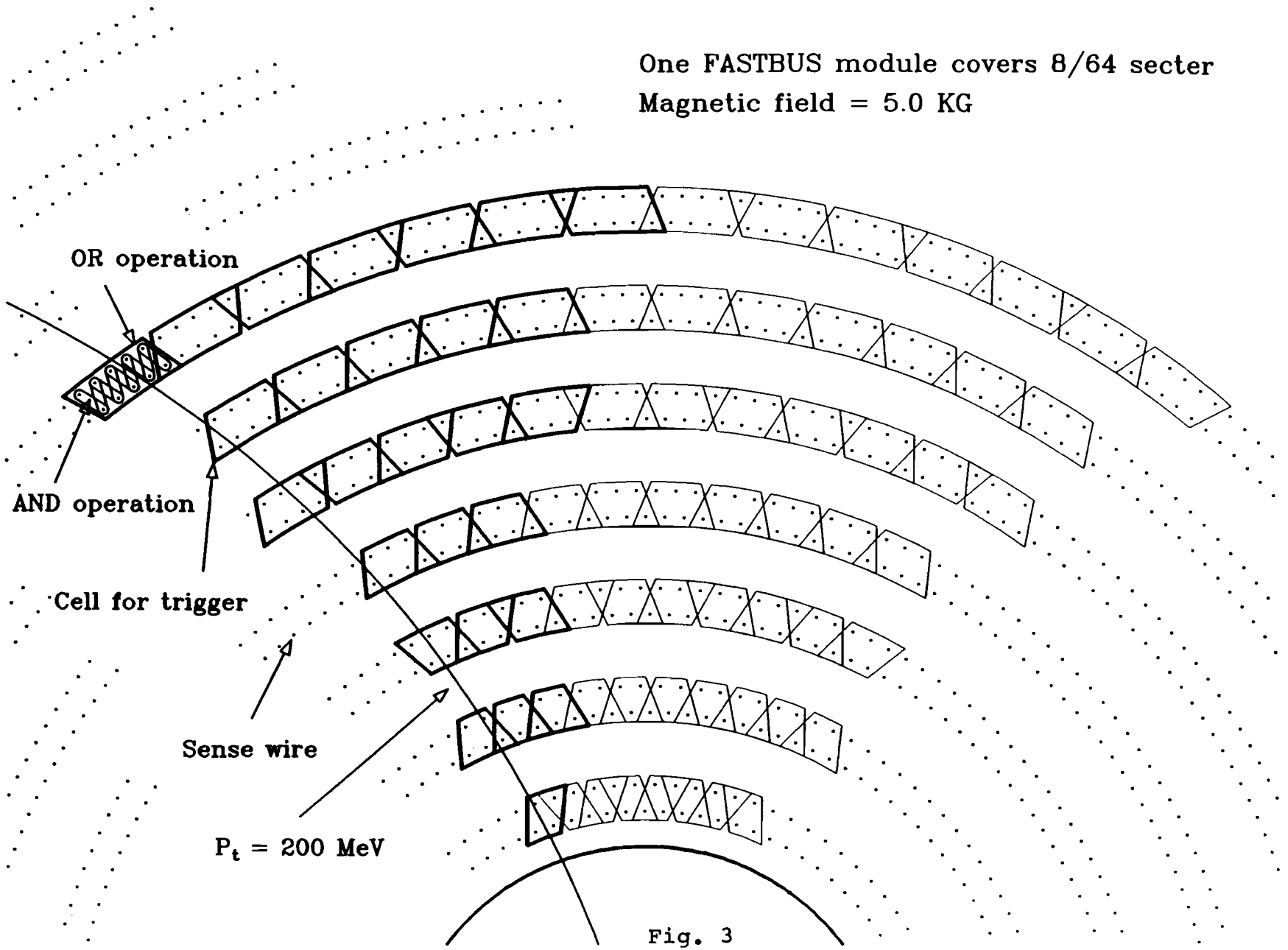
One FASTBUS module covers 8/64 secter
Magnetic field = 5.0 KG
OR operation
AND operation
Cell for trigger
Sense wire
P_t = 200 MeV

Fig. 3

Fig. 4

One FUSTBUS module covers 8/64 sectors.
Processing time from BCS timing signal
to trigger out is 120 nsec.

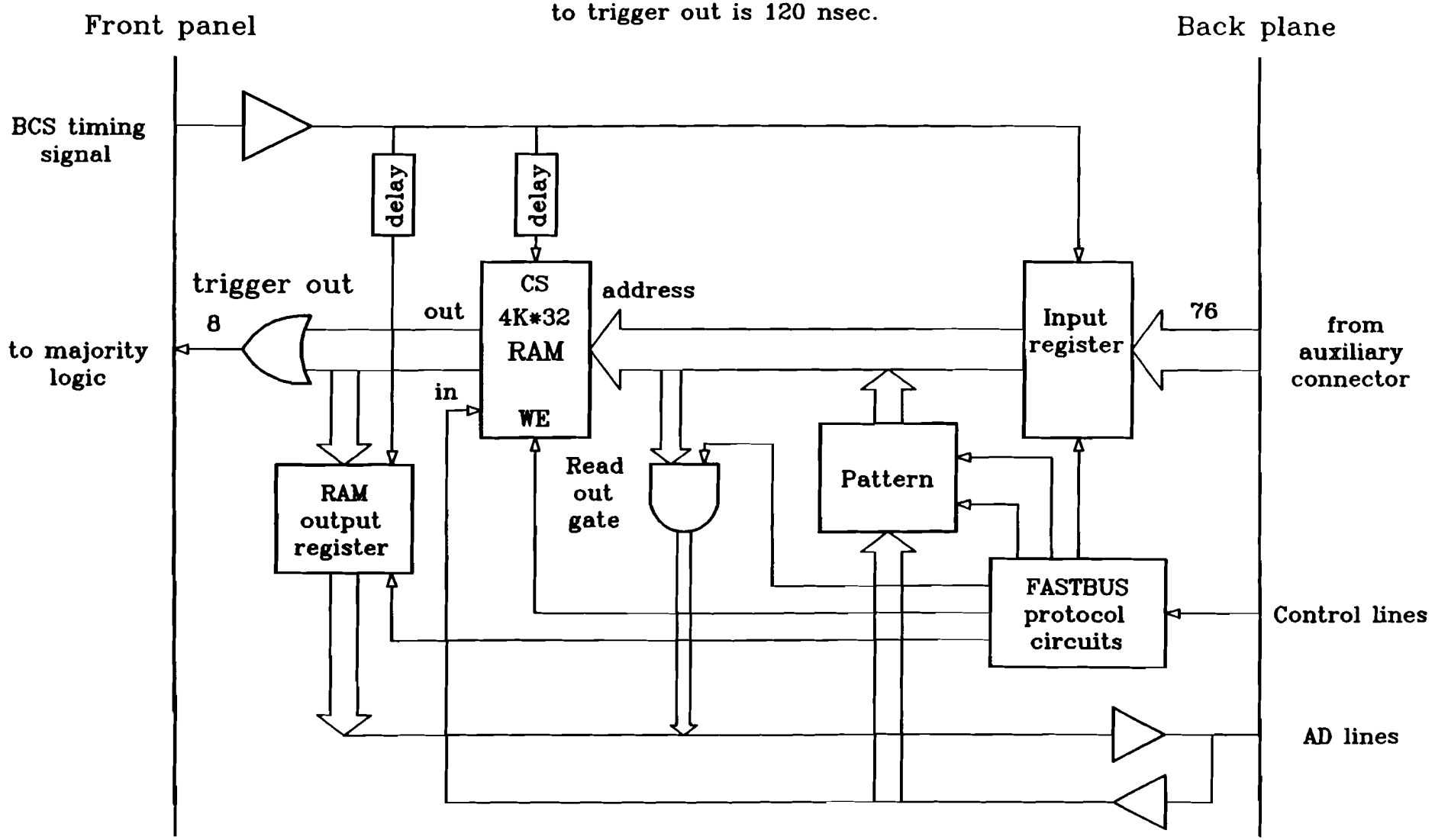

Fig. 5

Decision Processor

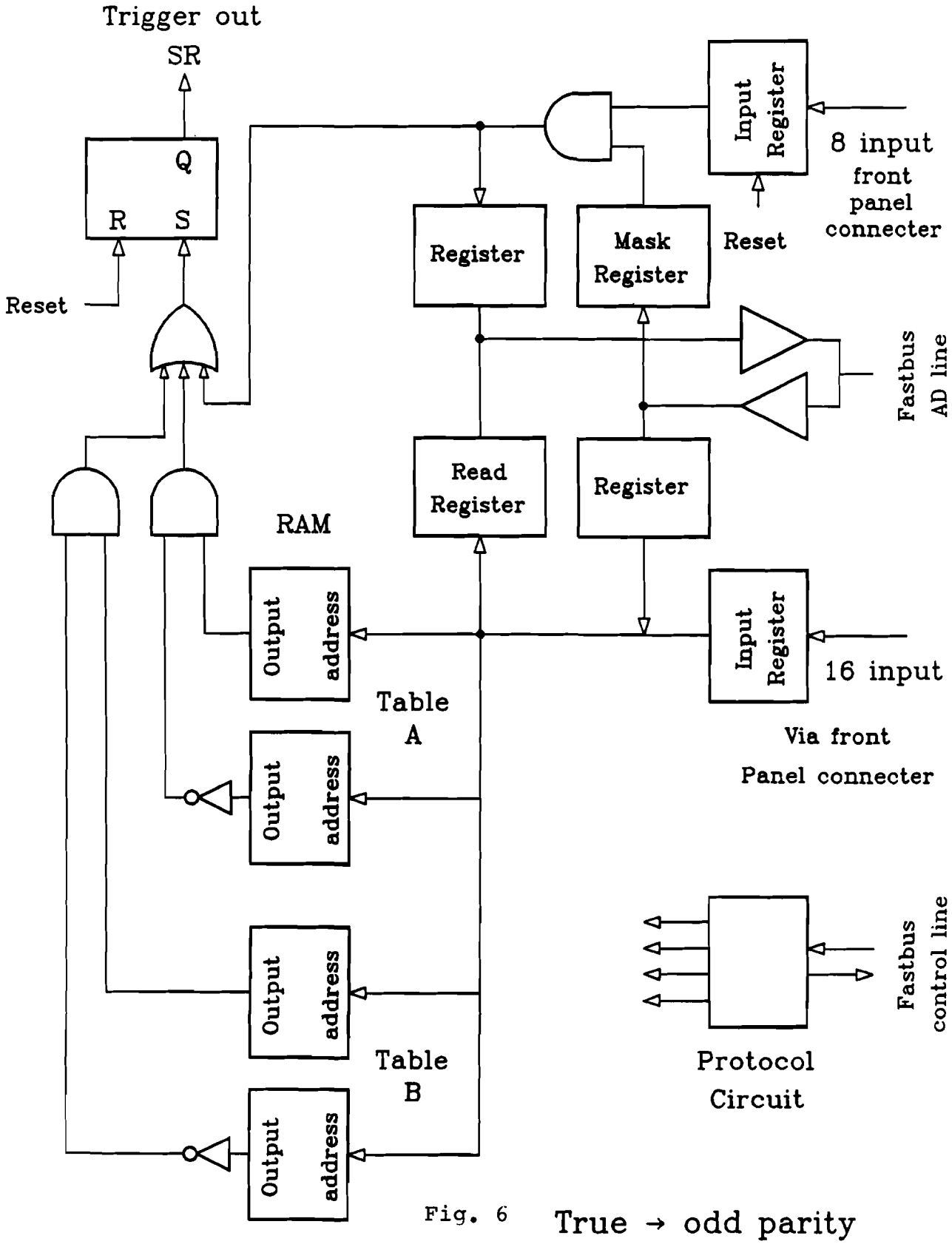

Fig. 6 True → odd parity

On-chip Look-up Table

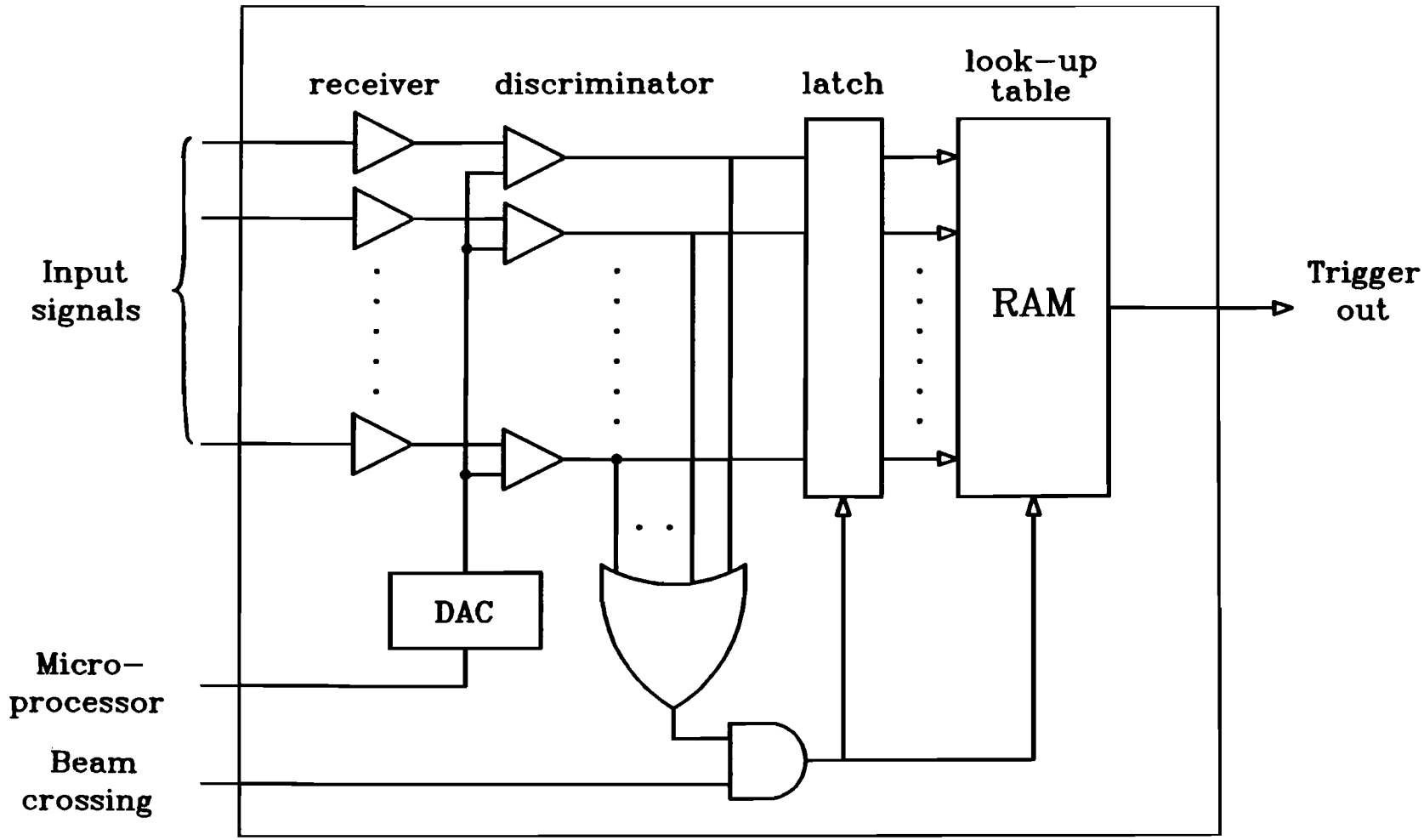

Fig. 7