THE CDF TRACK PROCESSOR - PROSPECTS FOR THE SSC

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Summary

This paper describes the CDF fast track-finding processor and discusses the prospects for using this device at the SSC. The primary purpose of the processor is to reduce the muon trigger rate from pion and kaon decays to an acceptable level. This provides an alternative to several meters of magnetized iron.

Introduction

The SSC will produce a wide variety of physics phenomena involving events with at least one muon with a momentum of 20 GeV/c or greater in the final state. Thus any general purpose 4π detector should have as complete a muon coverage as possible, not only because of interest in studying the muons themselves, but also to ensure hermiticity in the measurement of event energy. The standard approach to muon identification is to range out highly ionizing particles with large amounts of iron. This technique places an effective energy cutoff of approximately 1 GeV/meter of iron for a minimum ionizing track. It is estimated that $\sim$ 4 meters of magnetized iron will be necessary to filter out most of the background of nonprompt muons from π and K decays and hadron punchthru at the SSC. In addition, tracks with momentum below 20 GeV/c must be rejected using measurements obtained from wire chambers interleaved throughout the iron at every meter.

An alternative approach to rejecting nonprompt muons is to use a tracking chamber[1] to make a good measurement of the azimuthal angle and momentum of a charged track and then match this information to a track segment in a moderately thick ($\sim$ 1 meter) muon system. This demands

the development of a high speed track-finding processor which can locate the track in the data from the tracking chamber, calculate the track's momentum, and apply the desired momentum cut. This is the approach taken by the Collider Detector Facility (CDF) at the Fermilab Tevatron.

General Description

Processors which can use information from drift chambers to efficiently locate and measure high transverse momentum charged tracks on a very short time scale can serve several important purposes.

For Example:

1. Combining knowledge of track momenta with calorimetric information will be vital in reducing the nonprompt muon and fake electron trigger rates.

2. Smart processors can use the tracking information to trigger on specific event topologies, such as those characterizing hadronic decays of the tau lepton.

3. Information from a track processor can serve as an event filter and aid in pattern recognition for higher level triggering schemes involving CPU farms and in offline processing.

In this paper, we discuss the design of such a track-finding system for use with the CDF central track chamber (CTC). This is followed by a short discussion on its use at the SSC, and our conclusions. A general description of the CDF detector can be found in reference 2. Here we will briefly describe only the CTC.

The CTC is an axial wire chamber with 84 layers arranged into 9 superlayers. The chamber is $\sim 1m$ in radius with the outermost layer $\sim 1.3m$ from the intersection region. There are 5 axial superlayers composed of 12 concentric layers of sense wires. The remaining 4 superlayers are composed of 6 stereo layers of sense wires. Both the axial and stereo superlayers are

divided into supercells containing 12 and 6 sense wires, respectively. Since the CTC will sit in a magnetic field of 1.5 tesla, the supercells are tilted at an angle of 45° with respect to the radial direction (see figure 1) so that the drift direction is largely circumferential.

The CDF detector implements a multi-level trigger system[3]. Initially the collider will operate with 3 proton bunches and an intercollision time of $\sim 7\mu sec$. The Level 1 trigger decision is completed in less than this time. The Level 2 decision is typically completed in $< 10\mu sec$. Our design consists of two processors, each acting at a different stage of the trigger process. The first processor takes advantage of the fact that the CTC is designed so that any reasonably stiff track going through its volume must pass within $3.5mm$ of at least one sense wire in each superlayer, thereby generating so-called "prompt" hits. The first processor examines the wire patterns of these prompt hits and attempts to detect patterns corresponding to those expected for tracks with transverse momentum (p_t) of $\sim 3\ GeV/c$ or greater. Since the prompt hit information from the CTC is available $350ns$ after the beam crossing and since the systematics of this scheme depend primarily on knowledge of the CTC wire positions and the measurement accuracy on the width of the coincidence gate, the main advantages of this processor are speed and simplicity. For these reasons, this processor will be included in the first stage (level 1) trigger for CDF to aid in identification of primary muons and high p_t electrons.

There are several potential problems which must be faced by any track processor in the $p - \bar{p}$ environment. These include possible confusion from beam related noise, high occupancy rates, many low momentum tracks, etc. Use of timing information on the hits in the CTC can largely eliminate these problems and, in addition, increase the resolution of the track finding by as much as an order of magnitude over the prompt hit scheme. Therefore, we have designed a second processor which records the wire number and time (with a bin width of about $40ns$) of hits in the CTC. The device then searches the stored data for each supercell for wire-time patterns corresponding to the passage of a high transverse momentum charged

track ($p_t > 3\ GeV/c$) through that supercell, as shown in figure 2. A successfully matched pattern in a supercell forms a track "segment" for the superlayer containing the supercell. In its final stage, the second processor attempts to link together those segments which are consistent with coming from a single high momentum track. Monte Carlo simulations of this scheme show that it is possible to attain resolutions of $\Delta\phi \sim 1$ milliradian and $\Delta p_t/p_t^2 \sim 1\%$. Since the operation of this device is inherently slower than that of the first processor, its information is designed to be used in the second trigger stage (level 2) of CDF. For simplicity of design, both the prompt hit processor and the second stage processor have been designed to work with information from the axial superlayers only.

Prompt Hit Processor

The prompt hit processor is implemented in 2 hardware stages. The first stage latches all wires which are above discriminator threshold during the prompt hit gate. An 8-bit zeroes-catching latch with gate and 3-state output is formed from an advanced low power Schottky Programmable array shift register which has one flip-flop attached to each wire output from the time-to-distance converters (TDC's). The second stage reads in the prompt hits from the shift register outputs on each superlayer and searches them for all wire-hit patterns which are consistent with being from tracks with transverse momentum greater than 3 GeV/c. Each interesting wire-hit pattern is defined by a single hit in the outermost superlayer, a single hit in the innermost superlayer, and any allowed path between them in the 3 remaining axial superlayers. All interesting patterns are determined from Monte Carlo studies and then stored in a RAM array so that corrections for dead wires, off-center beam spots, changes in transverse momentum thresholds, etc. are all easily adjustable. Each interesting pattern is associated in the RAM array with a phi position where a hit in the CDF central muon detector is expected if the found track is a primary muon and a phi position where a shower in the central electromagnetic calorimetry is expected if the

track is an electron.

The prompt hit track processor is composed of 3 types of printed circuit cards. Prompt hits are stored in Latch cards which reside in the back of FASTBUS crates housing the Lecroy TDC's which process the axial superlayer data. There are 46 of these cards. Each one plugs into the Auxilliary FASTBUS connector behind a TDC module. There is one Latch Controller for each of the 4 inner axial superlayers. Each of these FASTBUS sized cards occupy one slot in each crate containing axial TDC's. There is one Master card that collates data from the 4 axial superlayer Latch Controllers and from the outermost superlayer. This card is responsible for searching through the prompt hit data for stiff tracks and for delivering information on these tracks to the Level 1 trigger system. The card is FASTBUS sized and sits in the crate containing the TDC's for the outermost superlayer.

Segment Finding Processor

The Level 2 track processor or segment finder is composed of 4 types of printed circuit cards. The first card, called the Time Memory, records the time and wire number of hits as measured by the TDC. Since recording the times for hits on all 12 sense wires in each axial supercell would be prohibitively expensive, our design stores timing information in RAM memory for only 8 of these wires. The times of the hits are binned by an onboard clock which adjusts the address for storage in the RAM memory every $40ns$. Thus, the distance of a hit from a given wire is known to an accuracy of about $2mm$ for a typical drift velocity of about 50 microns/ns. The RAM memory has the capability of storing information for 16 such bins so that hits from any part of the $3.5cm$ cell width will be recorded.

The Mask Library card stores in RAM a set of wire-time masks which represent wire *vs* time patterns in a supercell for tracks with transverse momentum greater than about 3 GeV/c (the system can be programmed to find tracks with p_t's as small as 2 GeV/c). The set of wire-time masks is generated from a Monte Carlo simulation of the passage of a charged track

through an axial supercell and includes all effects expected from varying entry angles of the track into the supercell, multiple scattering, propagation delays, etc. After the 16 bins of the Time Memory RAMs have been filled, this card then addresses those RAMs with the stored wire-time masks in an attempt to find matching patterns in the data from the TDC. A successful match constitutes a "found" track segment. Information representing the absolute phi relative to the CTC origin and the momentum of this segment are stored on the third card, a simple FIFO memory array. Since all supercells in all 5 axial superlayers are processed in parallel, the time taken to search for all interesting track segments is simply equal to the number of masks stored times the clock cycle of the 3 cards just described. We have implemented our design of these cards in ECL so that a $20ns$ clock cycle can be used. Monte Carlo studies indicate that the number of interesting masks to be stored is about 250 for the momentum resolution and cutoff stated. Thus, all track segments will be found in roughly 5 microseconds. We note that this time is independent of the complexity of the event since all supercells are searched in parallel. The speed of this stage can be enhanced if necessary by requiring less resolution in the wire-time masks. Since the number of clock cycles needed to locate all interesting track segments is simply equal to the number of wire-time masks used in the search, reducing the resolution (i.e. number of masks) by some fraction decreases the segment search time by the same fraction.

After all stored masks have been compared to the data in each supercell, the fourth card of this system reads in the data stored on the FIFO card and attempts to link together those track segments in each superlayer which are consistent with coming from a single high p_t track. The procedure for linking segments is based on the fact that if a track of transverse momentum p_t is produced with production angle ϕ_o, then, in the small angle approximation, the orientation of the track at a radial distance r from the production vertex is given by $\phi_f = \phi_o + .03Br/p_t$ where B is the value of the magnetic field of the CDF solenoid. If we characterize the position of the track segment by the azimuthal angle phi of a line drawn from the

event vertex to the track segment, then

$$\phi = \phi_o + .03Br/2p_t.$$

Thus, the difference in absolute phi between track segments in two different superlayers can be used to determine whether or not the segments are consistent with being from a single high p_t track. Our design starts with a segment from the outermost or next to outermost superlayer and loops through all track segments found in the remaining superlayers. Phi differences are calculated using a PROM lookup. If the phi difference is sufficiently small, then the segments are said to be linked. After information from the remaining superlayers has been searched, the number of segments linked to the starting segment is counted. If the number is 3 or more, then the phi and transverse momentum of the track is determined from the combined information and written to a separate FIFO memory for further processing by other Level 2 trigger hardware. The process continues until all track segments in the 2 outermost superlayers have been analyzed. Since the expected resolution of the system is $\sim 1mr$ in ϕ and $\sim 1\% \times p_t(GeV/c)$ for p_t values between 5 and 10 GeV/c, we have allotted 11 bits of phi information and 4 bits of momentum information for use by the CPU farm of the Level 3 trigger. The polar angles of these tracks can be determined by combining our information with that from a set of drift tubes which reside just outside the CTC.

Since only track segments corresponding to nearly radial tracks will be found by our set of wire-time masks, information from low momentum tracks and random hits is almost completely eliminated from the linking stage. Therefore, the efficiency of the linking card is expected to be quite high and the number of track segments to be operated on should be quite low. For this reason, we have implemented the design of this card in TTL. The designed cycle time of the card is $80ns$. We have used Monte Carlo studies to determine the average number of found segments per superlayer for typical minimum bias events and find that the average time for processing by the linking stage should be less than $4\mu s$. The total time for

locating and linking of track segments is estimated to be $10\mu sec$ or less for such events.

All of the printed circuit cards for the segment finding track processor reside in FASTBUS crates. FASTBUS protocol is used to communicate with other Level 2 processors. The cards will be tested, programmed, and read out with the host computer via a SLAC Scanner Processor. The complete system consists of 46 Time Memory cards (1 per axial layer TDC), 5 Mask Library cards (1 for each superlayer), 6 FIFO cards and 6 Linker cards (each card processes data for 1/6 of the CTC). Thus, the entire set of 63 cards can be contained in a rack of 4 FASTBUS crates. Each card is implemented with $\sim$ 200 integrated circuits.

SSC Trigger Processor

We have considered several points in regards to extending the above design to an SSC detector. The first obviously relates to the physics motivation for such a device. As we have noted, having high-quality tracking information online can greatly ease the problem of quickly identifying leptons in an event. Associating high p_t charged tracks to showers in an electromagnetic calorimeter or to hits in a muon detector is an obvious example of a way to decrease the rate for lepton triggers. Given the high resolution of the device we have described, we have determined from Monte Carlo studies that it may even be possible to flag some fraction of the muons from kaon decays by observing the kink. However, we also note that even simple missing E_T triggers are aided by information on the number of high p_t muons in an event since they can carry a substantial fraction of the energy not found in the calorimeter. If high-resolution secondary vertex detectors are to be used for triggering, then the good azimuthal information of a track processor such as ours can be matched to hits in these detectors, thereby substantially reducing the pattern recognition problem.

Given that the information provided by a track processor can be useful in triggering at the SSC, the next issue is one of speed. The high luminosity

design requires beams to collide ~ every 30*nsec.* Can the information be delivered fast enough? If we wish to maintain the resolution stated above, then it is likely that the largest increase in the speed of the segment finder will come from implementing various parts of the design as single chips rather than as a collection of integrated circuits. This may be possible with semi-custom IC design methods since, in order to be flexible in the programming of the device, we have implemented most of the design as a set of simple RAM or PROM lookups. We expect that present single chip technology can reduce the time necessary to find tracks in the CDF detector from 10μs to about 1μs. This is accomplished by the increased speeds and densities (allowing more parallelism in the design) of the semi-custom IC's. This speed would make the segment finder adequate for inclusion in both the Level 1 and Level 2 trigger decisions. Since our track processor has been designed to work for an incident trigger rate at CDF of 10^5Hz, a Level 0 trigger which reduces the rate for an SSC detector from 10^8Hz down to 10^5Hz may allow a very similar design to be used.

Conclusion

A good tracking device and a fast track-finding processor provide an alternative to the canonical 4 meters of magnetized iron as a way of studying prompt muons at the SSC. Furthermore, the advances expected in custom and semi-custom chips technologies in the next couple of years appear to make the 30*ns* crossing times at the SSC more tractable than originally thought. This is of course still a difficult and challenging problem and requires more detailed studies. Finally, we emphasize the success of such a processor will ultimately depend largely on the ability to do charged particle tracking at the SSC successfully, and this represents the largest uncertainty in this approach.

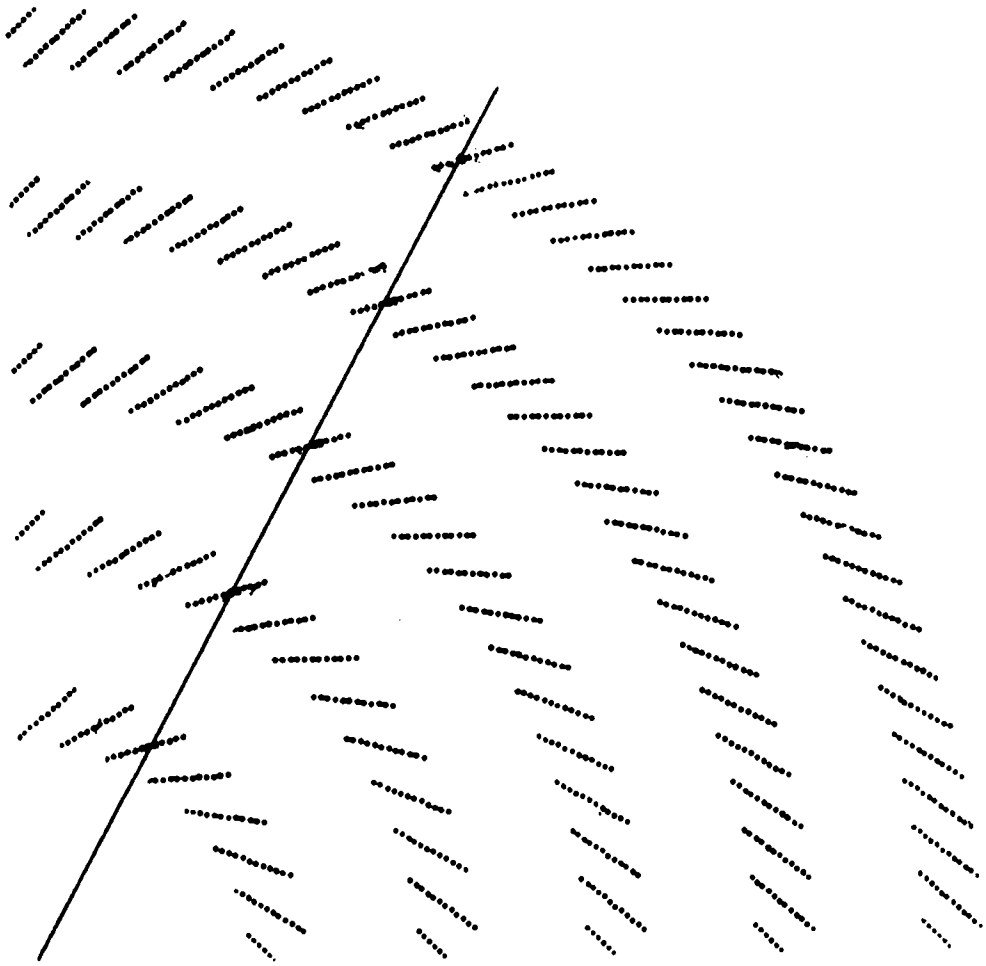

Fig.1

One quadrant of the CDF central tracking chamber along with a Monte Carlo produced charged track. Only axial layers are shown.

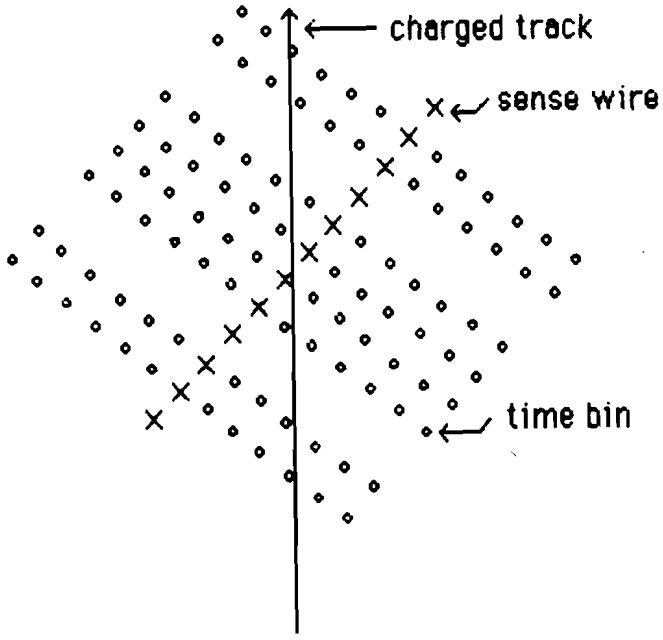

Fig. 2

Example of a wire-time plot. The small circles indicate the boundaries of the 40ns time bins. Only time bins for the 8 wires used in the segment finder are displayed.