THE MPS II - A TRACKING DETECTOR SYSTEM FOR LARGE HIGH RATE EXPERIMENTS*

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Introduction

The MPS II tracking detector system was developed for a variety of low cross section experiments that are only practical in a high beam rate environment. It was built as a general purpose device for use in a fixed target (AGS) situation where the beam passes through all elements of the detector. The electronics is dead-timeless so that high efficiency is achieved at event rates as high as 10^6/sec/ch. This capability would allow these detectors to be used as close as 20 cm from a hadron-hadron collider at 1 Tev of luminosity up to $10^{33}/cm^2/sec$.

Detector Configuration

The detector is a multilayer-modular drift chamber using stereo projections to provide for 3-dimensional event reconstruction. Figure 1 shows three planes of

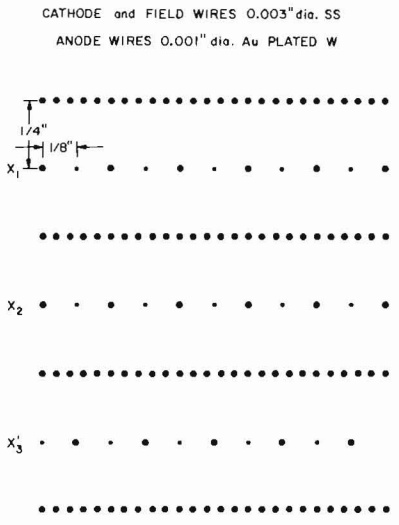

Figure 1 Three x planes in drift chamber module

the x-measuring electrodes. The compact drift cells have a linear drift time vs. distance even in a magnetic field of 10 KG. The three anode planes occupy only one inch so that straight line fits can be done locally in the module since curvature due to the magnetic field is negligible. The straight line fits usually resolve both the right-left ambiguity and give unambiguous point-slope vectors. The point-slope vectors greatly reduce the combinational problem that arises in high track multiplicity pattern recognition.

A complete module is shown in Fig. 2. In addition to the triple planes there is a double Y (vertical projection) and a U & V which are ± 30° to the Y. This completed module has all of the electronics that are replicated on an anode-by-anode basis mounted directly in the support frame space of the chamber.

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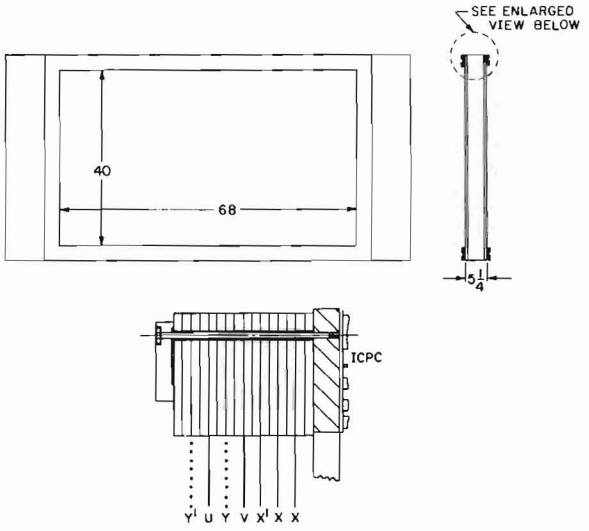

Figure 2 MPS II drift chamber module

Electronics

In order to fit the electronics that are repeated for each anode into the frame space with an anode density of 4 per inch it was necessary to develop a number of custom IC's. To insure essentially deadtimeless operation no regenative devices are allowed. Except for one fast differentiation the system is dc coupled. Figure 3 is a block diagram of the circuit. Efficiency

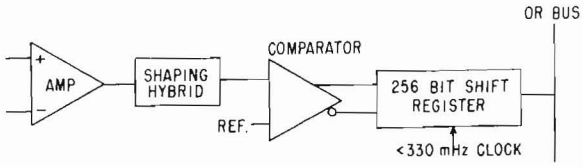

Figure 3 Block diagram of MPS II electronics

loss begins to appear only when input pulses get closer together than about 50 ns (20 MHz) per channel. All IC's and the hybrid contain 4 channels. Thus there is 3/4 of an active component per channel.

The amplifier is a transresistance amplifier -- some specifications are given in Table I. The comparator is a time over threshold device -- its performance is shown in Table II. The most remarkable element in

TABLE I

Typical Specifications for LeCroy TRA-401 4-Channel Amplifier

Input Impedance	80	ohms
Gain	17	K ohms
Noise-referred to Input	0.25	μA RMS
Input Protection	10^{-4}	Joules
Rise Time	4	ns
V^+	5.5	v
I^+	65	ma
V^-	- 2.5	v
I^-	45	ma

TABLE II

Typical Specifications for LeCroy MVL-400
4-Channel Comparator

Input Resistance	> 3	K ohms
Threshold Match	< 5	mv
Threshold Hysteresis	6	mv
Output Risetime	4	ns
Slewing 2X to 20X	3	ns
V^+	+ 5	v
I^+	170	ma
V^-	- 5	v
I^-	22	ma

the system is the digital delay-serial register which is a 256 bit shift register capable of acquiring data at speeds up to 330 MHz. To achieve this performance at reasonable power and cost a technology known as CMOS-SILICON ON SAPPHIRE (SOS) was used. To resolve events in time it is only necessary to distinguish clock ticks at a prescribed rate. So to resolve events separated by 3 ns a straightforward approach is to build a 330 MHz shift register. However, a carefully matched set of 8 phase shift registers running 1/8th as fast also resolves 3 ns. Figure 4 is a block diagram of one channel of this design. In this 8 phase

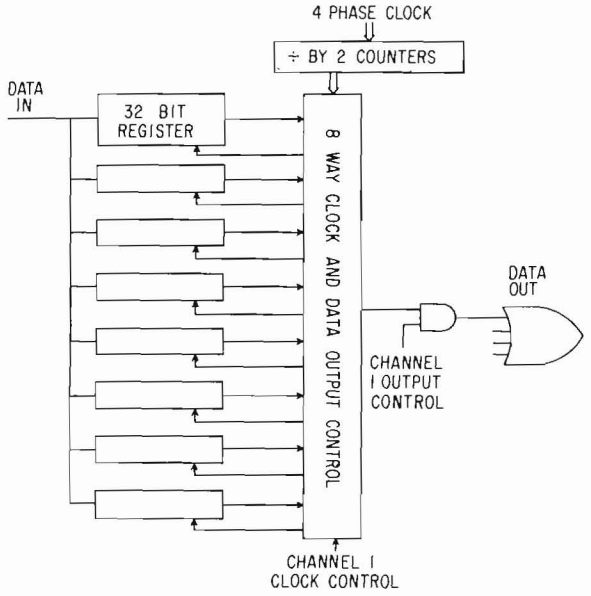

Figure 4 One channel of 8 phase shift register

register it is of great importance that the relative delay between the clock pulses and the time data is actually acquired in each of the 8 phases be accurately matched. With a primary clock of 250 MHz this phase-to-phase delay has been measured to be 4 ± .5 ns on a large number of devices. The standard deviation of this variance, a number of greater importance in drift chamber applications, is 0.3 ns.

The 4-channel shift register (SR) with control (enabling) circuitry is shown in Fig. 5. During data acquisition, 4 "ones" are in the enable register. This allows the 4-phase clock to drive all 4 channels of the SR. The data is acquired by running this 4-phase clock at 250/4 = 62.5 MHz. Precisely 1 μs after an event of interest has occurred, the 4-phase clock is stopped. Channels with data will then have a string of "ones" somewhere in the last 32 elements of the SR, the position of the furthest 1 being a precise measure of the drift time for that drift chamber cell.

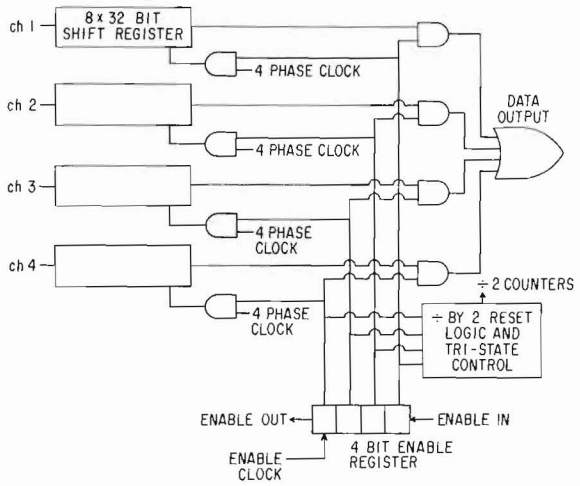

Figure 5 4-channel shift register with enable circuitry

Table III gives some important specifications for this shift register. Data is extracted by use of

TABLE III

4-Channel 256-Bit Shift Register

Clock Frequency (Effective)	DC to > 330 MHz
Phase-to-Phase Delay Match	< 1 ns
Maximum Readout Frequency (with 16 way or tie)	> 20 MHz
Power Dissipation at 250 MHz	< 200 mw

the enable circuitry which allows selection for clocking of one channel only and gating of the last register element onto a common "OR" bus. Once a channel has been selected for readout, the 4-phase clock is turned on at < 20 MHz for 32 primary ticks and the "OR" bus data is digitized by an encoder common to one whole plane of the chamber. In this way the data from a whole X plane (273 anodes) appears on a single coax cable. In addition, 2 cables bring the 4-phase clock to the plane and an additional enable-in coax and enable-clock coax completes the communication with the plane. Thus data and control for 273 anodes (or more for larger chambers) is compacted to 5 coax cables. It should be noted that the enable and clock cables are common for the whole module. Figure 6 is a picture of an ICPC containing the electronics for 64 channels.

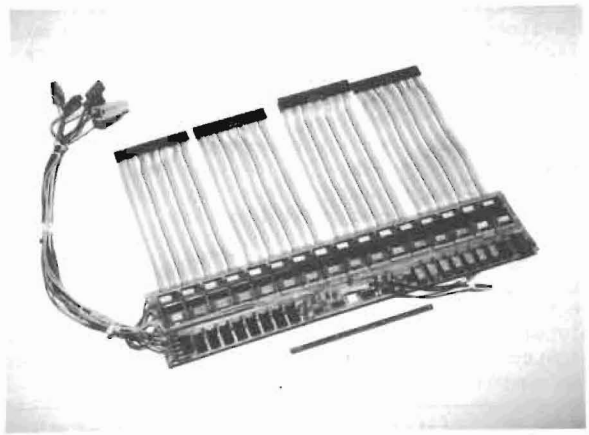

Figure 6 64 channel ICPC with input pigtail

Event Reconstruction

The MPS II has 8 drift chamber modules that can be located in the magnet to optimize the acceptance for a given experiment. Figure 7 shows the arrangement for the first experiment that has been performed. In this

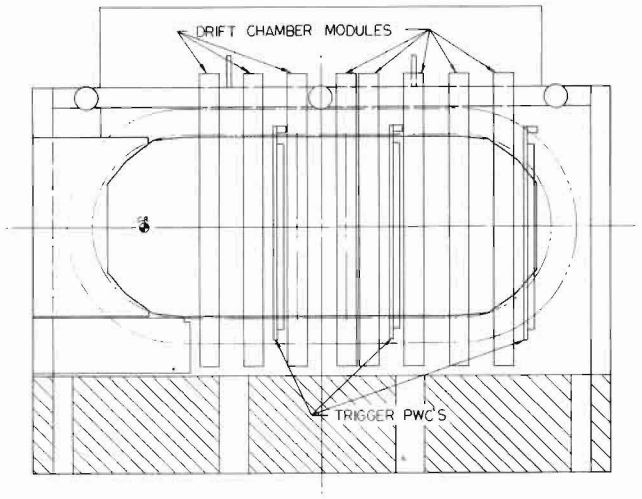

Figure 7 MPS II layout for $\phi\phi$ experiment

experiment a 22 GeV/c π^- beam produced $\phi\phi x$ from the protons in a liquid H_2 target. The $\phi \to K^+K^-$ branching ratio served as a trigger signature. Thus the experiment required $2K^+$ and a K^- or $2K^-$ and a K^+ in the momentum range of 3 to 12 GeV/c. Because of the low Q value of ϕ decay and the relative dominance of the $\phi\phi$ cross section near threshold most of the K tracks were within a few centimeters of each other in the front modules. The pattern recognition would initiate tracks on the downstream end where the tracks were spread further apart. The procedure was to find point-slopes in X and Y in each module and then track it to the adjacent module. This method greatly reduced the combinational problem associated with high multiplicity and high track density. The $\phi\phi$ reconstruction efficiency is ≈ 80% although much of the time all 4 Kaons are within 2 cm of each other in the front modules. Figure 8 shows the effective mass spectrum where all

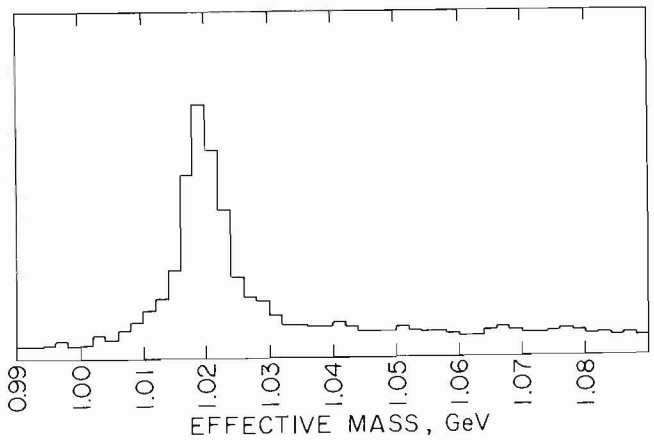

Figure 8 ϕ effective mass where all 4 tracks are identified as not a pion

four decay tracks are identified as not a pion. The unfolded resolution is σ = 4 MeV with no unexpected tails, indicating little difficulty with the track overlap on the upstream end. The missing mass spectrum shown in Fig. 9 is also very clean and is consistent with a position resolution of σ = 200 μ.

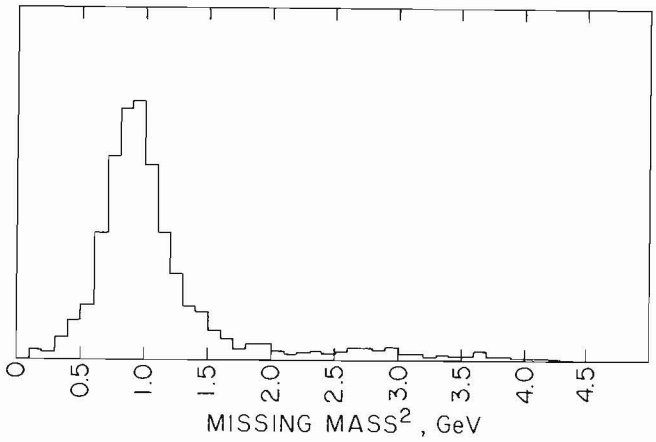

Figure 9 Missing mass where all 4 tracks are identified as not a pion and the positive and negative pairs have the ϕ effective mass.

Performance

The MPS II drift chamber system was first installed in the magnet in March 1982. By the first of June the experiment described above had acquired 1200 $\phi\phi n$ events. This was done with a beam level of 3 x 10^6 particles per second through the drift chambers. The rapid turn-on and successful operation are attributed to several factors that should be relevent to future high luminosity detectors. The system is inherently simple, utilizing less than one active component per channel. MPS II has > 12K channels and at a resolution level of 200 μ it requires no channel-to-channel corrections either for time to digital conversion factors, or position vs. time in a magnetic field.

High rate operation is limited by ion space charge buildup which at a chamber gain of ≈ 10^5 begins to reduce the gain at particle fluxes > 2 x 10^4 tracks per mm of anode wire. The other limiting parameter is pileup in the shaping circuitry which causes a few percent efficiency loss at > 10^6/s tracks per anode wire. The ion buildup limit point can probably be raised ≈ 3X by operating at lower chamber gain which implies lower electronic threshold (currently 5 μa). The pileup limit can also probably be raised ≈ 2X by use of a shorter time constant. However, even without these changes this type of detector is usable within 20 cm of a $10^{33}/cm^2$ luminosity collider as discussed in the following paper.