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## **Operation and Tests of a DDC101 A/D**

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## 1 Introduction

For the KTeV PMT laser monitoring system, one needs a high resolution device with a large dynamic range to be used for digitizing PIN photodiodes. The dynamic range should be wider than or comparable to the KTeV digitizer (17-bits). The Burr-Brown DDC101 is a precision, wide dynamic range, charge digitizing A/D converter with 20-bit resolution, packaged in a 28-pin plastic, double-wide DP. Low level current output devices, such as photosensors can be directly connected to its input. The digital output can be clocked-out serially from the pins. For typical operations, a relatively wide gate of 1 msec should be used. The full scale charge is 500 pC for unipolar mode. The bipolar mode scale is  $\pm 250$  pC. The advertised integral nonlinearity is 0.003% of FSR. This document describes only the basic DDC101 operations since full detail can be found in the DDC101 manual. Tests and results are given in section 3.

## 2 Theory of Operation

The DDC101 is used typically to digitize voltage inputs or low level current inputs that vary slowly compared to 1 kHz. Some additional work is required to digitize fast, PMT-like signals. The digitization of these type of signals is described below.

The DDC101 block diagram is shown in figure 1. There are basically 3 steps in an integration cycle. First, the DDC101 finds any initial offset charges which may be present. Next, a charge from the photosensitive device is dumped entirely onto  $C_{ext}$ , a capacitance provided by the user.  $C_{ext}$  is chosen such that the maximum voltage is less than 2.5 Volts. The DDC101 internal logic tries to keep the input at virtual ground by *transferring* charge from  $C_{ext}$  to  $C_{int}$ . Charge transfer is performed by adjusting  $C_{int}$  (to 20-bit accuracy) while keeping  $V_{ref}$  to +5 Volts. Lastly, the digital output is the final value of  $C_{int}$ , which is the value for which the charge on  $C_{ext}$  has been depleted, *minus* the offset  $C_{int}$ , which is the value found at the start of the integration cycle. Both the offset  $C_{int}$  and the final  $C_{int}$  are oversampled M times, which is just the digital filter aspect of the DDC101.

The device requires a system clock for controlling the integration cycle, and a data clock for serial data transfer. Typical clock rates are 2 MHz and 8 Mhz respectively. The user selects in software (1) K clock cycles for acquisition, (2) M clock cycles for oversampling, (3) the mode of the input signal (unipolar or bipolar), and (4) the output format.

The integration cycle is controlled by the user via  $\overline{FDS}$  (Final Data Point Start). The rising edge of  $\overline{FDS}$  initiates the beginning of the integration period (see figure 2). The first of the K clock cycles is used to reset  $C_{int}$ , which by virtue of the connections also resets  $C_{ext}$ . The following K-1 clock cycles are used by the logic to track the initial voltages present on the input. Once the initial voltage has been acquired and locked, the following M clock cycles are used for oversampling the input. The resulting M measurements is then the measure of the offset charges present.

At the end of M initial oversamplings, the pulse to be digitized is to be transferred to  $C_{ext}$ . Then, in the following N clock periods, the tracking logic, in trying to keep the input at virtual ground, transfers the charge from  $C_{ext}$  to  $C_{int}$  at a rate not exceeding  $7.8 \mu\text{A}$ . The transfer is done by adjusting  $C_{int}$  (to 20-bit accuracy) while keeping  $V_{ref}$  at +5 Volts. N should be sufficiently large in order to ensure complete charge tranference.

The falling edge of  $\overline{FDS}$  triggers the following end-of-integration activities in chronological order: (1) the taking of M final oversampling points, (2) resetting  $C_{int}$ , and (3) issuing the data valid out. The digital output is the final M oversampling measurements *minus* the initial M oversampling measurements. The subtraction is performed automatically. The data valid is issued 1/2 clock cycle after the final oversampling finishes. For a 8 Mhz data clock, 20 bits can be transferred in  $2.5 \mu\text{sec}$ . The next integration cycle can start as soon as the data has been transferred.

The duration of the entire integration cycle depends on K, M, and N, the system clock rate, and the data clock rate. Assuming, 2 Mhz for the system clock rate, one gets:

$$T \approx (K + M + N + M) \cdot 500 \text{ nsec} + 250 \text{ nsec} + \text{Data Transfer Time}$$

The user controls N indirectly by controlling T, i.e. the rising and falling edge of the  $\overline{FDS}$  signal. T should be chosen such that N is sufficiently long for complete charge tranference. The maximum transfer rate is  $7.8 \mu\text{A}$ . For 300 pC, this only takes  $38 \mu\text{sec}$  or  $N = 77$  system clock cycles. However, the charge tranference rate will decrease according to the remaining charge on  $C_{ext}$ , and so a much lower rate is to be expected. For  $T = 1 \text{ msec}$ ,  $K = 16$ ,  $M = 256$ , one gets  $N \approx 1472$  cycles.

### 3 Results

The DDC101 was tested using a 386-PC interfaced to the DEM-DDC101P-C evaluation fixture available from Burr-Brown. A PIN photodiode,<sup>1</sup> with no additional amplification, was connected to  $C_{ext} = 250$  pF connected to the input. Here, T, K, M, and the system clock are 1 msec, 16, 256, and 2 Mhz respectively. The device was operated in bipolar mode. Figure 3 shows the pedestal mean and rms, where the mean is due to dark current in the PIN diode. Here, the maximum digital output has been assigned the value of 1, also corresponding to 250 pC. The mean PIN diode pedestal value would imply a dark current of about  $9.1 \times 10^{-4} \cdot 250 \text{pC} / (1 \text{ msec}) \approx 0.2$  nA. Also, one sees that the rms noise is then  $1.4 \times 10^{-5}$  of the maximum digital output. With the PIN diode disconnected, the pedestal mean and rms is shown in figure 4. Figure 5 shows the pedestal (with PIN connected) variations over a 24 hour period. The origin of the variations maybe related to temperature variations. Further studies on this subject are under way.

Next, the PIN diode (PIN DDC) was exposed to pulsed light from a scintillator, which was pumped by a laser. Another PIN diode digitized by a LeCroy 2249W ADC (PIN 2249W) simultaneously viewed the pulsed light. The light level was varied such that PIN 2249W varied between 50 and 1000 counts.

Figure 6 shows PIN DDC vs. PIN 2249W, the residual from the line fit, the percentage residual from the line fit, and  $\text{rms}(\text{PIN DDC}) / (\text{PIN DDC})$  vs. PIN 2249W. The last plot indicates a 'relative error' of 0.05% at 1000 PIN 2249W counts. Again, the maximum digital output was assigned a value of 1. The PIN DDC charge at PIN 2249W = 1000 is then  $\approx 125$  pC.

Figures 7, 8, and 9 show the same for PIN DDC charge (at PIN 2249W = 1000) equal to 58 pC, 7.5 pC, and, 0.85 pC respectively. The PIN DDC charge scale was set by placing a neutral density filter in from of PIN DDC while keeping PIN 2249W unattenuated. For all PIN DDC charges, the figures show good linearity relative to the PIN 2249W. There is smooth behavior throughout the range 0-125 pC. Figures 6-8 show small relative errors, basically identical to each other. In figure 9, one begins to see the contribution of noise to the relative error. The offset due to the PIN dark current is clearly seen. From the pedestal rms, one would predict a pedestal error of  $1.4 \times 10^{-5} / (0.0034) = 0.4\%$ , which is consistent with the figure 9. Even for a charge of 0.85 pC, the PIN output is due to  $\approx 10^6$  e-h pairs, so the photostatistical error is still small.

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<sup>1</sup>A unity gain device.

## 4 Acknowledgments

It is my pleasure to thank Sten Hansen for introducing to me this chip and his explanation of its workings. I also thank the Physics Department E-shop for their support.

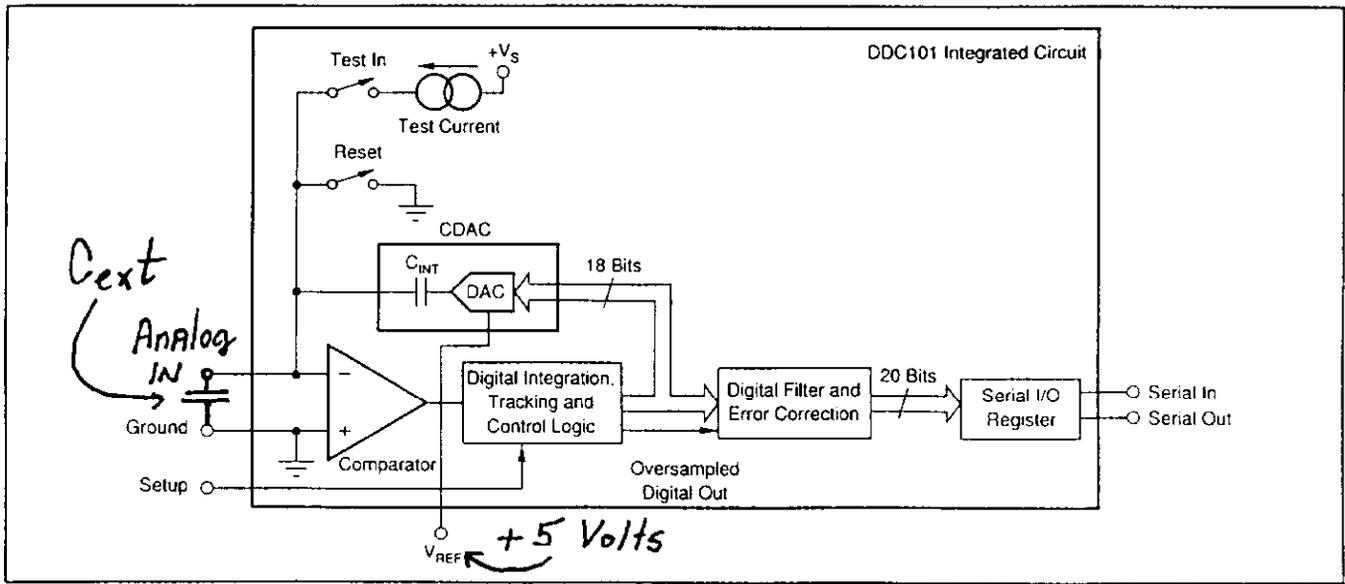


Figure 1

# DDC101 Integration Cycle

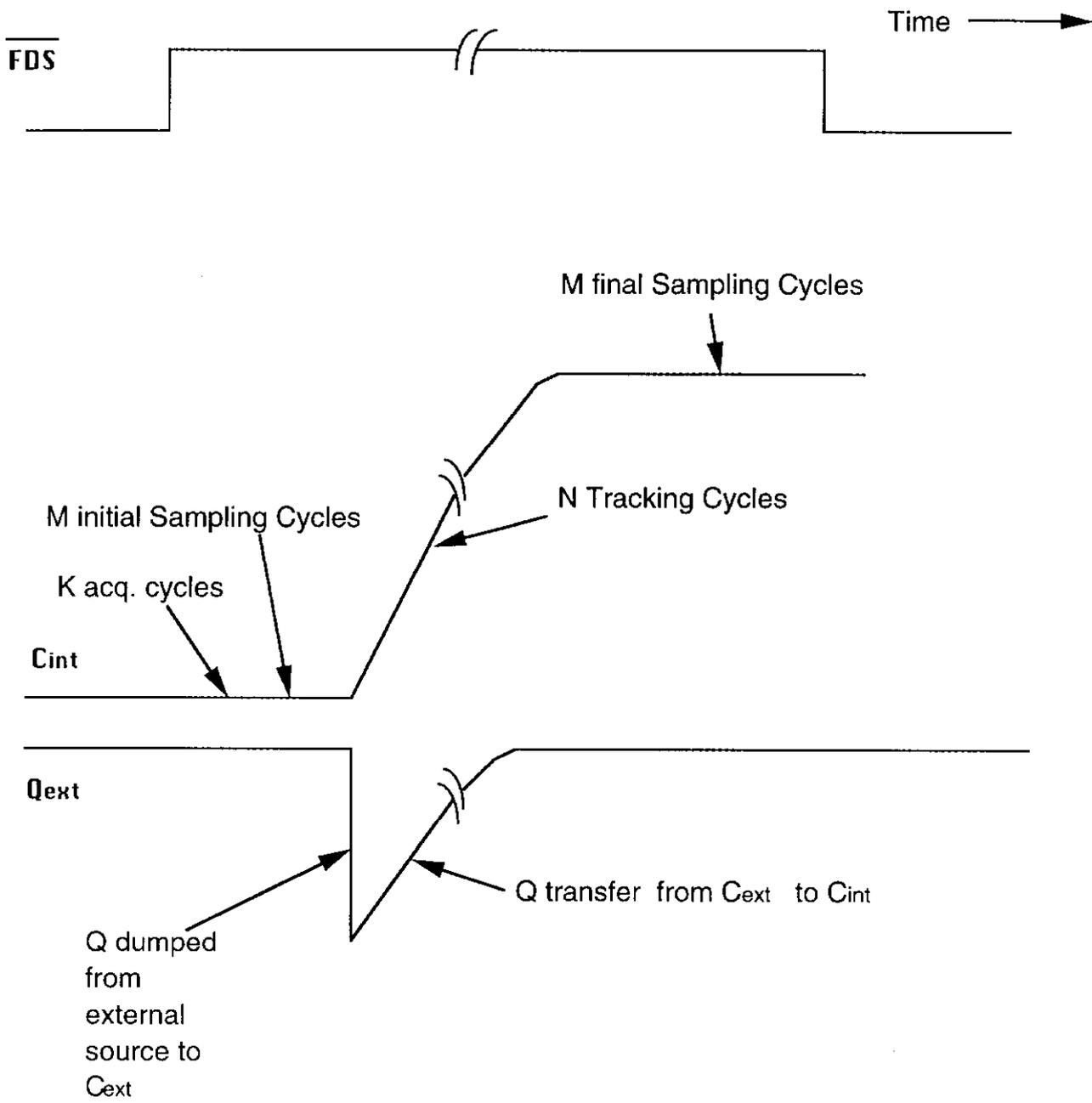


Figure 2

Fig. 3

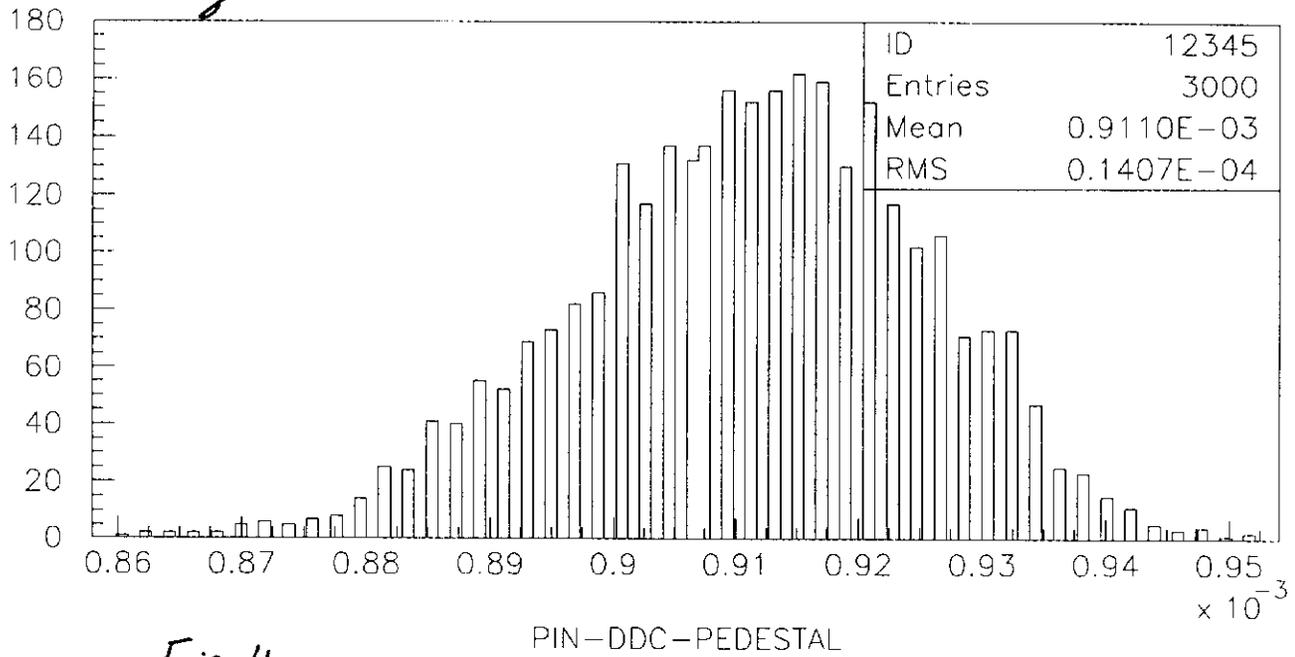
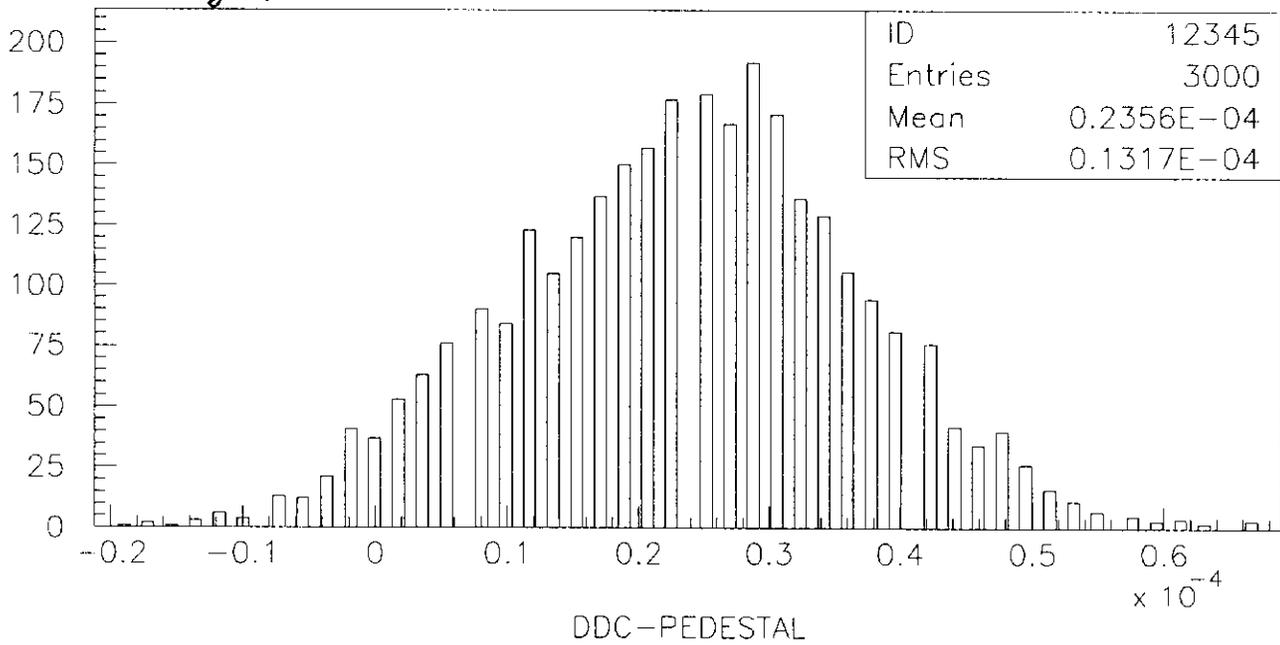


Fig. 4



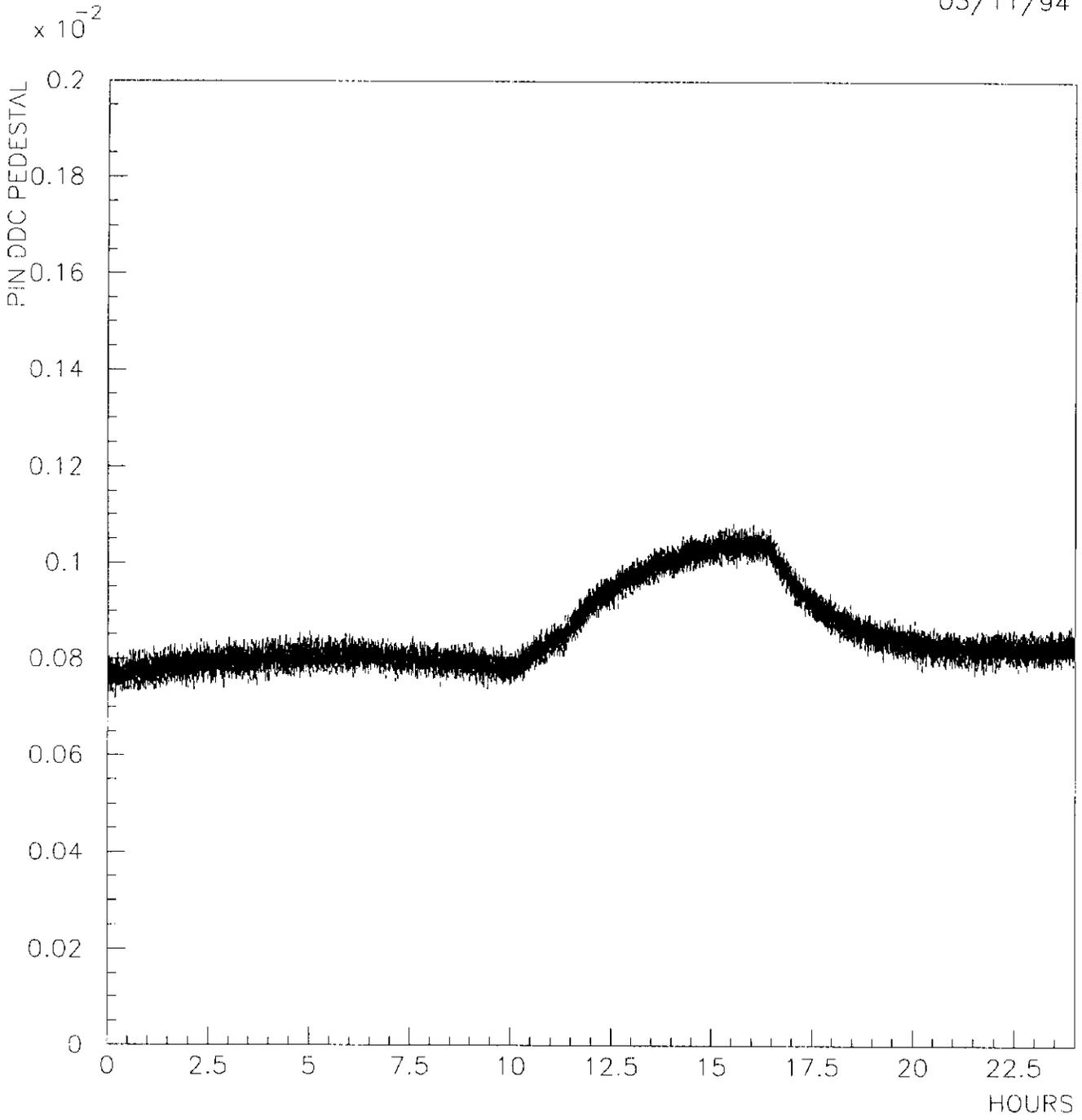


Figure 5

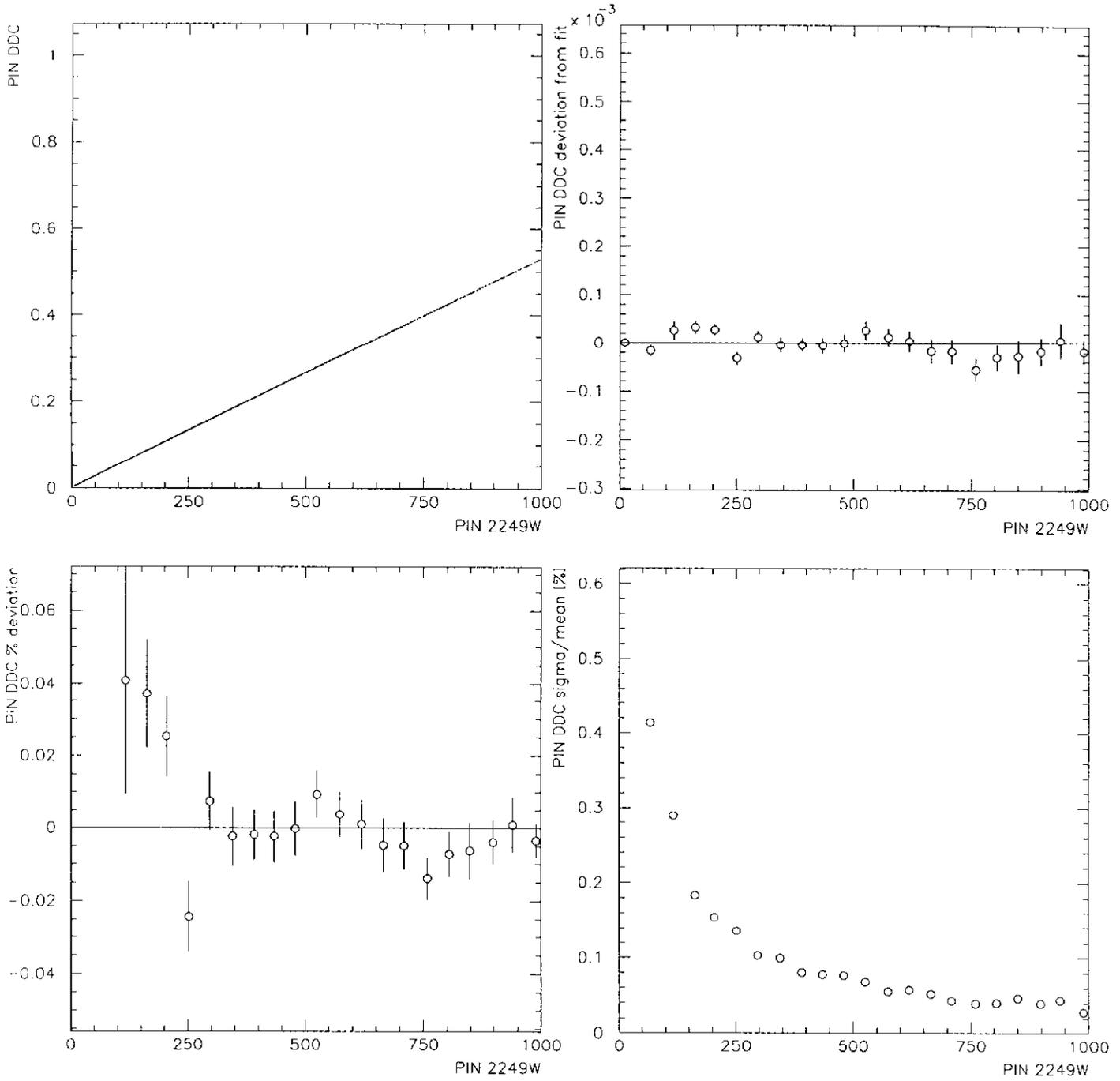


Figure 6

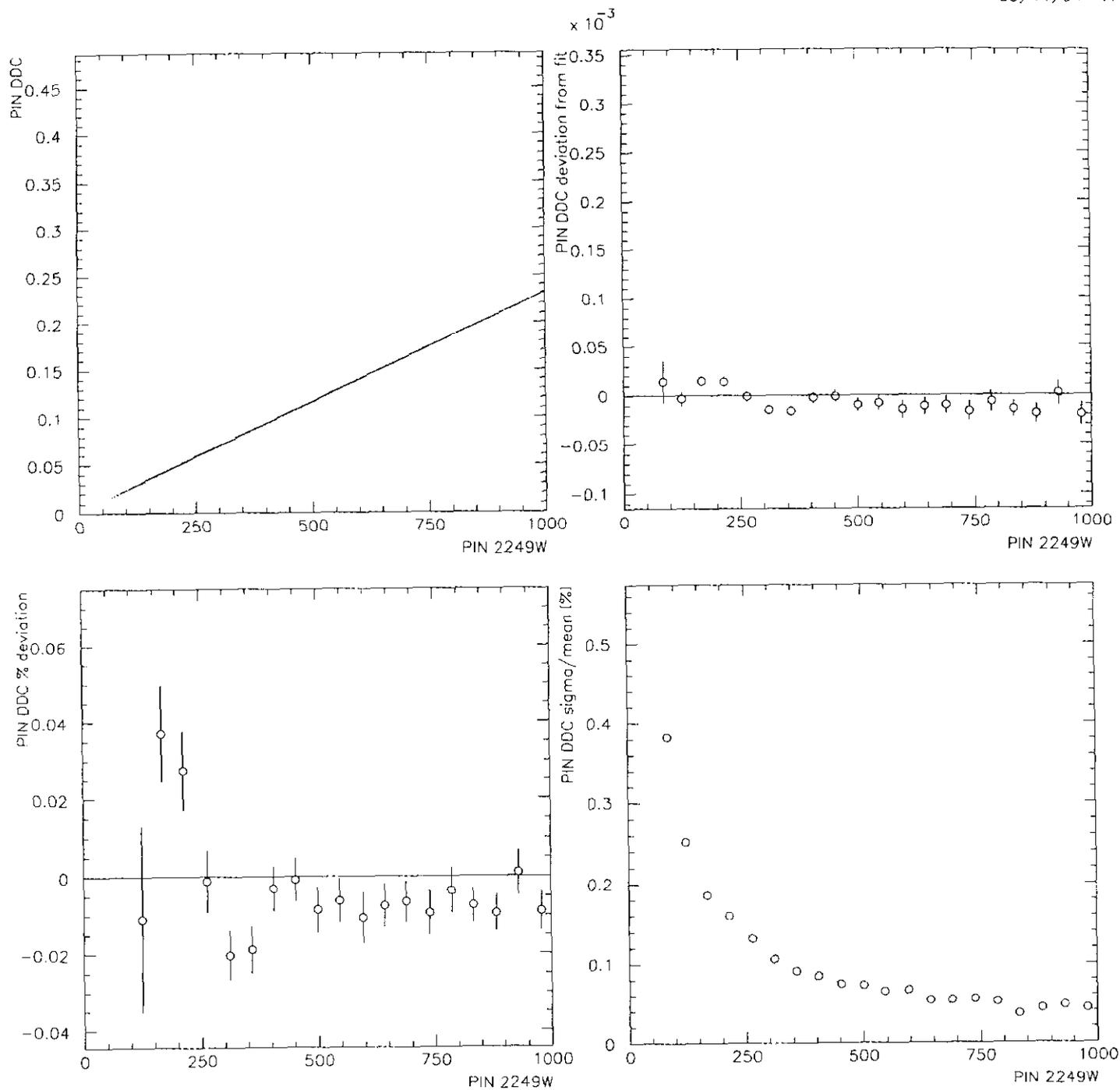


Figure 7

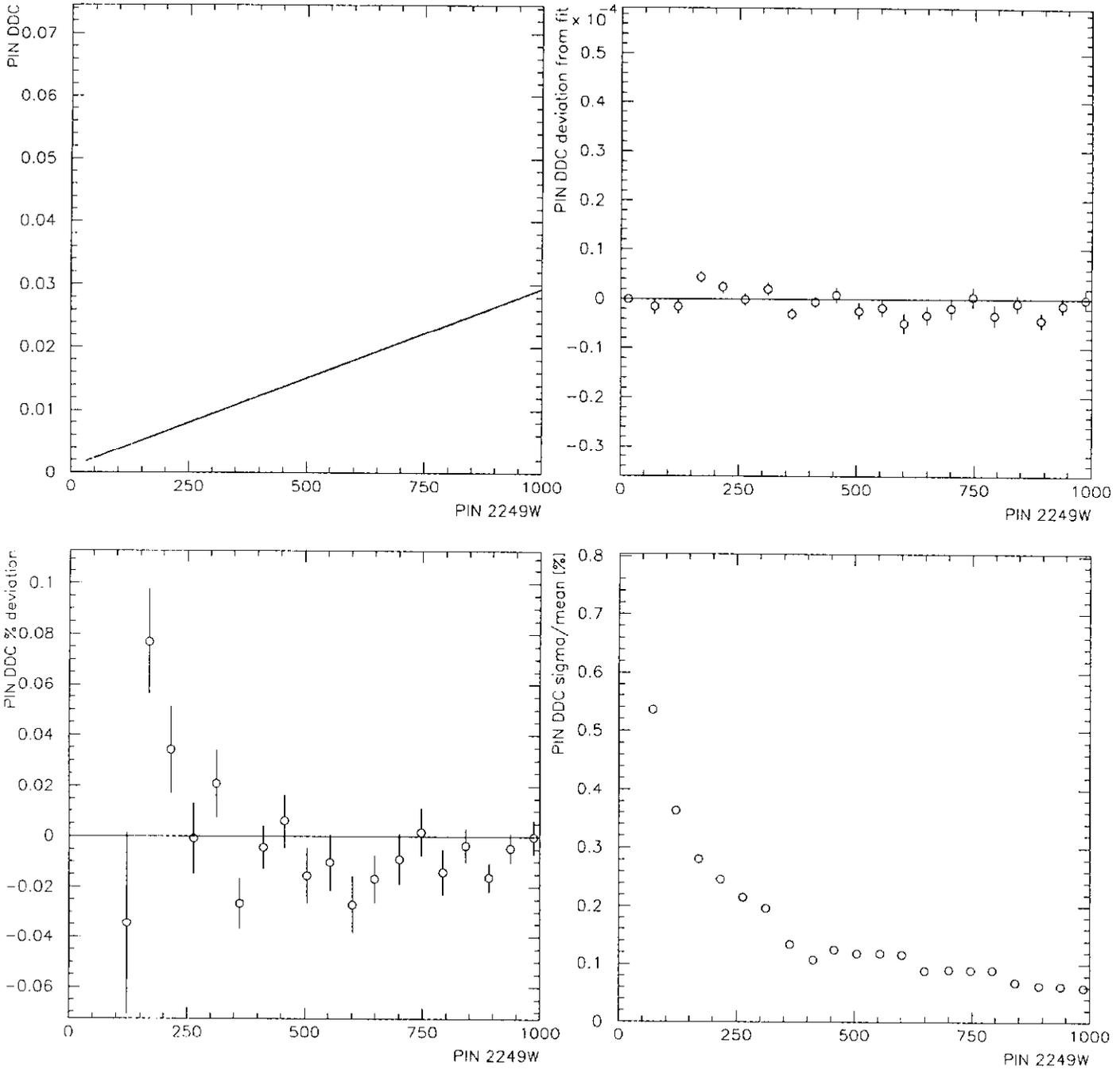


Figure 8

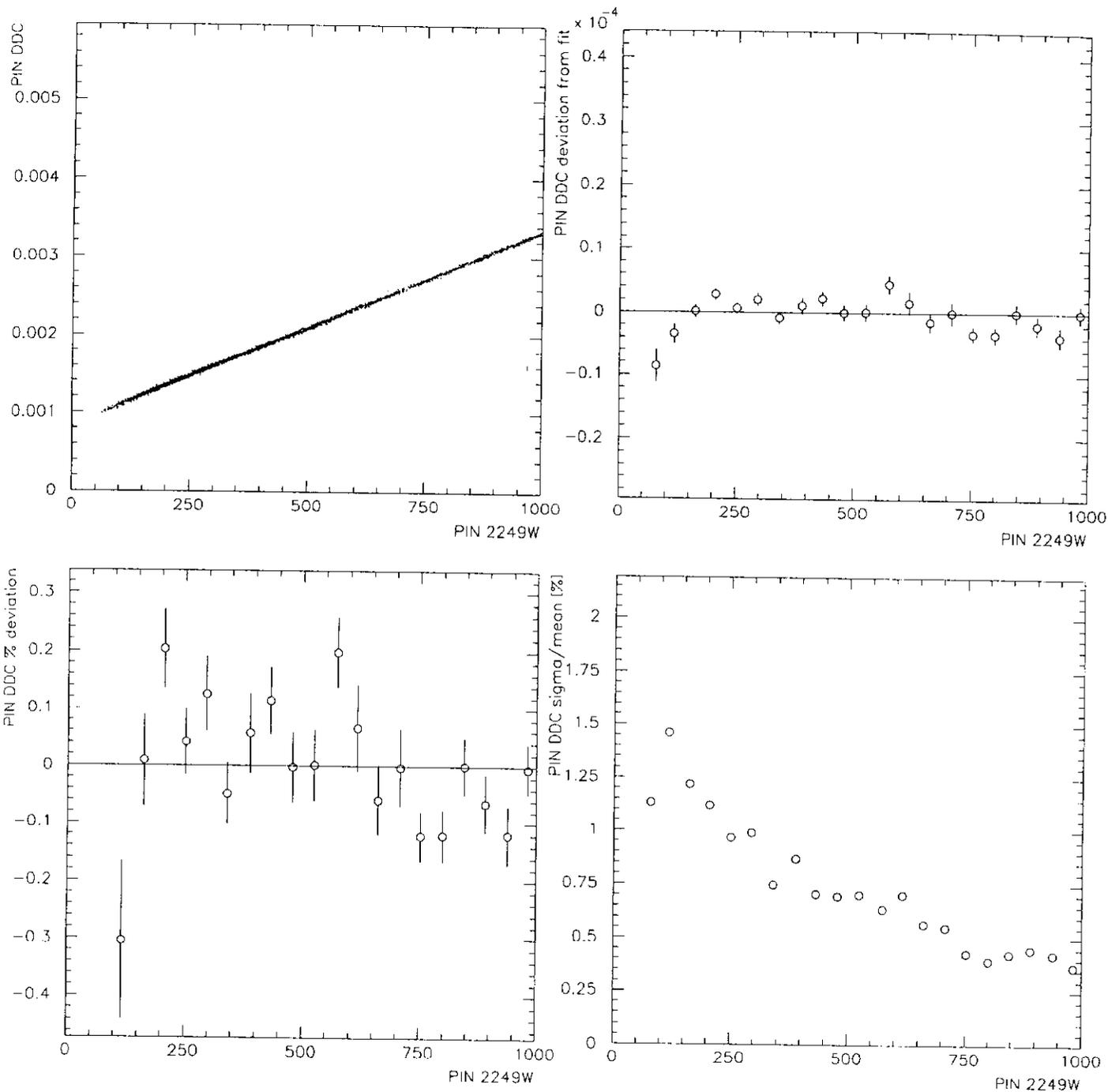


Figure 9