Bt501

Bt502

ECL / TTL Octal Transceiver and Translator

Distinguishing Features

- 10KH or 100K ECL Compatible
- Optional Single +5 V Operation
- Separate TTL and ECL Supply Pins
- Three-Statable TTL Pins
- TTL-Compatible Control Inputs
- 24-pin 0.3" DIP Package
- Typical Power Dissipation: 800 mW

Benefits

- Flexible Power Supply
- Reduced Component Count
- Simplifies PCB Layout
- Reduces PCB Interconnect
- Low Bus Loading

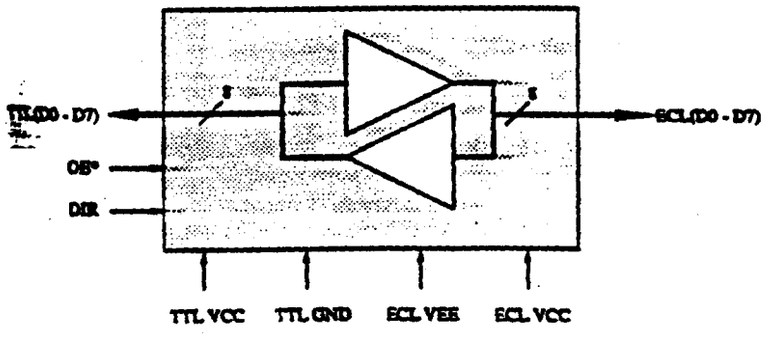
Product Description

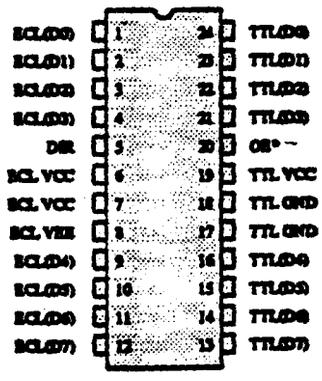
The Bt501 and Bt502 are octal ECL/TT bidirectional transceivers and translators. Tl Bt501 is 10KH ECL compatible, and the Bt502 100K ECL compatible.

The direction and output enable control inpu TTL compatible to simplify interfacing to standard MPU.

Both devices provide a bidirectional interface between TTL signals and ECL signals. The ECL input/output signals may be generated from normal ECL, single +5 V, or split ECL supplies.

Functional Block Diagram





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Circuit Description

	Nominal Voltages Applied		
Supply Pin	Single Supply System	Dual Supply System	Split ECL Supply System
TTL VCC	+5.0 V	+5.0 V	+5.0 V
TTL GND	0 V	0 V	0 V
ECL VCC	+5.0 V	0 V	+2.0 V
ECL VEE	0 V	-5.2 V	-3.2 V

Bt501 Supply Operation.

	Nominal Voltages Applied		
Supply Pin	Single Supply System	Dual Supply System	Split ECL Supply System
TTL VCC	+5.0 V	+5.0 V	+5.0 V
TTL GND	0 V	0 V	0 V
ECL VCC	+5.0 V	0 V	+2.0 V
ECL VEE	0 V	-4.5 V	-2.5 V

Bt502 Supply Operation.

Note: The TTL (D0–D7), DIR, and OE* pins are TTL compatible regardless of the ECL power supply parameters. Changing the ECL power supply parameters affects the threshold levels of only the ECL (D0–D7) pins.

DIR	OE*	Function
0	0	TTL (D0–D7) --> ECL (D0–D7)
1	0	ECL (D0–D7) --> TTL (D0–D7)
x	1	TTL (D0–D7) three-stated, ECL (D0–D7) = 0

Control Truth Table.

Bt501—Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	Volts
ECL Device Ground	ECL VCC	0	0	0	Volts
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	Volts
ECL Power Supply	ECL VEE	–4.9	–5.2	–5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Bt501—Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	Volts
TTL VCC (measured to TTL GND)				+7.0	Volts
Voltage on Any ECL Pin		ECL VCC		ECL VEE	Volts
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	Volts
ECL(D0–D7) Output Current				–50	mA
TTL(D0–D7) Short Circuit Output Current	IOS	–50		–150	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Bt501—ECL DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Input High Voltage*	VIH	0 +25 +70	-1170 -1130 -1070		-840 -810 -735	mV mV mV
Input Low Voltage*	VIL	0 +25 +70	-1950 -1950 -1950		-1480 -1480 -1450	mV mV mV
Output High Voltage*	VOH	0 +25 +70	-1020 -980 -920		-840 -810 -735	mV mV mV
Output Low Voltage*	VOL	0 +25 +70	-1950 -1950 -1950		-1630 -1630 -1600	mV mV mV
Input High Current (Vin = VIHmax)	IIH	0 +25 +70			10 10 10	µA µA µA
ECL VEE Supply Current	IEE	0 +25 +70			75 75 75	mA mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to -2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to ECL VCC.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Bt501—TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage*	VIL	TTL GND −0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			−0.7	mA
Output High Voltage* (IOH = −2.0 mA)	VOH	2.5			Volts
Output Low Voltage* (IOL = 20 mA)	VOL			0.5	Volts
Three-State Output Current	IOZ				
Vout = VOHmin				10	µA
Vout = VOLmax				−10	µA
TTL VCC Supply Current	ICC			85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D loading of 50 Ω to −2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to TTL GND.

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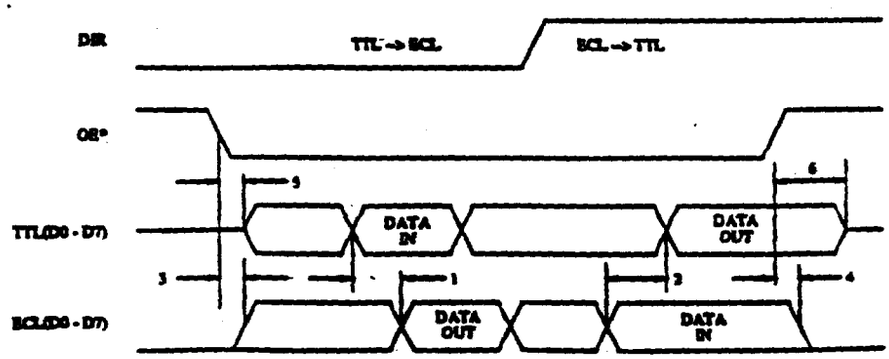
Bt501—AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL -> ECL Propagation Delay	1	2		7	ns
ECL -> TTL Propagation Delay	2	5		11	ns
ECL (D0–D7) Enable Time	3	7		13	ns
ECL (D0–D7) Disable Time*	4	7		13	ns
TTL (D0–D7) Enable Time	5	4		10	ns
TTL (D0–D7) Disable Time*	6	6		12	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to –2.0 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are –0.80 to –2.0 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on *nominal temperature*, i.e., *room*, and *nominal voltage*, i.e., 5 V.

*Subject to capacitive loading.



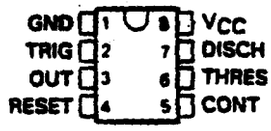
Input/Output Timing.

D1889, SEPTEMBER 1973—REVISED OCTOBER 1

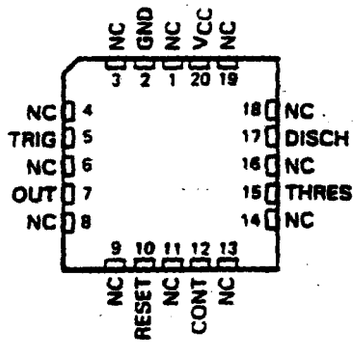
- Timing from Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up to 200 mA
- Functionally Interchangeable with the Signetics SE555, SE555C, SA555, NE555; Have Same Pinout

SE555C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

SE555, SE555C . . . JG PACKAGE
SA555, NE555 . . . D, JG, OR P PACKAGE
(TOP VIEW)



SE555, SE555C . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

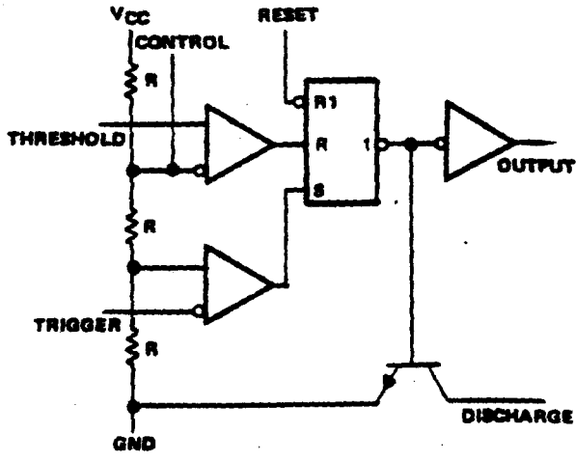
These devices are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The SE555 and SE555C are characterized for operation over the full military range of −55°C to 125°C. The SA555 is characterized for operation from −40°C to 85°C, and the NE555 is characterized for operation from 0°C to 70°C.

functional block diagram



Reset can override Trigger, which can override Threshold.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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AVAILABLE OPTIONS

T_A RANGE	V_{three} MAX V_{CC} = 15 V	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	11.2 V	NE555D		NE555JG	NE555P
−40°C to 85°C	11.2 V	SA555D		SA555JG	SA555P
−55°C to 125°C	10.8 V 11.2 V		SE555FK SE555CFK	SE555JG SE555CJG	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) ..... 18 V
Input voltage (control, reset, threshold, and trigger) ..... V_{CC}
Output current ..... ±225 mA
Continuous total dissipation ..... see Dissipation Rating Table
Operating free-air temperature range: SE555, SE555C ..... −55°C to 125°C
SA555 ..... −40°C to 85°C
NE555 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (SE555, SE555C)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (SA555, NE555)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	SE555		SE555C		SA555		NE555		UNI
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control, reset, threshold, and trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	m
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°

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Special Functions

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electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise n

PARAMETER	TEST CONDITIONS		SE555			SE555C, SA555, NE555			U
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 2)				30	250		30	250	n
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.3	0.7	1	0.3	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1.5	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.2		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B$ = 3.4 MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE555			SE555C, SA555, NE555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100	200		100	300	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each proce run.
§Values specified are for a device in a monostable circuit similar to Figure 9, with component values as follow: R_A = 2 kΩ to C = 0.1 μF.
¶Values specified are for a device in an astable circuit similar to Figure 12, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

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TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

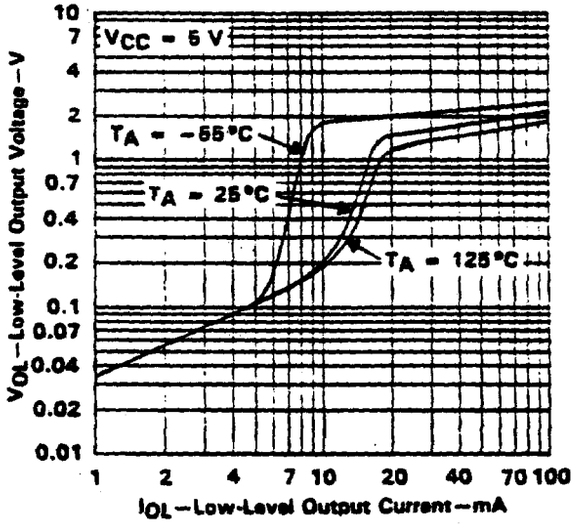

FIGURE 1

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

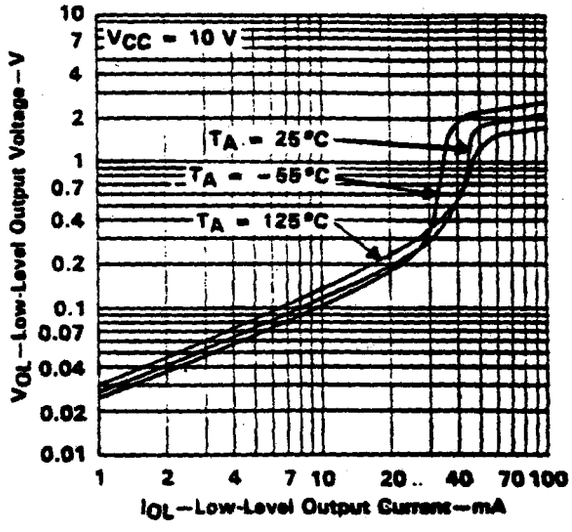

FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

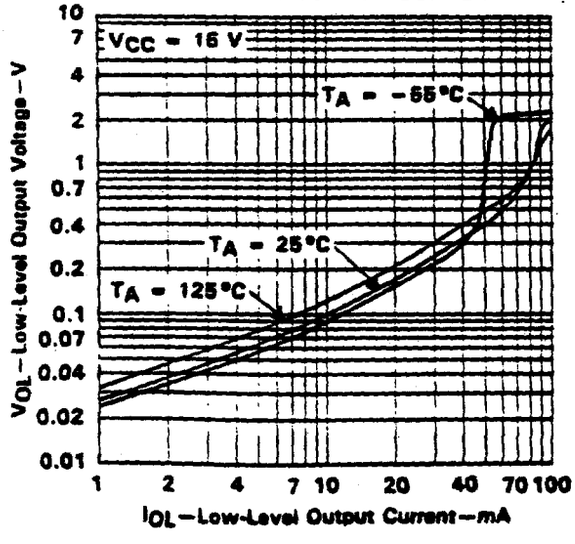

FIGURE 3

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

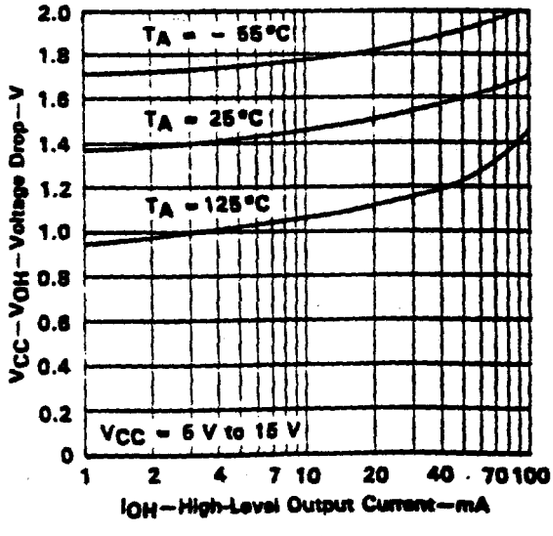

FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

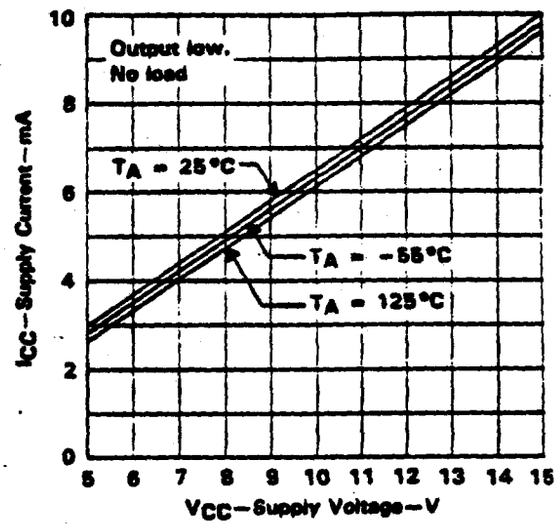


FIGURE 5

NORMALIZED OUTPUT PULSE DURATI
(MONOSTABLE OPERATION)
vs
SUPPLY VOLTAGE

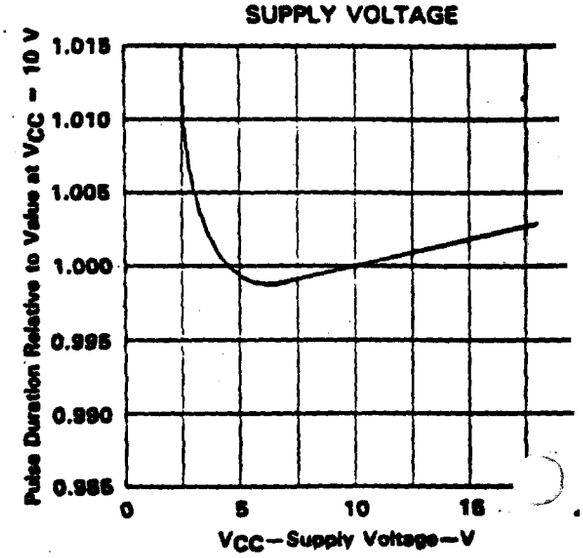


FIGURE 6

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
FREE-AIR TEMPERATURE

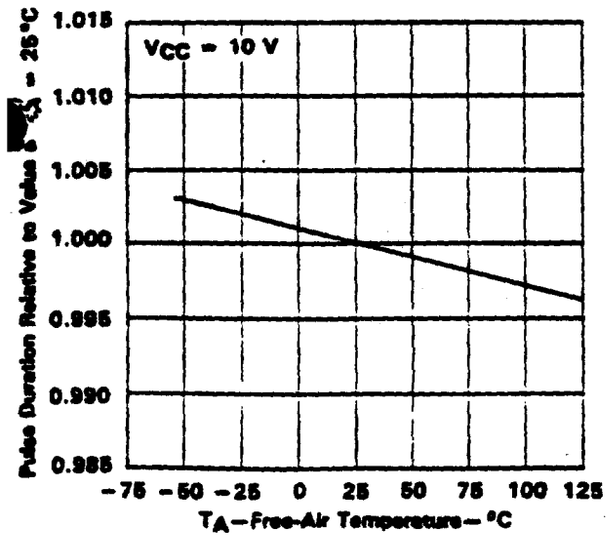


FIGURE 7

PROPAGATION DELAY TIME
vs
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE

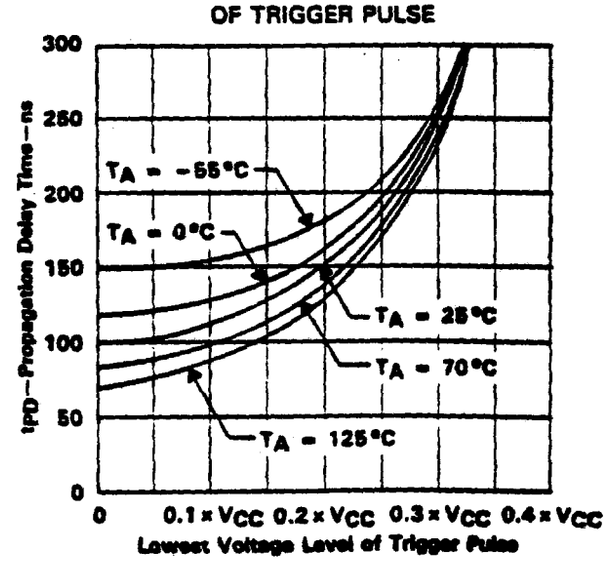


FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

TYPICAL APPLICATION DATA

monostable operation

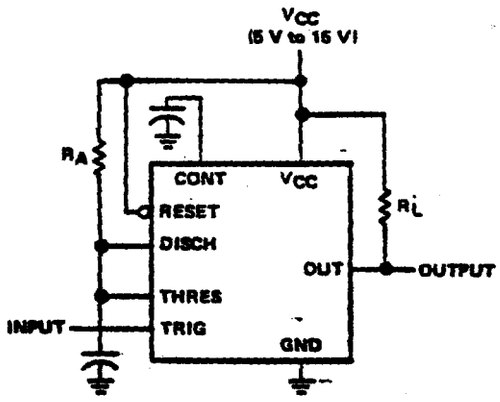


FIGURE 9. CIRCUIT FOR MONOSTABLE OPERATION

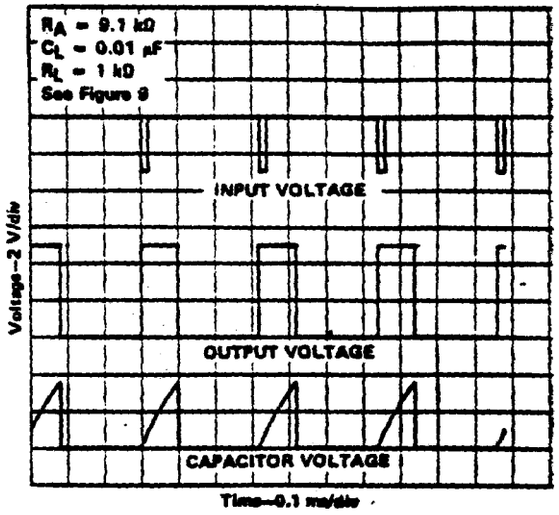


FIGURE 10. TYPICAL MONOSTABLE WAVEFORMS

For monostable operation, any of these timers may be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger input sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold input. If the trigger input has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\overline{Q}$ goes high), drive the output low, and discharge C through Q1.

Monostable operation is initiated when the trigger input voltage falls below the trigger threshold. Once initiated, the sequence ends only if the trigger input is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1\ R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{CC}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to the reset and trigger terminals during the timing interval discharges C and re-initiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when the reset input is not used, it should be connected to V_{CC}.

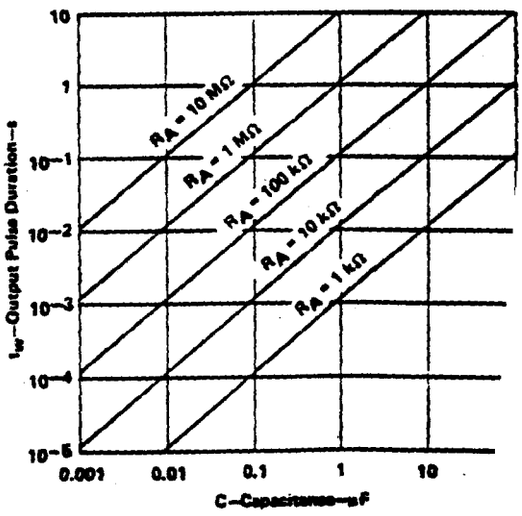
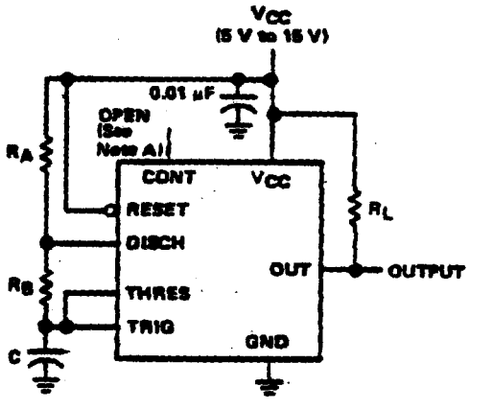


FIGURE 11. OUTPUT PULSE DURATION vs CAPACITANCE

TYPICAL APPLICATION DATA

astable operation



NOTE A: Decoupling the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

FIGURE 12. CIRCUIT FOR ASTABLE OPERATION

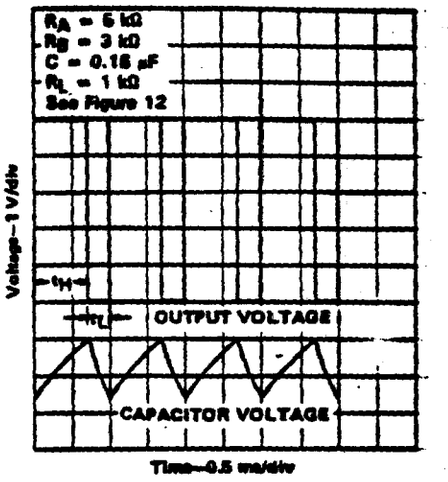


FIGURE 13. TYPICAL ASTABLE WAVEFO

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B and then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \cdot V_{CC}$) and the trigger-voltage level ($\approx 0.33 \cdot V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L may be calculated as follows:

$$t_H = 0.693\,(R_A + R_B)\,C$$

$$t_L = 0.693\,(R_B)\,C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\,(R_A + 2R_B)\,C$$

$$\text{frequency} = \frac{1.44}{(R_A + 2R_B)\,C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

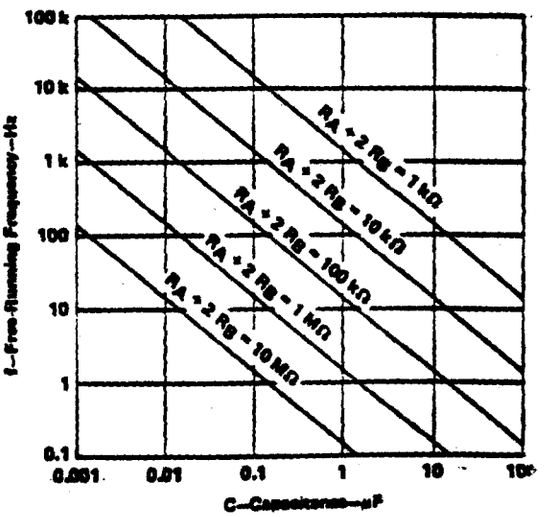


FIGURE 14. FREE-RUNNING FREQUENCY

TYPICAL APPLICATION DATA

missing-pulse detector

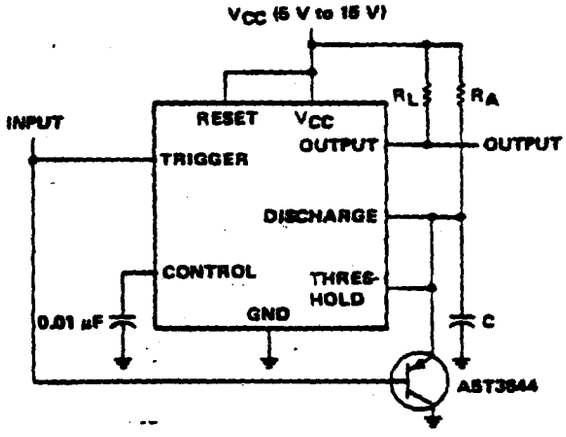


FIGURE 15. CIRCUIT FOR MISSING-PULSE DETECTOR

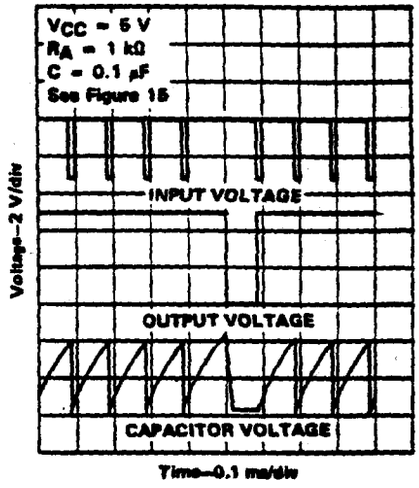


FIGURE 16. MISSING-PULSE DETECTOR WAVEFORMS

The circuit shown in Figure 15 may be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 16.

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 illustrates a divide-by-3 circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

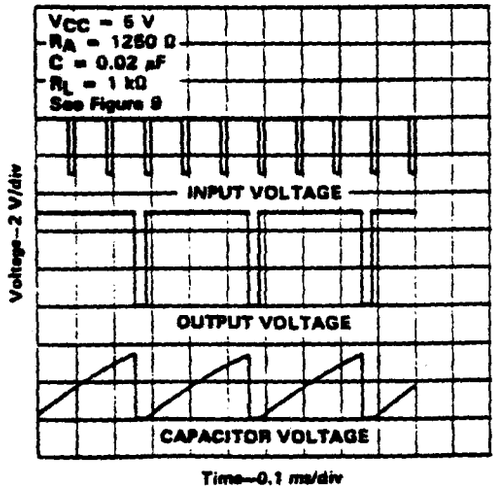
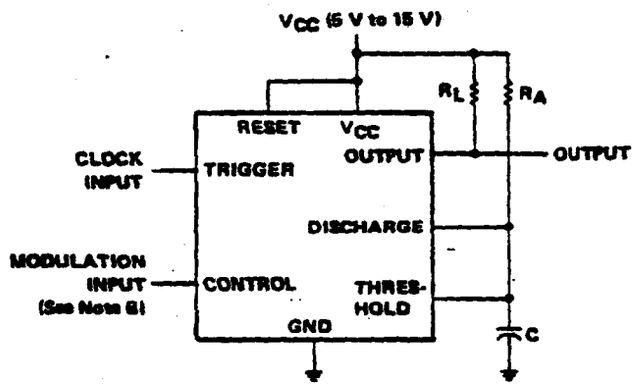


FIGURE 17. DIVIDE-BY-THREE CIRCUIT WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

pulse-width modulation



NOTE B: The modulating signal may be direct or capacitively coupled to the control terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 18. CIRCUIT FOR PULSE-WIDTH MODULATION

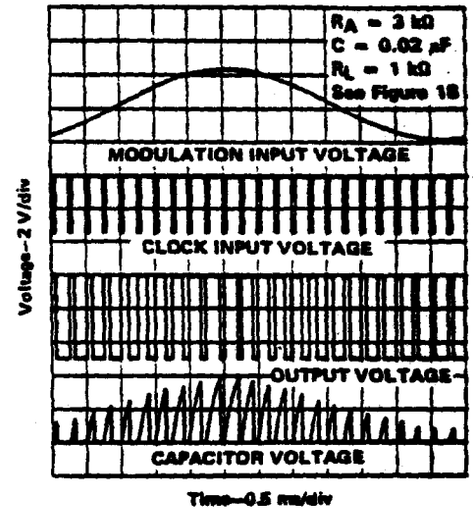
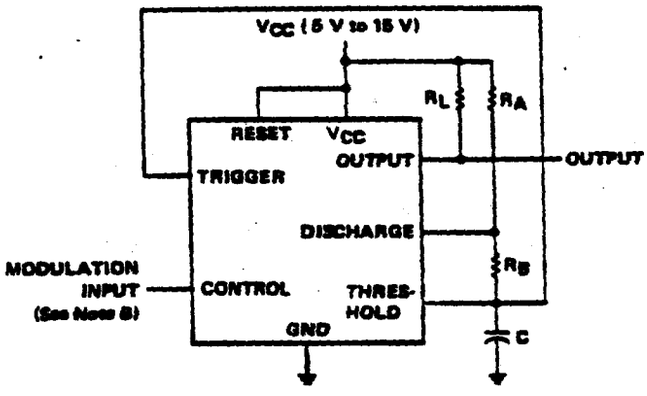


FIGURE 19. PULSE-WIDTH MODULATIO WAVEFORMS

The operation of the timer may be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to the control pin. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 illustrates the resulting output pulse-width modulation. While a sine-wave modulation signal is illustrated, any wave shape could be used.

TYPICAL APPLICATION DATA

pulse-position modulation



NOTE B: The modulating signal may be direct or capacitively coupled to the control terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 20. CIRCUIT FOR PULSE-POSITION MODULATION

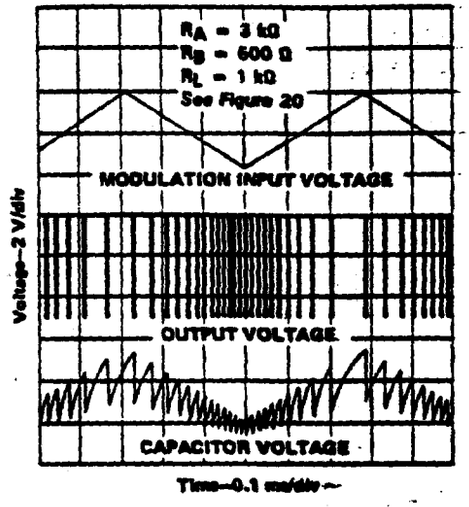


FIGURE 21. PULSE POSITION-MODULATION WAVEFORMS

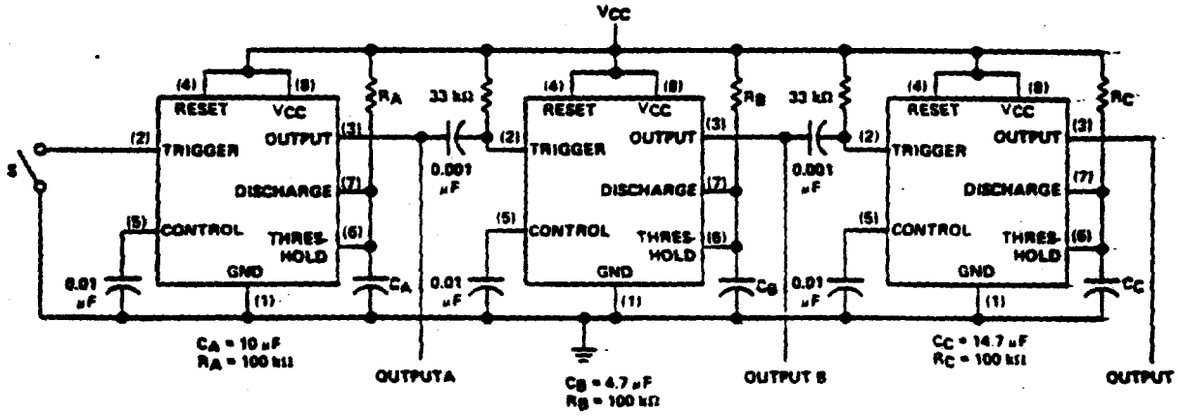
As shown in Figure 20, any of these timers may be used as a pulse-position modulator. This applicatio modulates the threshold voltage, and thereby the time delay, of a free-running oscillator. Figure 21 illustrate a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

4 Special Functions

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

sequential timer



S closes momentarily at t = 0.

FIGURE 22. SEQUENTIAL TIMER CIRCUIT

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 illustrates a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

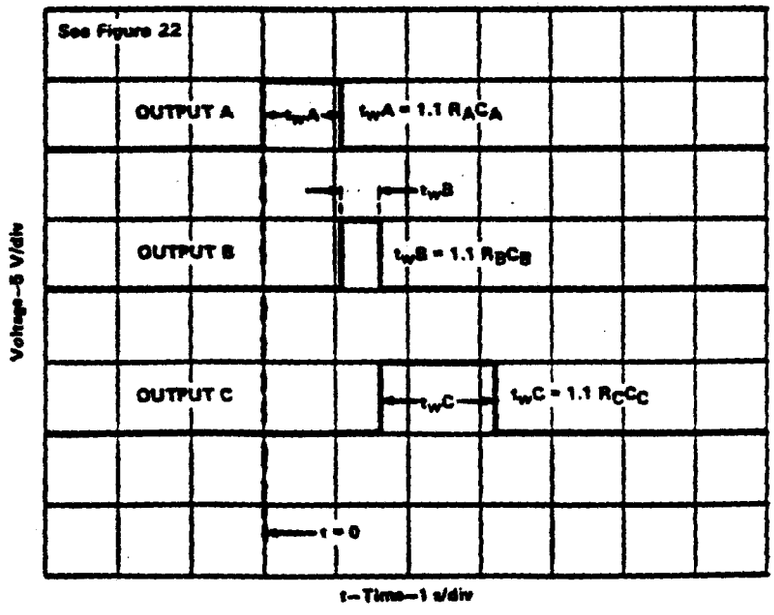


FIGURE 23. SEQUENTIAL TIMER WAVEFORMS

MC10E016
MC100E016

8-BIT SYNCHRONOUS BINARY UP COUNTER

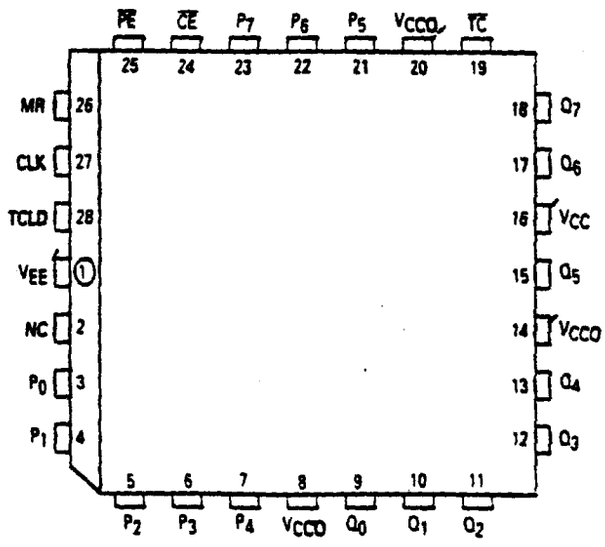
Product Preview

- 700 MHz Min. Count Frequency
- 1000 ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset

The MC10E/100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10KH family, extended to 8-bits, as shown in the logic symbol.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically re-load upon $\overline{TC}$ = LOW, thus functioning as a programmable counter.

PINOUT: 28-LEAD PLCC (TOP VIEW)



FUNCTION TABLE

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	Function
L	L	X	L	Z	Load Parallel (P_n to Q_n)
H	L	X	L	Z	Load Parallel (P_n to Q_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count: Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	Z	Reset (Q_n := LOW, $\overline{TC}$:= HIGH)

Z = clock pulse (low to high);
ZZ = clock pulse (high to low)

PIN NAMES

Pin	Function
P_0–P_7	Parallel Data (Preset) Inputs
Q_0–Q_7	Data Outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC-Load Control Input

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

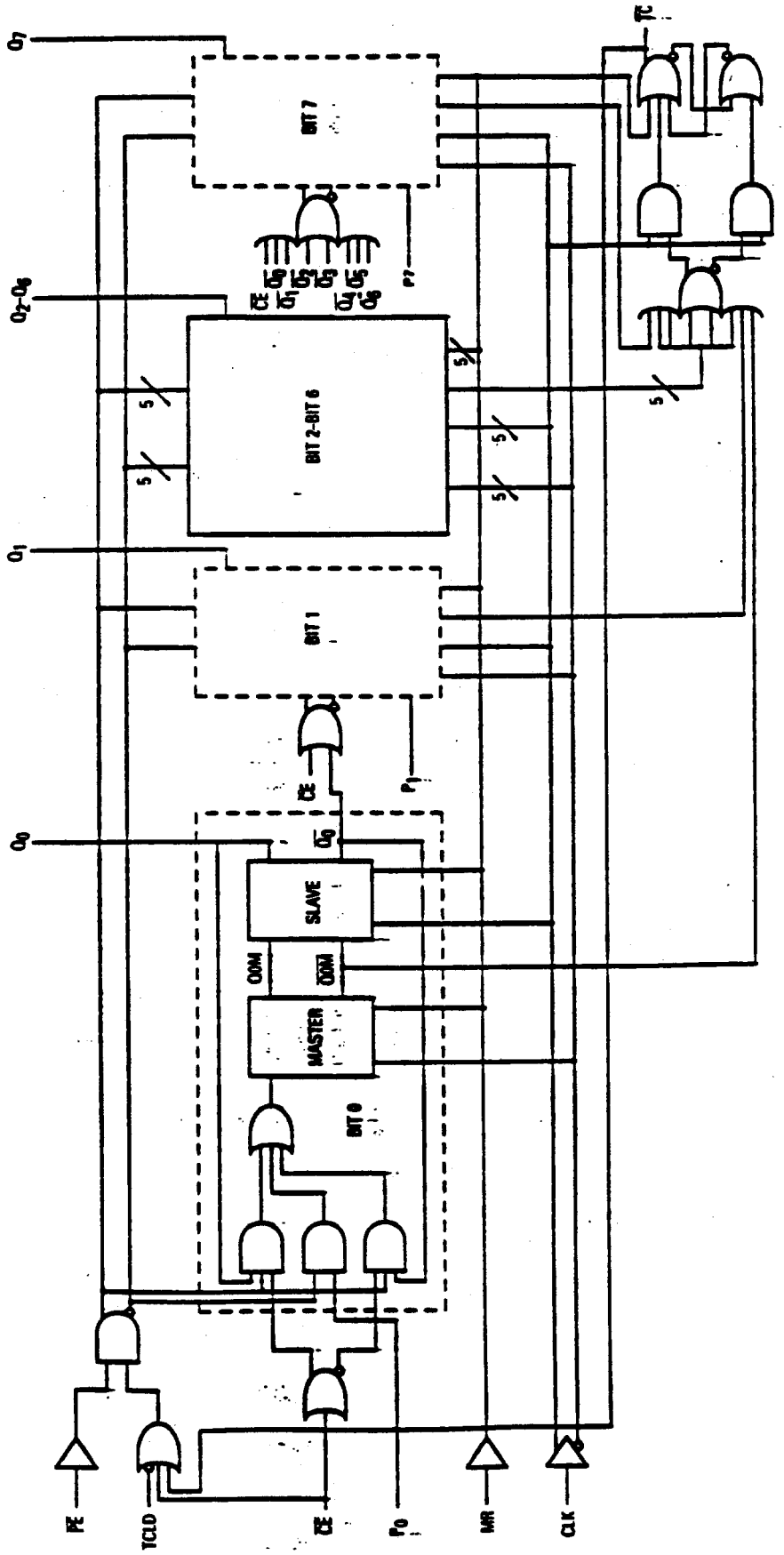
DC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

Symbol	Characteristic	T_A = 0°C			T_A = 25°C			T_A = 85°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		151	181		151	181		151	181		
	100E		151	181		151	181		174	208		

AC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

Symbol	Characteristic	T_A = 0°C			T_A = 25°C			T_A = 85°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{COUNT}	Max. Count Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK to Q	450		1000	450		1000	450		1000		
	MR to Q	450		1000	450		1000	450		1000		
	CLK to $\overline{TC}$	400		900	400		900	400		900		
	MR to $\overline{TC}$	400		900	400		900	400		900		

8-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate del

3wks

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

25 13 10 500 11 20

XC 10E101

MC10E101
MC100E101

Product Preview

- 500 ps Max. Propagation Delay

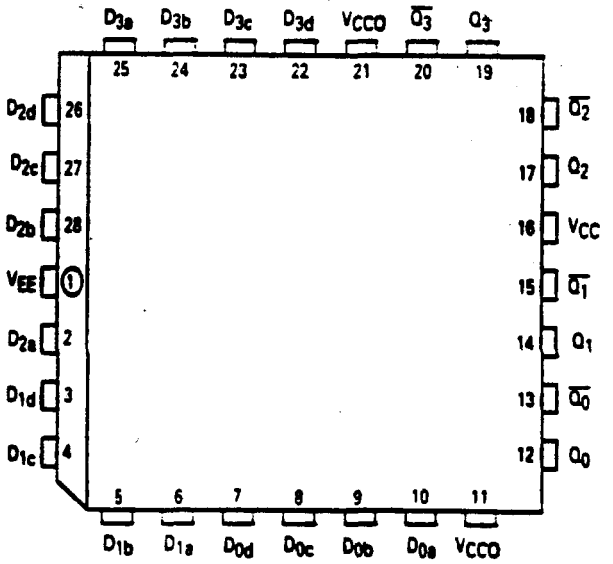
The MC10E/100E101 is a quad 4-input OR/NOR gate.

QUAD 4-INPUT
OR/NOR GATE

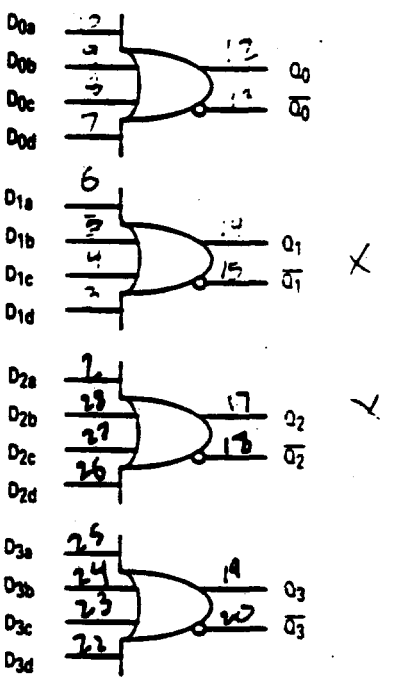
490-9500

PAM KELEZA KULESZA

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
D_{0a}–D_{3d}	Data Inputs
Q_0–Q_3	True Outputs
$\overline{Q_0}$–$\overline{Q_3}$	Inverting Outputs

500 20 20

50K PULL

016 5wks 23 50

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

8

8

DC CHARACTERISTICS: $V_{EE} = V_{EE}$ (min) to V_{EE} (max); $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current D			150			150			150	μA	
I_{EE}	Power Supply Current 10E 100E		30 30	36 36		30 30	36 36		30 35	36 42	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE}$ (min) to V_{EE} (max); $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D	150		500	150		500	150		500	ps	

MOTOROLA

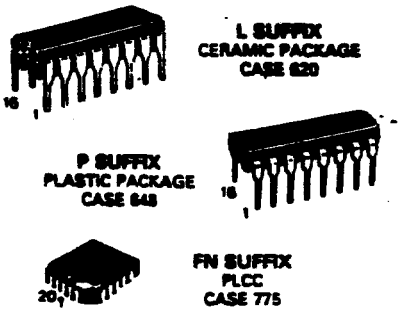
MC10H115

QUAD LINE RECEIVER

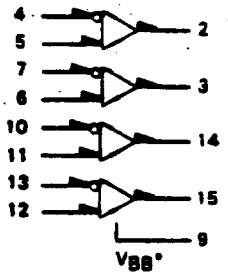
The MC10H115 is a quad differential amplifier designed for use in sensing differential signals over long lines. This 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

The base bias supply (V_{BB}) is made available at Pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (Pin 9) to prevent upsetting the current source bias network.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 110 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



LOGIC DIAGRAM



When input pin with bubble goes positive, the output goes negative.

*V_{BB} to be used to supply bias to the MC10H115 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

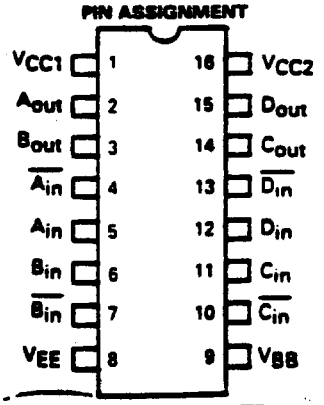
Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current	I_{inH}	—	150	—	95	—	95	μA
	I_{CBO}	—	1.5	—	1.0	—	1.0	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc
Reference Voltage	V_{BB}	−1.38	−1.27	−1.35	−1.25	−1.31	−1.19	Vdc

AC PARAMETERS

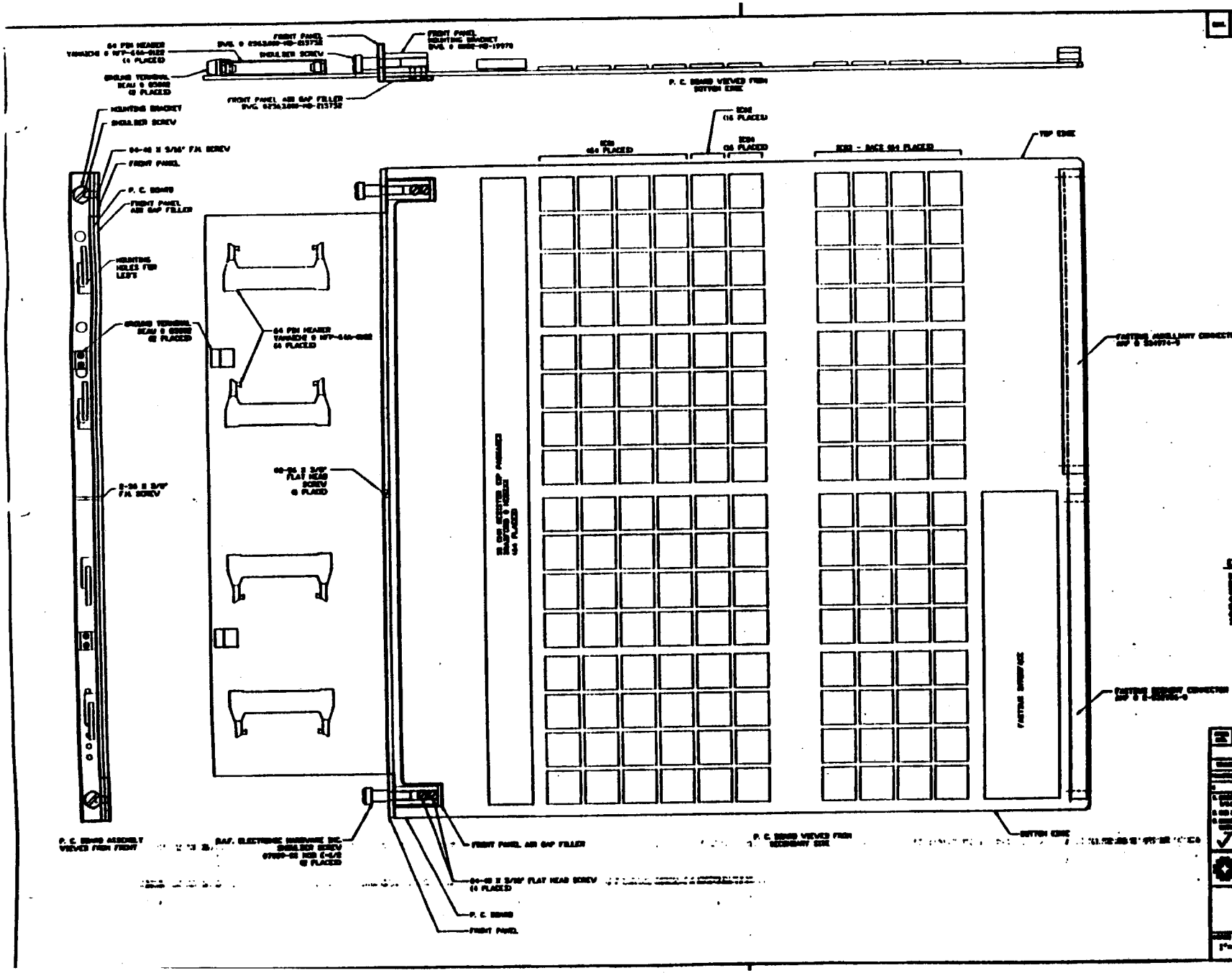
Propagation Delay	t_{pd}	0.4	1.3	0.4	1.3	0.45	1.45	ns
Rise Time	t_r	0.5	1.4	0.5	1.5	0.5	1.6	ns
Fall Time	t_f	0.5	1.4	0.5	1.5	0.5	1.6	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to −2.0 volts.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-31.



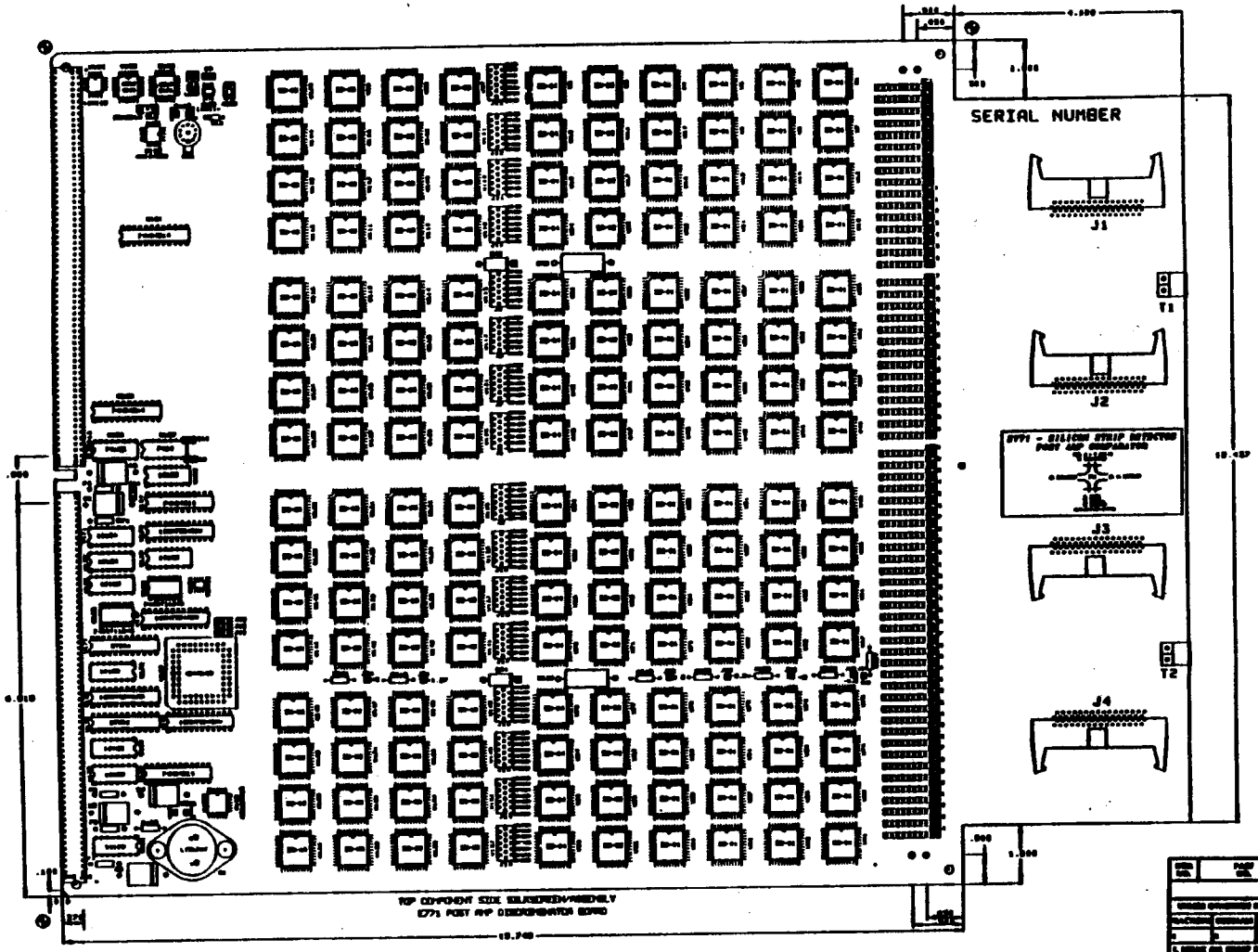
E771 - POST AMP COMPARATOR DRAWING LIST

1) WIRING DETAILS - [illegible]
2) BOTTOM EDGE ASSEMBLY - [illegible]
3) TOP ASSEMBLY - [illegible]
4) DRILL DRAWING - [illegible]
5) LAYUP AND BOARD OUTLINE - [illegible]
6) POWER TEST POINT DETAILS - [illegible]
7) PARTS LIST - [illegible]

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

ECD
E771 - POST AMP COMPARATOR VER III
P. C. BOARD ASSEMBLY

2563400-MD-013003



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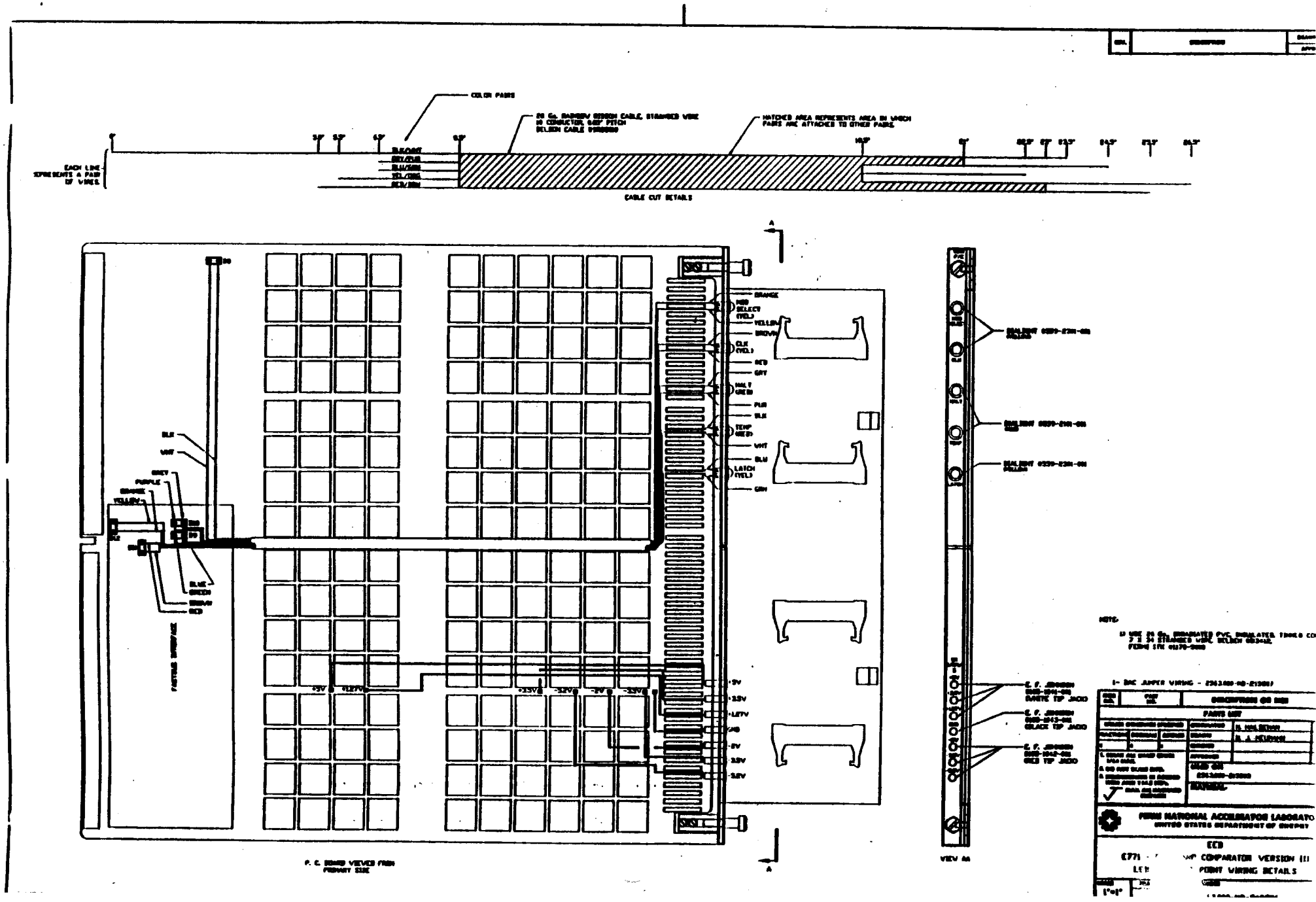
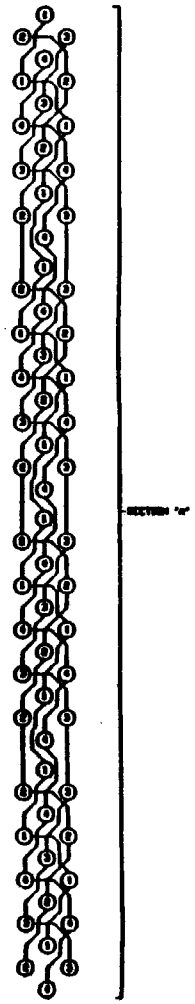
UNITED STATES DEPARTMENT OF ENERGY

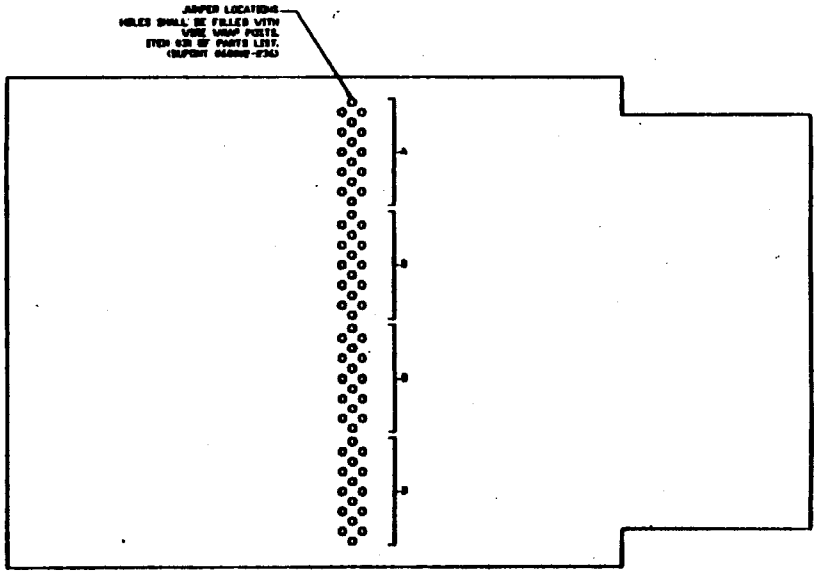

COLOR PAIRS
HATCHED AREA REPRESENTS AREA IN WHICH PAIRS ARE ATTACHED TO OTHER PAIRS.
EACH LINE REPRESENTS A PAIR OF WIRES.
CABLE CUT DETAILS
P. C. BOARD VIEWED FROM PRIMARY SIDE
VIEW AA
NOTE:
PARTS LIST
FERMI NATIONAL ACCELERATOR LABORATO
UNITED STATES DEPARTMENT OF ENERGY
ECD
COMPARATOR VERSION III
POINT WIRING DETAILS



BAC JUMPER DETAILS

BAC DIAGRAM TO THE LEFT IS TO BE USED WHEN A EC-[illegible] 44-PIN PLUG ECF ARE DUPLICATED. THE 4 PLUG'S SHOULD EXCEPT LOCATIONS [illegible], [illegible] AND [illegible]. USE 30 AWG WIRE WRAP WIRE WITH SYNRO INSULATION. REPEAT THE DIAGRAM FOR SECTIONS B, C AND D USE DRAWG OUTLINE AT ABOVE. COLOR CODE WIRES AS FOLLOWS:

PIN 01 WIRING - BLUE WIRE
PIN 02 WIRING - RED WIRE
PIN 03 WIRING - WHITE WIRE
PIN 04 WIRING - YELLOW WIRE



P. C. BOARD OUTLINE

REV.	DESCRIPTION	DRAWN	DATE
		APPR.	

REV.	PART NO.	DESCRIPTION OR NOTE	QT
		PARTS LIST	

DRAWN		E. HALBERG	[illegible]
CHECKED		E. J. HOGAN	[illegible]
ENGINEER			
APPROVED			

USED ON
F36A,B,C,D-NO-SYMBOL

NEXT ASSY

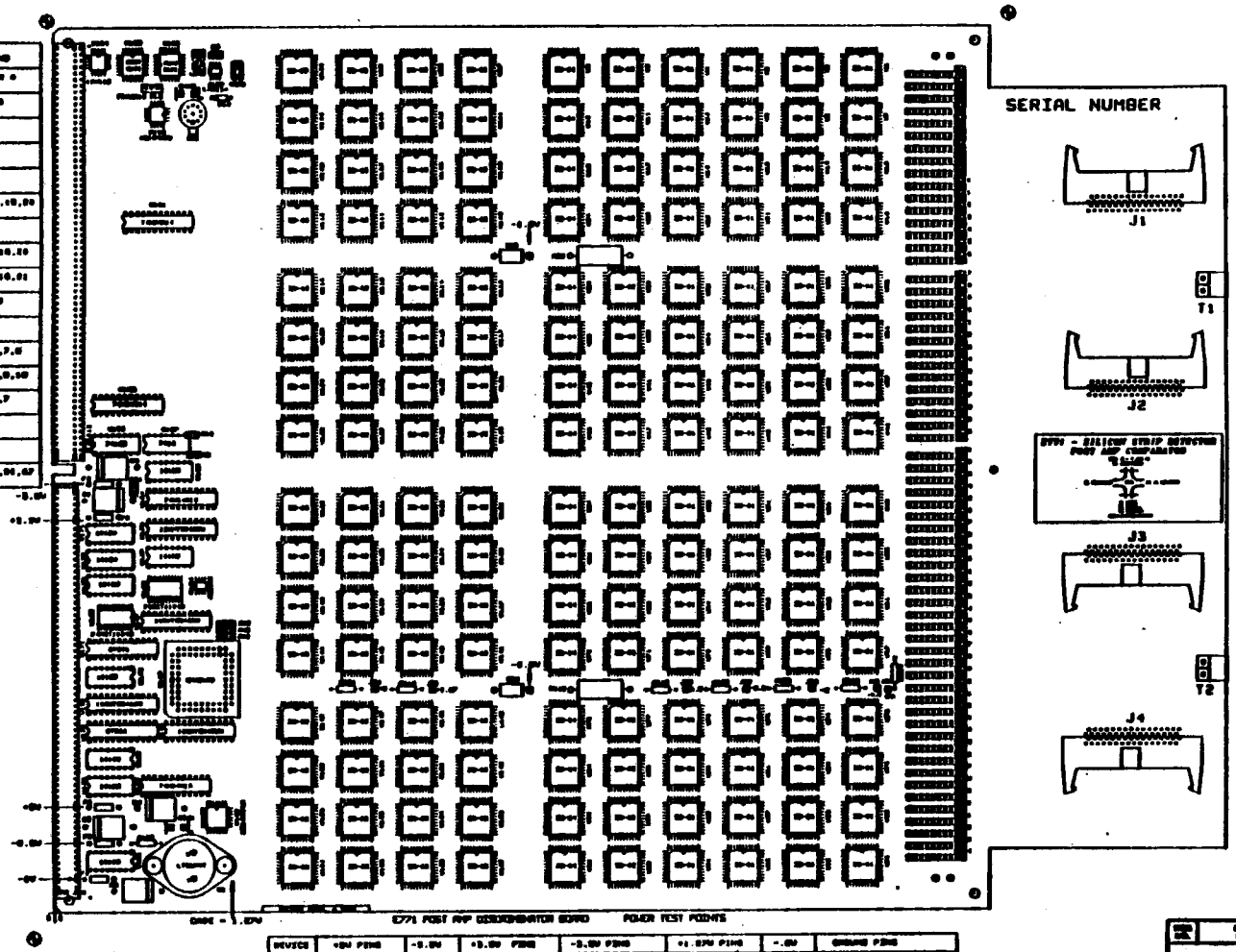
FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

ECD

E771 - POST AMP COMPARATOR VER III
BAC JUMPER DIAGRAM

SIZE	CODE	DRAWING NUMBER	REV
NONE		[illegible]	

DEVICE PART #	ID #	+5V PIN#	-5.2V PIN#	GROUND PIN #
[illegible]	[illegible]		[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]		[illegible]
[illegible]	[illegible]	[illegible]		[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]		[illegible]	[illegible]
[illegible]	[illegible]		[illegible]	[illegible]
[illegible]	[illegible]		[illegible]	[illegible]
[illegible]	[illegible]	[illegible]		[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]		[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]		[illegible]



E771 POST AMP DISCRIMINATOR BOARD POWER TEST POINTS

DEVICE	+5V PINS	-5.2V	+5.2V PINS	-5.2V PINS	+1.5V PINS	-1.5V	GROUND PINS
IC-01			[illegible]	[illegible]			[illegible]
IC-02		[illegible]	[illegible]				[illegible]
IC-03	[illegible]				[illegible]	[illegible]	[illegible]
IC-04		[illegible]	[illegible]				[illegible]

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

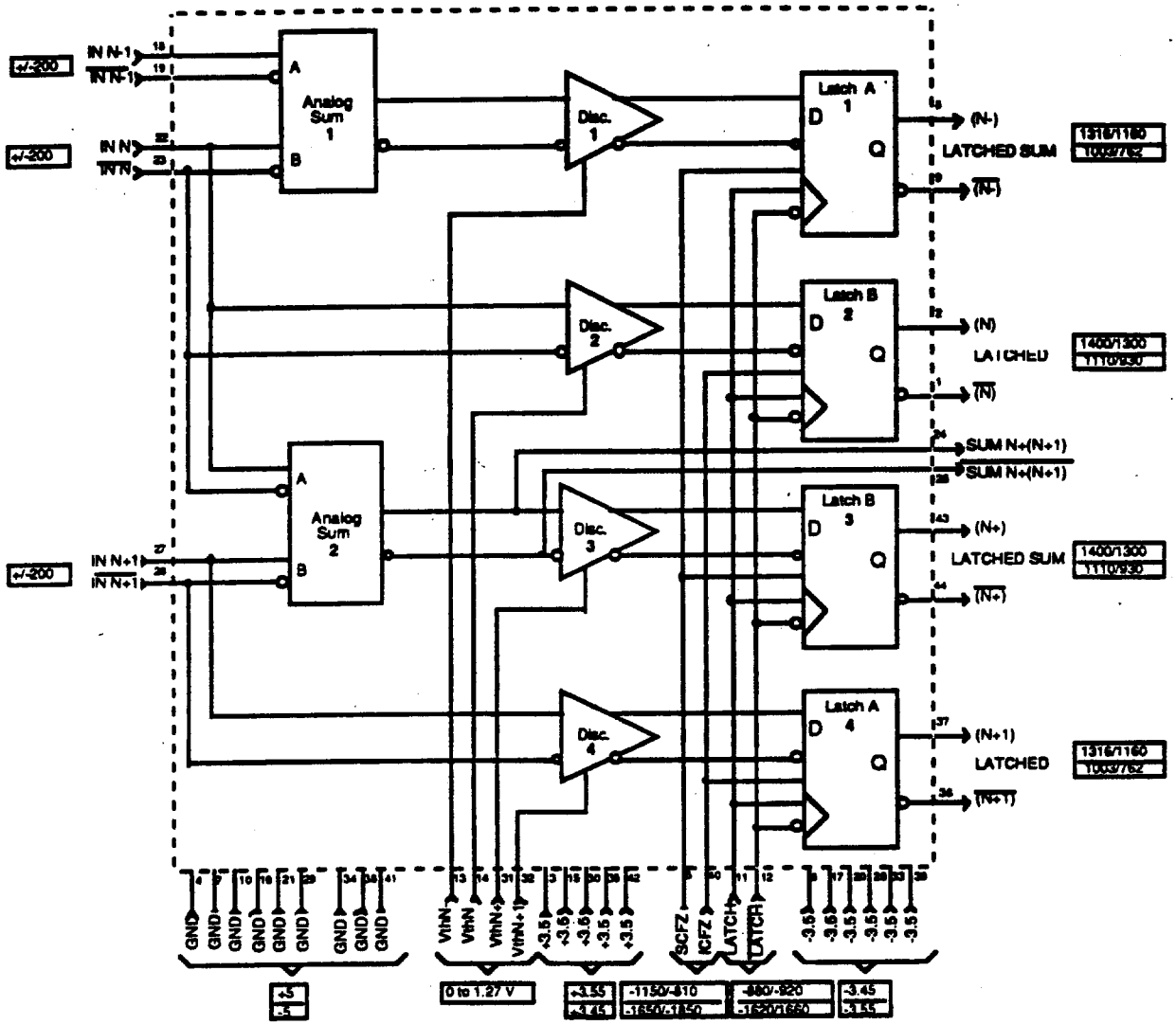
E771- POST AMP DISCRIMINATOR VER III
PARTS LIST
HD-215608

APPENDIX E - DATA SHEETS

This appendix contains data sheets for the ASICs IC-01, IC-02 and IC-04 as well as data sheets for all parts on the P/C moduele.

IC-01: SSD TWO CHANNEL SUM, DISCRIMINATOR AND LATCH

Cavity Down



Part Number IC-01

NOTES:

1. All input and output signals are full differential except power, threshold (Vthi#)
2. The discriminator compares the input amplitude with the threshold setting. If the input exceeds the setting, an output exists for the time over
3. The "LATCH" signal must be at least 1 Nanosecond wide.
4. Power dissipation is typically 406 mW ; 504 mW max.
5. Power supply currents: +3.5 V @typically 48 mA ; 56 mA
   -3.5 V @typically 66 mA ; 88 mA
6. Voltages in boxes are given in millivolts. Max / Min

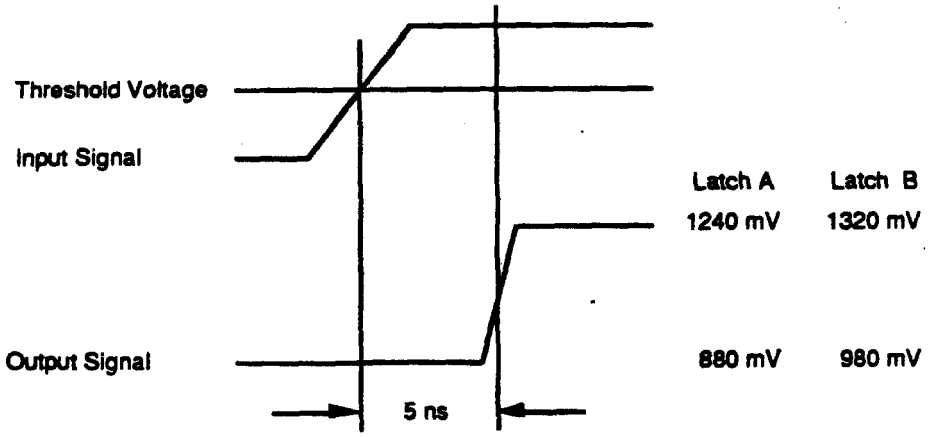
Created 1-24-89
Revised 2-14-91
Merle Haldeman / Scott Heim

IC-01 Typical Characteristics

Package 44 Pin PLCC

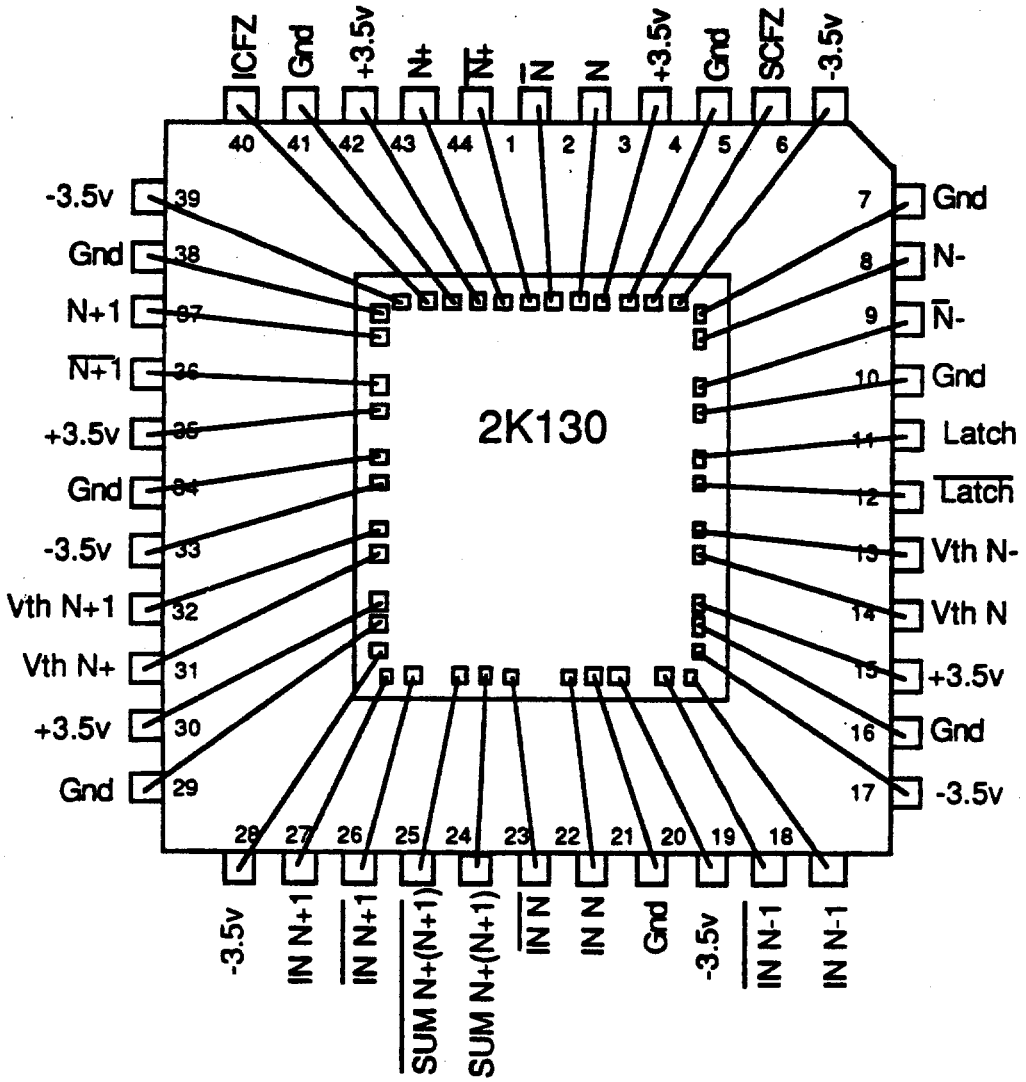
	Tektronix Package Code= 44PLCC4
Power Supply	+3.5 Volts @ 48 mA -3.5 Volts @ 68 mA
Power Dissipation Discriminators	406 mW ≈180 mW
Thermal Resistance	43°C/W$_{JA}$ 6°C/W$_{JC}$
Differential Input Signal Range	90 mV
Common Mode Signal Range	+/- 1 Volt
Input Resistance	4 kΩ
Input Bias Current	3 µA
Differential Output Voltage	710 mV
Output Current	Source 5 mA Sink 1.25 mA
Propagation Delay	5 ns
Adjacent Channel Crosstalk	40 db
Hysteresis	10 mV
Triggering Uncertainty	0.5 mV
Ambient Temperature Range	0 to 70°C

IC-01 TIMING



IC-01: SSD TWO CHANNEL SUM, DISCRIMINATOR and LATCH
Cavity Down
Thermally Enhanced, 44 Lead Plastic Chip Carrier

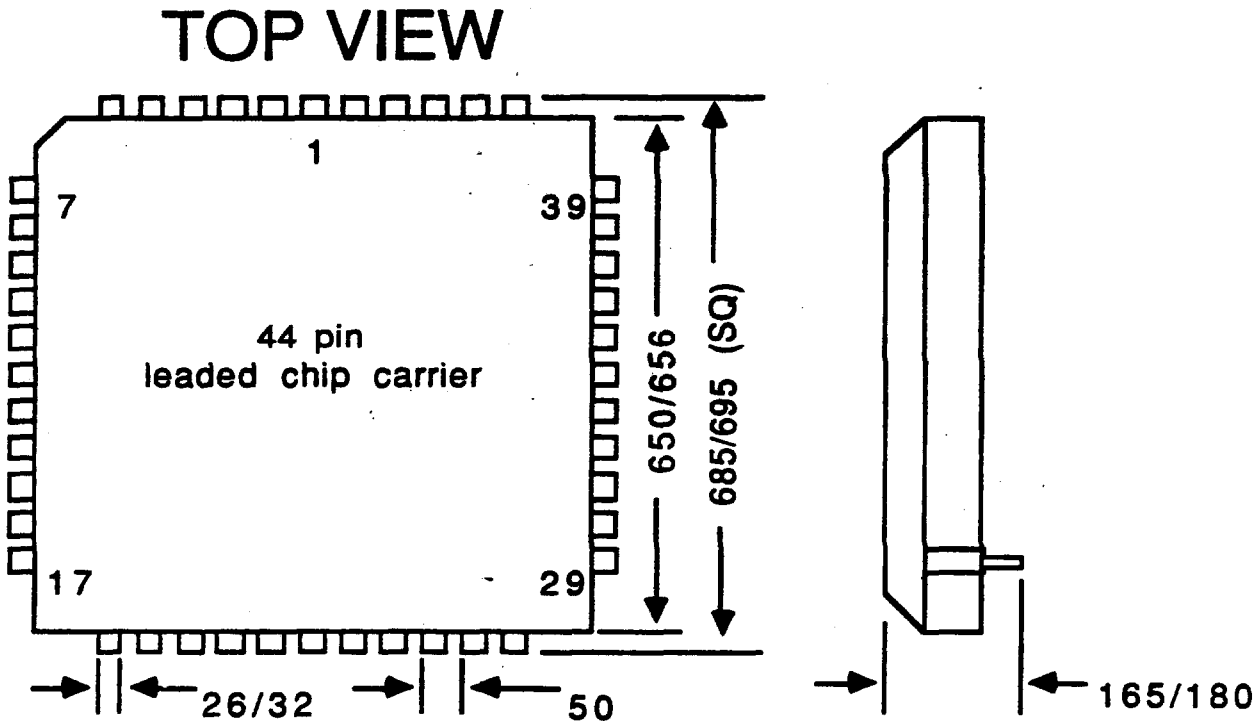
Part Number IC-01



BOTTOM VIEW

Created 8-28-89
Revised
Merle Haldeman / Scott Holm

IC-01: SSD TWO CHANNEL SUM, DISCRIMINATOR and LATCH
Cavity Down



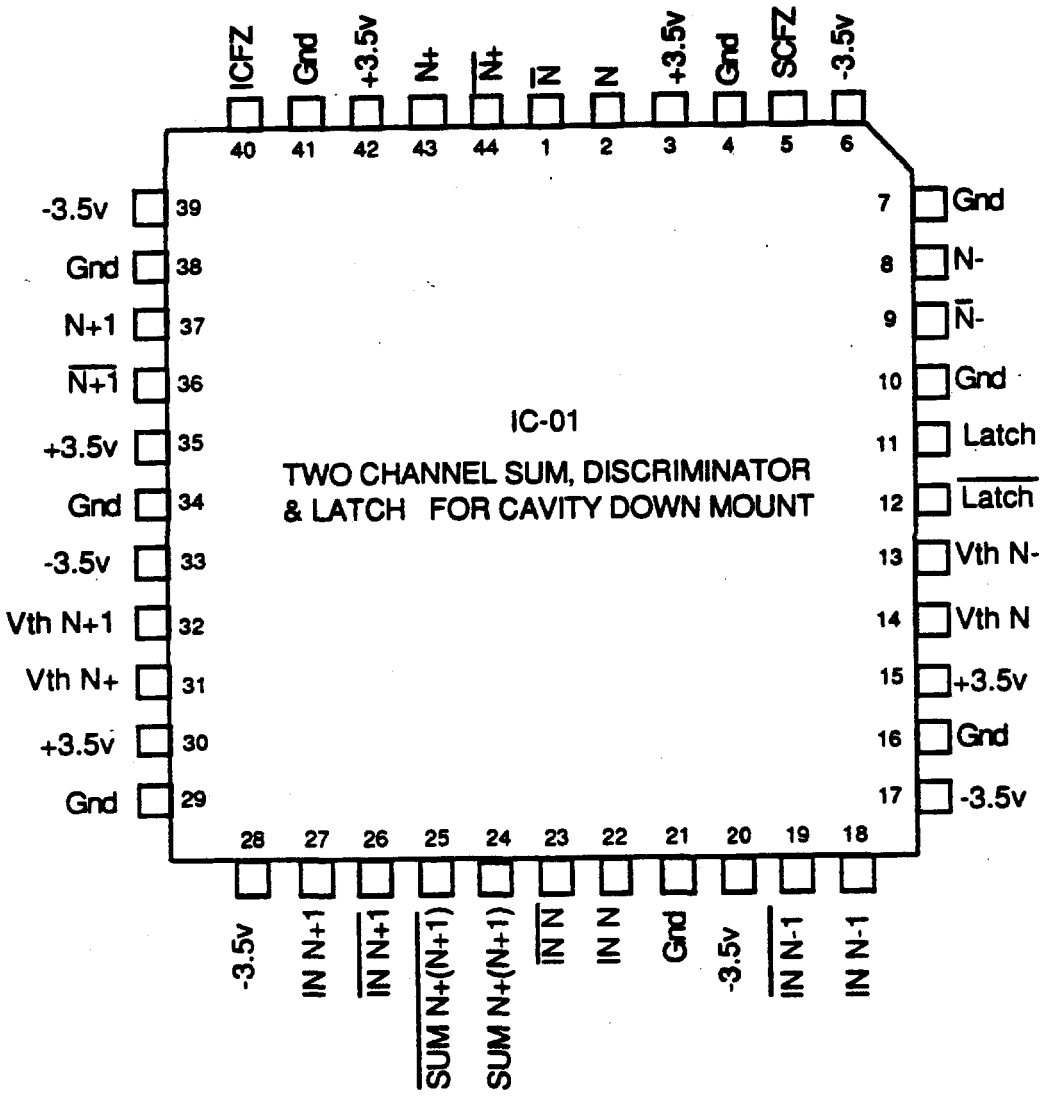
Part Number IC-01

IC-01 Package Dimension Diagram Notes.

1. All dimensions are in mils. (Min/Max)

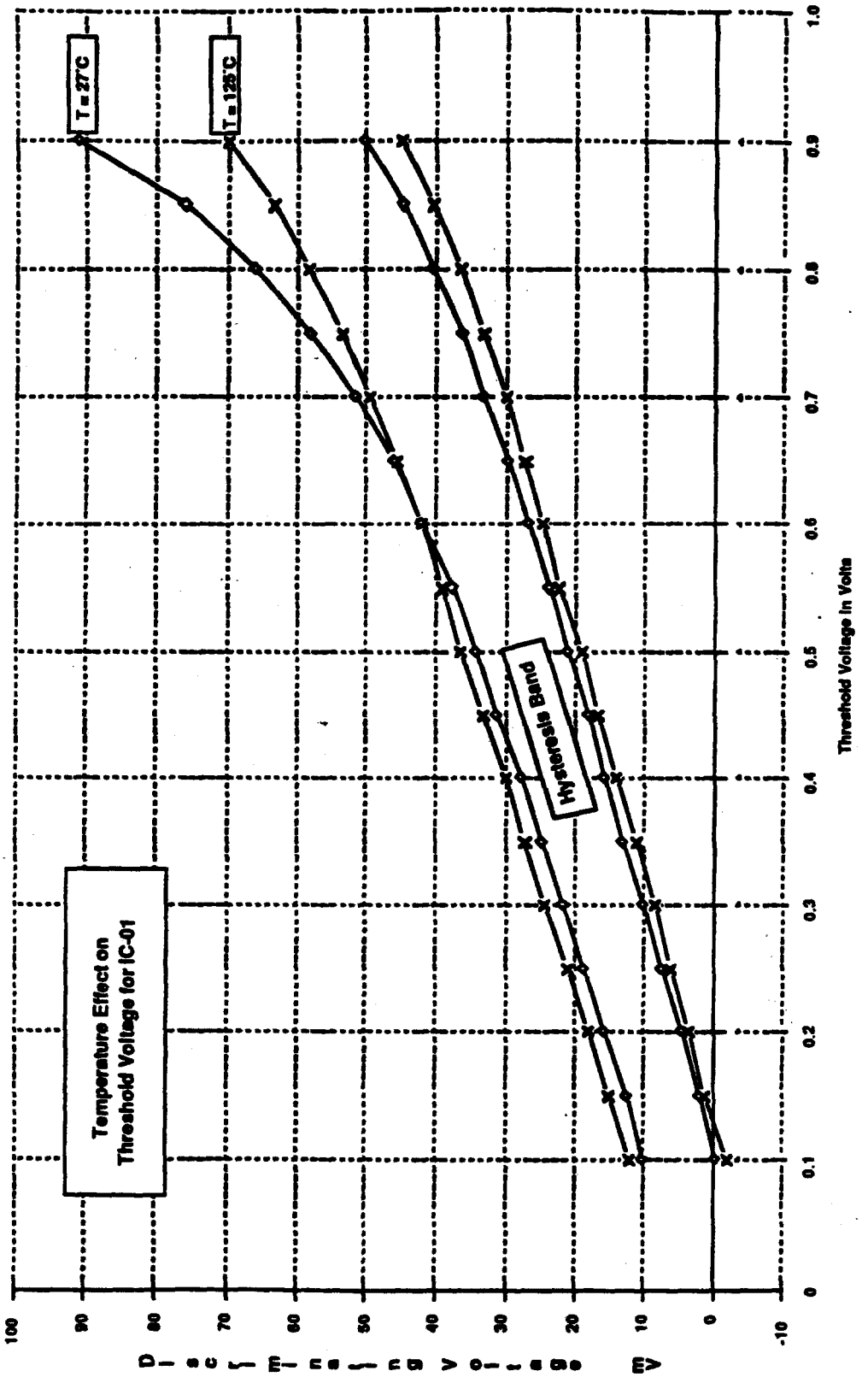
IC-01: SSD TWO CHANNEL SUM, DISCRIMINATOR and LATCH
Cavity Down

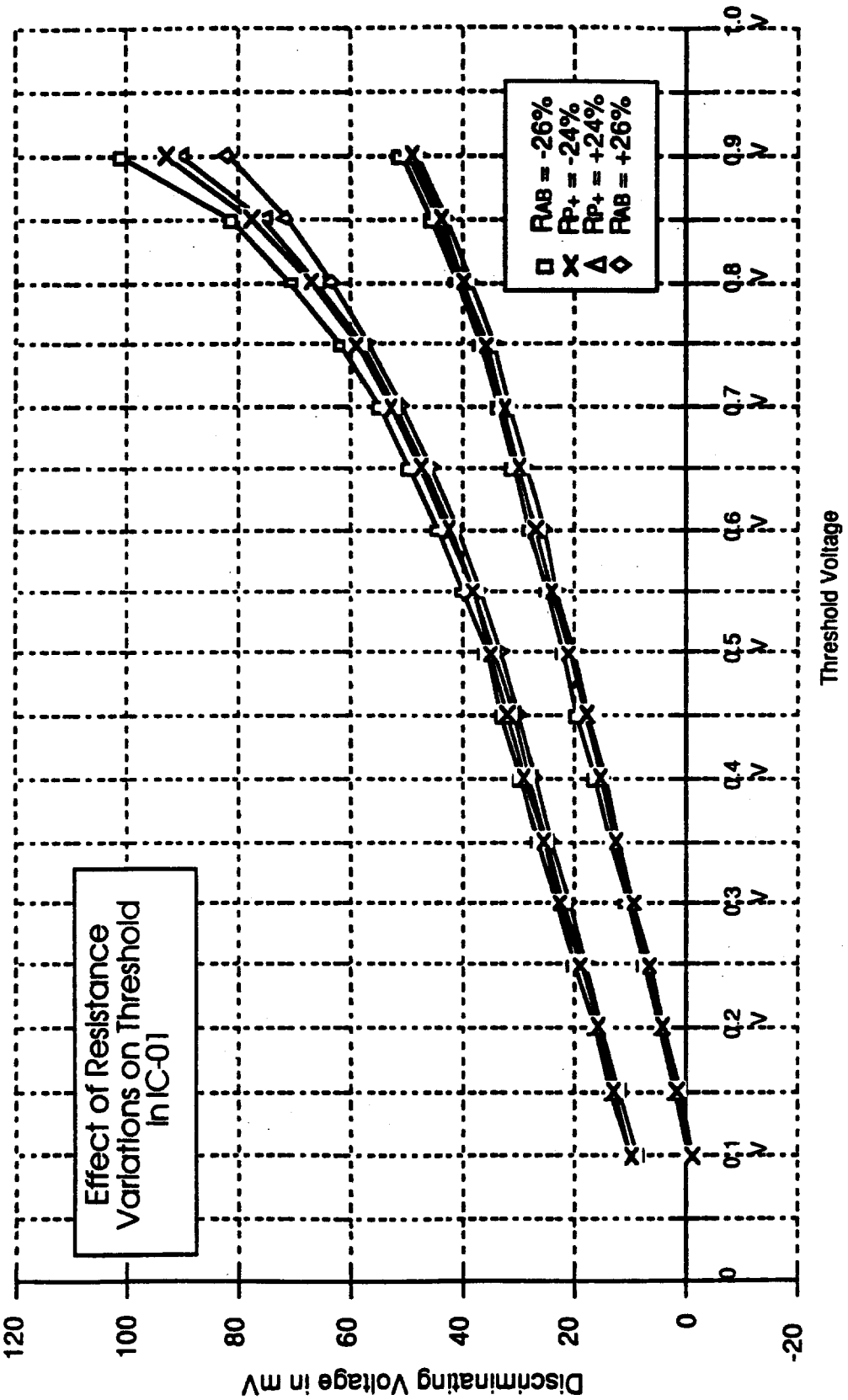
Part Number IC-01

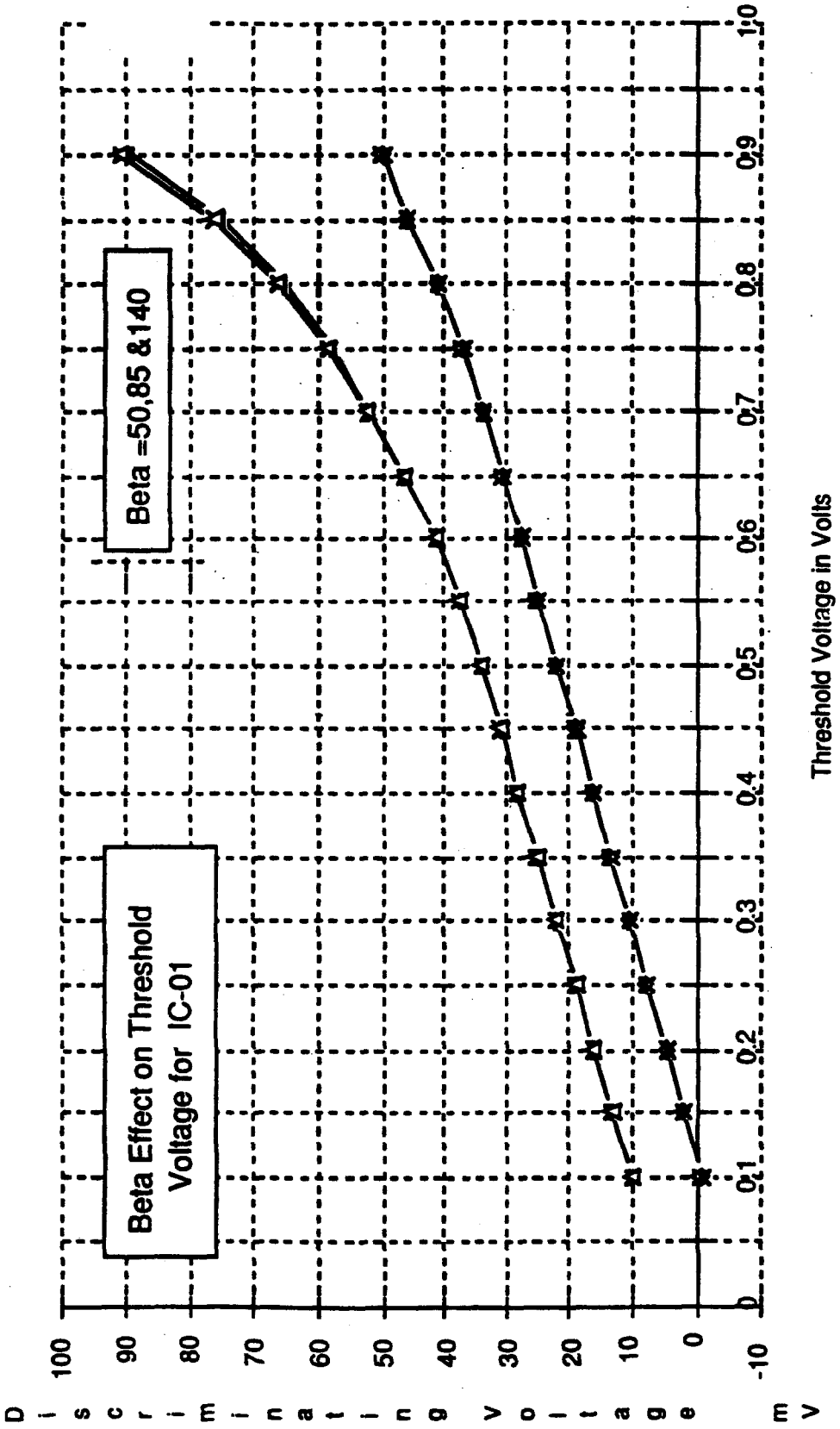


BOTTOM VIEW

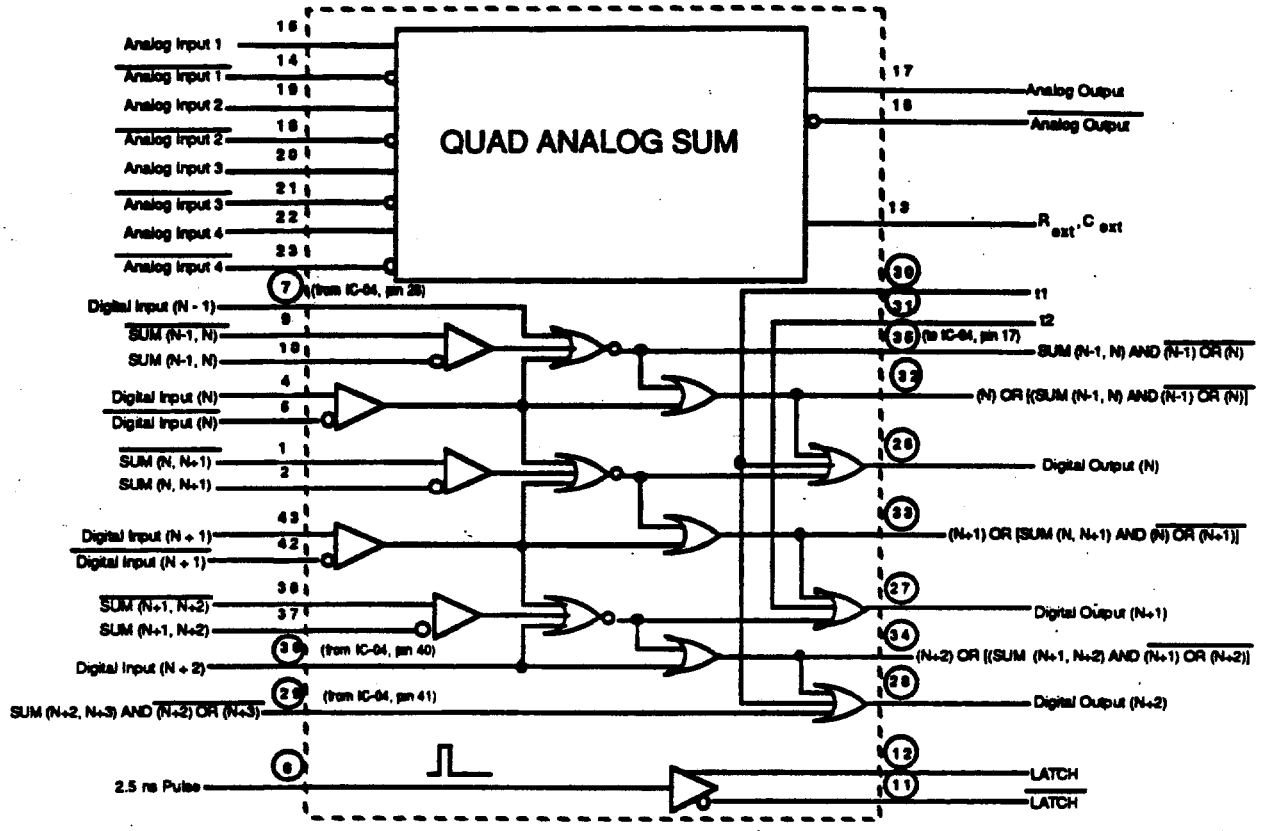
Created 1-24-89
Revised 7-14-89
Merle Haldeman / Scott Holm


Temperature Effect on
Threshold Voltage for IC-01
T = 27°C
T = 125°C
Hysteresis Band
Threshold Voltage in Volts
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
100
90
80
70
60
50
40
30
20
10
0
-10


Effect of Resistance Variations on Threshold in IC-01
RAB = -26%
RP+ = -24%
RP+ = +24%
RAB = +26%
Discriminating Voltage in mV
120
100
80
60
40
20
0
-20
0
0.1 V
0.2 V
0.3 V
0.4 V
0.5 V
0.6 V
0.7 V
0.8 V
0.9 V
1.0 V
Threshold Voltage


Beta Effect on Threshold Voltage for IC-01
Beta =50,85 &140
Discriminating Voltage mV
100
90
80
70
60
50
40
30
20
10
0
-10
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Threshold Voltage in Volts

IC-02: 3-CHANNEL LOGIC,QUAD ANALOG SUM & LATCH DRIVER



IMPLICIT PINS

GROUND pins: 3 (GND1 - Logic Circuitry)
39 (GND2 - Logic Output)
24 (GND3 - Analog)

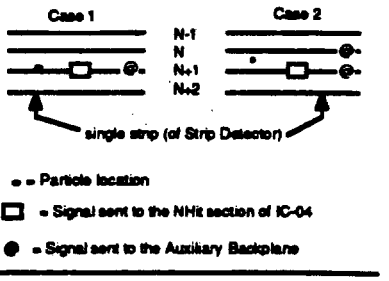
+ 3.5 V pins: 25 - 44

- 5.2 V pins: 6 - 40 - 41

NOTES

1. Digital outputs (pins # 26, 27, 28) go to the Auxiliary Backplane
2. Some Output Sums (pins # 32, 33, 34) go to the NHit section of IC-04
3. Lines entering circled pins follow ECL levels.
4. Power dissipation is 410 mW typical, 559 mW max.
5. Power supply currents: + 3.5 V: @ 19 mA Typical, 26 mA max.
   - 5.2 V: @ 66 mA Typical, 80 mA max.

RELATIONSHIP BETWEEN PART ICLE LOCATION IN THE DETECTOR AND PIC MOD ULE OUTPUT



TRUE TABLE

INPUTS					OUTPUTS	
N	SUM (N, N+1)	N+1	SUM (N+1, N+2)	N+2	N+1	N+1 OR [(SUM (N, N+1) AND $\overline{(N) \text{ OR } (N+1)}$]
X	X	1	X	X	1	1
0	1	0	X	X	1	1
X	X	0	1	0	1	

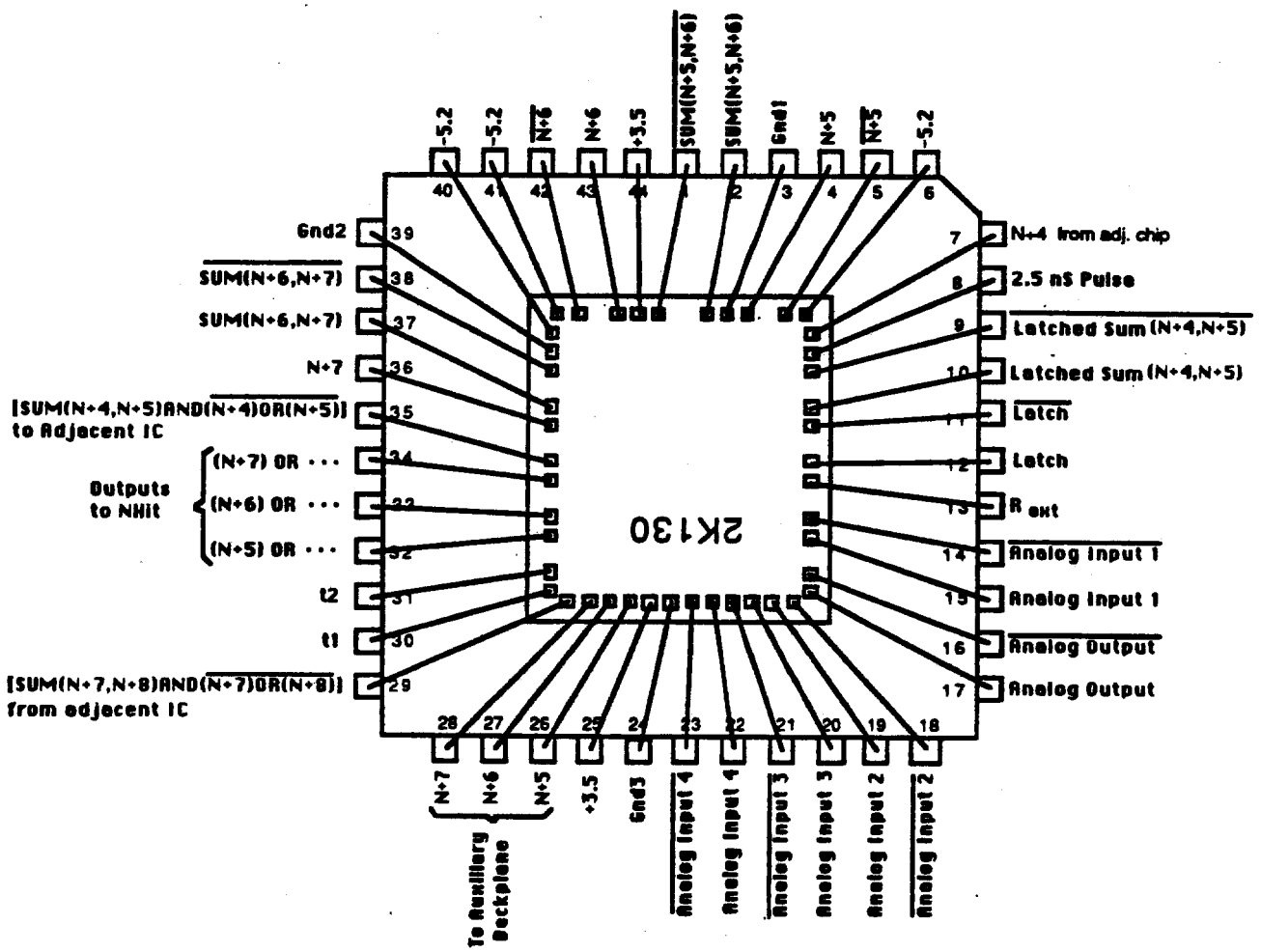
All other input conditions produce zero outputs. X = Dont Care

IC-02: SSD 3-CHANNEL LOGIC, QUAD ANALOG SUM and LATCH DRIVER

Cavity Down

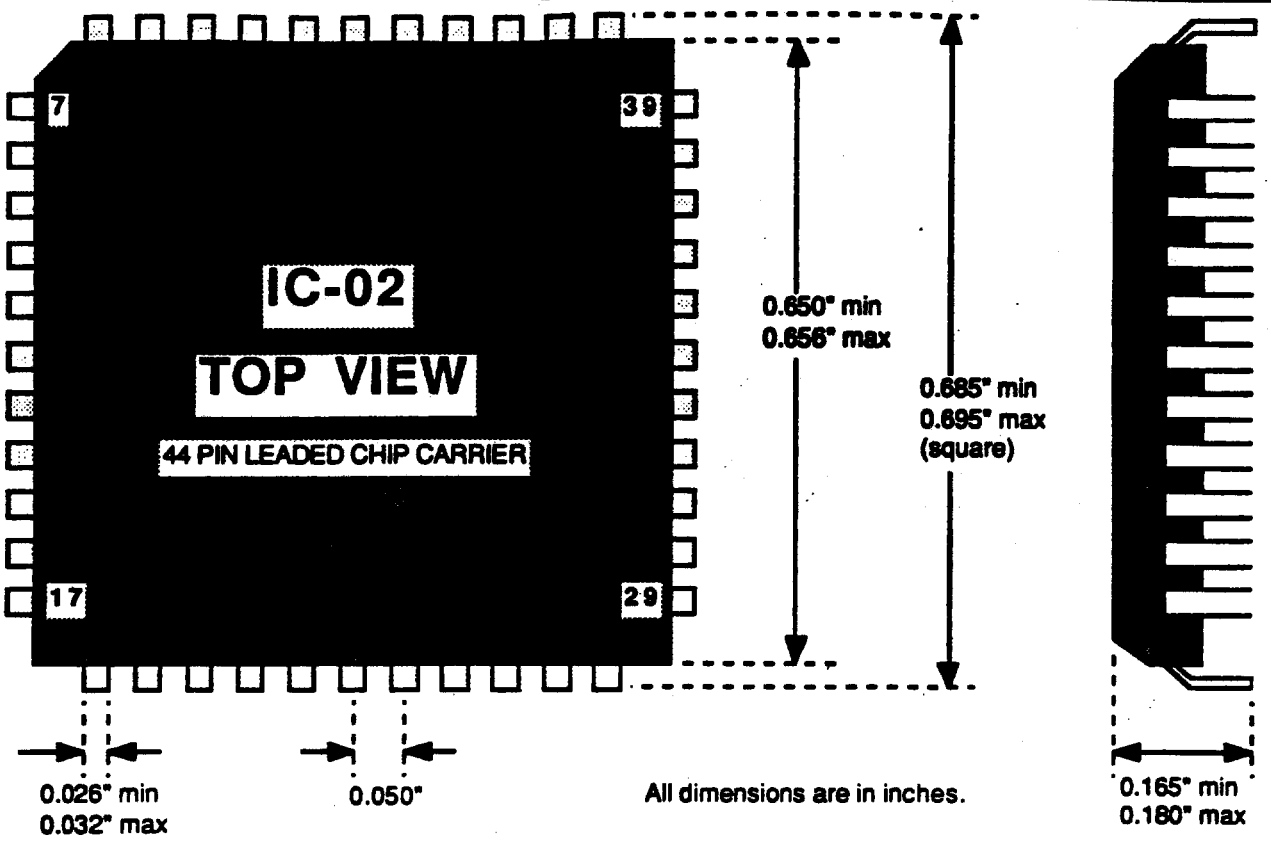
Thermally Enhanced, 44 Lead Plastic Chip Carrier

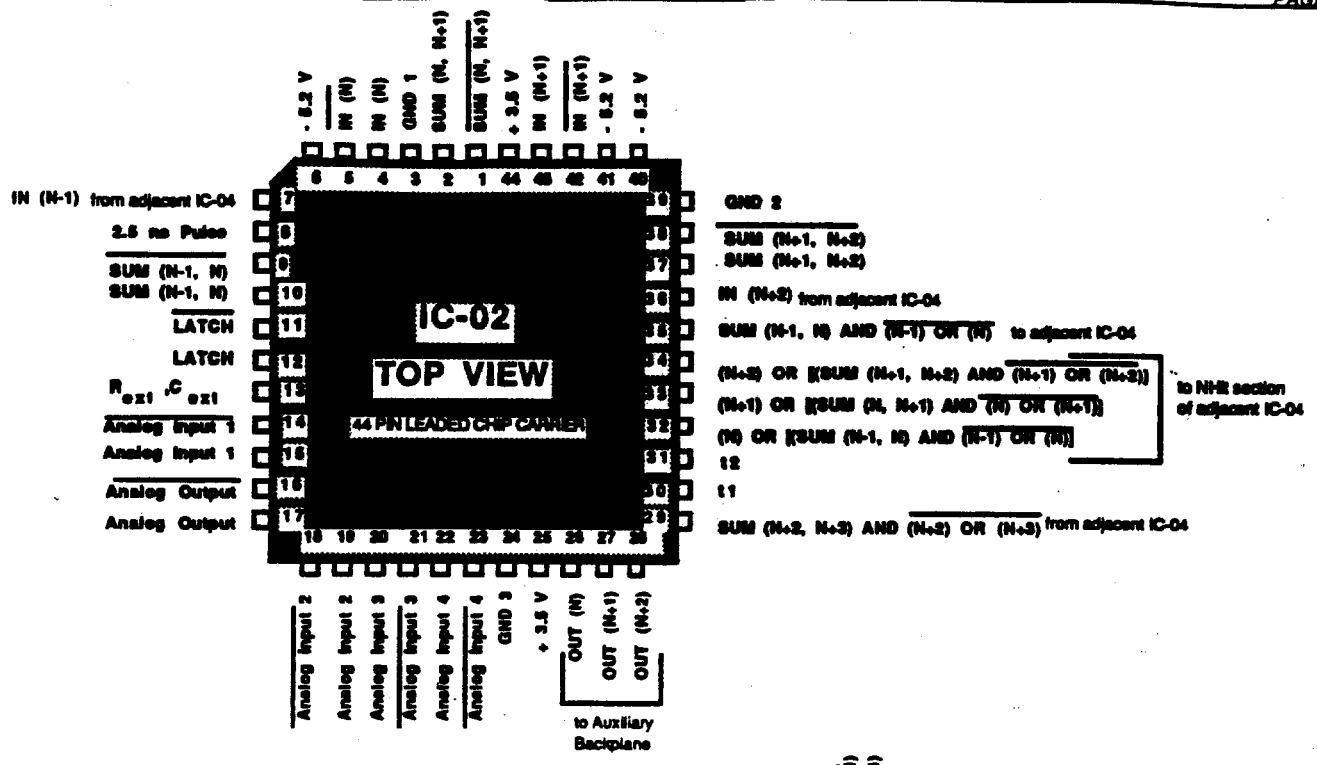
Part Number IC-02

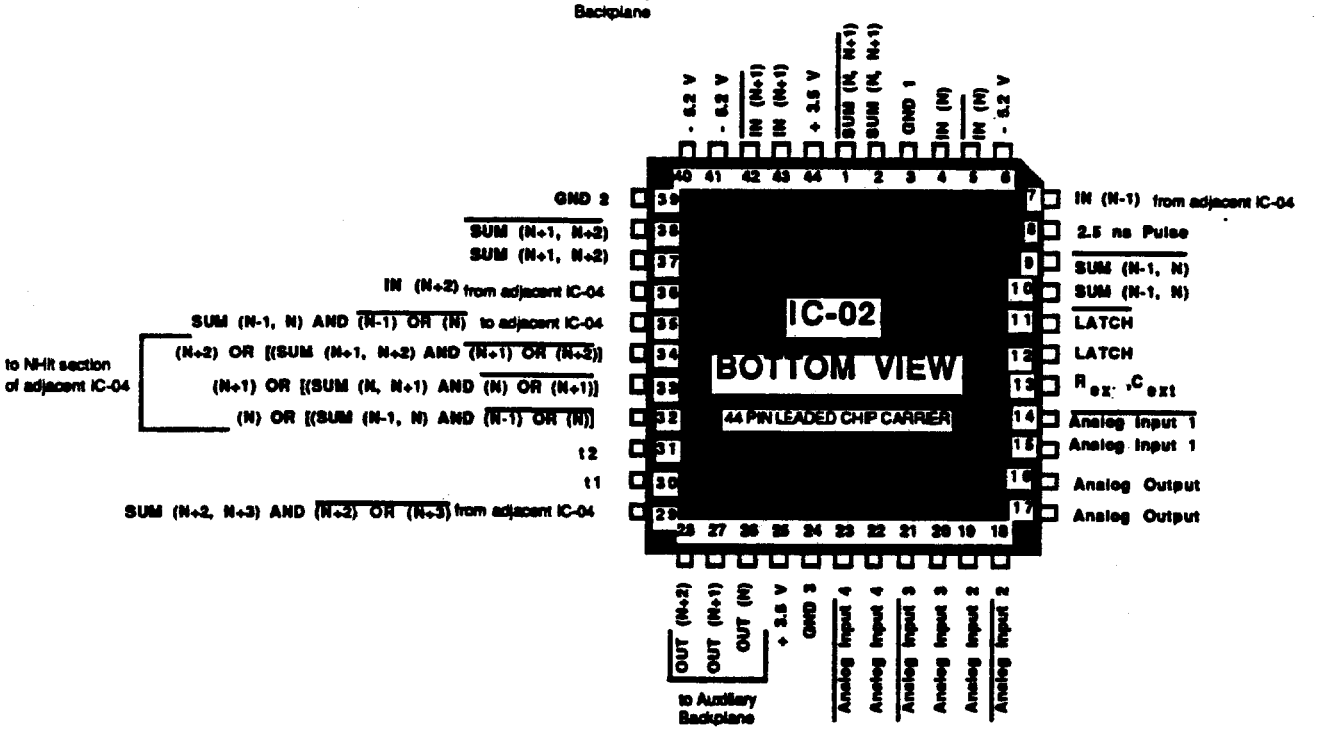


BOTTOM VIEW

Created 8-28-89
Revised
Merle Haldeman / Bruce Merkel

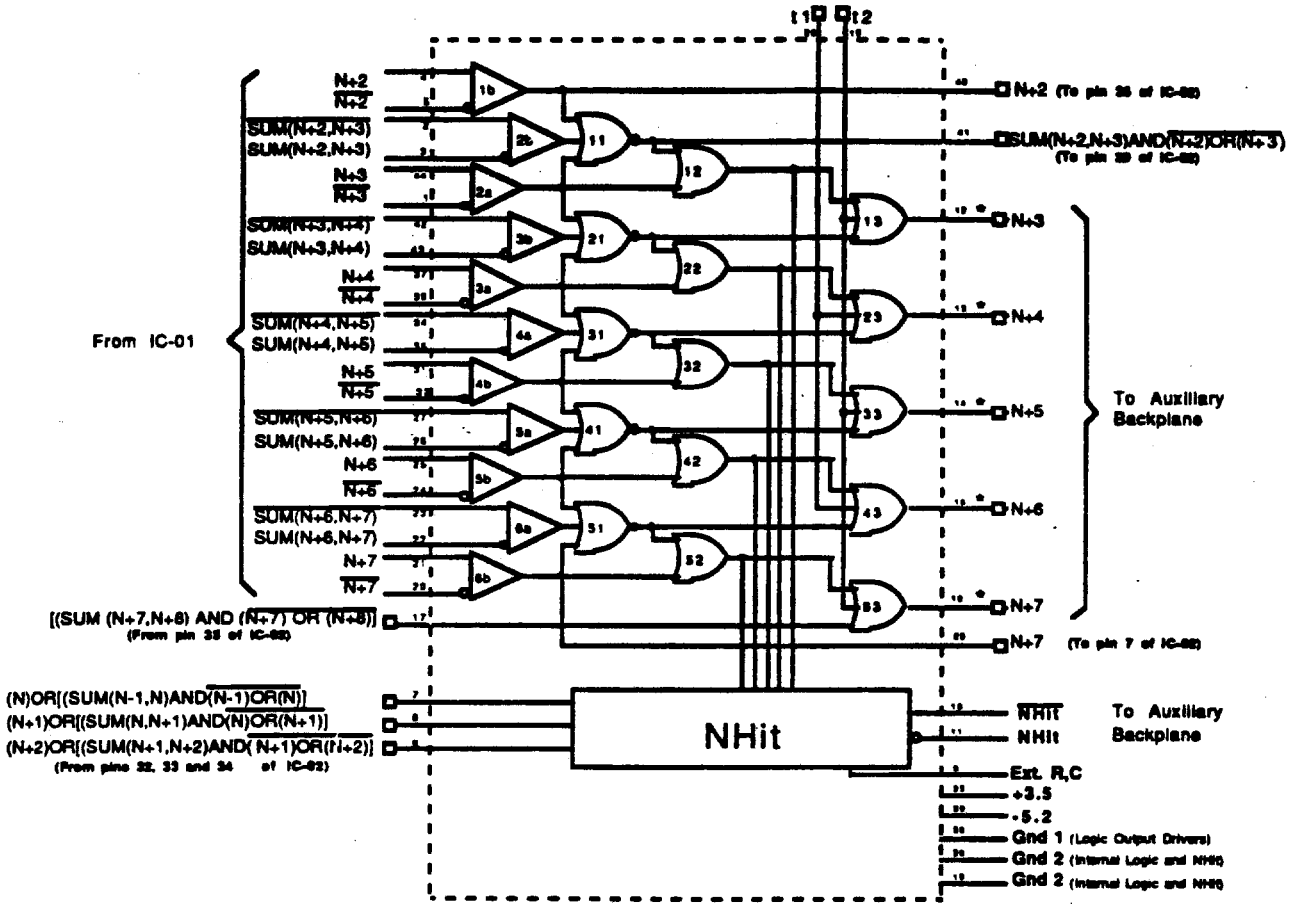

7
39
IC-02
TOP VIEW
44 PIN LEADED CHIP CARRIER
17
29
0.650" min
0.656" max
0.685" min
0.695" max
(square)
0.026" min
0.032" max
0.050"
All dimensions are in inches.
0.165" min
0.180" max


IC-02
TOP VIEW
44 PIN LEADED CHIP CARRIER
- 5.2 V
IN (N)
IN (N)
GND 1
SUM (N, N+1)
SUM (N, N+1)
+ 3.5 V
IN (N+1)
IN (N+1)
- 5.2 V
- 5.2 V
IN (N-1) from adjacent IC-04
2.5 ns Pulse
SUM (N-1, N)
SUM (N-1, N)
LATCH
LATCH
Rext ,Cext
Analog Input 1
Analog Input 1
Analog Output
Analog Output
GND 2
SUM (N+1, N+2)
SUM (N+1, N+2)
IN (N+2) from adjacent IC-04
SUM (N-1, N) AND (N-1) OR (N) to adjacent IC-04
(N+2) OR [(SUM (N+1, N+2) AND (N+1) OR (N+2))]
(N+1) OR [(SUM (N, N+1) AND (N) OR (N+1))]
(N) OR [(SUM (N-1, N) AND (N-1) OR (N))]
to N-1 section of adjacent IC-04
t2
t1
SUM (N+2, N+3) AND (N+2) OR (N+3) from adjacent IC-04
Analog Input 2
Analog Input 2
Analog Input 3
Analog Input 3
Analog Input 4
Analog Input 4
GND 3
+ 3.5 V
OUT (N)
OUT (N+1)
OUT (N+2)
to Auxiliary Backplane


IC-02
BOTTOM VIEW
44 PIN LEADED CHIP CARRIER
- 5.2 V
- 5.2 V
IN (N+1)
IN (N+1)
+ 3.5 V
SUM (N, N+1)
SUM (N, N+1)
GND 1
IN (N)
IN (N)
- 5.2 V
GND 2
SUM (N+1, N+2)
SUM (N+1, N+2)
IN (N+2) from adjacent IC-04
SUM (N-1, N) AND (N-1) OR (N) to adjacent IC-04
(N+2) OR [(SUM (N+1, N+2) AND (N+1) OR (N+2))]
(N+1) OR [(SUM (N, N+1) AND (N) OR (N+1))]
(N) OR [(SUM (N-1, N) AND (N-1) OR (N))]
to N-1 section of adjacent IC-04
t2
t1
SUM (N+2, N+3) AND (N+2) OR (N+3) from adjacent IC-04
IN (N-1) from adjacent IC-04
2.5 ns Pulse
SUM (N-1, N)
SUM (N-1, N)
LATCH
LATCH
Rext ,Cext
Analog Input 1
Analog Input 1
Analog Output
Analog Output
OUT (N+2)
OUT (N+1)
OUT (N)
+ 3.5 V
GND 3
Analog Input 4
Analog Input 4
Analog Input 3
Analog Input 3
Analog Input 2
Analog Input 2
to Auxiliary Backplane

IC-04: SSD 5-Channel Log ic and Octal NHit

Part Number IC-04 V2.0

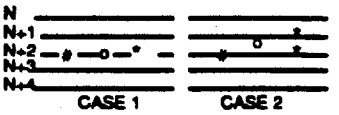


Power Dissipation: 514 mW typ.; 700 mW max. (Outputs: 100 ohms to -2.0 V)
Power supply currents: +3.5 @ 28 mA typ. ; 38 mA max.
-5.2 @ 80 mA typ. ; 109 mA max.

□ ECL Levels

INPUTS					OUTPUTS	
N	SUM(N,N+1)	N+1	SUM(N+1,N+2)	N+2	N+1	N+1 OR ["***]
X	X	1	X	X	1	1
0	1	0	X	X	1	1
X	X	0	1	0	1	

All other input conditions produce zero outputs
X = Don't Care



o Location of particle in SSD
Signals to NHit
* Signals to Auxiliary Backplane

Created 4-23-90
Revised 4-2-90
Merle Haldeman / Jim Hoff

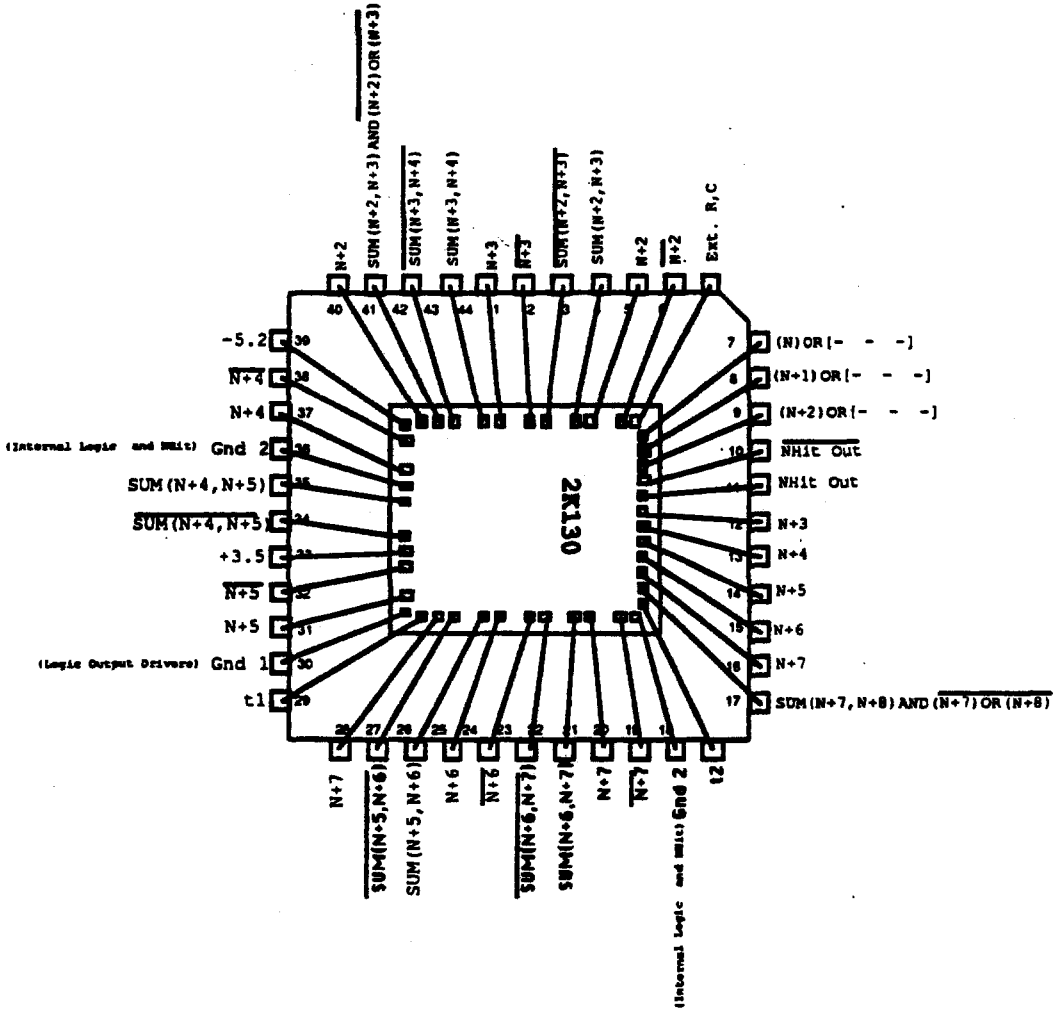
43 Pads Used

IC-04: SSD 5-CHANNEL LOGIC & OCTAL NHit

Cavity Down

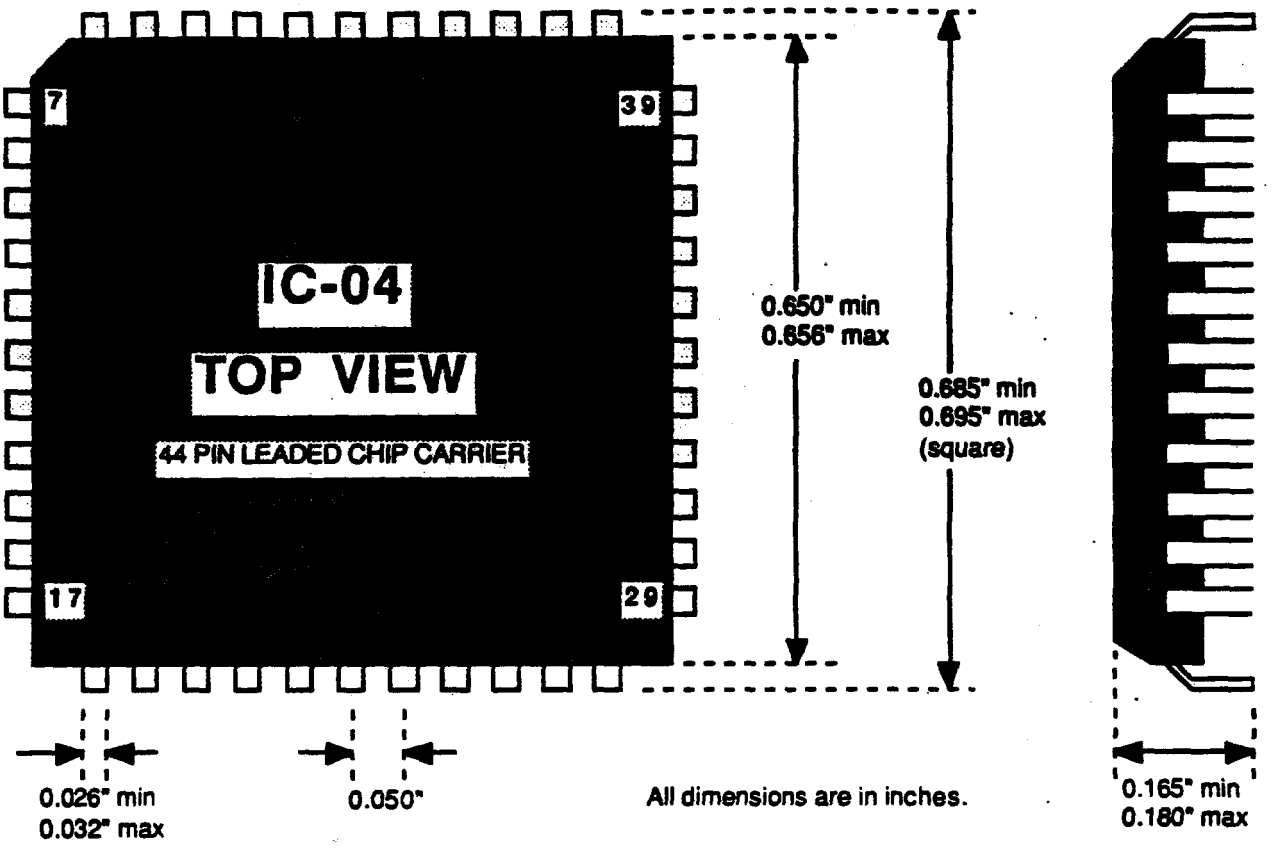
Thermally Enhanced, 44 Lead Plastic Chip Carrier

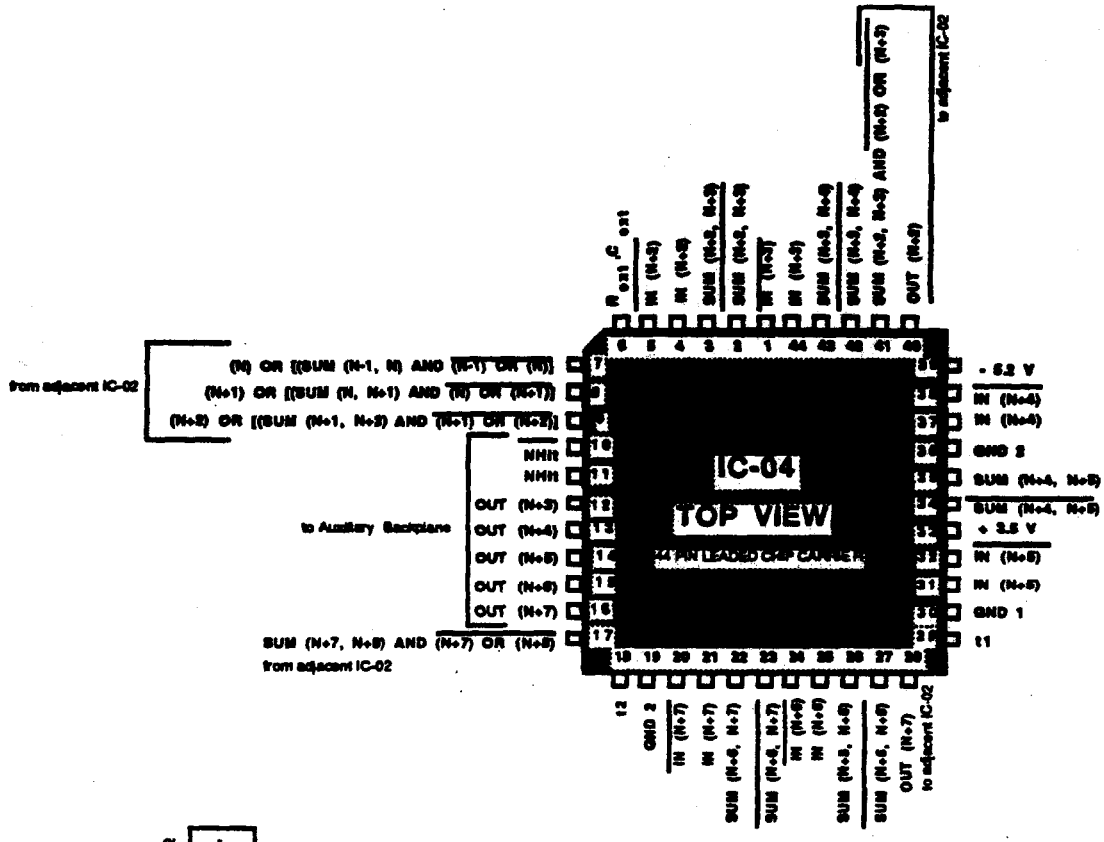
Part Number IC-04, V2.0

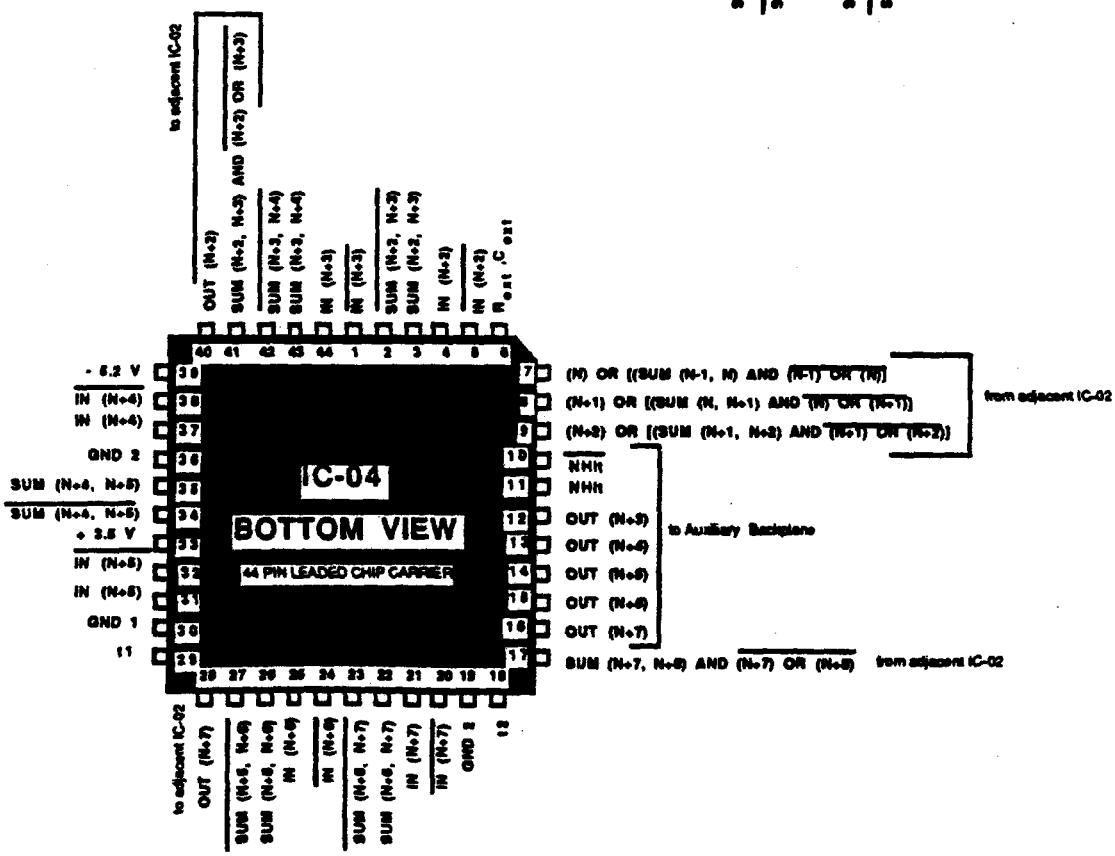


BOTTOM VIEW

Created 8-28-89
Revised 10-13-89
Merle Haldeman / Jim Hoff


7
39
IC-04
TOP VIEW
44 PIN LEADED CHIP CARRIER
17
29
0.650" min
0.656" max
0.685" min
0.695" max
(square)
0.026" min
0.032" max
0.050"
All dimensions are in inches.
0.165" min
0.180" max


IC-04
TOP VIEW
44 PIN LEADED CHIP CARRIER
from adjacent IC-02
(N) OR [(SUM (N-1, N) AND (N-1) OR (N)]
(N+1) OR [(SUM (N, N+1) AND (N) OR (N+1)]
(N+2) OR [(SUM (N+1, N+2) AND (N+1) OR (N+2)]
to Auxiliary Backplane
NHN
NHN
OUT (N+3)
OUT (N+4)
OUT (N+5)
OUT (N+6)
OUT (N+7)
SUM (N+7, N+8) AND (N+7) OR (N+8)
from adjacent IC-02
- 5.2 V
IN (N+4)
IN (N+4)
GND 2
SUM (N+4, N+5)
SUM (N+4, N+5)
+ 3.5 V
IN (N+5)
IN (N+5)
GND 1
t1
t2
GND 2
IN (N+7)
IN (N+7)
SUM (N+6, N+7)
SUM (N+6, N+7)
IN (N+6)
IN (N+6)
SUM (N+5, N+6)
SUM (N+5, N+6)
OUT (N+7)
to adjacent IC-02
OUT (N+2)
SUM (N+2, N+3) AND (N+2) OR (N+3)
to adjacent IC-02


IC-04
BOTTOM VIEW
44 PIN LEADED CHIP CARRIER
OUT (N+3)
SUM (N+2, N+3) AND (N+2) OR (N+3)
SUM (N+3, N+4)
SUM (N+3, N+4)
IN (N+3)
IN (N+3)
SUM (N+2, N+3)
SUM (N+2, N+3)
IN (N+2)
IN (N+2)
- 5.2 V
IN (N+4)
IN (N+4)
GND 2
SUM (N+4, N+5)
SUM (N+4, N+5)
+ 3.5 V
IN (N+5)
IN (N+5)
GND 1
t1
(N) OR [(SUM (N-1, N) AND (N-1) OR (N)]
(N+1) OR [(SUM (N, N+1) AND (N) OR (N+1)]
(N+2) OR [(SUM (N+1, N+2) AND (N+1) OR (N+2)]
from adjacent IC-02
NHN
NHN
OUT (N+3)
OUT (N+4)
OUT (N+5)
OUT (N+6)
OUT (N+7)
to Auxiliary Backplane
SUM (N+7, N+8) AND (N+7) OR (N+8)
from adjacent IC-02
to adjacent IC-02
OUT (N+7)
SUM (N+6, N+8)
SUM (N+6, N+8)
IN (N+6)
IN (N+6)
SUM (N+6, N+7)
SUM (N+6, N+7)
IN (N+7)
IN (N+7)
GND 2
t2