3.5 HARDWARE JUMPERS

3.5.1 DAC/ADC Jumpers

The illustration is an abbreviated pattern of the IC-03 DAC/ADC jumpering scheme which exists on the P/C Module.

There are 256 DACs which are addressed via CSR addresses C000_0000 through C000_00FF inclusive. DAC address 00 (Hex), will always set the threshold voltage on the uppermost trace which is the threshold for the discriminator connected to the output of the summed channel which takes the sum of channel -1 and channel 0 (Σ-1,0). Likewise DAC address 01 (Hex), will always set the threshold voltage on the trace immediately below the uppermost trace which is the threshold for the discriminator connected directly to the individual channel #0 input. DAC address 02 (Hex), will always set the threshold voltage for the discriminator connected to the output of the summed channel which takes the sum of channel 0 and channel 1 (Σ0,1). DAC address 03 (Hex), will always set the threshold voltage for the discriminator connected directly to the individual channel #1 input. This pattern continues for the 256 DACs and the 256 discriminator threshold setting inputs.

It should be obvious that if all 256 DAC's are employed, no jumpers are required and each discriminator has an individual DAC to control it's threshold. However, in the event that only 4 of the 256 DAC's are mounted on the P/C Module, the jumpers would probably be applied such that DAC 00 (hex) would drive every other sum channel. i.e., Σ(0), Σ(1,2), Σ(3,4), Σ(5,6) etc. DAC 01 (hex) would drive the even individual channels; DAC 02 (hex) would drive sum channels Σ(0,1), Σ(2,3), Σ(4,5), Σ(6,7) etc., and DAC 03 (hex) would drive the odd, individual channels.

The common choices of DAC populations are 4,8,16,32,64,128 or 256 which corresponds to 1,2,4,8,16,32 and 64 IC-03 packages. It seems reasonable to assume that for four DAC's every fourth threshold lead would be connected together and so on. However, any and all possibilities exist for connecting DAC outputs to threshold inputs and the method used may be dictated by the detector geometry.

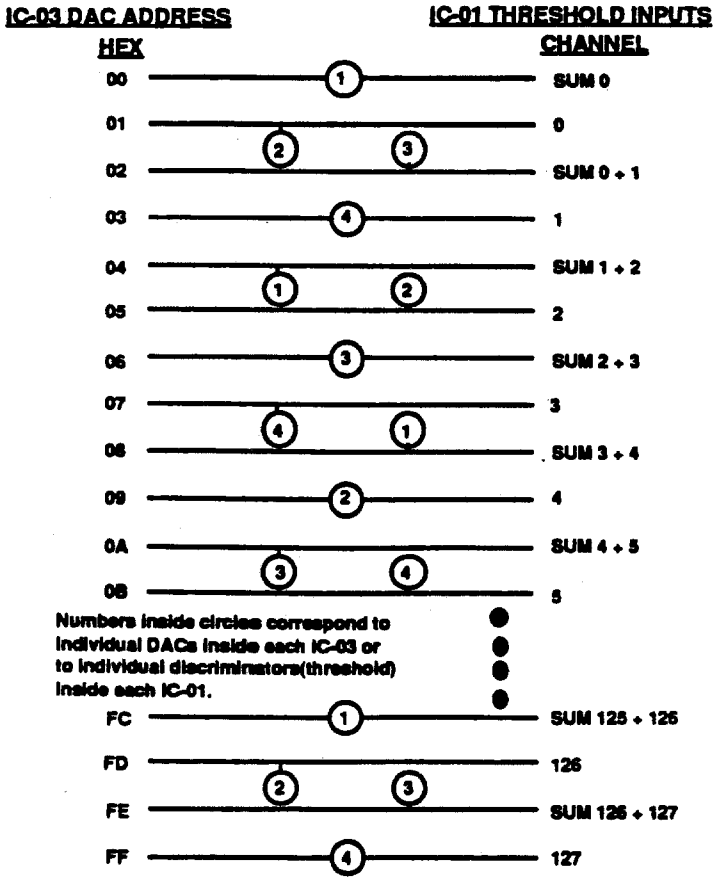


Figure 21: DAC/ADC Jumpering

3.5.2 CSR10 Jumpers

The value found in CSR10 corresponds to the configuration of three, two position jumpers(JU2, JU3, and JU4) that connect a signal trace to ground(GND) or +5V. The physical module location of the three posts for each jumper, and their connections are shown below. Table 1 on the following page provides the relationship between DAC population, jumper location, CSR10 readback and lowest ordered address for each DAC chip.
When less than 256 DAC's are utilized, the P/C module will be populated from the lowest address onward without skipping addresses, this is done by a mapping routine within the EPM5128 programmable PAL. It has been done this way to make the DACs accessible by block transfer. The PAL receives a 3 bit code from the jumpers to indicate the number of IC-03 DAC/ADC chips mounted and coverts the sequential DAC address it receives from an external source to the appropriate DAC module address. I.E. if only two IC-03s(8 DACs) are used and located at DAC board address 0 through 3(U97) and DAC board address 64 through 67(U129), the PAL knowing from the jumpering scheme will only accept DAC addresses 0 through 7 from an external source and in turn converts external address 0 to DAC board address 0 and so on up to external address 7 to DAC board address 67. When less than 256 DACs are employed the IC-03s physical location is important to insure that the external address received is converted to the appropriate DAC board address. The physical locations for the common number of IC-03s used are shown in Table 2 on the following page.

CSR10 JUMPERING DIAGRAM

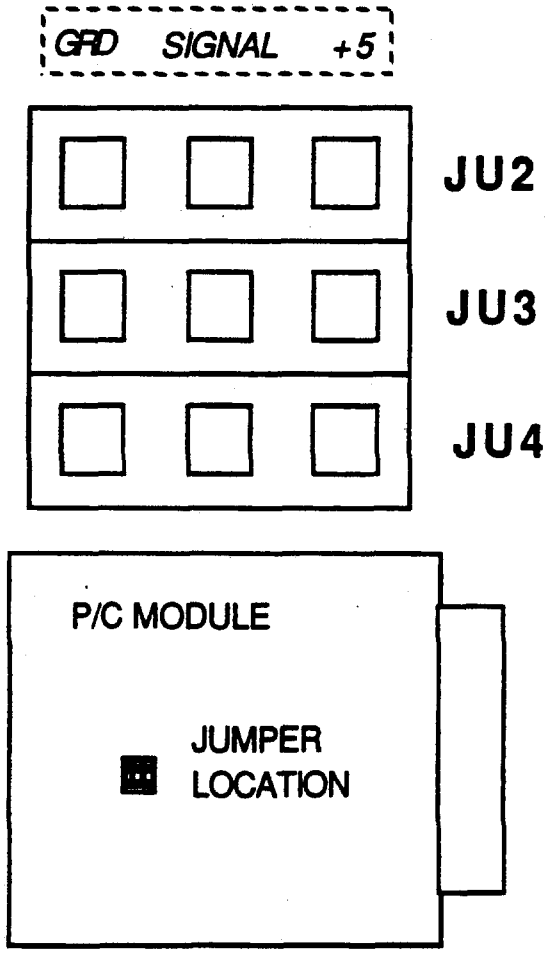


Figure 22: CSR10 Jumpering

Table 1

Jumper Numbers			# of DACs	CSR10 Value	First DAC board address of each IC-03
JU2	JU3	JU4			
Gnd	Gnd	Gnd	????	0	This is a special case, unique to the user.
Gnd	Gnd	+5V	4	1	0
Gnd	+5V	Gnd	8	2	0,80
Gnd	+5V	+5V	16	4	0,40,80,C0
+5V	Gnd	Gnd	32	8	0,20,40,60,80,A0,C0,E0
+5V	Gnd	+5 V	64	10	0,10,20,30,40,50,60,70,80,90,A0,B0,C0,D0,E0,F0
+5V	+5V	Gnd	128	20	0,8,10,18,20,28,30,38,40,48,50,58,60,68,70,7880,88,90,98,A0,A8,B0,B8,C0,C8,D0,D8,E0,E8, F0,F8
+5V	+5V	+5V	256	40	All addresses from 00 through FF inclusive are valid

Table 2

Number of IC-03s mounted(#DACs)	IC-03 Physical location on module
1(4)	U97
2(8)	U97, U129
4(16)	U97, U113, U129, U145
8(32)	U97, U105, U113, U121, U129, U137, U145, U153
16(64)	U97, U101, U105, U109, U113, U117, U121, U125, U129, U133, U137, U141, U145, U149, U153, U157
32(128)	U97, U99, U101, U103, U105, U107, U109, U111, U113, U115, U117, U119, U121, U123, U125, U127, U129, U131, U133, U135, U137, U139, U141, U143, U145, U147, U149, U151, U153, U155, U157, U159
64(256)	ALL LOCATIONS

4.0 P/C MODULE - TESTING AND CALIBRATION

4.1 UNPOWERED TEST

A test should be performed to check for shorts between the power planes (layers) of the P/C module. The test should verify no direct connection between any of the following power planes: -5.2V, -3.5V, -2V, -.8V top, -.8V bottom, +5V, +3.5V, +1.25V, and ground. The test can be done with an OHM METER. Connection to the power plane can be found at the following locations, with the measured impedances between the power and ground plane with the PC board fully assembled(number of IC-03s equals four).

-5.2V = right side of D5	= 8 ohm
-3.5V = right side of fuse f4	= 3 ohm
-2V = right side of fuse f1	= 22 ohm
-.8V top = right side of CR2	= 23 ohm
-.8V bottom = right side of CR4	= 23 ohm
+5V = right side of fuse f6	= 400 ohm(90 ohm with EPM5128 installed)
153 = right side of fuse f2	= 580 ohm
+1.25V = case of Q1	= 73 ohm
GROUND = left side of D5	

NOTE: Right side is towards the front of the board where the LABEL is located. The drawing "POWER TEST POINT DETAILS"#2563.000-MD-215808 shows the power pin locations of various devices on the top side of the board, this should help in finding shorts.

4.2 AUTOMATED TESTING

Their is an "Acceptance Test Description" document that uses two software packages to verify wether a P/C module is acceptable from an outside vendor. This document can be found in APPENDIX A.

4.3 CALIBRATION

Adjusting the value at which the ***TEMP*** LED on the front panel of the P/C module will turn on is the only calibration needed for the module. Adjusting trim pot R295 sets the temperature at which the LED will turn on and off, the setting of R295 controls the voltage on pin 2 of U185. If pin 3 of U185 which is connected to the LM35 temperature sensor is at a more positive value than pin 2 of U185 the LED will turn on. The voltage on pin 2 should be set to 0.5V this corresponds to 50 degrees Celsius. The LM35 will output to pin 3 of the U185 a 10 mV per degree Celsius voltage level. If the temperature rises above 50 degrees Celsius(0.5V on pin 3) the LED will turn on. The LED will turn off if the temperature falls below 50 degrees Celsius. The ***TEMP*** LED and associated circuitry can be tested by adjusting R295 for a voltage on pin 2 of U185 that is less than the value on pin 3 of U185, the lower voltage should cause the ***TEMP*** LED to turn on.

5.0 APPENDICES

APPENDIX A - TEST SOFTWARE
APPENDIX B - FASTBUS INTERFACE PAL PROGRAM
APPENDIX C - POSTAMP/COMPARATOR MODULE - SCHEMATIC
APPENDIX D - MODULE DRAWINGS
APPENDIX E - DATA SHEETS

APPENDIX A - TEST SOFTWARE

This appendix contains an acceptance criteria specification that pertains to the testing of the POSTAMP/COMPARATOR printed circuit board.

POSTAMP/COMPARATOR MODULE - ACCEPTANCE TEST DESCRIPTION

The party performing the acceptance test on the POSTAMP/COMPARATOR module should be familiar with the "IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control system"(ANSI/IEEE Std. 960-1986), the POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100, and the two software packages listed below which the acceptance criteria is based upon. Questions pertaining to the documents should be addressed to the appropriate originator.

SILICON STRIP DETECTOR (SSD)
System Test Software Guide
Version: 0 15 march 1991

Originators:
Wolfgang Kowald Duke University
EXP.771 #708-840-4250
Panagiotis Spentzouris UCA
EXP.771 #708-840-4250
Dave Slimmer Fermilab
Computing Dept. #708-840-4334

SILICON STRIP DETECTOR SYSTEM "SINGLE BOARD DIAGNOSTICS TESTS"-PN434
Software Description
Version: 1 4/25/91

Originator:
Garry R. Moore Fermilab
Computing Dept. #708-840-4059

POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100
Complete Module Documentation Manual
Version: 3 5/7/91

Originators:
Merle Haldeman Fermilab
RD/DEG group #708-840-3958
Scott Holm Fermilab
RD/DEG group #708-840-4340
Bruce Merkel Fermilab
RD/DEG group #708-840-3263

In order for the PC module to be accepted, the PC module must pass the following four tests.

1. PC_TEST

Refer to the "SINGLE BOARD DIAGNOSTICS TESTS" documentation listed above.

PC_TEST is a menu driven software tool capable of effectively testing and/or exercising all FASTBUS accessible circuitry of the POSTAMP/COMPARATOR module. The test should be run in the "Exercise Postamp Comparator" mode; this is #3 under the PC_TEST main menu. This option will fully exercise all FASTBUS accessible circuitry of the PC module including all geographical address, secondary address, and DAC/ADC circuitry.

ACCEPTANCE- The software will respond with errors if the module responds incorrectly. The module is unacceptable when any errors are reported.

EXCEPTIONS: A part of the test writes and then reads a series of IC-03 DAC values, the software will respond with an error if the DAC value read back is more than plus or minus one LSB different than the written value. The module however, will be accepted when the DAC value read back is within two LSB's of the written value.

Refer to the "SILICON STRIP DETECTOR (SSD)" documentation listed on page 1 for the remaining three tests.

2. PC test counter test

This test uses an 8-bit counter on the PC module to generate 256 patterns used for testing the output portion(IC-02 and IC-04 ASIC's) of the PC module. The 8-bit counter cycles through 256 output pattern possibilities which are sent to the IC-02 and IC-04 test inputs; t1 and t2. The outputs of the IC-02s and IC-04s provide 256 different 128-bit patterns which are sent to the DE module through the FASTBUS auxiliary backplane. This test effectively tests the outputs of all IC-02 and IC-04 ASIC's as well as their connections to the backplane. The DE module has 256 memory locations which are continually being loaded with the 256 pattern possibilities. In this test an individual DE memory location is always being loaded with the same pattern generated by the PC module test counter.(Refer to section 5.4.2 PC test counter test and to APPENDIX A for test counter patterns).

ACCEPTANCE- The PC module is acceptable if no errors occur. The software will know in which memory location in the DE module each pattern generated by PC module's IC-02 and IC-04 ASICs are stored. When a memory location in the DE module is read by the software, the 128-bit pattern in that location is compared with the 128-bit pattern that was expected for that location. An error is reported if the values do not match.

3. PC channel characterization tests

This test characterizes individual and sum channel threshold voltage sensitivity for the PC module discriminator electronics. Characterizing a channel involves placing a test signal at a channel input and then scanning through the threshold setting DAC, value range with the software recording the highest threshold voltage(DAC value) at which the channel discriminator was able to detect the input test signal. The test should be performed in the default mode(DAC vs CHANNEL mode). In this mode, five separate routines need to be run on the module. These routines are listed in a menu that is displayed after "PC channel characterization test"(h) is selected from the System test menu. Invoking any one of the routines, automatically sets up the PC module for that

routine, i.e. turning on individual channel or sum channel mode, and placing the PC module in the RUN mode.

The first routine, "INDIVIDUAL CHANNEL", tests all individual channels of the PC module. The software performs in the following way: the TSM module's 256 word by 128 bit memory(refer to TSM document#) is loaded with a pattern of alternating words consisting of all A's and 5's, which means adjacent bits in a given word have opposite values as well as a given bit in adjacent memory addresses. The TSM module feeds this pattern to the LS module(refer to LS module documentation#)which continually places this pattern at the PC module input. The DE continuously updates its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. At the start, all DACs are set to the highest value in their range(1.25v) and at some instance the software performs 8 nonconsecutive reads of a DE memory location, recording which if any of the 128 channels were on(hit) during each of the 8 reads. The DAC value is then lowered 1 LSB(5mv) and the DE module memory is read 8 more times, this continues until the DACs are at their lowest value in their range(0mv). A graph is made that shows the DAC values at which a channel responded to 8 out of 8 reads with the channel on(hit) and also when the channel responds at least once but less than 8 out of 8 times.

The remaining four routines test the SUM channels. Each routine uses a different pattern such as 1's, 2's, 4's or 8's, i.e. for the 2's pattern every 2nd channel of a 4 channel combination will be toggling on and for the 8's pattern every 4th channel of a 4 channel combination will be toggling on. A graph is made for each routine. In the SUM channel mode when placing an input signal on one channel the adjacent channels also receive this input signal, therefor the adjacent channels should also turn on and the graphs should reflect this.(Refer to section 5.4.6 PC Channel Characterization Tests).

ACCEPTANCE- The input signal from the LS module should be set for a 40mv peak to peak differential amplitude. The PC module passes the test if the resulting graphs that are produced by the software are as follows. ***{SHOW GRAPHS}***The DAC values of all channels may vary no more than plus or minus 15 counts from the norm, i.e. if the norm is at the DAC value of 90, acceptable DAC values range from 75 to 105. A module is unacceptable if a channel is characterized outside of the plus or minus 15 count range.

4. PC Crosstalk Test

PC Crosstalk test will test the ability of the PC module to reject crosstalk to other channels from an input signal of substantial amplitude on a certain other channel. The Crosstalk test uses the TSM and LS modules as in the PC characterization test. In this test the TSM memory is loaded with a 1 in one of the 128 bits of the first word and the remaining 255 words have a 0 in all 128 bits. This means that 1 channel is being stimulated with a 18.9ns pulse every 4.8us. The TSM module feeds this pattern to the LS module which continuously places the pattern at the PC module input, meanwhile the DE is continuously updating its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. Initially, all DACs are set to the highest value in their range(1.25v). The software reads the DE memory location containing the channel that is on(hit), the 128-bit value read, should contain only the one bit that is on. More than one bit on indicates crosstalk. The DAC value is then lowered 1 LSB(5mv) and the DE memory is read again, this repeats until the DAC output is reduced to 150mv. The software then shifts the pattern in the TSM memory one bit so that the next channel is being stimulated with a large amplitude signal, the process of reading the DE memory and lowering the DAC values is repeated. The shifting continues until all 128 channels have been stimulated. Crosstalk is reported each time a nonstimulated channel is on. This procedure shows that channels not responding to the

signals on other channels have less than 3% crosstalk.(Refer to section 5.4.7 PC Crosstalk test).

ACCEPTANCE-The signal amplitude of the input should be set to 500mv peak to peak differential amplitude. The PC module is unacceptable if crosstalk is found on any channel.

SCOTT HOLM 5/8/91

APPENDIX B - FASTBUS INTERFACE PAL PROGRAM

This appendix contains the information on the programming of the EPM5128 PAL that is used for the FASTBUS interface on the POSTAMP/COMPARATOR printed circuit board.

E:\KEN\SSD\PACMP\REVE\PACMPI.RPT

MAX+PLUS Compiler Report File
Version 2.50 05/31/90

** Design compiled without errors

Title: PA/CMP FASTBUS INTERFACE
Company: Fermilab
Designer: KEN TREPTOW
Rev: E
Date: 3:06p 11-15-1990
Turbo: ON
Security: OFF

```
                                                                  R
                BA BA BA BA BA                    I    O O O  E
                AD AD AD AD AD IDS VCC IAS IEG IWT GND MS2 ODK OSS0 OSS1 OSS2 AD/
                4  3  2  1  0  S  C  S  G  T  D  2  K  0  1  2  /
              ---------------------------------------------------------------
            /   9  8  7  6  5  4  3  2  1 68 67 66 65 64 63 62 61   |
     BAD5 | 10                                                  60 | STROBE
     BAD6 | 11                                                  59 | LDCNTR/
     BAD7 | 12                                                  58 | RDCNTR/
     BAD8 | 13                                                  57 | OAK
     BAD9 | 14                                                  56 | RUN
    BAD21 | 15                                                  55 | ENIC
      GND | 16                                                  54 | VCC
    BAD22 | 17                                                  53 | ENSC
    BAD23 | 18                  EPM5128JC-2                     52 | CCLKEN/
    BAD24 | 19                                                  51 | SEL0/
      VCC | 20                                                  50 | GND
    BAD30 | 21                                                  49 | SEL1/
    BAD31 | 22                                                  48 | SEL2/
     IGA0 | 23                                                  47 | SEL3/
     IGA1 | 24                                                  46 | DACRD
     IGA2 | 25                                                  45 | SW2
     IGA3 | 26                                                  44 | SW1
          |_  27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43  _|
              ---------------------------------------------------------------
                IGA IAD INVAD CLK SW IAK GND IRD IMS IMS VCC DNTA DNTA DNTA DNTA NTA1 NTA0
                4   18  D    1ON 0                0   1       5   4   3   2
                                N
```

** RESOURCE USAGE **

ic Array Block	Macrocells	I/O Pins	Expanders	External Interconnect
A: MC1 - MC16	15/16(93%)	8/ 8(100%)	27/32(84%)	19/24(79%)
B: MC17 - MC32	7/16(43%)	5/ 5(100%)	11/32(34%)	19/24(79%)
C: MC33 - MC48	4/16(25%)	5/ 5(100%)	1/32(3%)	6/24(25%)
D: MC49 - MC64	15/16(93%)	8/ 8(100%)	0/32(0%)	11/24(45%)
E: MC65 - MC80	16/16(100%)	8/ 8(100%)	15/32(46%)	23/24(95%)
F: MC81 - MC96	6/16(37%)	5/ 5(100%)	15/32(46%)	17/24(70%)
G: MC97 - MC112	7/16(43%)	5/ 5(100%)	3/32(9%)	24/24(100%)
H: MC113 - MC128	16/16(100%)	8/ 8(100%)	12/32(37%)	23/24(95%)

Total dedicated input pins used:	8/ 8 (100%)
Total I/O pins used:	52/ 52 (100%)
Total macrocells used:	86/128 (67%)
Total expanders used:	84/256 (32%)

Total input pins required:	20
Total output pins required:	24
Total bidirectional pins required:	16
Total macrocells required:	86
Total expanders in database:	69

Synthesized macrocells:	0/128 (0%)

** FILE HIERARCHY **

```
¦DACMAP:78¦
¦DACMAP:78¦74139:28¦
¦DACMAP:78¦74151:30¦
¦DACMAP:78¦74151:18¦
¦DACMAP:78¦74151:17¦
¦DACMAP:78¦74151:16¦
¦DACMAP:78¦74151:15¦
¦DACMAP:78¦74151:5¦
¦NTAREG:48¦
¦NTAREG:48¦DACSEL:108¦
¦NTAREG:48¦DACSEL:108¦74138H:11¦
¦NTAREG:48¦CT8:93¦
¦CONTROL:45¦
¦CONTROL:45¦DELAY:165¦
¦GASEL:46¦
¦OUTMUX:50¦
¦OUTMUX:50¦74153:81¦
¦OUTMUX:50¦74138H:82¦
¦OUTMUX:50¦74153:74¦
¦OUTMUX:50¦74153:75¦
¦OUTMUX:50¦74153:76¦
¦OUTMUX:50¦74153:77¦
¦OUTMUX:50¦74153:78¦
   TMUX:50¦74153:79¦
   TMUX:50¦74153:80¦
¦CSR0:49¦
```

** INPUTS **

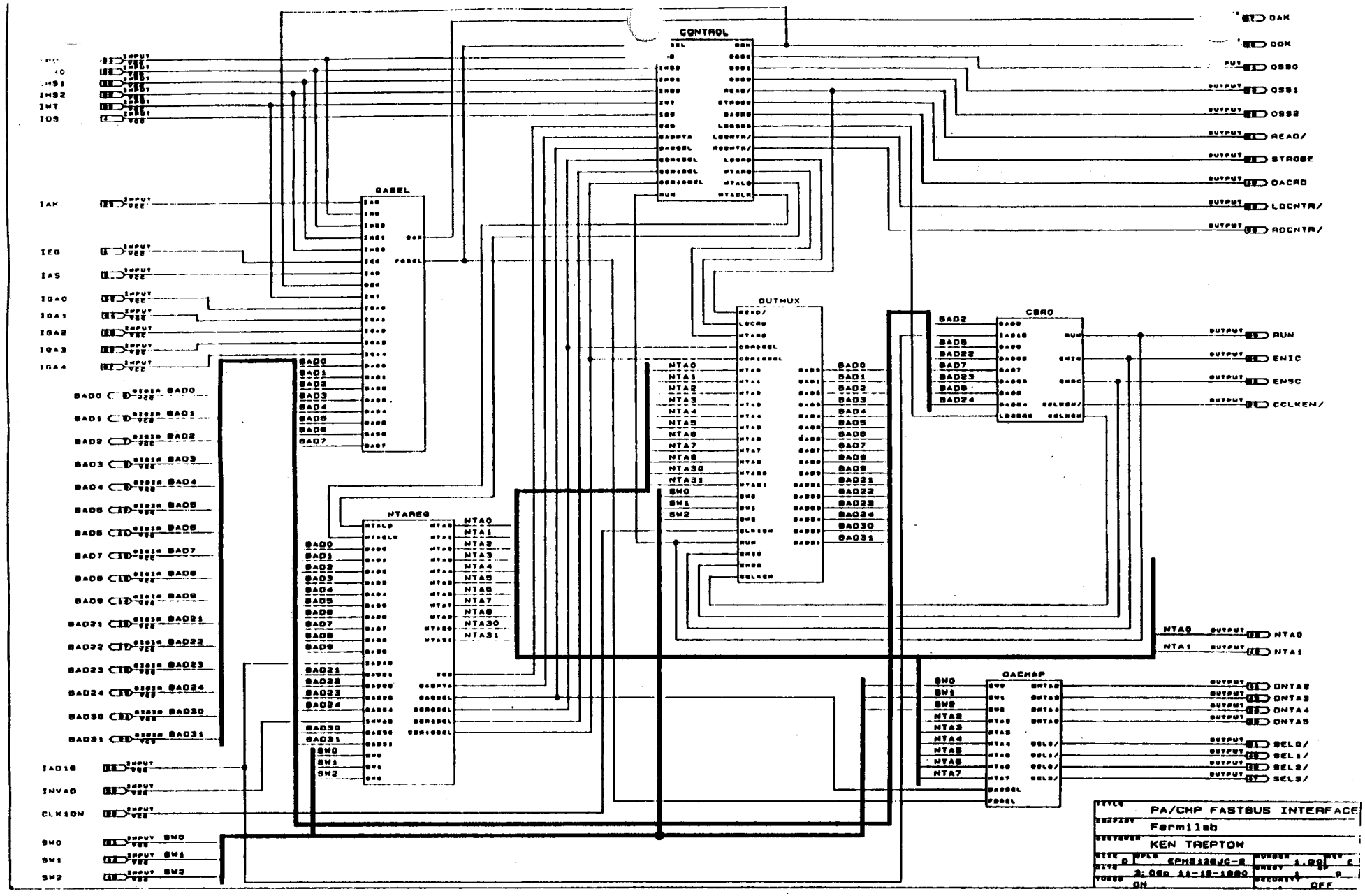
				Expanders		Fan-In		
٦	MCell	LAB	Primitive	Total	Shared	INP	FBK	Name
5	(2)	(A)	INPUT	0	0	0	0	BAD0
6	(3)	(A)	INPUT	0	0	0	0	BAD1
7	(4)	(A)	INPUT	0	0	0	0	BAD2
8	(5)	(A)	INPUT	0	0	0	0	BAD3
9	(6)	(A)	INPUT	0	0	0	0	BAD4
10	(7)	(A)	INPUT	0	0	0	0	BAD5
11	(8)	(A)	INPUT	0	0	0	0	BAD6
12	(17)	(B)	INPUT	0	0	0	0	BAD7
13	(18)	(B)	INPUT	0	0	0	0	BAD8
14	(19)	(B)	INPUT	0	0	0	0	BAD9
15	(20)	(B)	INPUT	0	0	0	0	BAD21
17	(21)	(B)	INPUT	0	0	0	0	BAD22
18	(33)	(C)	INPUT	0	0	0	0	BAD23
19	(34)	(C)	INPUT	0	0	0	0	BAD24
21	(35)	(C)	INPUT	0	0	0	0	BAD30
22	(36)	(C)	INPUT	0	0	0	0	BAD31
30	(55)	(D)	INPUT	0	0	0	0	CLK1ON
28	(53)	(D)	INPUT	0	0	0	0	IAD18
32	-	-	INPUT	0	0	0	0	IAK
2	-	-	INPUT	0	0	0	0	IAS
4	(1)	(A)	INPUT	0	0	0	0	IDS
1	-	-	INPUT	0	0	0	0	IEG
23	(37)	(C)	INPUT	0	0	0	0	IGA0
24	(49)	(D)	INPUT	0	0	0	0	IGA1
25	(50)	(D)	INPUT	0	0	0	0	IGA2
6	(51)	(D)	INPUT	0	0	0	0	IGA3
27	(52)	(D)	INPUT	0	0	0	0	IGA4
35	-	-	INPUT	0	0	0	0	IMS0
36	-	-	INPUT	0	0	0	0	IMS1
66	-	-	INPUT	0	0	0	0	IMS2
29	(54)	(D)	INPUT	0	0	0	0	INVAD
34	-	-	INPUT	0	0	0	0	IRD
68	-	-	INPUT	0	0	0	0	IWT
31	(56)	(D)	INPUT	0	0	0	0	SW0
44	(71)	(E)	INPUT	0	0	0	0	SW1
45	(72)	(E)	INPUT	0	0	0	0	SW2

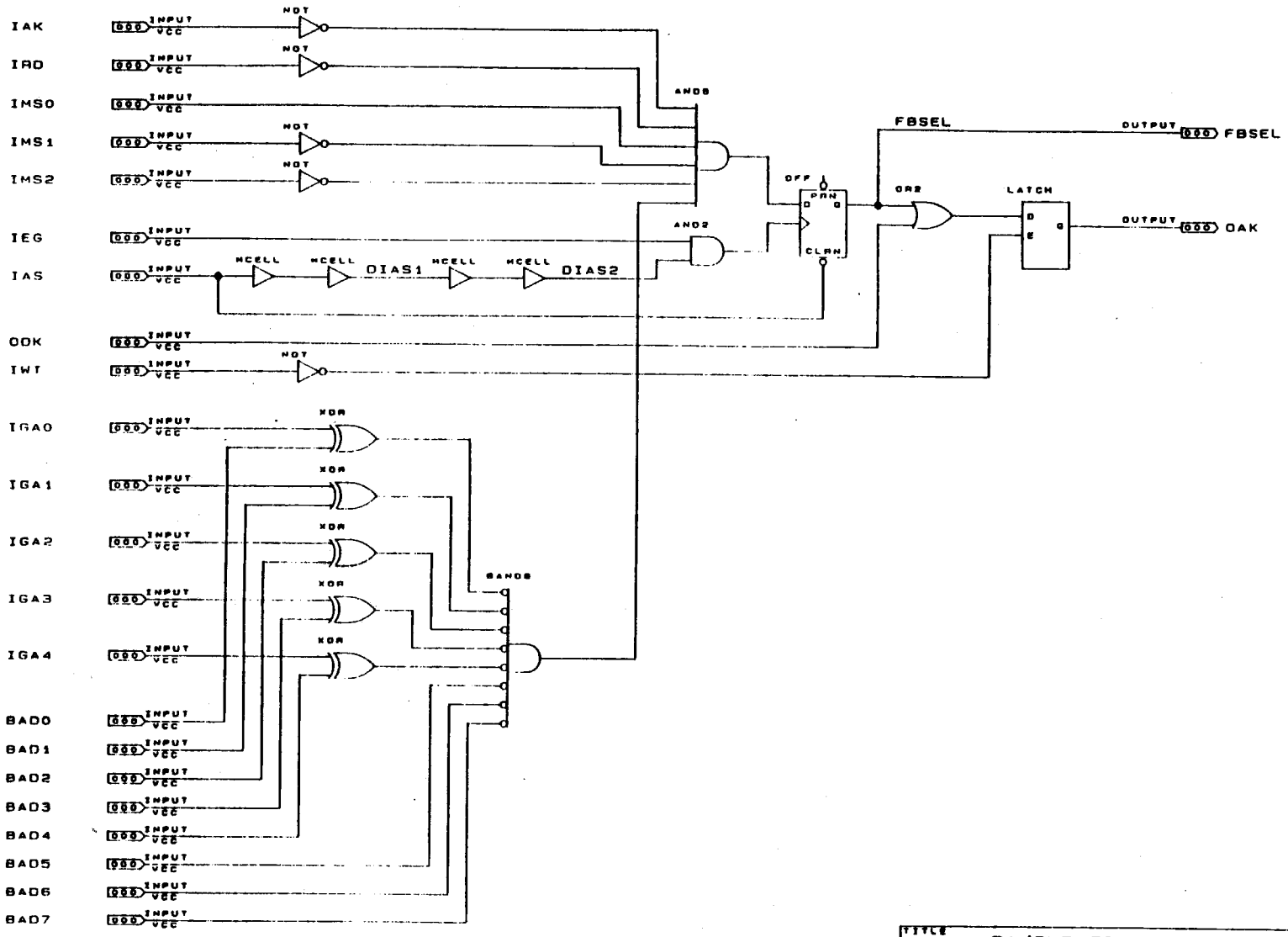
** OUTPUTS **

Pin	MCell	LAB	Primitive	Expanders Total	Expanders Shared	Fan-In INP	Fan-In FBK	Name
5	2	A	OR4	11	11	7	14	BAD0
6	3	A	OR4	11	11	7	14	BAD1
7	4	A	OR4	11	11	7	15	BAD2
8	5	A	OR4	11	11	7	14	BAD3
9	6	A	OR4	11	11	7	15	BAD4
10	7	A	OR4	11	11	7	14	BAD5
11	8	A	OR4	11	11	7	15	BAD6
12	17	B	OR4	11	11	4	15	BAD7
13	18	B	OR4	1	1	4	6	BAD8
14	19	B	OR4	1	1	5	4	BAD9
15	20	B	OR4	1	1	4	4	BAD21
17	21	B	OR4	1	1	4	2	BAD22
18	33	C	OR4	1	1	4	4	BAD23
19	34	C	OR4	1	1	4	4	BAD24
21	35	C	OR4	1	1	4	5	BAD30
22	36	C	OR4	1	1	4	5	BAD31
52	97	G	MCELL	0	0	0	1	CCLKEN/
46	81	F	OUTPUT	0	0	4	7	DACRD
41	68	E	OUTPUT	0	0	3	1	DNTA2
40	67	E	OUTPUT	0	0	3	2	DNTA3
39	66	E	OUTPUT	0	0	3	3	DNTA4
38	65	E	OUTPUT	5	0	3	4	DNTA5
55	99	G	DFF	3	3	6	15	ENIC
53	98	G	DFF	3	3	6	15	ENSC
59	114	H	OUTPUT	0	0	4	15	LDCNTR/
3	70	E	DFF	0	0	1	3	NTA0
2	69	E	DFF	0	0	1	4	NTA1
57	101	G	LATCH	0	0	1	2	OAK
65	120	H	LATCH	0	0	1	2	ODK
64	119	H	OUTPUT	0	0	3	3	OSS0
63	118	H	OUTPUT	8	7	4	11	OSS1
62	117	H	OUTPUT	7	7	4	10	OSS2
58	113	H	OUTPUT	0	0	3	13	RDCNTR/
61	116	H	OUTPUT	0	0	4	2	READ/
56	100	G	DFF	3	3	6	15	RUN
51	85	F	OUTPUT	5	0	3	11	SEL0/
49	84	F	OUTPUT	3	0	3	11	SEL1/
48	83	F	OUTPUT	4	0	3	11	SEL2/
47	82	F	OUTPUT	3	0	3	11	SEL3/
60	115	H	OUTPUT	0	0	3	10	STROBE

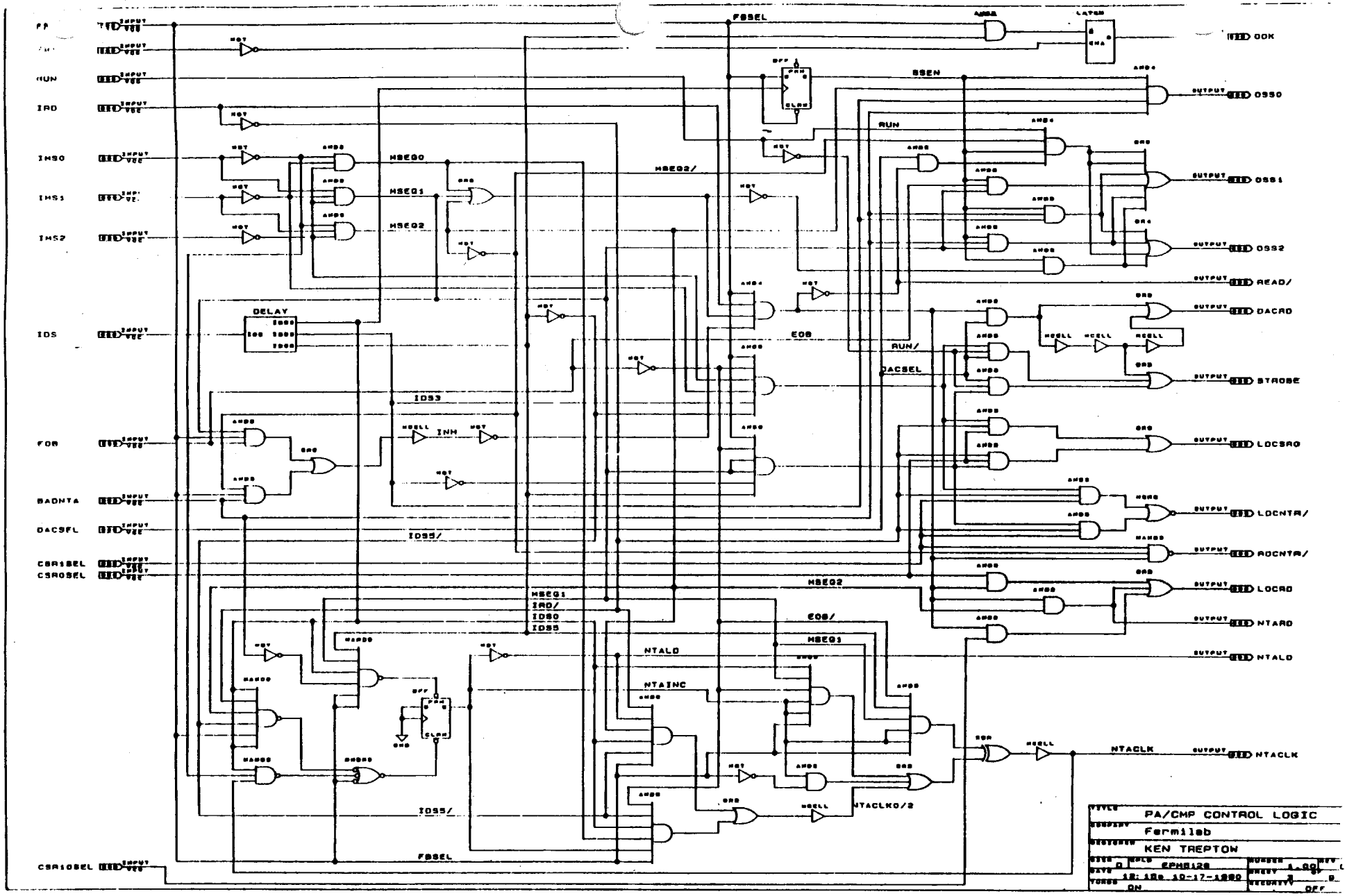
** BURIED LOGIC **

ı	MCell	LAB	Primitive	Expanders Total	Expanders Shared	Fan-In INP	Fan-In FBK	Name
-	64	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS0
-	63	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS1
-	62	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS2
-	61	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS3
-	60	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS4
-	80	E	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS5
-	57	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:34
(27)	52	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:37
-	59	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:38
-	58	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:39
(31)	56	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:41
(30)	55	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:42
-	79	E	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:43
(29)	54	D	MCELL	0	0	1	0	¦CONTROL:45¦DELAY:165¦:46
(26)	51	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:49
(25)	50	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:50
-	128	H	MCELL	0	0	3	3	¦CONTROL:45¦INH
-	78	E	MCELL	0	0	3	6	¦CONTROL:45¦NTACLK
-	77	E	MCELL	0	0	4	5	¦CONTROL:45¦NTACLK0/2
-	76	E	DFF	3	0	4	5	¦CONTROL:45¦NTAINC
-	96	F	DFF	0	0	0	2	¦CONTROL:45¦SSEN
-	16	A	MCELL	0	0	4	6	¦CONTROL:45¦:187
-	15	A	MCELL	0	0	0	1	¦CONTROL:45¦:188
-	14	A	MCELL	0	0	0	1	¦CONTROL:45¦:189
-	127	H	DFF	3	3	6	15	¦CSR0:49¦CCLKEN
-	13	A	MCELL	0	0	0	1	¦GASEL:46¦DIAS1
-	112	G	MCELL	0	0	0	1	¦GASEL:46¦DIAS2
-	75	E	DFF	7	0	20	1	¦GASEL:46¦FBSEL
-	12	A	MCELL	0	0	1	0	¦GASEL:46¦:21
-	111	G	MCELL	0	0	0	1	¦GASEL:46¦:51
-	126	H	MCELL	0	0	0	12	¦NTAREG:48¦BADNTA
-	31	B	DFF	0	0	1	5	¦NTAREG:48¦CT8:93¦Q2
-	74	E	DFF	0	0	1	6	¦NTAREG:48¦CT8:93¦Q3
-	73	E	DFF	0	0	1	7	¦NTAREG:48¦CT8:93¦Q4
(45)	72	E	DFF	0	0	1	8	¦NTAREG:48¦CT8:93¦Q5
(44)	71	E	DFF	0	0	1	9	¦NTAREG:48¦CT8:93¦Q6
-	125	H	DFF	0	0	1	10	¦NTAREG:48¦CT8:93¦Q7
-	11	A	SOFT	7	0	3	6	¦NTAREG:48¦DACSEL:108¦:52
-	10	A	SOFT	7	0	3	8	¦NTAREG:48¦DACSEL:108¦:53
-	124	H	MCELL	0	0	0	13	¦NTAREG:48¦EN/
-	123	H	DFF	1	0	0	15	¦NTAREG:48¦EOB
(28)	53	D	DFF	0	0	8	2	¦NTAREG:48¦NTA8
-	122	H	DFF	0	0	1	2	¦NTAREG:48¦NTA30
-	121	H	DFF	0	0	1	2	¦NTAREG:48¦NTA31
-	9	A	SOFT	2	0	4	13	¦OUTMUX:50¦:90
-	32	B	SOFT	0	0	4	12	¦OUTMUX:50¦:91

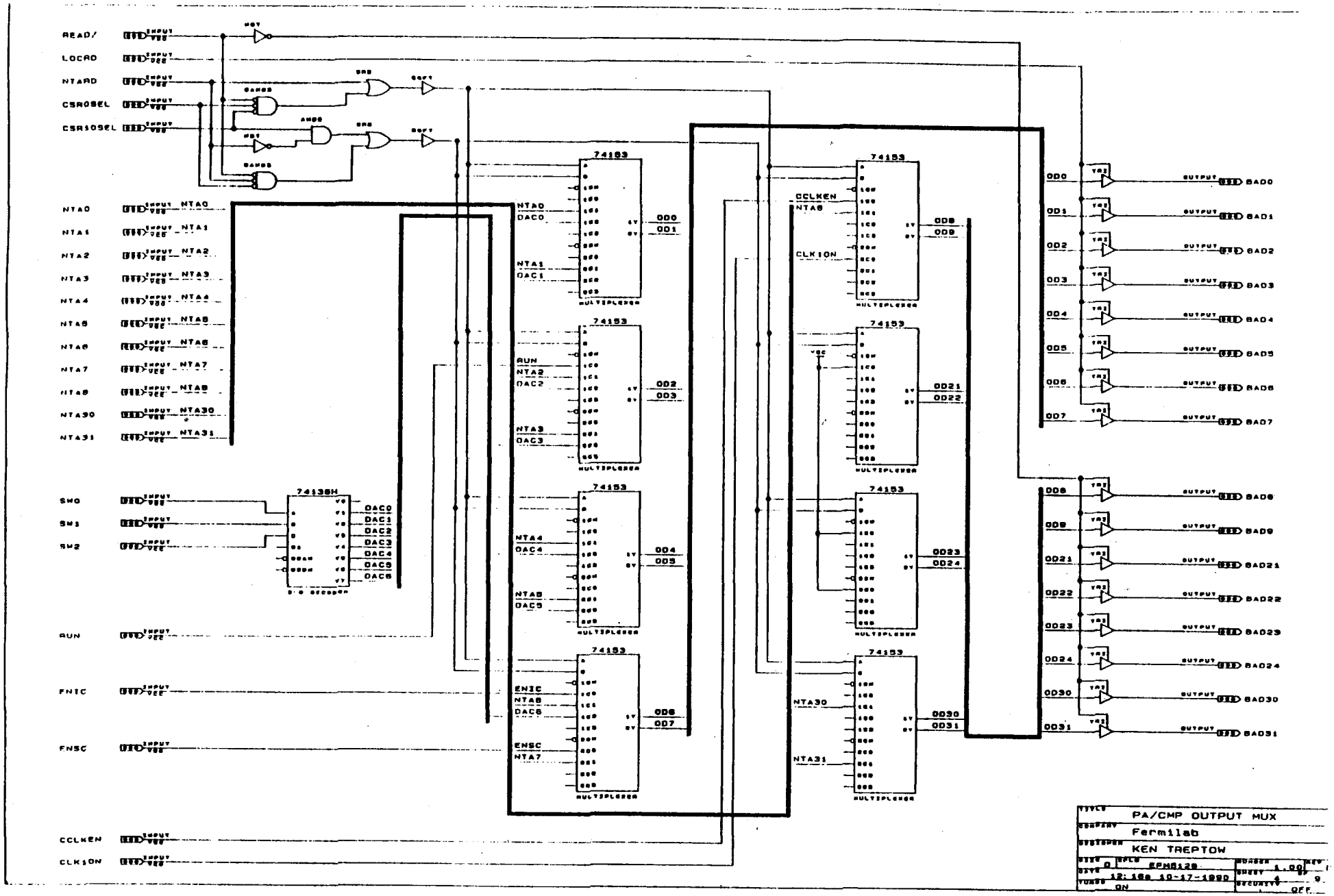

CONTROL
GASEL
OUTMUX
CSRO
NTAREG
DACMAP
IMS1
IMS2
IMT
IOS
IAK
IEG
IAS
IGA0
IGA1
IGA2
IGA3
IGA4
BAD0
BAD1
BAD2
BAD3
BAD4
BAD5
BAD6
BAD7
BAD8
BAD9
BAD21
BAD22
BAD23
BAD24
BAD30
BAD31
IAD18
INVAD
CLK10N
SW0
SW1
SW2
OAK
OOK
OSS0
OSS1
OSS2
READ/
STROBE
DACRD
LDCNTR/
RDCNTR/
RUN
ENIC
ENSC
CCLKEN/
NTA0
NTA1
DNTA2
DNTA3
DNTA4
DNTA5
SEL0/
SEL1/
SEL2/
SEL3/
TITLE PA/CMP FASTBUS INTERFACE
COMPANY Fermilab
DESIGNER KEN TREPTOW
SIZE D
EPM5128JC-2
NUMBER 1.00
REV E
DATE 3:08p 11-15-1980
SHEET 1 OF 9
TUNED ON
SECURITY OFF

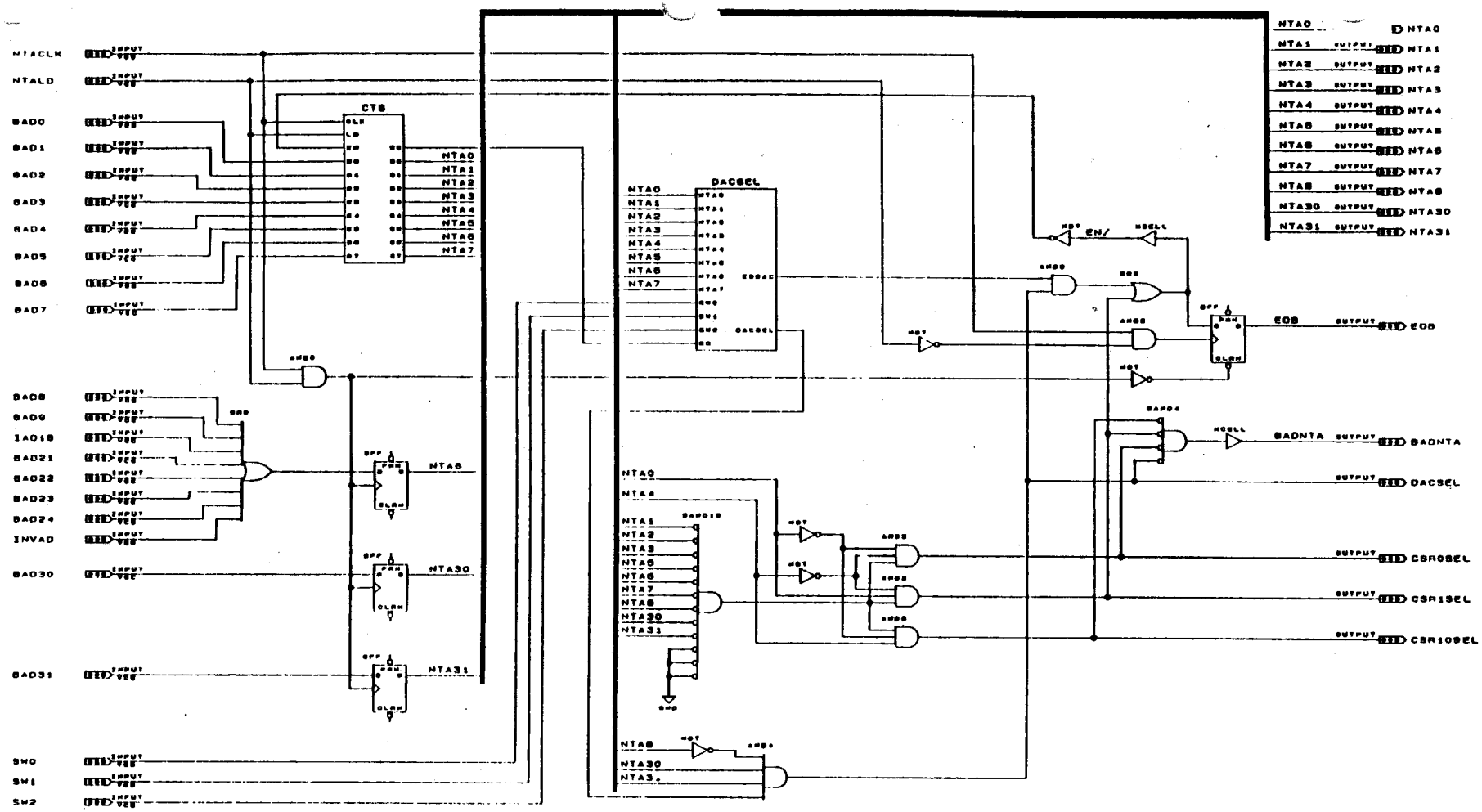


TITLE	PA/CMP FB GA SEL LOGIC
COMPANY	FERMILAB
DESIGNER	KEN TREPTOW
SIZE C	EPLD EPM5128
NUMBER 1.00	REV B
DATE 6/11/90	SHEET 2 OF 9
TURBO ON	SECURITY OFF



RUN
IRD
IMS0
IMS1
IMS2
IDS
EOB
BADNTA
DACSEL
CSR1SEL
CSR0SEL
CSR10SEL
DELAY
IDS3
INH
IDS5/
MSEQ0
MSEQ1
MSEQ2
MSEQ2/
FBSEL
SSEN
RUN
EOB
RUN/
DACSEL
MSEQ2
EOB/
MSEQ1
NTALD
NTAINC
NTACLK0/2
NTACLK
OOK
OSS0
OSS1
OSS2
READ/
DACRD
STROBE
LDCSRQ
LDCNTR/
RDCNTR/
LDCRD
NTARD
NTALD
NTACLK
PA/CMP CONTROL LOGIC
Fermilab
KEN TREPTON
EPM5128
12:15a 10-17-1990
ON
OFF


READ/
LOCRD
NTARD
CSR0SEL
CSR10SEL
NTA0
NTA1
NTA2
NTA3
NTA4
NTA5
NTA6
NTA7
NTA8
NTA30
NTA31
SW0
SW1
SW2
RUN
FNIC
FNSC
CCLKEN
CLK10N
74138H
74153
MULTIPLEXER
OD0
OD1
OD2
OD3
OD4
OD5
OD6
OD7
OD8
OD9
OD21
OD22
OD23
OD24
OD30
OD31
BAD0
BAD1
BAD2
BAD3
BAD4
BAD5
BAD6
BAD7
BAD8
BAD9
BAD21
BAD22
BAD23
BAD24
BAD30
BAD31
PA/CMP OUTPUT MUX
Fermilab
KEN TREPTOW
EPM5128
12:16a 10-17-1990
ON
OFF



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COMPANY	Fermilab
DESIGNER	KEN TREPTOW
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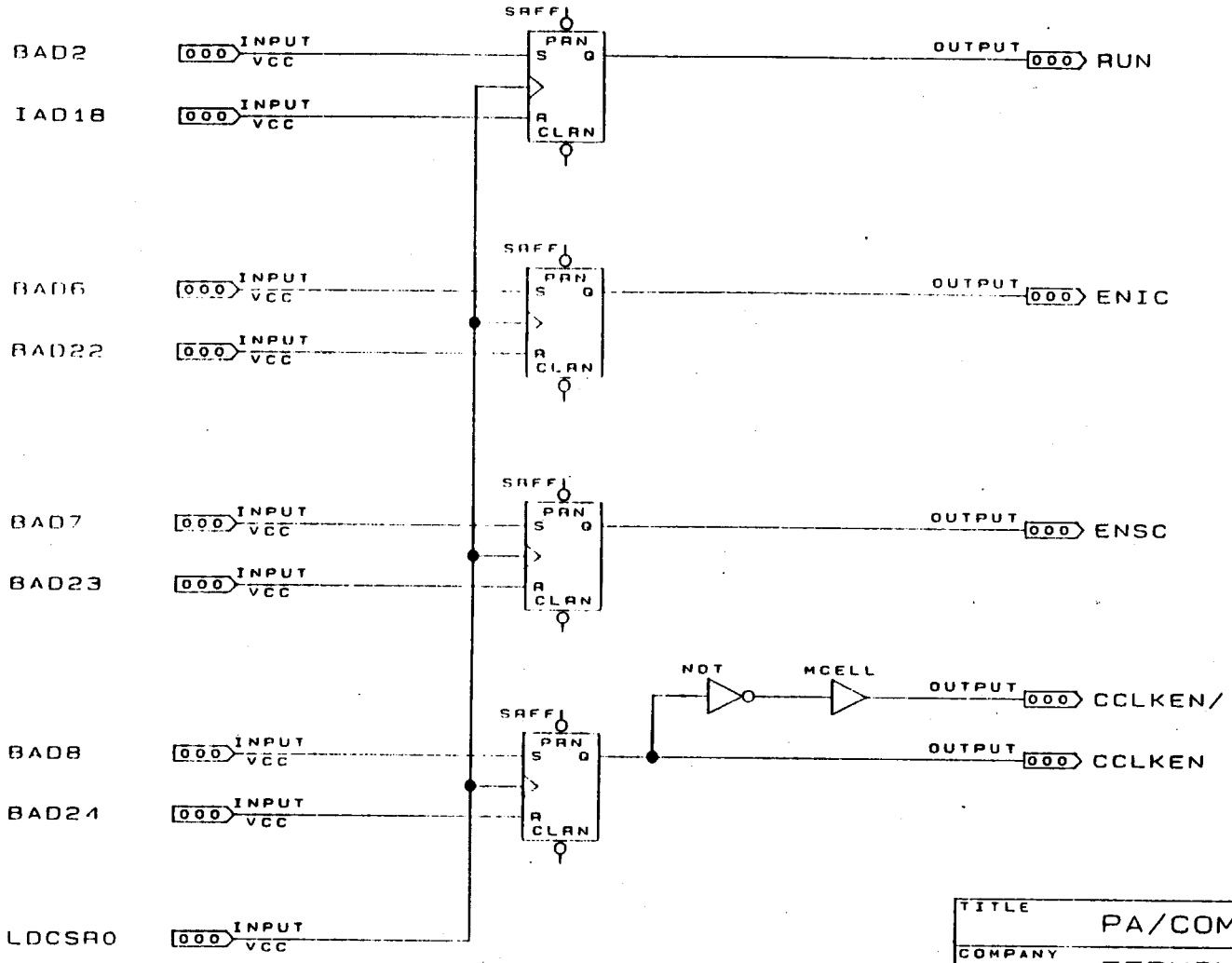
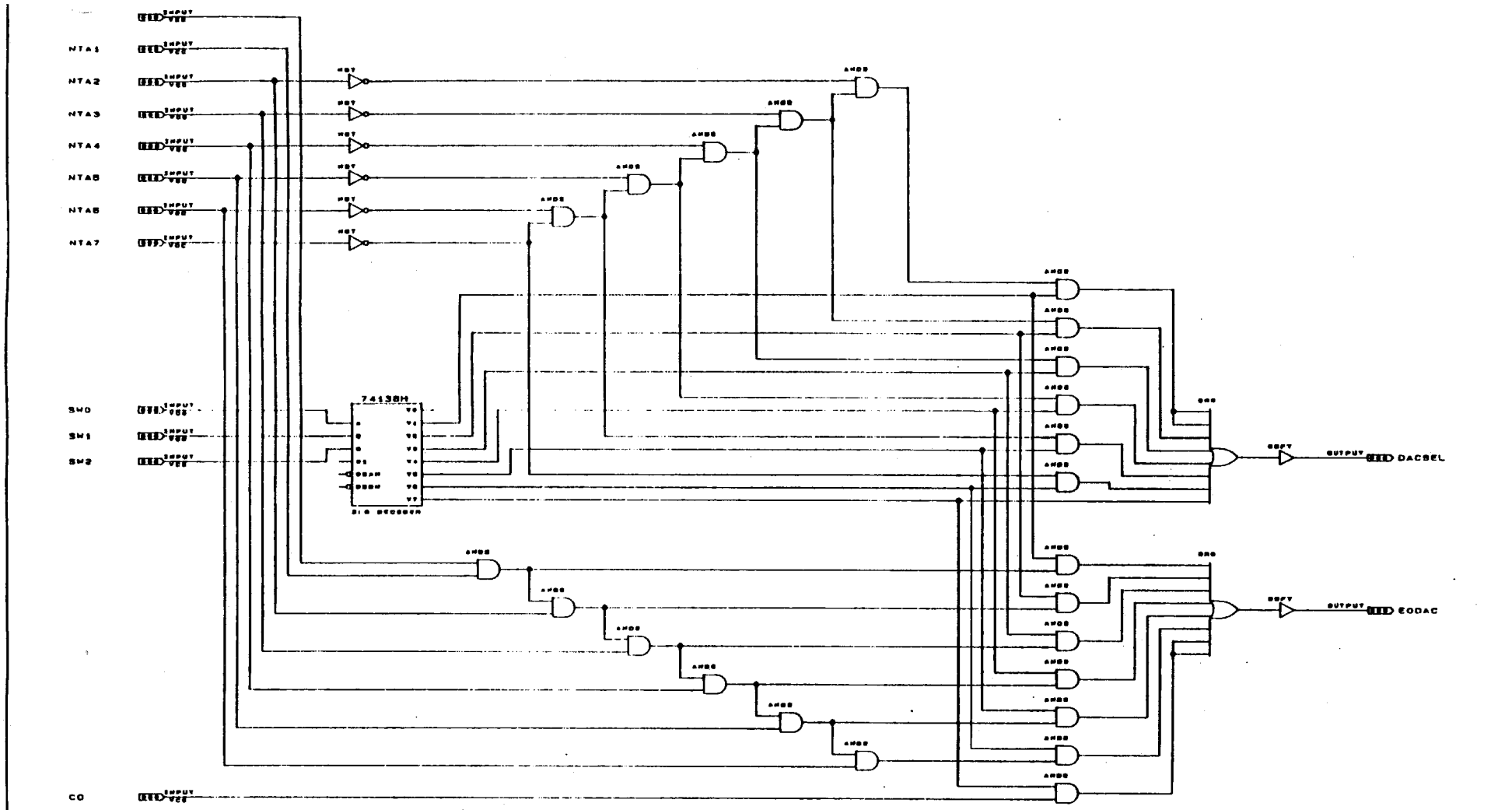
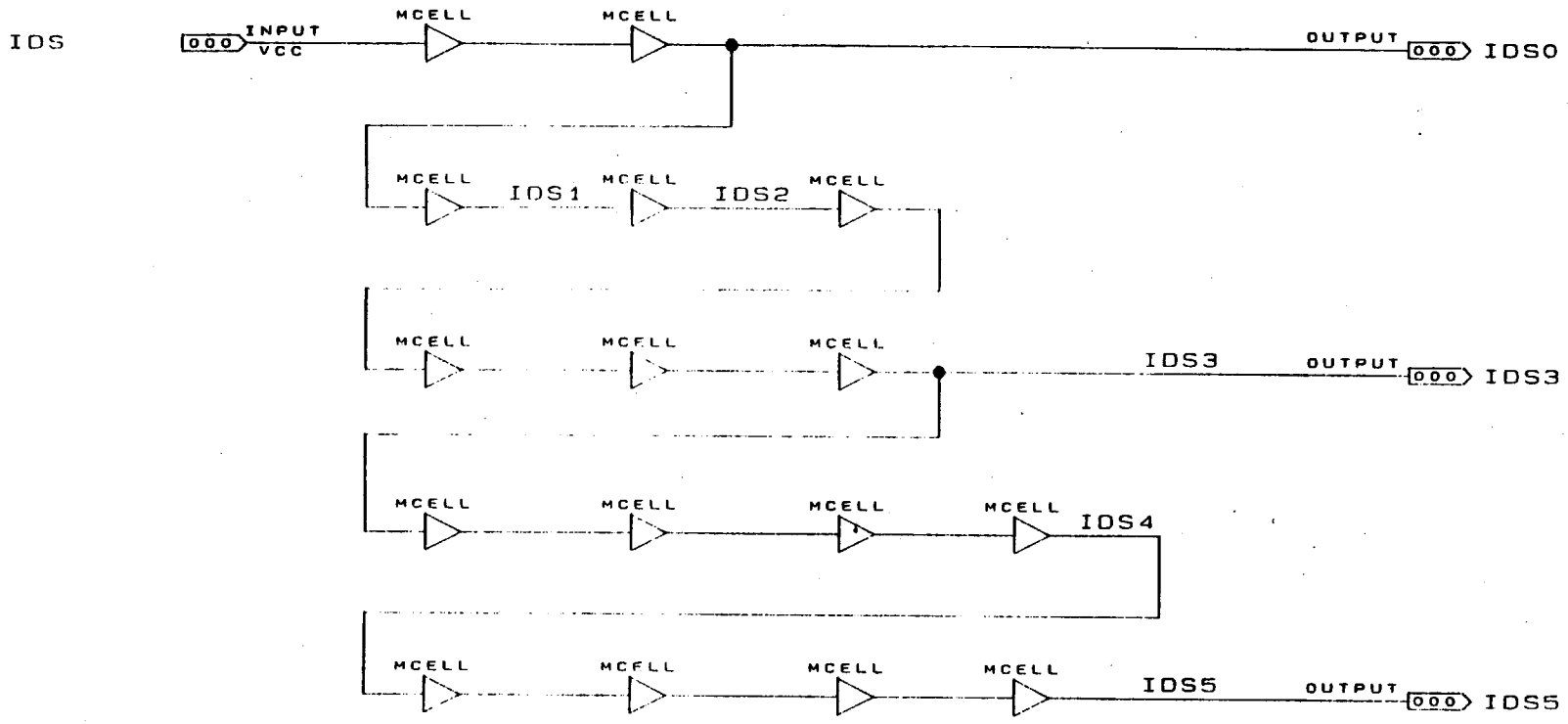
NUMBER	1.00
SHEET	8 OF 8
SECURITY	OFF



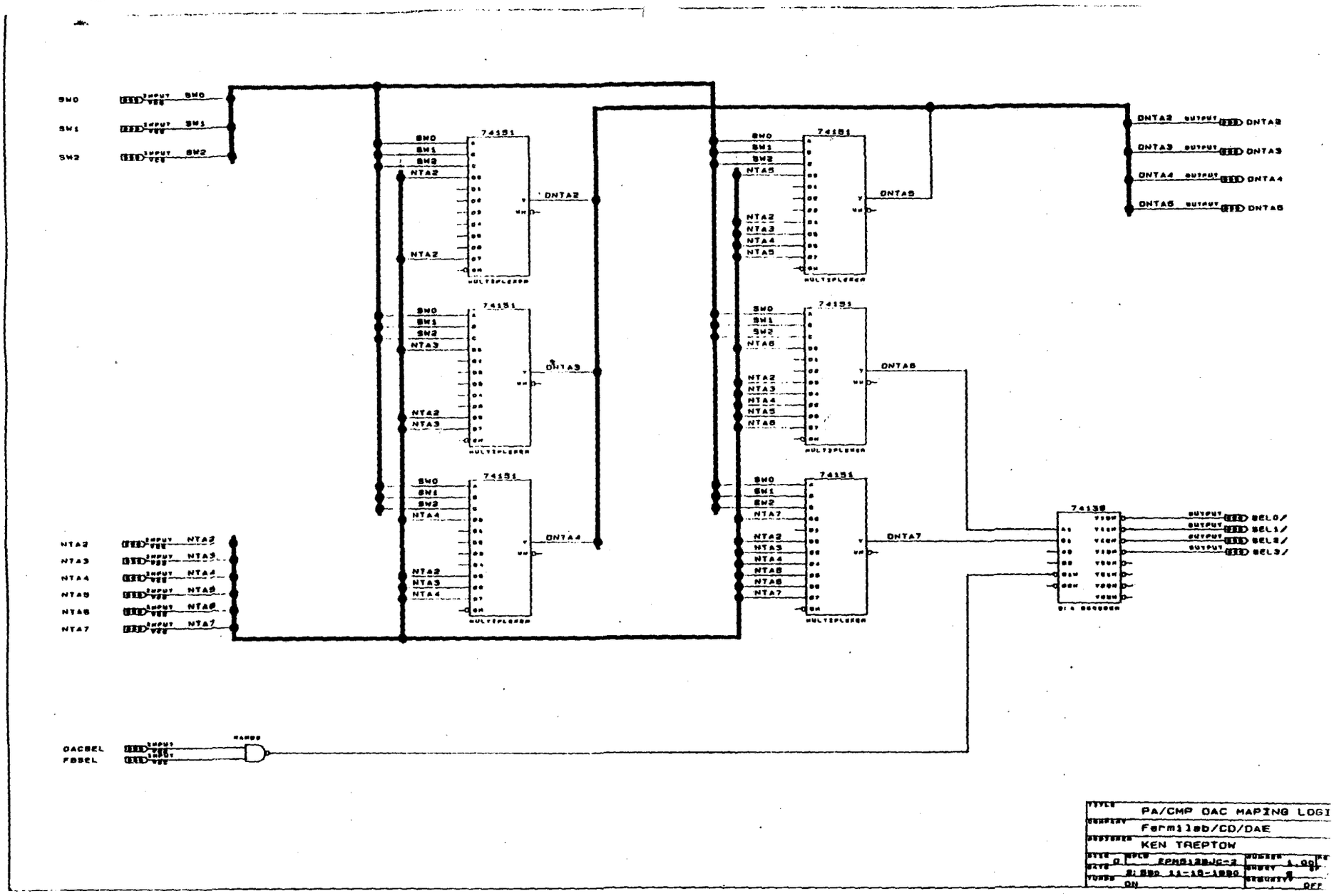
TITLE	PA/COMP CSR0		
COMPANY	FERMILAB/CD/DAE		
DESIGNER	KEN TREPTOW		
SIZE B	EPLD EPM5128	NUMBER 1.00	REV B
DATE 6/26/90		SHEET 6 OF 9	
TURBO ON		SECURITY OFF	



TITLE	PA/CMP DAC ADDR DECODE
COMPANY	Fermilab
DESIGNER	KEN TREPTOW
SIZE D	DPLD EPM5128
DATE	12:17a 10-17-1990
TURBO	ON
NUMBER	1.00 REV A
SHEET 7 OF 9	
SECURITY	OFF



TITLE	PA/CMP DS DELAYS		
COMPANY	Fermilab		
DESIGNER	KEN TREPTOW		
SIZE B	EPLD EPM5128	NUMBER 1.00	REV A
DATE 10:22a 11-13-1990		SHEET 8 OF 9	
TURBO ON		SECURITY OFF	


SW0
SW1
SW2
NTA2
NTA3
NTA4
NTA5
NTA6
NTA7
DACSEL
FBSEL
74151
74139
DNTA2
DNTA3
DNTA4
DNTA5
DNTA6
DNTA7
SEL0/
SEL1/
SEL2/
SEL3/
PA/CMP DAC MAPING LOGI
Fermilab/CD/DAE
KEN TREPTOW
ON
OFF

3.5 HARDWARE JUMPERS

3.5.1 DAC/ADC Jumpers

The illustration is an abbreviated pattern of the IC-03 DAC/ADC jumpering scheme which exists on the P/C Module.

There are 256 DACs which are addressed via CSR addresses C000_0000 through C000_00FF inclusive. DAC address 00 (Hex), will always set the threshold voltage on the uppermost trace which is the threshold for the discriminator connected to the output of the summed channel which takes the sum of channel -1 and channel 0 (Σ-1,0). Likewise DAC address 01 (Hex), will always set the threshold voltage on the trace immediately below the uppermost trace which is the threshold for the discriminator connected directly to the individual channel #0 input. DAC address 02 (Hex), will always set the threshold voltage for the discriminator connected to the output of the summed channel which takes the sum of channel 0 and channel 1 (Σ0,1). DAC address 03 (Hex), will always set the threshold voltage for the discriminator connected directly to the individual channel #1 input. This pattern continues for the 256 DACs and the 256 discriminator threshold setting inputs.

It should be obvious that if all 256 DAC's are employed, no jumpers are required and each discriminator has an individual DAC to control it's threshold. However, in the event that only 4 of the 256 DAC's are mounted on the P/C Module, the jumpers would probably be applied such that DAC 00 (hex) would drive every other sum channel. i.e., Σ(0), Σ(1,2), Σ(3,4), Σ(5,6) etc. DAC 01 (hex) would drive the even individual channels; DAC 02 (hex) would drive sum channels Σ(0,1), Σ(2,3), Σ(4,5), Σ(6,7) etc., and DAC 03 (hex) would drive the odd, individual channels.

The common choices of DAC populations are 4,8,16,32,64,128 or 256 which corresponds to 1,2,4,8,16,32 and 64 IC-03 packages. It seems reasonable to assume that for four DAC's every fourth threshold lead would be connected together and so on. However, any and all possibilities exist for connecting DAC outputs to threshold inputs and the method used may be dictated by the detector geometry.

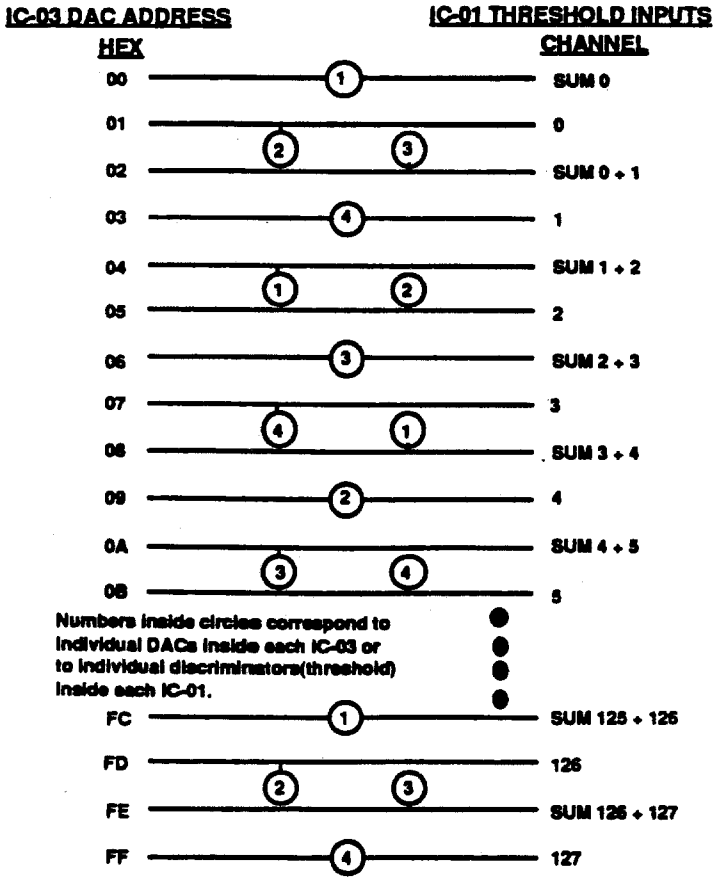


Figure 21: DAC/ADC Jumpering

3.5.2 CSR10 Jumpers

The value found in CSR10 corresponds to the configuration of three, two position jumpers(JU2, JU3, and JU4) that connect a signal trace to ground(GND) or +5V. The physical module location of the three posts for each jumper, and their connections are shown below. Table 1 on the following page provides the relationship between DAC population, jumper location, CSR10 readback and lowest ordered address for each DAC chip.
When less than 256 DAC's are utilized, the P/C module will be populated from the lowest address onward without skipping addresses, this is done by a mapping routine within the EPM5128 programmable PAL. It has been done this way to make the DACs accessible by block transfer. The PAL receives a 3 bit code from the jumpers to indicate the number of IC-03 DAC/ADC chips mounted and coverts the sequential DAC address it receives from an external source to the appropriate DAC module address. I.E. if only two IC-03s(8 DACs) are used and located at DAC board address 0 through 3(U97) and DAC board address 64 through 67(U129), the PAL knowing from the jumpering scheme will only accept DAC addresses 0 through 7 from an external source and in turn converts external address 0 to DAC board address 0 and so on up to external address 7 to DAC board address 67. When less than 256 DACs are employed the IC-03s physical location is important to insure that the external address received is converted to the appropriate DAC board address. The physical locations for the common number of IC-03s used are shown in Table 2 on the following page.

CSR10 JUMPERING DIAGRAM

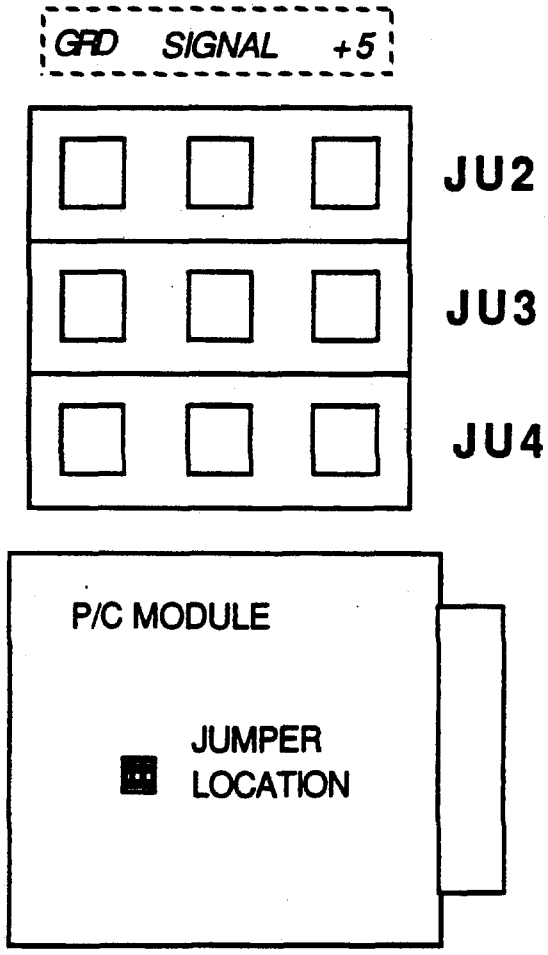


Figure 22: CSR10 Jumpering

Table 1

Jumper Numbers			# of DACs	CSR10 Value	First DAC board address of each IC-03
JU2	JU3	JU4			
Gnd	Gnd	Gnd	????	0	This is a special case, unique to the user.
Gnd	Gnd	+5V	4	1	0
Gnd	+5V	Gnd	8	2	0,80
Gnd	+5V	+5V	16	4	0,40,80,C0
+5V	Gnd	Gnd	32	8	0,20,40,60,80,A0,C0,E0
+5V	Gnd	+5 V	64	10	0,10,20,30,40,50,60,70,80,90,A0,B0,C0,D0,E0,F0
+5V	+5V	Gnd	128	20	0,8,10,18,20,28,30,38,40,48,50,58,60,68,70,7880,88,90,98,A0,A8,B0,B8,C0,C8,D0,D8,E0,E8, F0,F8
+5V	+5V	+5V	256	40	All addresses from 00 through FF inclusive are valid

Table 2

Number of IC-03s mounted(#DACs)	IC-03 Physical location on module
1(4)	U97
2(8)	U97, U129
4(16)	U97, U113, U129, U145
8(32)	U97, U105, U113, U121, U129, U137, U145, U153
16(64)	U97, U101, U105, U109, U113, U117, U121, U125, U129, U133, U137, U141, U145, U149, U153, U157
32(128)	U97, U99, U101, U103, U105, U107, U109, U111, U113, U115, U117, U119, U121, U123, U125, U127, U129, U131, U133, U135, U137, U139, U141, U143, U145, U147, U149, U151, U153, U155, U157, U159
64(256)	ALL LOCATIONS

4.0 P/C MODULE - TESTING AND CALIBRATION

4.1 UNPOWERED TEST

A test should be performed to check for shorts between the power planes (layers) of the P/C module. The test should verify no direct connection between any of the following power planes: -5.2V, -3.5V, -2V, -.8V top, -.8V bottom, +5V, +3.5V, +1.25V, and ground. The test can be done with an OHM METER. Connection to the power plane can be found at the following locations, with the measured impedances between the power and ground plane with the PC board fully assembled(number of IC-03s equals four).

-5.2V = right side of D5	= 8 ohm
-3.5V = right side of fuse f4	= 3 ohm
-2V = right side of fuse f1	= 22 ohm
-.8V top = right side of CR2	= 23 ohm
-.8V bottom = right side of CR4	= 23 ohm
+5V = right side of fuse f6	= 400 ohm(90 ohm with EPM5128 installed)
153 = right side of fuse f2	= 580 ohm
+1.25V = case of Q1	= 73 ohm
GROUND = left side of D5	

NOTE: Right side is towards the front of the board where the LABEL is located. The drawing "POWER TEST POINT DETAILS"#2563.000-MD-215808 shows the power pin locations of various devices on the top side of the board, this should help in finding shorts.

4.2 AUTOMATED TESTING

Their is an "Acceptance Test Description" document that uses two software packages to verify wether a P/C module is acceptable from an outside vendor. This document can be found in APPENDIX A.

4.3 CALIBRATION

Adjusting the value at which the ***TEMP*** LED on the front panel of the P/C module will turn on is the only calibration needed for the module. Adjusting trim pot R295 sets the temperature at which the LED will turn on and off, the setting of R295 controls the voltage on pin 2 of U185. If pin 3 of U185 which is connected to the LM35 temperature sensor is at a more positive value than pin 2 of U185 the LED will turn on. The voltage on pin 2 should be set to 0.5V this corresponds to 50 degrees Celsius. The LM35 will output to pin 3 of the U185 a 10 mV per degree Celsius voltage level. If the temperature rises above 50 degrees Celsius(0.5V on pin 3) the LED will turn on. The LED will turn off if the temperature falls below 50 degrees Celsius. The ***TEMP*** LED and associated circuitry can be tested by adjusting R295 for a voltage on pin 2 of U185 that is less than the value on pin 3 of U185, the lower voltage should cause the ***TEMP*** LED to turn on.

5.0 APPENDICES

APPENDIX A - TEST SOFTWARE
APPENDIX B - FASTBUS INTERFACE PAL PROGRAM
APPENDIX C - POSTAMP/COMPARATOR MODULE - SCHEMATIC
APPENDIX D - MODULE DRAWINGS
APPENDIX E - DATA SHEETS

APPENDIX A - TEST SOFTWARE

This appendix contains an acceptance criteria specification that pertains to the testing of the POSTAMP/COMPARATOR printed circuit board.

POSTAMP/COMPARATOR MODULE - ACCEPTANCE TEST DESCRIPTION

The party performing the acceptance test on the POSTAMP/COMPARATOR module should be familiar with the "IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control system"(ANSI/IEEE Std. 960-1986), the POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100, and the two software packages listed below which the acceptance criteria is based upon. Questions pertaining to the documents should be addressed to the appropriate originator.

SILICON STRIP DETECTOR (SSD)
System Test Software Guide
Version: 0 15 march 1991

Originators:
Wolfgang Kowald Duke University
EXP.771 #708-840-4250
Panagiotis Spentzouris UCA
EXP.771 #708-840-4250
Dave Slimmer Fermilab
Computing Dept. #708-840-4334

SILICON STRIP DETECTOR SYSTEM "SINGLE BOARD DIAGNOSTICS TESTS"-PN434
Software Description
Version: 1 4/25/91

Originator:
Garry R. Moore Fermilab
Computing Dept. #708-840-4059

POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100
Complete Module Documentation Manual
Version: 3 5/7/91

Originators:
Merle Haldeman Fermilab
RD/DEG group #708-840-3958
Scott Holm Fermilab
RD/DEG group #708-840-4340
Bruce Merkel Fermilab
RD/DEG group #708-840-3263

In order for the PC module to be accepted, the PC module must pass the following four tests.

1. PC_TEST

Refer to the "SINGLE BOARD DIAGNOSTICS TESTS" documentation listed above.

PC_TEST is a menu driven software tool capable of effectively testing and/or exercising all FASTBUS accessible circuitry of the POSTAMP/COMPARATOR module. The test should be run in the "Exercise Postamp Comparator" mode; this is #3 under the PC_TEST main menu. This option will fully exercise all FASTBUS accessible circuitry of the PC module including all geographical address, secondary address, and DAC/ADC circuitry.

ACCEPTANCE- The software will respond with errors if the module responds incorrectly. The module is unacceptable when any errors are reported.

EXCEPTIONS: A part of the test writes and then reads a series of IC-03 DAC values, the software will respond with an error if the DAC value read back is more than plus or minus one LSB different than the written value. The module however, will be accepted when the DAC value read back is within two LSB's of the written value.

Refer to the "SILICON STRIP DETECTOR (SSD)" documentation listed on page 1 for the remaining three tests.

2. PC test counter test

This test uses an 8-bit counter on the PC module to generate 256 patterns used for testing the output portion(IC-02 and IC-04 ASIC's) of the PC module. The 8-bit counter cycles through 256 output pattern possibilities which are sent to the IC-02 and IC-04 test inputs; t1 and t2. The outputs of the IC-02s and IC-04s provide 256 different 128-bit patterns which are sent to the DE module through the FASTBUS auxiliary backplane. This test effectively tests the outputs of all IC-02 and IC-04 ASIC's as well as their connections to the backplane. The DE module has 256 memory locations which are continually being loaded with the 256 pattern possibilities. In this test an individual DE memory location is always being loaded with the same pattern generated by the PC module test counter.(Refer to section 5.4.2 PC test counter test and to APPENDIX A for test counter patterns).

ACCEPTANCE- The PC module is acceptable if no errors occur. The software will know in which memory location in the DE module each pattern generated by PC module's IC-02 and IC-04 ASICs are stored. When a memory location in the DE module is read by the software, the 128-bit pattern in that location is compared with the 128-bit pattern that was expected for that location. An error is reported if the values do not match.

3. PC channel characterization tests

This test characterizes individual and sum channel threshold voltage sensitivity for the PC module discriminator electronics. Characterizing a channel involves placing a test signal at a channel input and then scanning through the threshold setting DAC, value range with the software recording the highest threshold voltage(DAC value) at which the channel discriminator was able to detect the input test signal. The test should be performed in the default mode(DAC vs CHANNEL mode). In this mode, five separate routines need to be run on the module. These routines are listed in a menu that is displayed after "PC channel characterization test"(h) is selected from the System test menu. Invoking any one of the routines, automatically sets up the PC module for that

routine, i.e. turning on individual channel or sum channel mode, and placing the PC module in the RUN mode.

The first routine, "INDIVIDUAL CHANNEL", tests all individual channels of the PC module. The software performs in the following way: the TSM module's 256 word by 128 bit memory(refer to TSM document#) is loaded with a pattern of alternating words consisting of all A's and 5's, which means adjacent bits in a given word have opposite values as well as a given bit in adjacent memory addresses. The TSM module feeds this pattern to the LS module(refer to LS module documentation#)which continually places this pattern at the PC module input. The DE continuously updates its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. At the start, all DACs are set to the highest value in their range(1.25v) and at some instance the software performs 8 nonconsecutive reads of a DE memory location, recording which if any of the 128 channels were on(hit) during each of the 8 reads. The DAC value is then lowered 1 LSB(5mv) and the DE module memory is read 8 more times, this continues until the DACs are at their lowest value in their range(0mv). A graph is made that shows the DAC values at which a channel responded to 8 out of 8 reads with the channel on(hit) and also when the channel responds at least once but less than 8 out of 8 times.

The remaining four routines test the SUM channels. Each routine uses a different pattern such as 1's, 2's, 4's or 8's, i.e. for the 2's pattern every 2nd channel of a 4 channel combination will be toggling on and for the 8's pattern every 4th channel of a 4 channel combination will be toggling on. A graph is made for each routine. In the SUM channel mode when placing an input signal on one channel the adjacent channels also receive this input signal, therefor the adjacent channels should also turn on and the graphs should reflect this.(Refer to section 5.4.6 PC Channel Characterization Tests).

ACCEPTANCE- The input signal from the LS module should be set for a 40mv peak to peak differential amplitude. The PC module passes the test if the resulting graphs that are produced by the software are as follows. ***{SHOW GRAPHS}***The DAC values of all channels may vary no more than plus or minus 15 counts from the norm, i.e. if the norm is at the DAC value of 90, acceptable DAC values range from 75 to 105. A module is unacceptable if a channel is characterized outside of the plus or minus 15 count range.

4. PC Crosstalk Test

PC Crosstalk test will test the ability of the PC module to reject crosstalk to other channels from an input signal of substantial amplitude on a certain other channel. The Crosstalk test uses the TSM and LS modules as in the PC characterization test. In this test the TSM memory is loaded with a 1 in one of the 128 bits of the first word and the remaining 255 words have a 0 in all 128 bits. This means that 1 channel is being stimulated with a 18.9ns pulse every 4.8us. The TSM module feeds this pattern to the LS module which continuously places the pattern at the PC module input, meanwhile the DE is continuously updating its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. Initially, all DACs are set to the highest value in their range(1.25v). The software reads the DE memory location containing the channel that is on(hit), the 128-bit value read, should contain only the one bit that is on. More than one bit on indicates crosstalk. The DAC value is then lowered 1 LSB(5mv) and the DE memory is read again, this repeats until the DAC output is reduced to 150mv. The software then shifts the pattern in the TSM memory one bit so that the next channel is being stimulated with a large amplitude signal, the process of reading the DE memory and lowering the DAC values is repeated. The shifting continues until all 128 channels have been stimulated. Crosstalk is reported each time a nonstimulated channel is on. This procedure shows that channels not responding to the

signals on other channels have less than 3% crosstalk.(Refer to section 5.4.7 PC Crosstalk test).

ACCEPTANCE-The signal amplitude of the input should be set to 500mv peak to peak differential amplitude. The PC module is unacceptable if crosstalk is found on any channel.

SCOTT HOLM 5/8/91

APPENDIX B - FASTBUS INTERFACE PAL PROGRAM

This appendix contains the information on the programming of the EPM5128 PAL that is used for the FASTBUS interface on the POSTAMP/COMPARATOR printed circuit board.

E:\KEN\SSD\PACMP\REVE\PACMPI.RPT

MAX+PLUS Compiler Report File
Version 2.50 05/31/90

** Design compiled without errors

Title: PA/CMP FASTBUS INTERFACE
Company: Fermilab
Designer: KEN TREPTOW
Rev: E
Date: 3:06p 11-15-1990
Turbo: ON
Security: OFF

```
                                                                                  R
                 B  B  B  B  B                                  I     O  O  O  E
                 A  A  A  A  A  I  V  I  I  I  G  M  O  S  S  S  A
                 D  D  D  D  D  D  C  A  E  W  N  S  D  S  S  S  D
                 4  3  2  1  0  S  C  S  G  T  D  2  K  0  1  2  /
              ---------------------------------------------------------
            /   9  8  7  6  5  4  3  2  1 68 67 66 65 64 63 62 61   |
     BAD5 | 10                                                  60 | STROBE
     BAD6 | 11                                                  59 | LDCNTR/
     BAD7 | 12                                                  58 | RDCNTR/
     BAD8 | 13                                                  57 | OAK
     BAD9 | 14                                                  56 | RUN
    BAD21 | 15                                                  55 | ENIC
      GND | 16                                                  54 | VCC
    BAD22 | 17                                                  53 | ENSC
    BAD23 | 18                  EPM5128JC-2                     52 | CCLKEN/
    BAD24 | 19                                                  51 | SEL0/
      VCC | 20                                                  50 | GND
    BAD30 | 21                                                  49 | SEL1/
    BAD31 | 22                                                  48 | SEL2/
     IGA0 | 23                                                  47 | SEL3/
     IGA1 | 24                                                  46 | DACRD
     IGA2 | 25                                                  45 | SW2
     IGA3 | 26                                                  44 | SW1
          |_  27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43  _|
              ---------------------------------------------------------
                 I  I  I  C  S  I  G  I  I  I  V  D  D  D  D  N  N
                 G  A  N  L  W  A  N  R  M  M  C  N  N  N  N  T  T
                 A  D  V  K  0  K  D  D  S  S  C  T  T  T  T  A  A
                 4  1  A  1              0  1     A  A  A  A  1  0
                    8  D  O                     5  4  3  2
                          N
```

** RESOURCE USAGE **

ic Array Block	Macrocells	I/O Pins	Expanders	External Interconnect
A: MC1 - MC16	15/16(93%)	8/ 8(100%)	27/32(84%)	19/24(79%)
B: MC17 - MC32	7/16(43%)	5/ 5(100%)	11/32(34%)	19/24(79%)
C: MC33 - MC48	4/16(25%)	5/ 5(100%)	1/32(3%)	6/24(25%)
D: MC49 - MC64	15/16(93%)	8/ 8(100%)	0/32(0%)	11/24(45%)
E: MC65 - MC80	16/16(100%)	8/ 8(100%)	15/32(46%)	23/24(95%)
F: MC81 - MC96	6/16(37%)	5/ 5(100%)	15/32(46%)	17/24(70%)
G: MC97 - MC112	7/16(43%)	5/ 5(100%)	3/32(9%)	24/24(100%)
H: MC113 - MC128	16/16(100%)	8/ 8(100%)	12/32(37%)	23/24(95%)

Total dedicated input pins used:	8/ 8 (100%)
Total I/O pins used:	52/ 52 (100%)
Total macrocells used:	86/128 (67%)
Total expanders used:	84/256 (32%)

Total input pins required:	20
Total output pins required:	24
Total bidirectional pins required:	16
Total macrocells required:	86
Total expanders in database:	69

Synthesized macrocells:	0/128 (0%)

** FILE HIERARCHY **

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¦DACMAP:78¦74151:30¦
¦DACMAP:78¦74151:18¦
¦DACMAP:78¦74151:17¦
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¦DACMAP:78¦74151:15¦
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¦NTAREG:48¦CT8:93¦
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¦GASEL:46¦
¦OUTMUX:50¦
¦OUTMUX:50¦74153:81¦
¦OUTMUX:50¦74138H:82¦
¦OUTMUX:50¦74153:74¦
¦OUTMUX:50¦74153:75¦
¦OUTMUX:50¦74153:76¦
¦OUTMUX:50¦74153:77¦
¦OUTMUX:50¦74153:78¦
   TMUX:50¦74153:79¦
   TMUX:50¦74153:80¦
¦CSR0:49¦
```

** INPUTS **

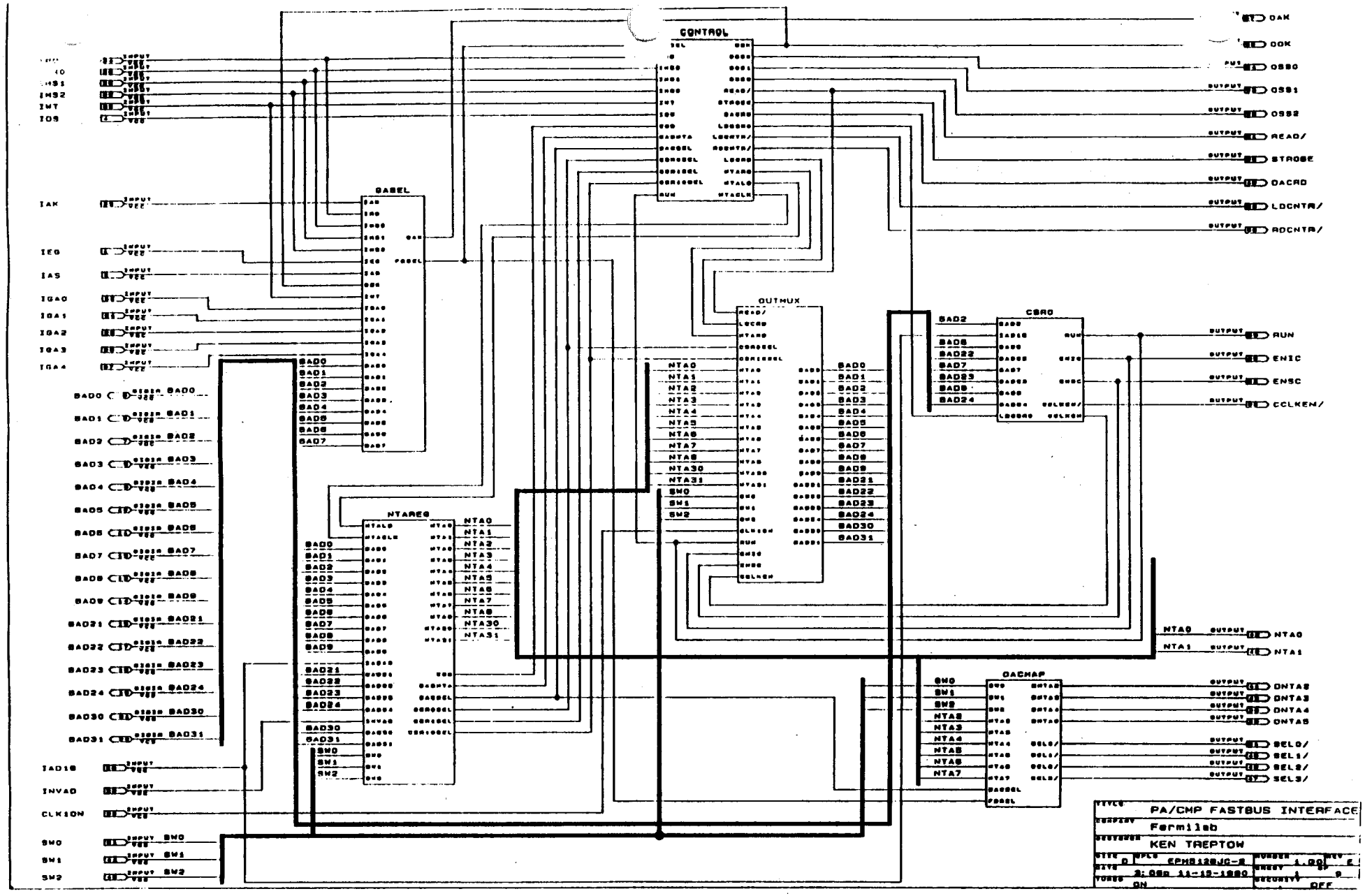
				Expanders		Fan-In		
٦	MCell	LAB	Primitive	Total	Shared	INP	FBK	Name
5	(2)	(A)	INPUT	0	0	0	0	BAD0
6	(3)	(A)	INPUT	0	0	0	0	BAD1
7	(4)	(A)	INPUT	0	0	0	0	BAD2
8	(5)	(A)	INPUT	0	0	0	0	BAD3
9	(6)	(A)	INPUT	0	0	0	0	BAD4
10	(7)	(A)	INPUT	0	0	0	0	BAD5
11	(8)	(A)	INPUT	0	0	0	0	BAD6
12	(17)	(B)	INPUT	0	0	0	0	BAD7
13	(18)	(B)	INPUT	0	0	0	0	BAD8
14	(19)	(B)	INPUT	0	0	0	0	BAD9
15	(20)	(B)	INPUT	0	0	0	0	BAD21
17	(21)	(B)	INPUT	0	0	0	0	BAD22
18	(33)	(C)	INPUT	0	0	0	0	BAD23
19	(34)	(C)	INPUT	0	0	0	0	BAD24
21	(35)	(C)	INPUT	0	0	0	0	BAD30
22	(36)	(C)	INPUT	0	0	0	0	BAD31
30	(55)	(D)	INPUT	0	0	0	0	CLK1ON
28	(53)	(D)	INPUT	0	0	0	0	IAD18
32	-	-	INPUT	0	0	0	0	IAK
2	-	-	INPUT	0	0	0	0	IAS
4	(1)	(A)	INPUT	0	0	0	0	IDS
1	-	-	INPUT	0	0	0	0	IEG
23	(37)	(C)	INPUT	0	0	0	0	IGA0
24	(49)	(D)	INPUT	0	0	0	0	IGA1
25	(50)	(D)	INPUT	0	0	0	0	IGA2
6	(51)	(D)	INPUT	0	0	0	0	IGA3
27	(52)	(D)	INPUT	0	0	0	0	IGA4
35	-	-	INPUT	0	0	0	0	IMS0
36	-	-	INPUT	0	0	0	0	IMS1
66	-	-	INPUT	0	0	0	0	IMS2
29	(54)	(D)	INPUT	0	0	0	0	INVAD
34	-	-	INPUT	0	0	0	0	IRD
68	-	-	INPUT	0	0	0	0	IWT
31	(56)	(D)	INPUT	0	0	0	0	SW0
44	(71)	(E)	INPUT	0	0	0	0	SW1
45	(72)	(E)	INPUT	0	0	0	0	SW2

** OUTPUTS **

Pin	MCell	LAB	Primitive	Expanders Total	Expanders Shared	Fan-In INP	Fan-In FBK	Name
5	2	A	OR4	11	11	7	14	BAD0
6	3	A	OR4	11	11	7	14	BAD1
7	4	A	OR4	11	11	7	15	BAD2
8	5	A	OR4	11	11	7	14	BAD3
9	6	A	OR4	11	11	7	15	BAD4
10	7	A	OR4	11	11	7	14	BAD5
11	8	A	OR4	11	11	7	15	BAD6
12	17	B	OR4	11	11	4	15	BAD7
13	18	B	OR4	1	1	4	6	BAD8
14	19	B	OR4	1	1	5	4	BAD9
15	20	B	OR4	1	1	4	4	BAD21
17	21	B	OR4	1	1	4	2	BAD22
18	33	C	OR4	1	1	4	4	BAD23
19	34	C	OR4	1	1	4	4	BAD24
21	35	C	OR4	1	1	4	5	BAD30
22	36	C	OR4	1	1	4	5	BAD31
52	97	G	MCELL	0	0	0	1	CCLKEN/
46	81	F	OUTPUT	0	0	4	7	DACRD
41	68	E	OUTPUT	0	0	3	1	DNTA2
40	67	E	OUTPUT	0	0	3	2	DNTA3
39	66	E	OUTPUT	0	0	3	3	DNTA4
38	65	E	OUTPUT	5	0	3	4	DNTA5
55	99	G	DFF	3	3	6	15	ENIC
53	98	G	DFF	3	3	6	15	ENSC
59	114	H	OUTPUT	0	0	4	15	LDCNTR/
3	70	E	DFF	0	0	1	3	NTA0
2	69	E	DFF	0	0	1	4	NTA1
57	101	G	LATCH	0	0	1	2	OAK
65	120	H	LATCH	0	0	1	2	ODK
64	119	H	OUTPUT	0	0	3	3	OSS0
63	118	H	OUTPUT	8	7	4	11	OSS1
62	117	H	OUTPUT	7	7	4	10	OSS2
58	113	H	OUTPUT	0	0	3	13	RDCNTR/
61	116	H	OUTPUT	0	0	4	2	READ/
56	100	G	DFF	3	3	6	15	RUN
51	85	F	OUTPUT	5	0	3	11	SEL0/
49	84	F	OUTPUT	3	0	3	11	SEL1/
48	83	F	OUTPUT	4	0	3	11	SEL2/
47	82	F	OUTPUT	3	0	3	11	SEL3/
60	115	H	OUTPUT	0	0	3	10	STROBE

** BURIED LOGIC **

ı	MCell	LAB	Primitive	Expanders Total	Expanders Shared	Fan-In INP	Fan-In FBK	Name
-	64	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS0
-	63	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS1
-	62	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS2
-	61	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS3
-	60	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS4
-	80	E	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦IDS5
-	57	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:34
(27)	52	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:37
-	59	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:38
-	58	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:39
(31)	56	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:41
(30)	55	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:42
-	79	E	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:43
(29)	54	D	MCELL	0	0	1	0	¦CONTROL:45¦DELAY:165¦:46
(26)	51	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:49
(25)	50	D	MCELL	0	0	0	1	¦CONTROL:45¦DELAY:165¦:50
-	128	H	MCELL	0	0	3	3	¦CONTROL:45¦INH
-	78	E	MCELL	0	0	3	6	¦CONTROL:45¦NTACLK
-	77	E	MCELL	0	0	4	5	¦CONTROL:45¦NTACLK0/2
-	76	E	DFF	3	0	4	5	¦CONTROL:45¦NTAINC
-	96	F	DFF	0	0	0	2	¦CONTROL:45¦SSEN
-	16	A	MCELL	0	0	4	6	¦CONTROL:45¦:187
-	15	A	MCELL	0	0	0	1	¦CONTROL:45¦:188
-	14	A	MCELL	0	0	0	1	¦CONTROL:45¦:189
-	127	H	DFF	3	3	6	15	¦CSR0:49¦CCLKEN
-	13	A	MCELL	0	0	0	1	¦GASEL:46¦DIAS1
-	112	G	MCELL	0	0	0	1	¦GASEL:46¦DIAS2
-	75	E	DFF	7	0	20	1	¦GASEL:46¦FBSEL
-	12	A	MCELL	0	0	1	0	¦GASEL:46¦:21
-	111	G	MCELL	0	0	0	1	¦GASEL:46¦:51
-	126	H	MCELL	0	0	0	12	¦NTAREG:48¦BADNTA
-	31	B	DFF	0	0	1	5	¦NTAREG:48¦CT8:93¦Q2
-	74	E	DFF	0	0	1	6	¦NTAREG:48¦CT8:93¦Q3
-	73	E	DFF	0	0	1	7	¦NTAREG:48¦CT8:93¦Q4
(45)	72	E	DFF	0	0	1	8	¦NTAREG:48¦CT8:93¦Q5
(44)	71	E	DFF	0	0	1	9	¦NTAREG:48¦CT8:93¦Q6
-	125	H	DFF	0	0	1	10	¦NTAREG:48¦CT8:93¦Q7
-	11	A	SOFT	7	0	3	6	¦NTAREG:48¦DACSEL:108¦:52
-	10	A	SOFT	7	0	3	8	¦NTAREG:48¦DACSEL:108¦:53
-	124	H	MCELL	0	0	0	13	¦NTAREG:48¦EN/
-	123	H	DFF	1	0	0	15	¦NTAREG:48¦EOB
(28)	53	D	DFF	0	0	8	2	¦NTAREG:48¦NTA8
-	122	H	DFF	0	0	1	2	¦NTAREG:48¦NTA30
-	121	H	DFF	0	0	1	2	¦NTAREG:48¦NTA31
-	9	A	SOFT	2	0	4	13	¦OUTMUX:50¦:90
-	32	B	SOFT	0	0	4	12	¦OUTMUX:50¦:91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OUTMUX
CSRO
NTAREG
DACMAP
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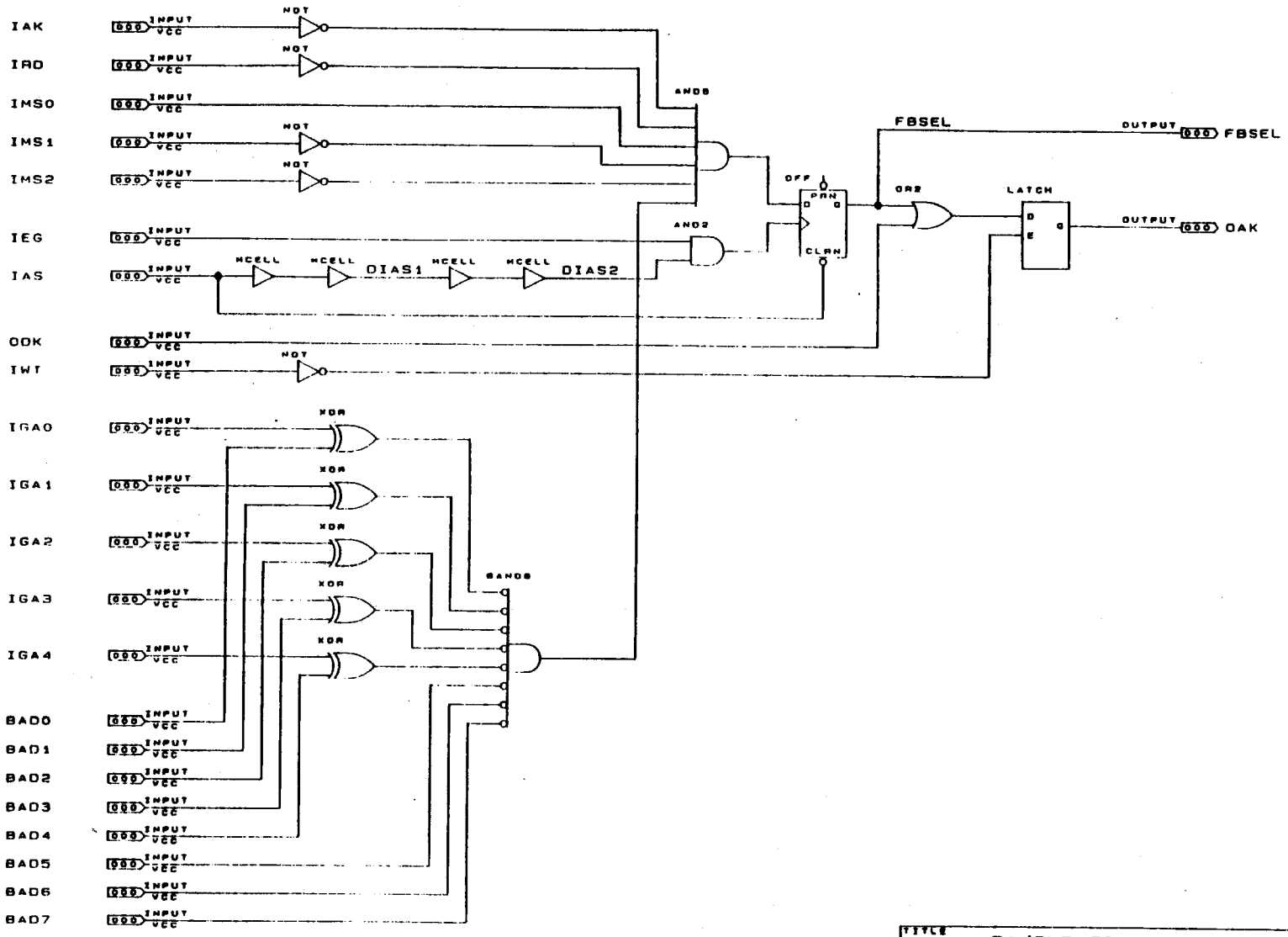
IMS2
IMT
IOS
IAK
IEG
IAS
IGA0
IGA1
IGA2
IGA3
IGA4
BAD0
BAD1
BAD2
BAD3
BAD4
BAD5
BAD6
BAD7
BAD8
BAD9
BAD21
BAD22
BAD23
BAD24
BAD30
BAD31
IAD18
INVAD
CLK10N
SW0
SW1
SW2
OAK
OOK
OSS0
OSS1
OSS2
READ/
STROBE
DACRD
LDCNTR/
RDCNTR/
RUN
ENIC
ENSC
CCLKEN/
NTA0
NTA1
DNTA2
DNTA3
DNTA4
DNTA5
SEL0/
SEL1/
SEL2/
SEL3/
TITLE PA/CMP FASTBUS INTERFACE
COMPANY Fermilab
DESIGNER KEN TREPTOW
SIZE D
EPM5128JC-2
NUMBER 1.00
REV E
DATE 3:08p 11-15-1980
SHEET 1 OF 9
TUNED ON
SECURITY OFF



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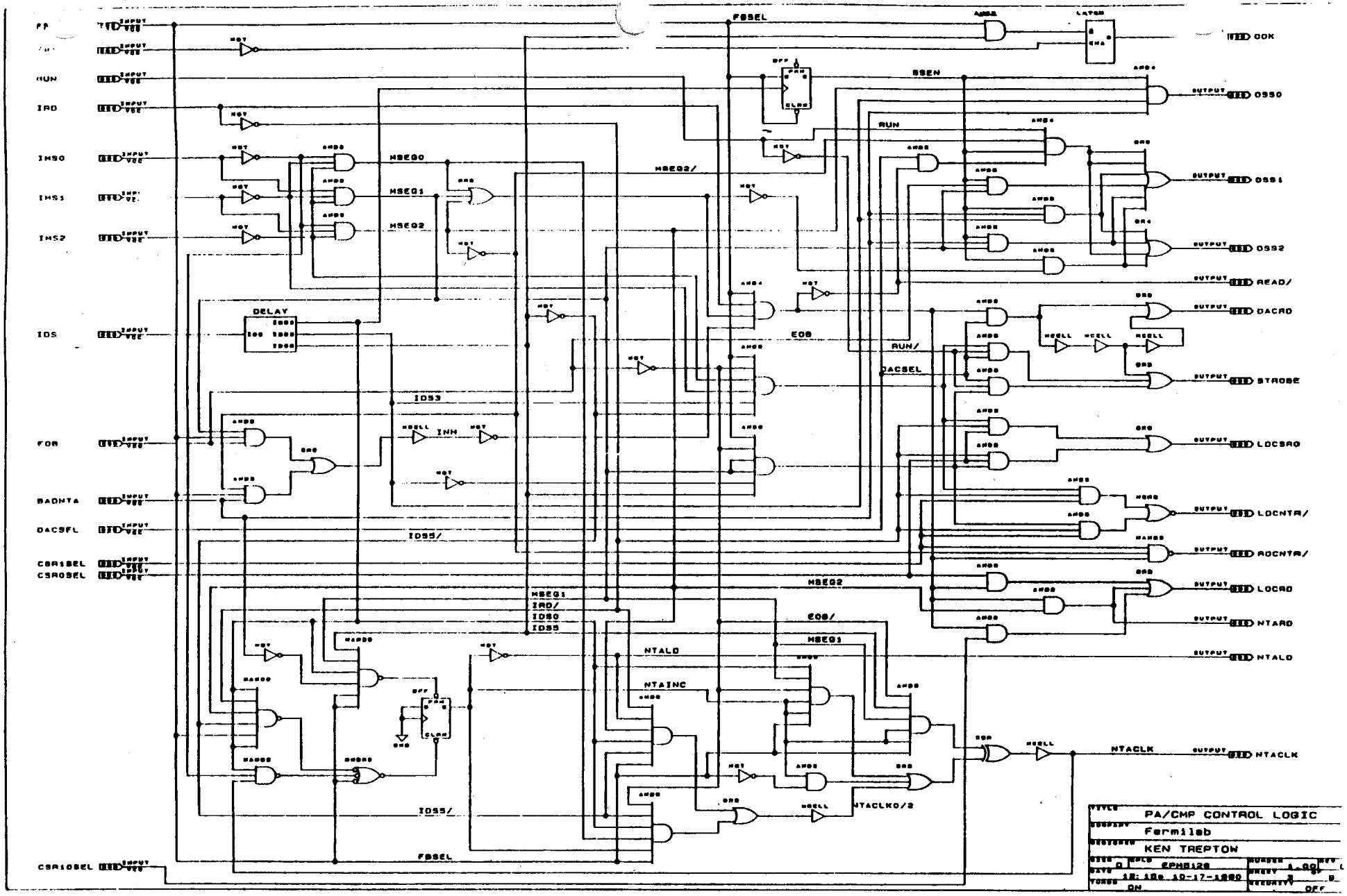
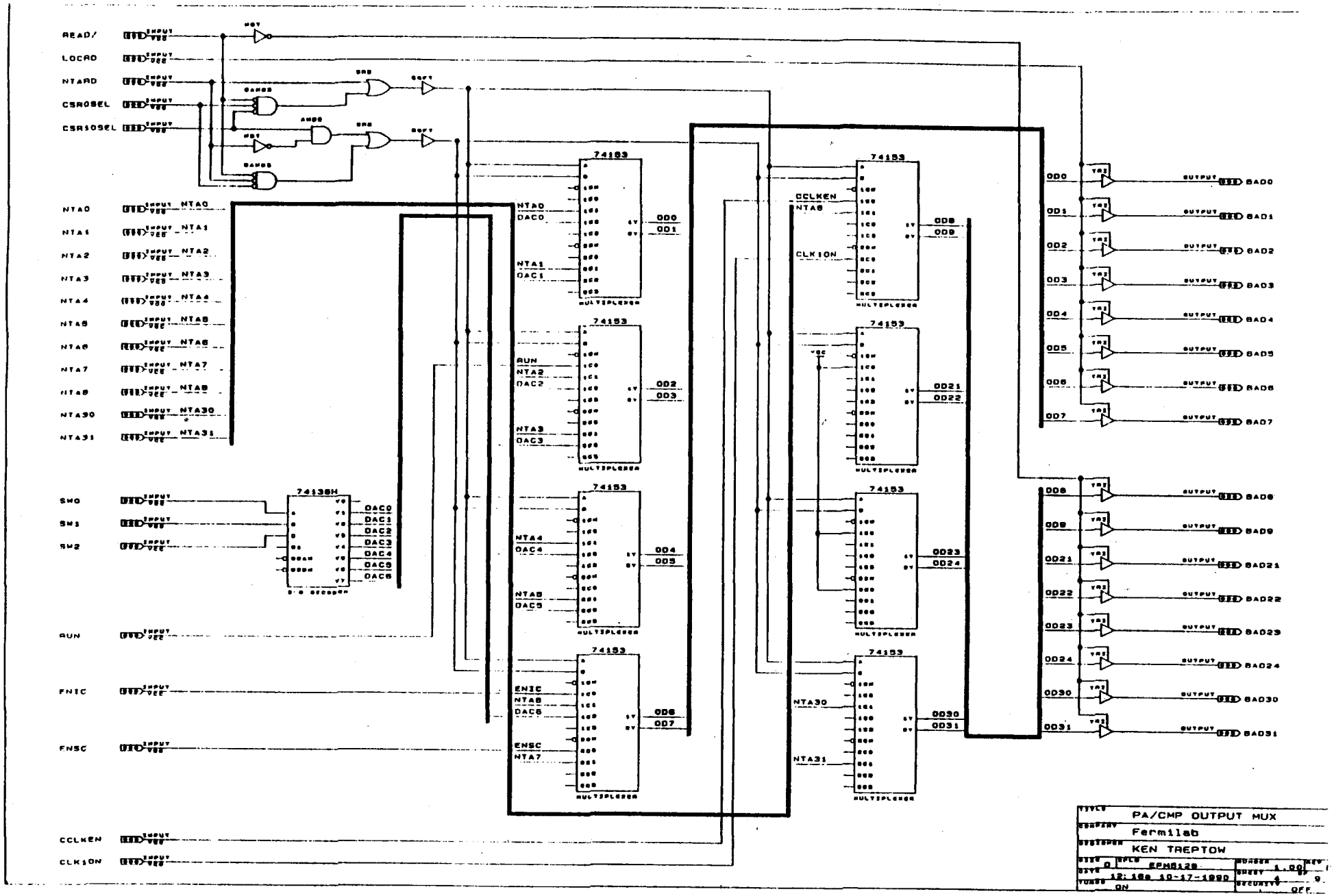
SIZE C	EPLD EPM5128
NUMBER 1.00	REV B
DATE 6/11/90	SHEET 2 OF 9
TURBO ON	SECURITY OFF



RUN
IRD
IMS0
IMS1
IMS2
IDS
EOB
BADNTA
DACSEL
CSR1SEL
CSR0SEL
CSR10SEL
DELAY
IDS3
INH
IDS5/
MSEQ0
MSEQ1
MSEQ2
MSEQ2/
FBSEL
SSEN
RUN
EOB
RUN/
DACSEL
MSEQ2
EOB/
MSEQ1
NTALD
NTAINC
NTACLK0/2
NTACLK
OOK
OSS0
OSS1
OSS2
READ/
DACRD
STROBE
LDCSRQ
LDCNTR/
RDCNTR/
LDCRD
NTARD
NTALD
NTACLK
PA/CMP CONTROL LOGIC
Fermilab
KEN TREPTON
EPM5128
12:15a 10-17-1990
ON
OFF


READ/
LOCRD
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CSR0SEL
CSR10SEL
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NTA1
NTA2
NTA3
NTA4
NTA5
NTA6
NTA7
NTA8
NTA30
NTA31
SW0
SW1
SW2
RUN
FNIC
FNSC
CCLKEN
CLK10N
74138H
74153
MULTIPLEXER
OD0
OD1
OD2
OD3
OD4
OD5
OD6
OD7
OD8
OD9
OD21
OD22
OD23
OD24
OD30
OD31
BAD0
BAD1
BAD2
BAD3
BAD4
BAD5
BAD6
BAD7
BAD8
BAD9
BAD21
BAD22
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PA/CMP OUTPUT MUX
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EPM5128
12:16a 10-17-1990
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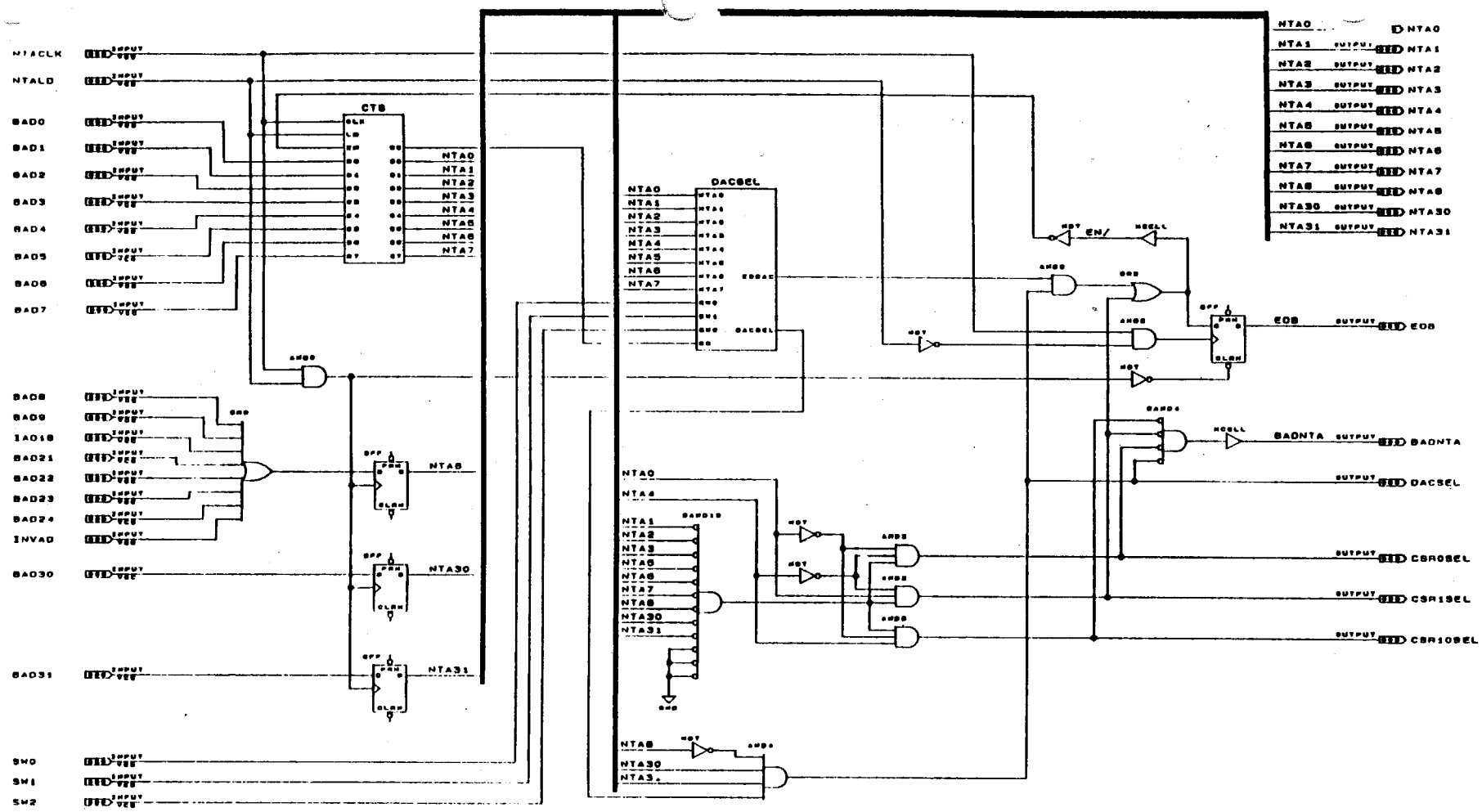
OFF



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COMPANY	Fermilab
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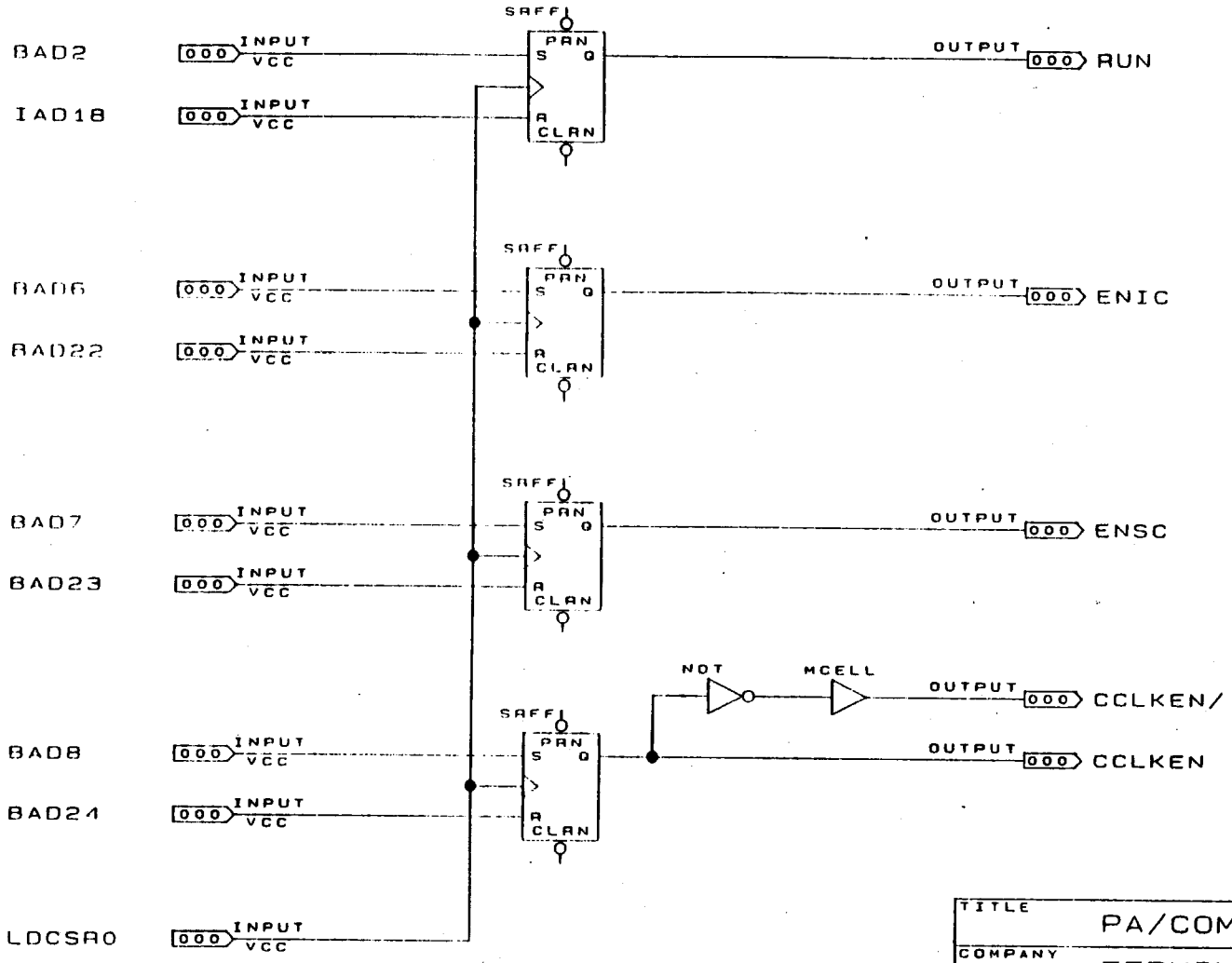
DATE	12:14a 10-17-1990
TURBO	ON
NUMBER	1.00
SHEET	8 OF 8
SECURITY	OFF



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COMPANY	FERMILAB/CD/DAE		
DESIGNER	KEN TREPTOW		
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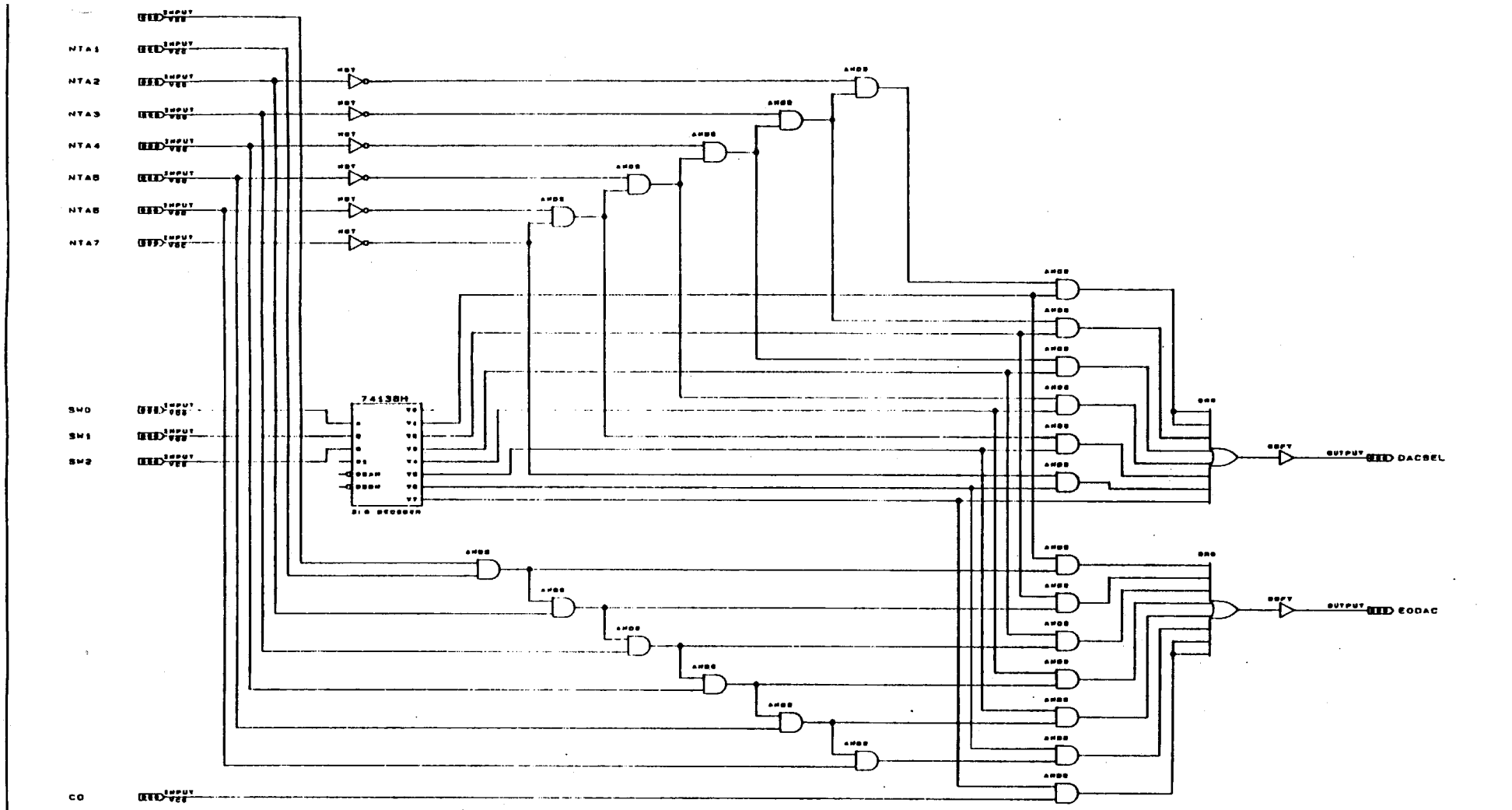
DATE 6/26/90		SHEET 6 OF 9	
TURBO ON		SECURITY OFF	



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DESIGNER	KEN TREPTOW
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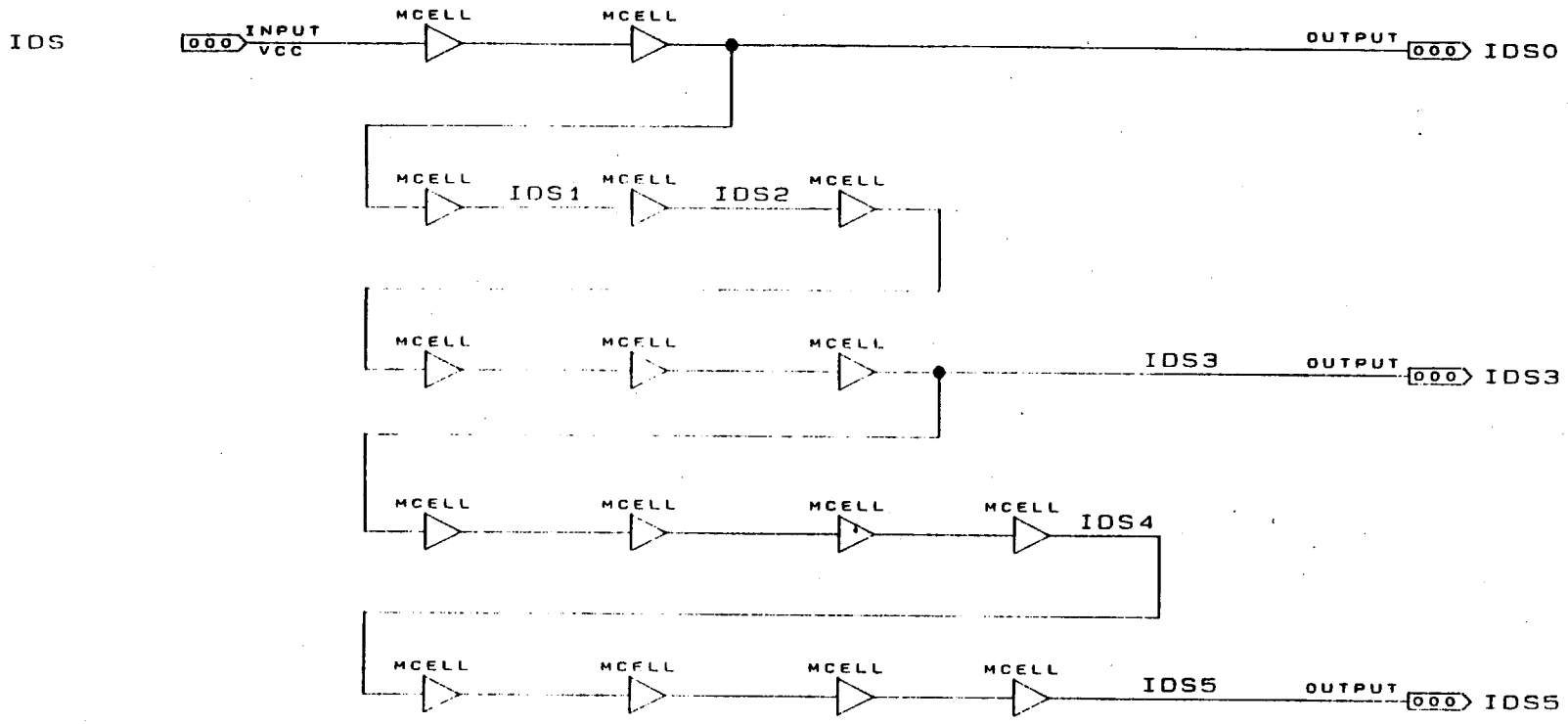
TURBO	ON
NUMBER	1.00 REV A
SHEET 7 OF 9	
SECURITY	OFF



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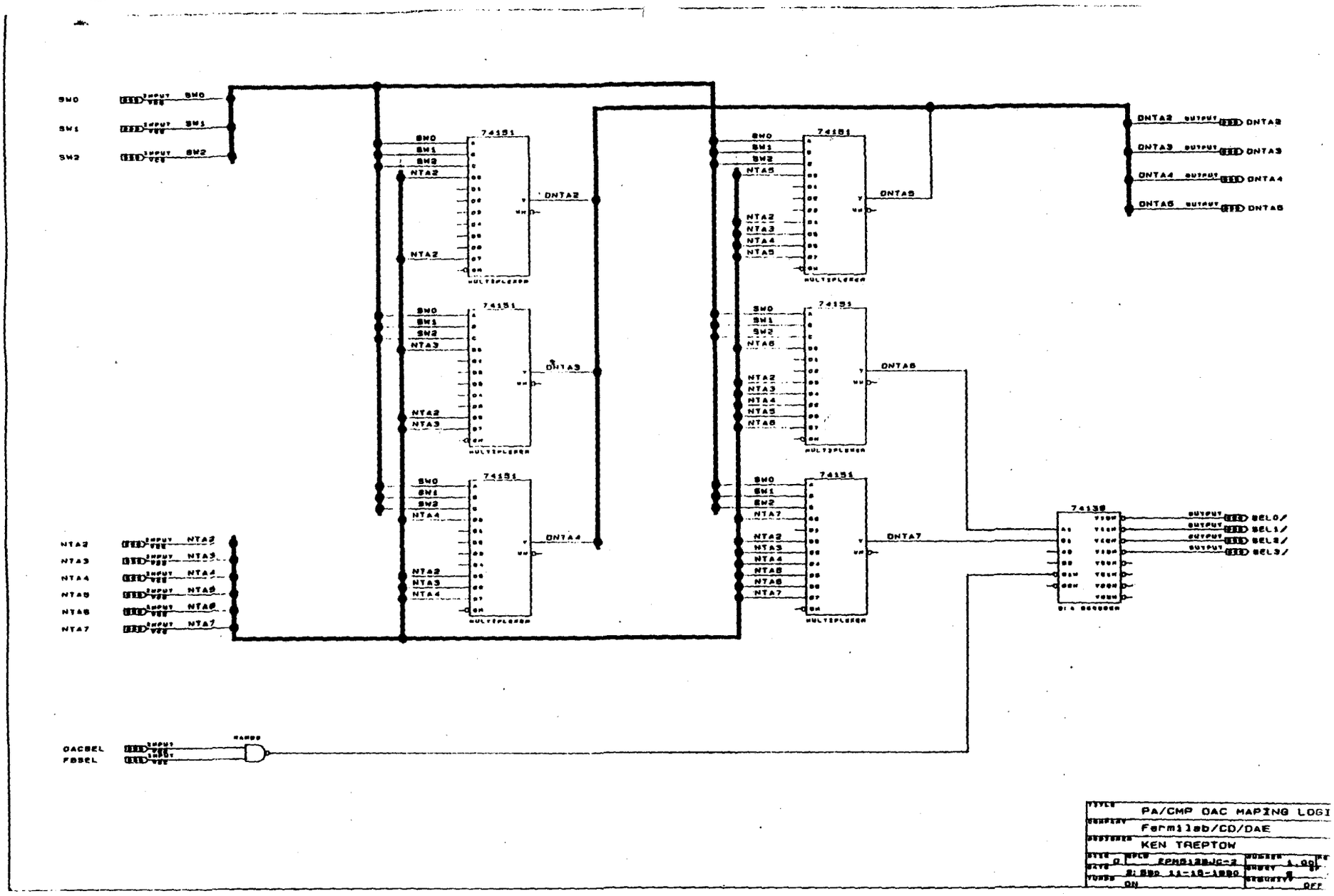
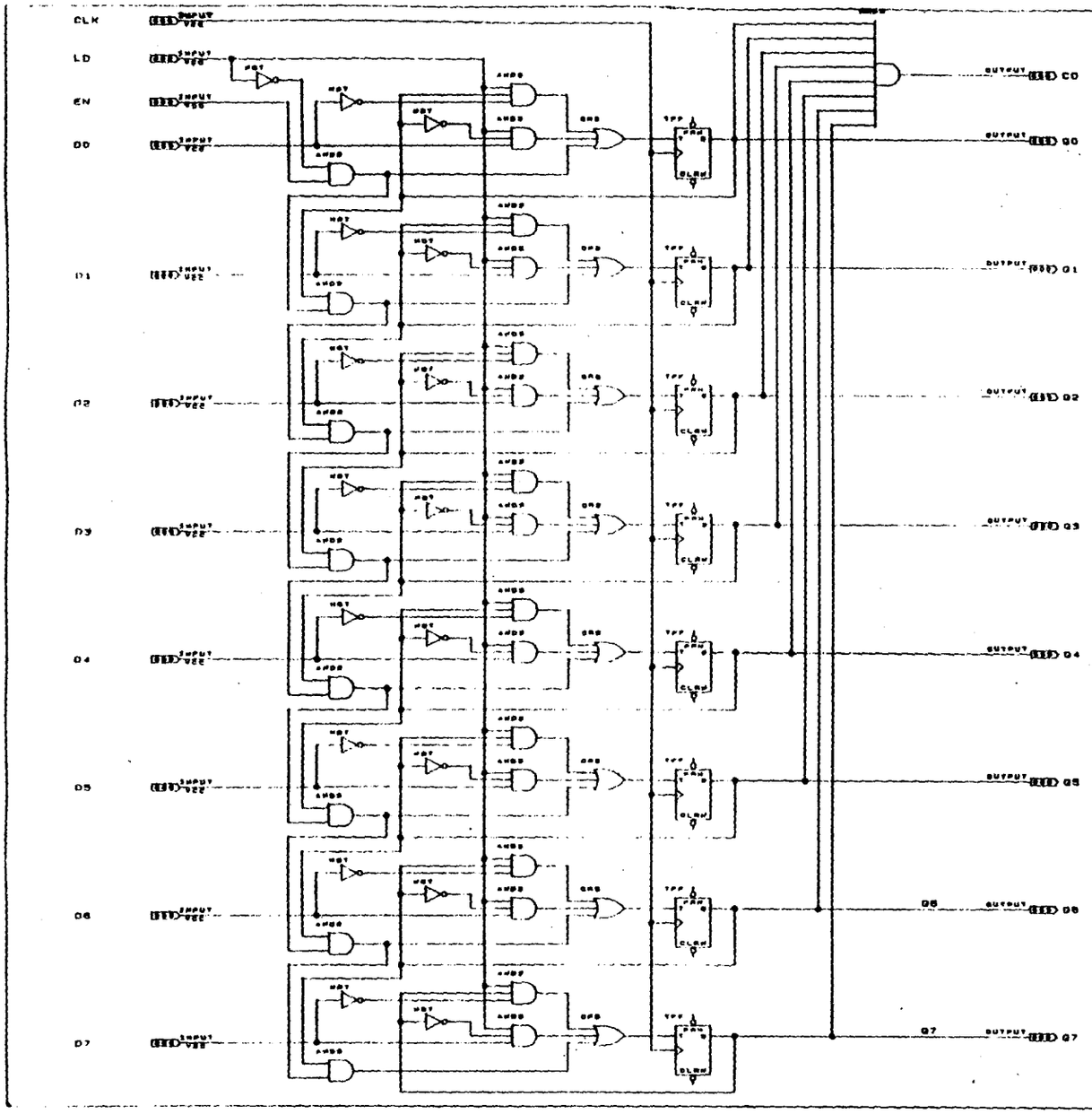
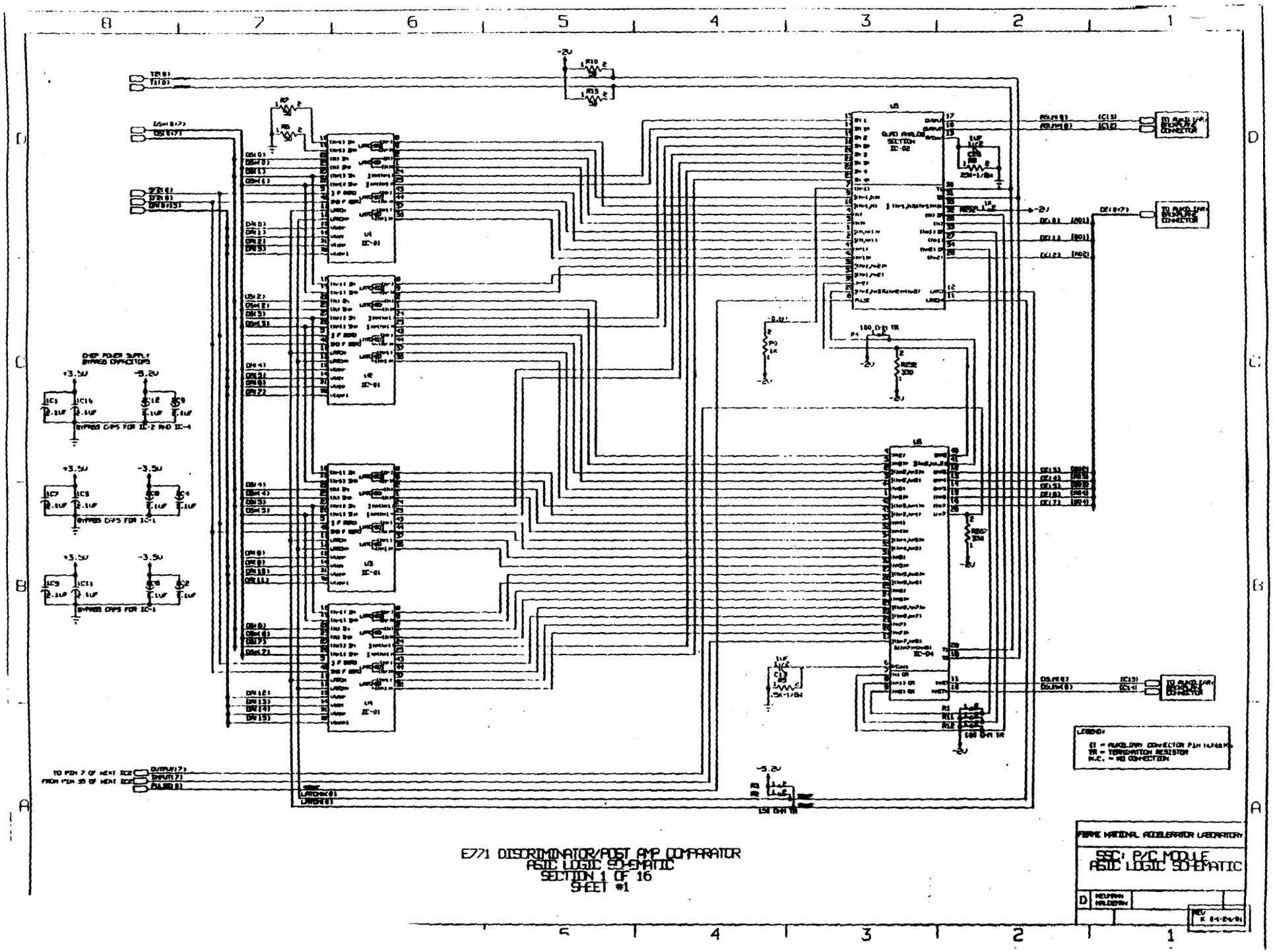
DESIGNER	KEN TREPTOW		
SIZE B	EPLD EPM5128	NUMBER 1.00	REV A
DATE 10:22a 11-13-1990		SHEET 8 OF 9	
TURBO ON		SECURITY OFF	

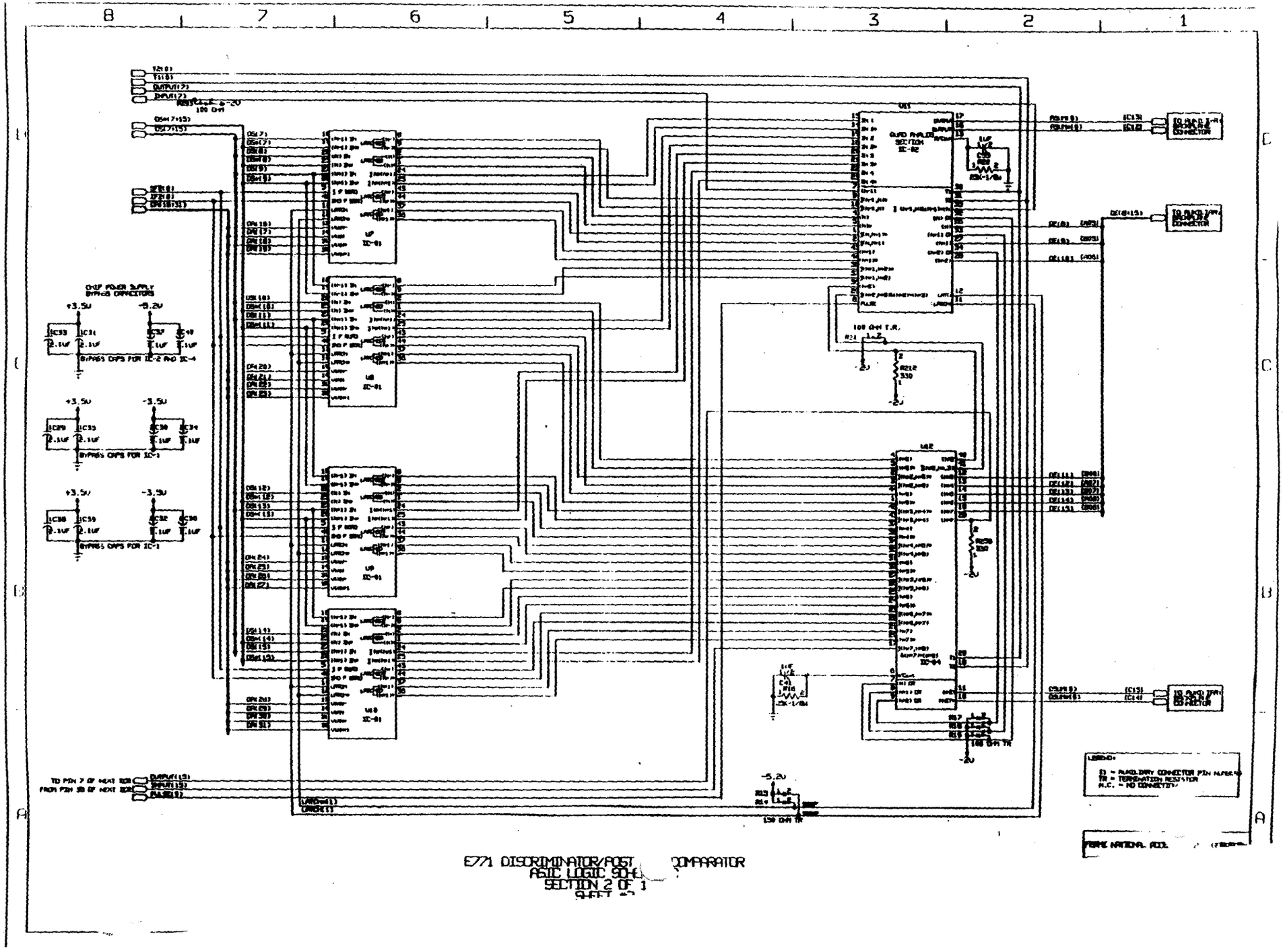

SW0
SW1
SW2
NTA2
NTA3
NTA4
NTA5
NTA6
NTA7
DACSEL
FBSEL
74151
74139
DNTA2
DNTA3
DNTA4
DNTA5
DNTA6
DNTA7
SEL0/
SEL1/
SEL2/
SEL3/
PA/CMP DAC MAPING LOGI
Fermilab/CD/DAE
KEN TREPTOW
ON
OFF



TITLE	B-BIT COUNTER
COMPANY	FERMILAB/RD/EEO/DES
DESIGNER	KEN TREPTOW
SIZE	0
SCALE	EPM5128
NUMBER	1.00
DATE	8/5/88
SHEET	1 OF 1
TURNS	ON
SECURITY	OFF

APPENDIX C - POSTAMP/COMPARATOR MODULE - SCHEMATIC

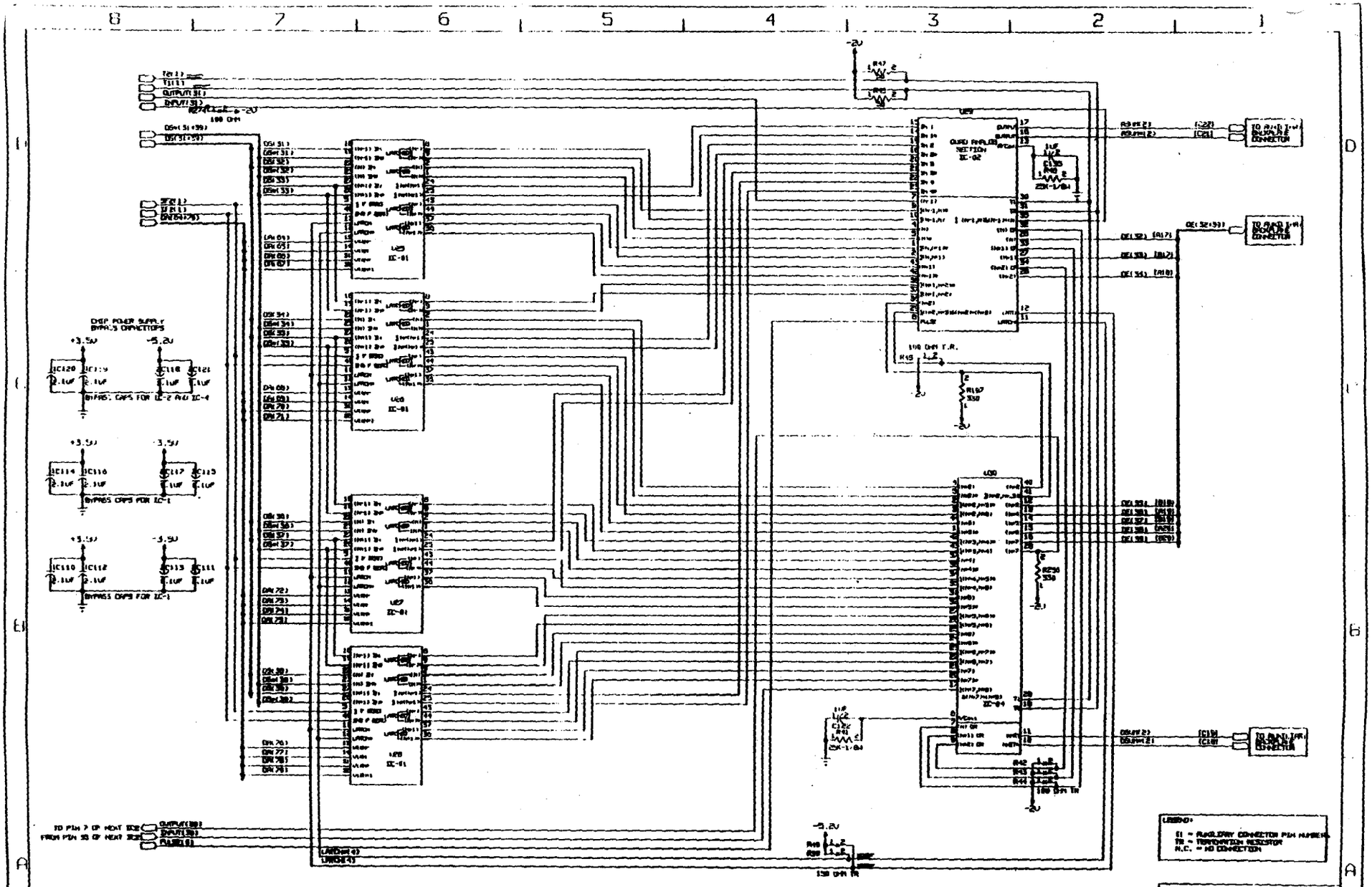

E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 1 OF 16
SHEET #1
FERMI NATIONAL ACCELERATOR LABORATORY
SSC: P/C MODULE
ASIC LOGIC SCHEMATIC



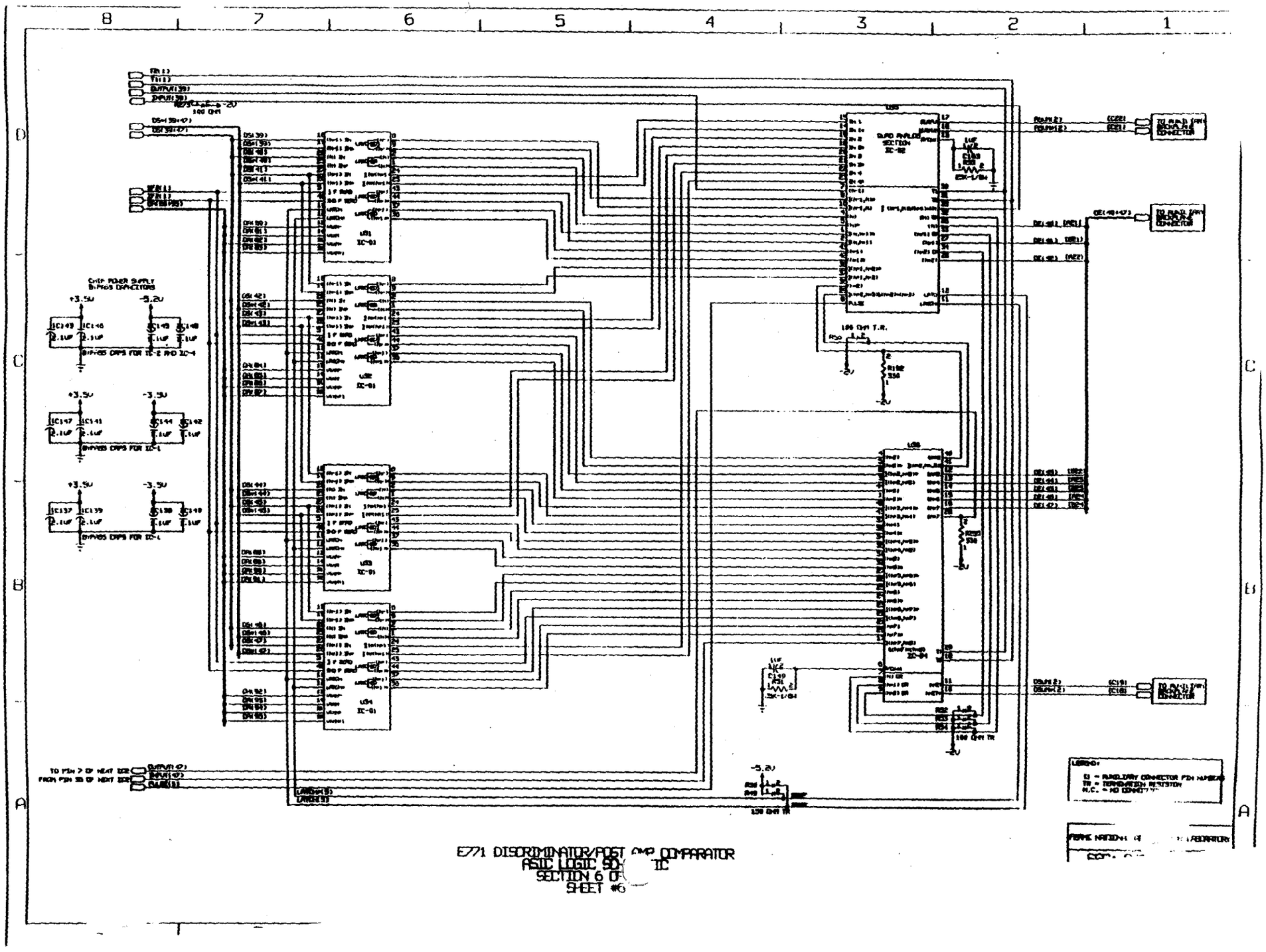
E771 DISCRIMINATOR/POST COMPARATOR
ASIC LOGIC SCH
SECTION 2 OF 1
SHEET 2

APPENDIX D - MODULE DRAWINGS

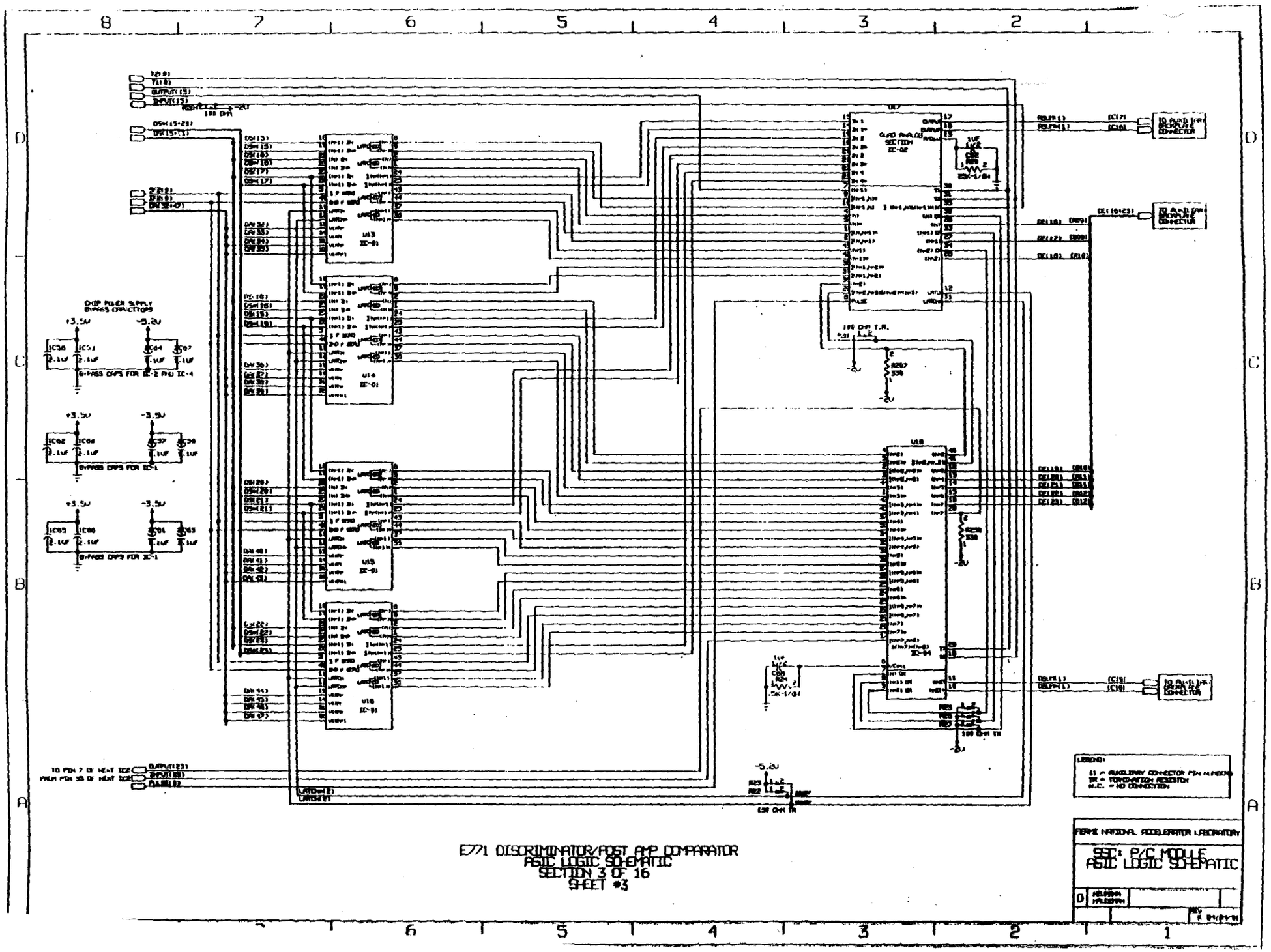
1.	2563.000-ED-215747	EED E771 - POST AMP COMPARATOR VER III SCHEMATIC DIAGRAM	REV. I
2.	2563.000-MD-215752	EED E771 - POST AMP COMPARATOR VER III FRONT PANEL & FRONT PANEL AIR GAP FILLER DETAILS	REV. A
3.	2563.000-MD-215753	EED E771 - POST AMP COMPARATOR VER III FRONT PANEL SILK-SCREEN	REV. C
4.	2563.000-MD-215790	EED E771 - POST AMP COMPARATOR VER III DRILL DRAWING	REV. -
5.	2563.000-MD-215802	EED E771 - POST AMP COMPARATOR VER III BOARD LAYUP AND OUTLINE DETAILS	REV. -
6.	2563.000-MD-215803	EED E771 - POST AMP COMPARATOR VER III P.C. BOARD ASSEMBLY	REV. -
7.	2563.000-MD-215804	EED E771 - POST AMP COMPARATOR VER III BOTTOM SIDE ASSEMBLY	REV. -
8.	2563.000-MD-215805	EED E771 - POST AMP COMPARATOR VER III TOP ASSEMBLY	REV. A
9.	2563.000-MD-215806	EED E771 - POST AMP COMPARATOR VER III LED AND TEST POINTS WIRING DETAILS	REV. -
10.	2563.000-MD-215807	EED E771 - POST AMP COMPARATOR VER III DAC JUMPER DIAGRAM	REV. -
11.	2563.000-MD-215808	EED E771 - POST AMP COMPARATOR VER III POWER TEST POINTS DETAILS	REV. -



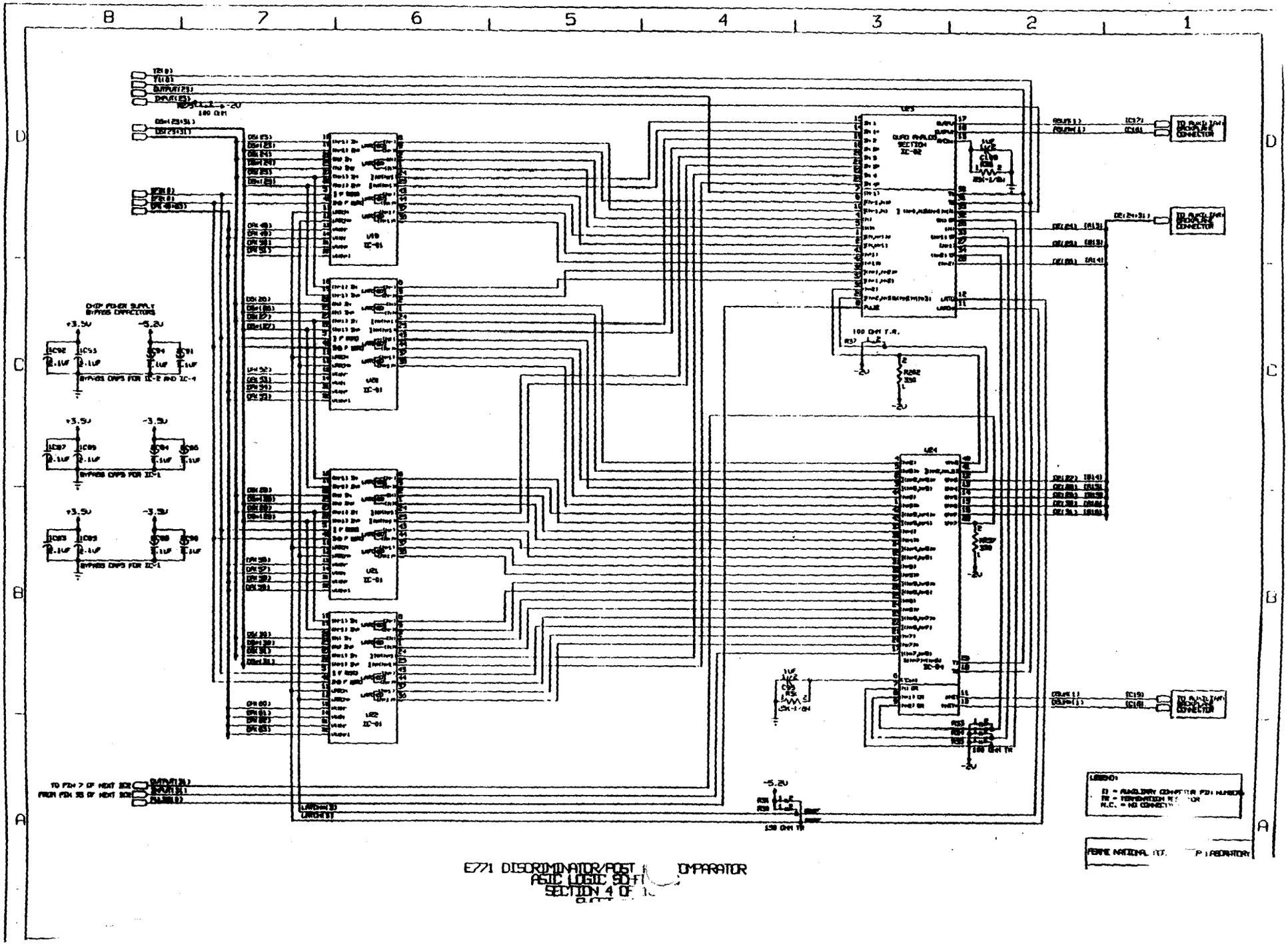
E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 5 OF 16
SHEET #5



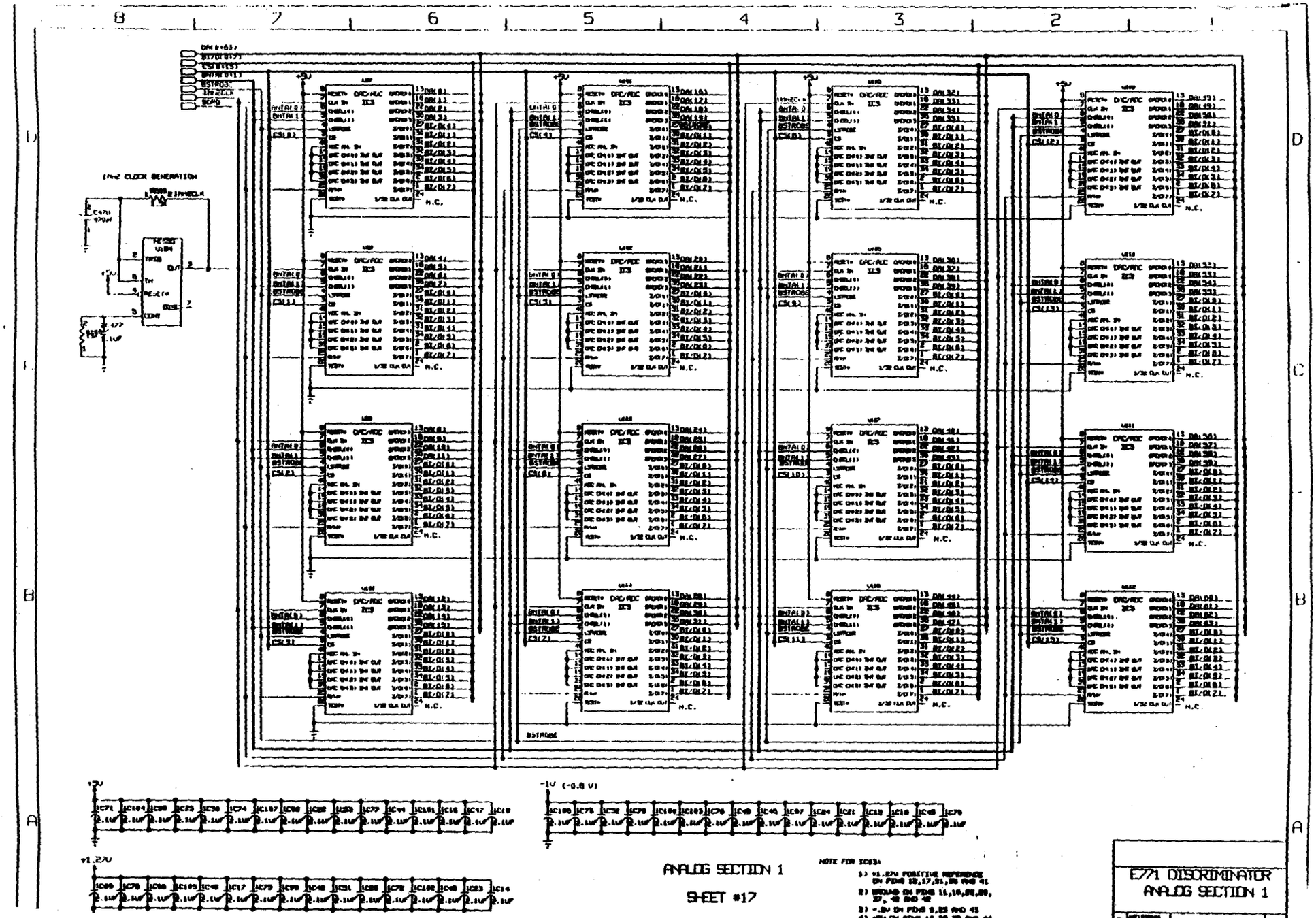
E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SD(IC
SECTION 6 OF
SHEET #6



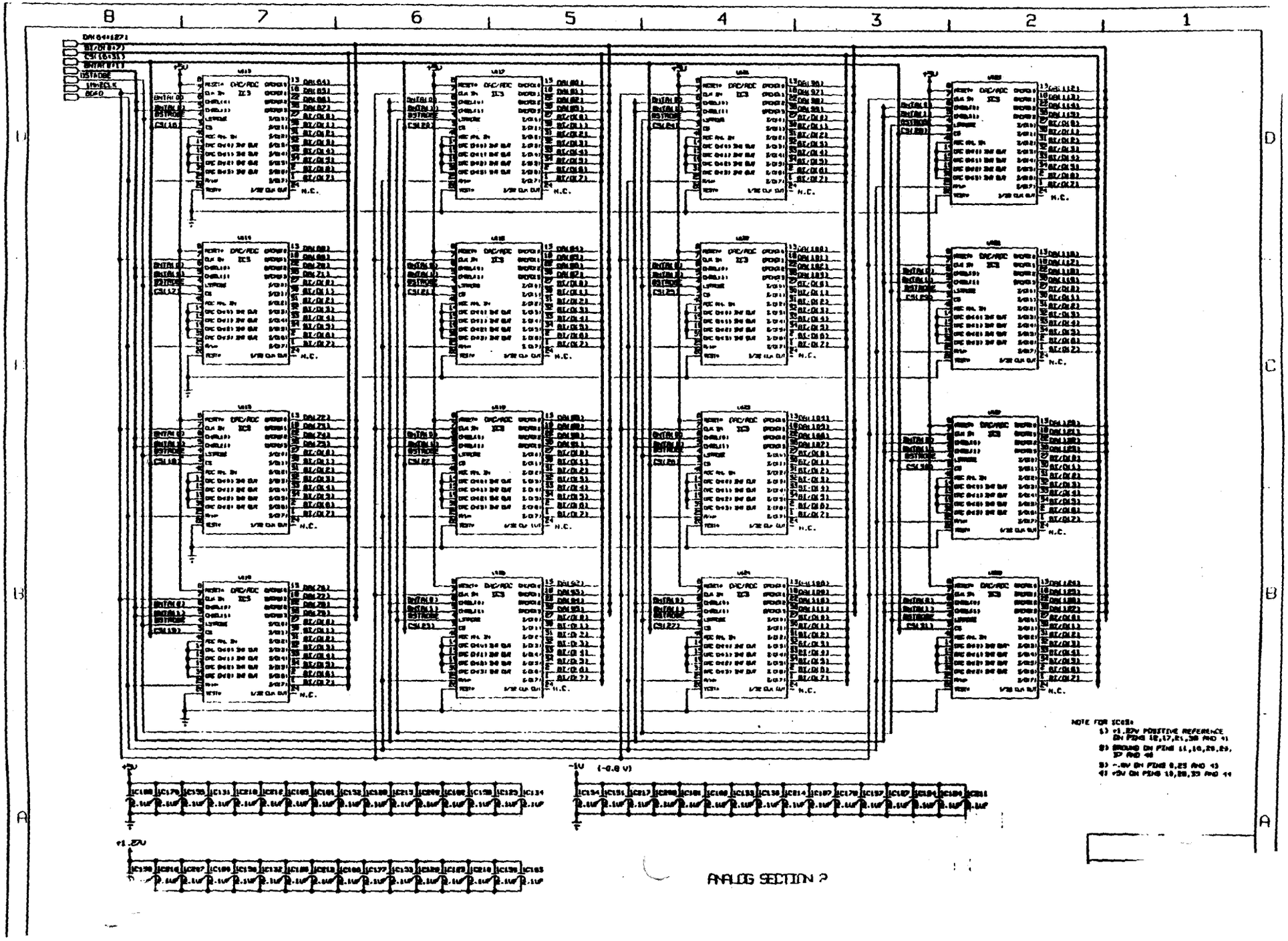
E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 3 OF 16
SHEET #3

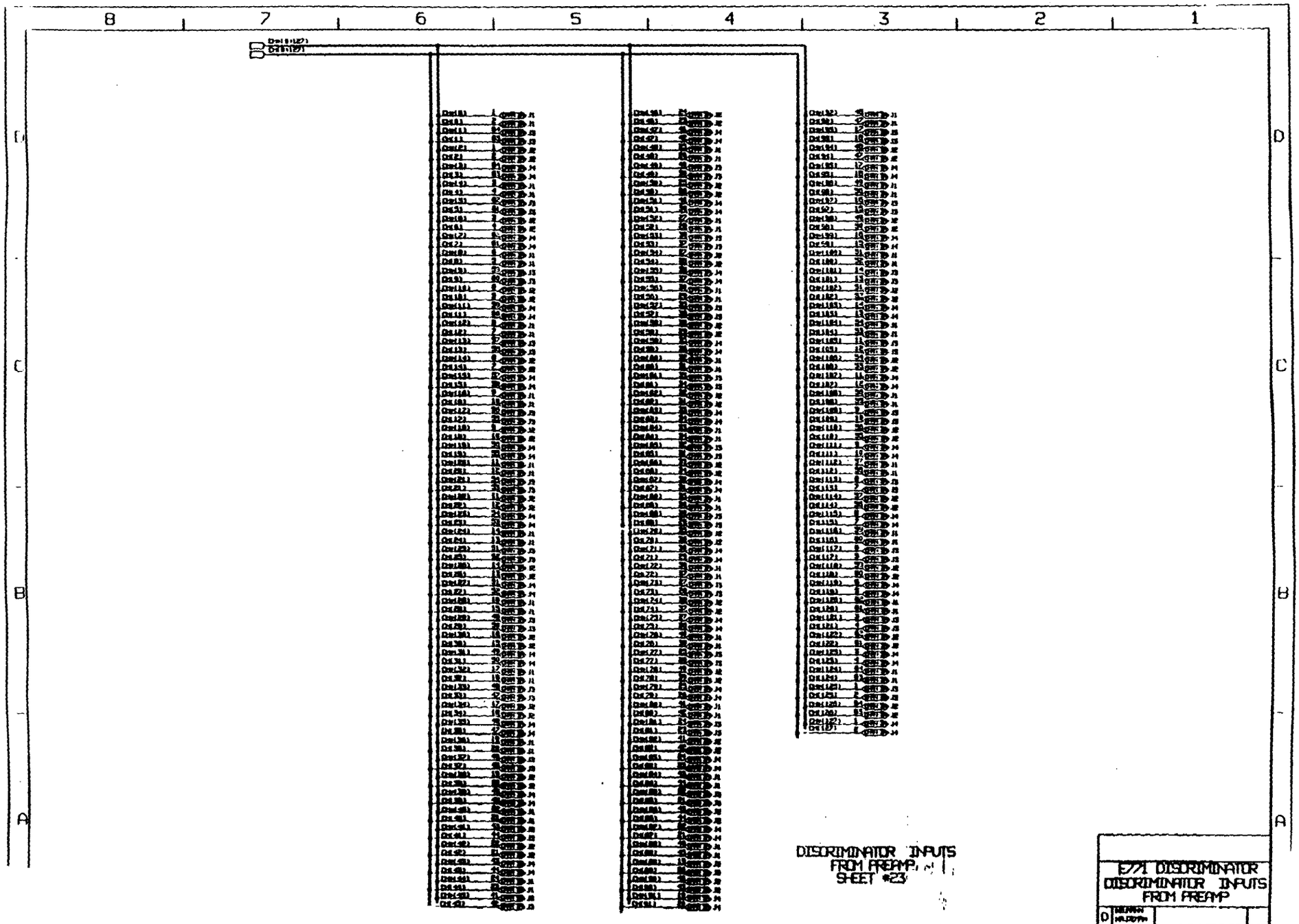


E771 DISCRIMINATOR/POST COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 4 OF 1



1MHz CLOCK GENERATION
DAC/ADC
IC3
N.C.
BSTROBE
+5V
-1V (-0.8 V)
+1.27V
ANALOG SECTION 1
SHEET #17
NOTE FOR IC03:
1) +1.27V POSITIVE REFERENCE ON PINS 12,17,21,38 AND 41
2) GROUND ON PINS 11,16,20,28, 37, 40 AND 42
3) -.8V ON PINS 9,23 AND 43
4) +5V ON PINS 10,28,33 AND 44
E771 DISCRIMINATOR
ANALOG SECTION 1
D

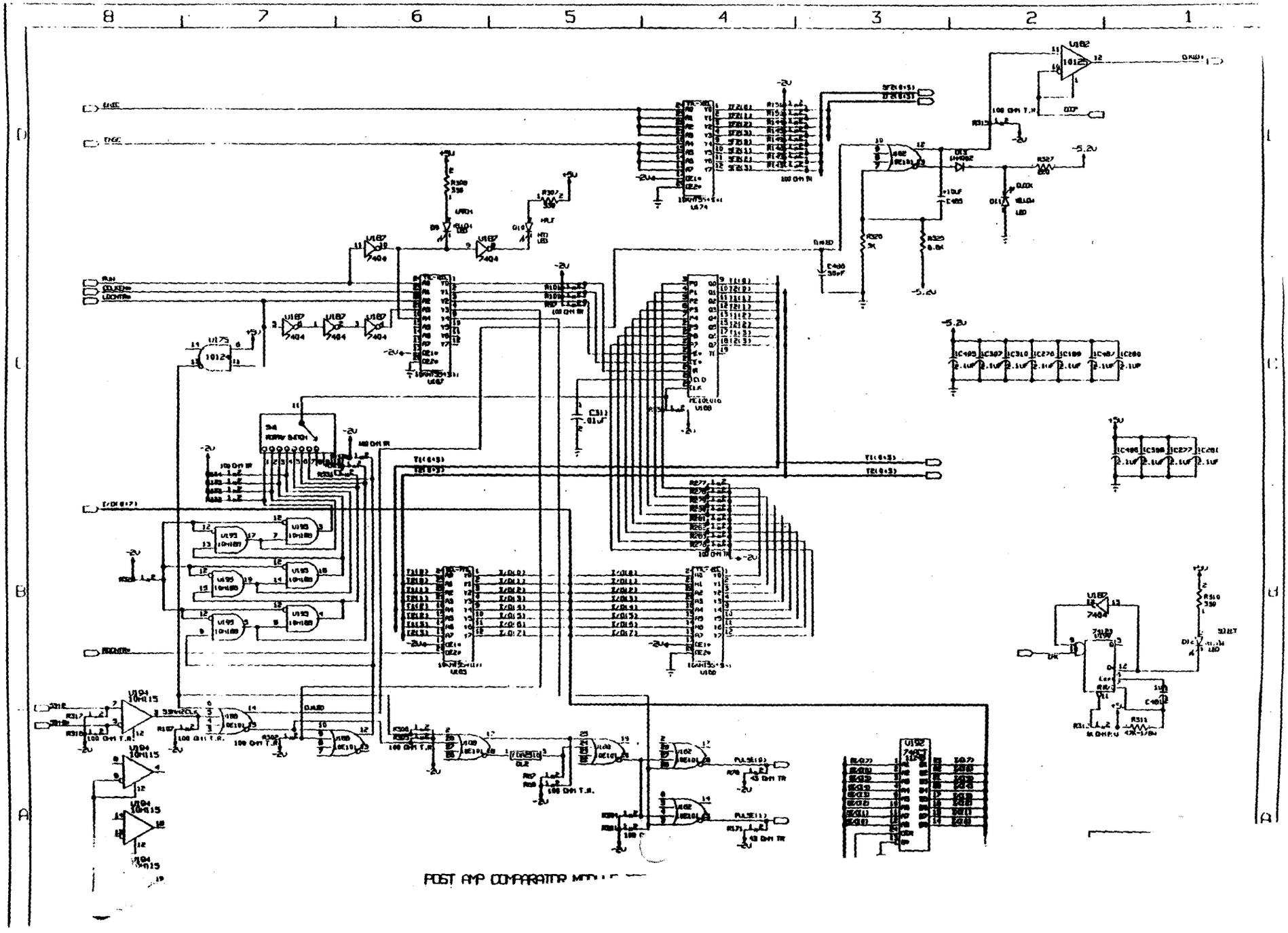

8
7
6
5
4
3
2
1
D
C
B
A
+5V
-1V (-0.8 V)
+1.2V
ANALOG SECTION 2

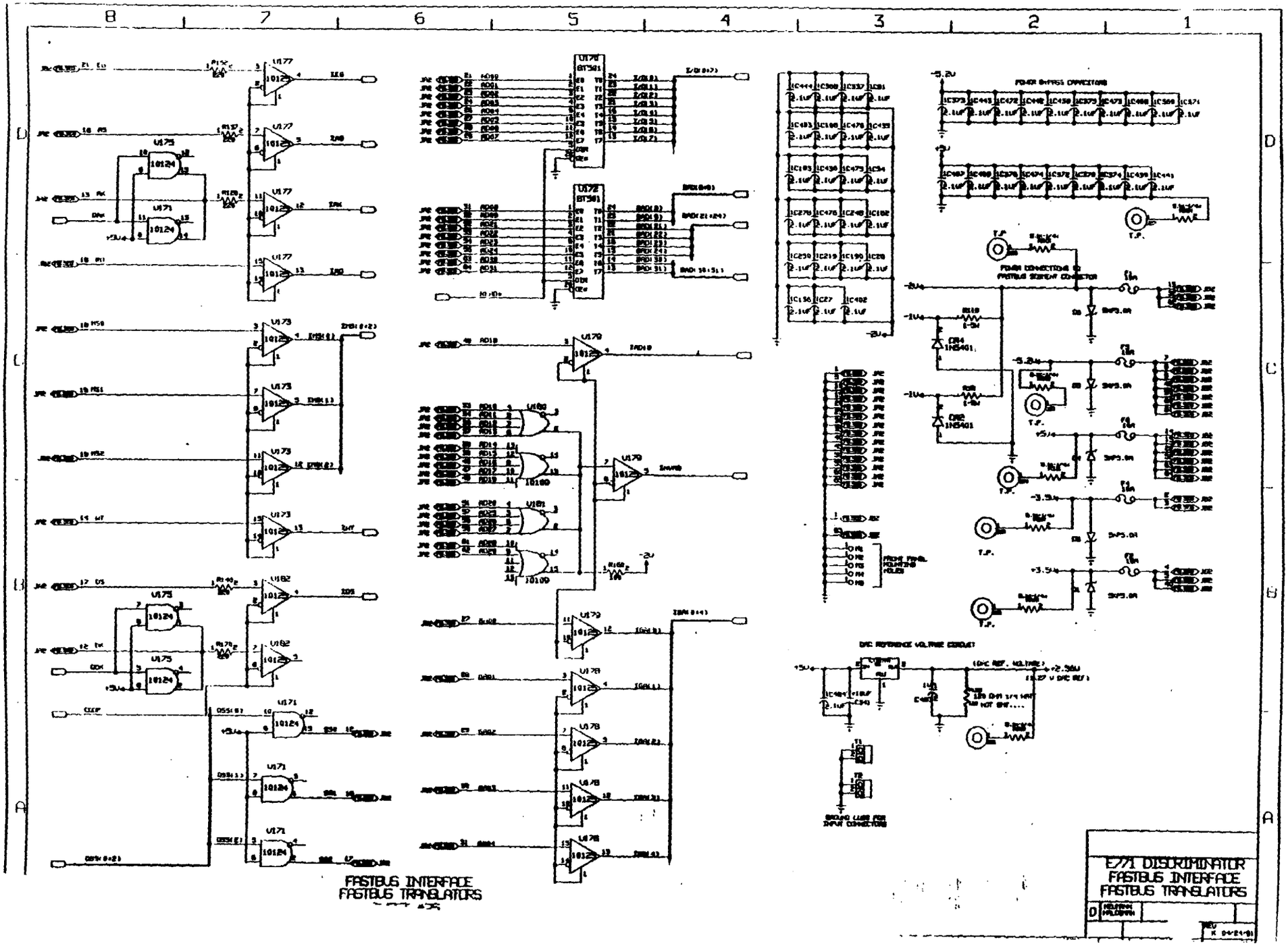


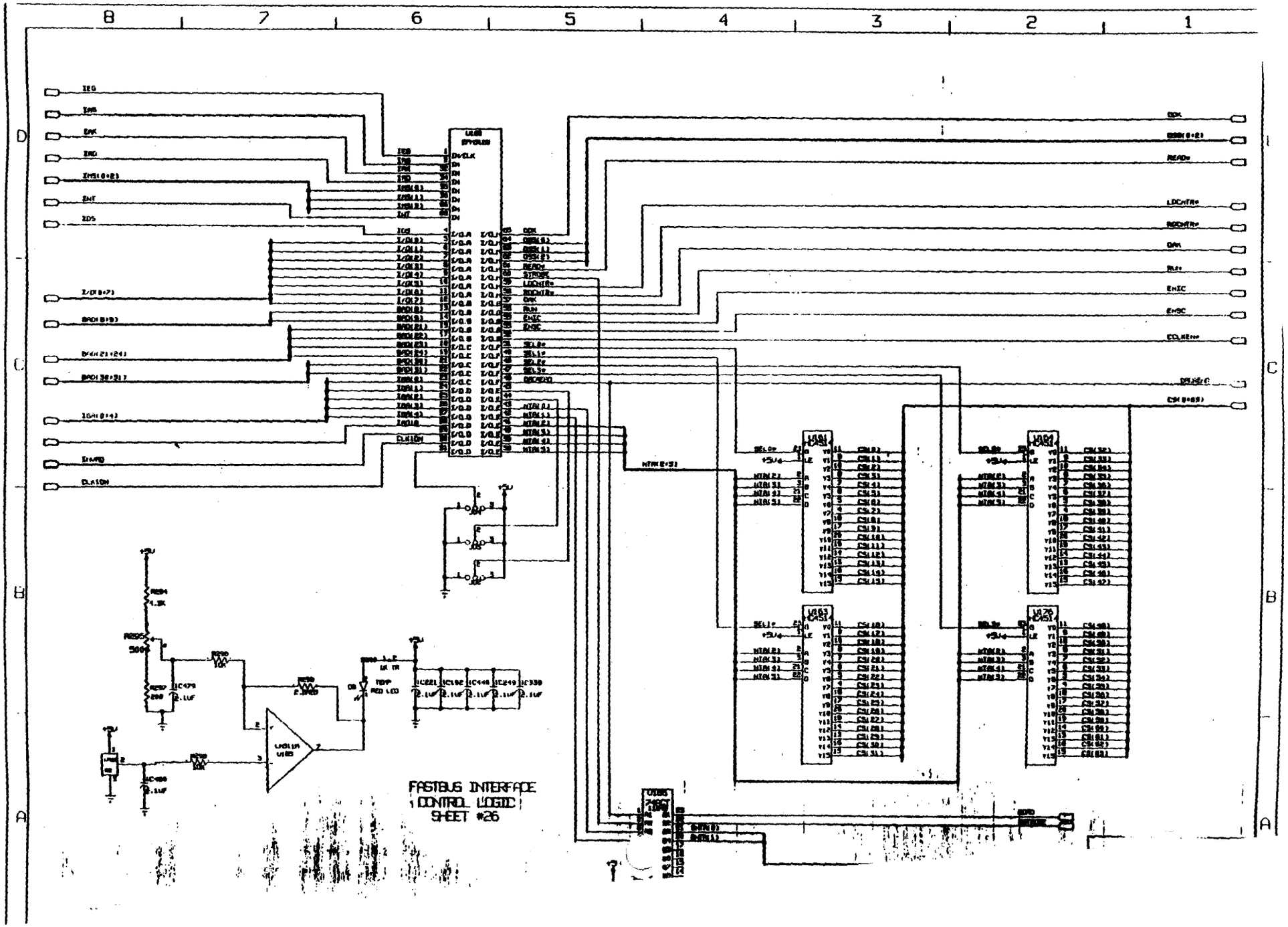
DISCRIMINATOR INPUTS
FROM PREAMP
SHEET #23

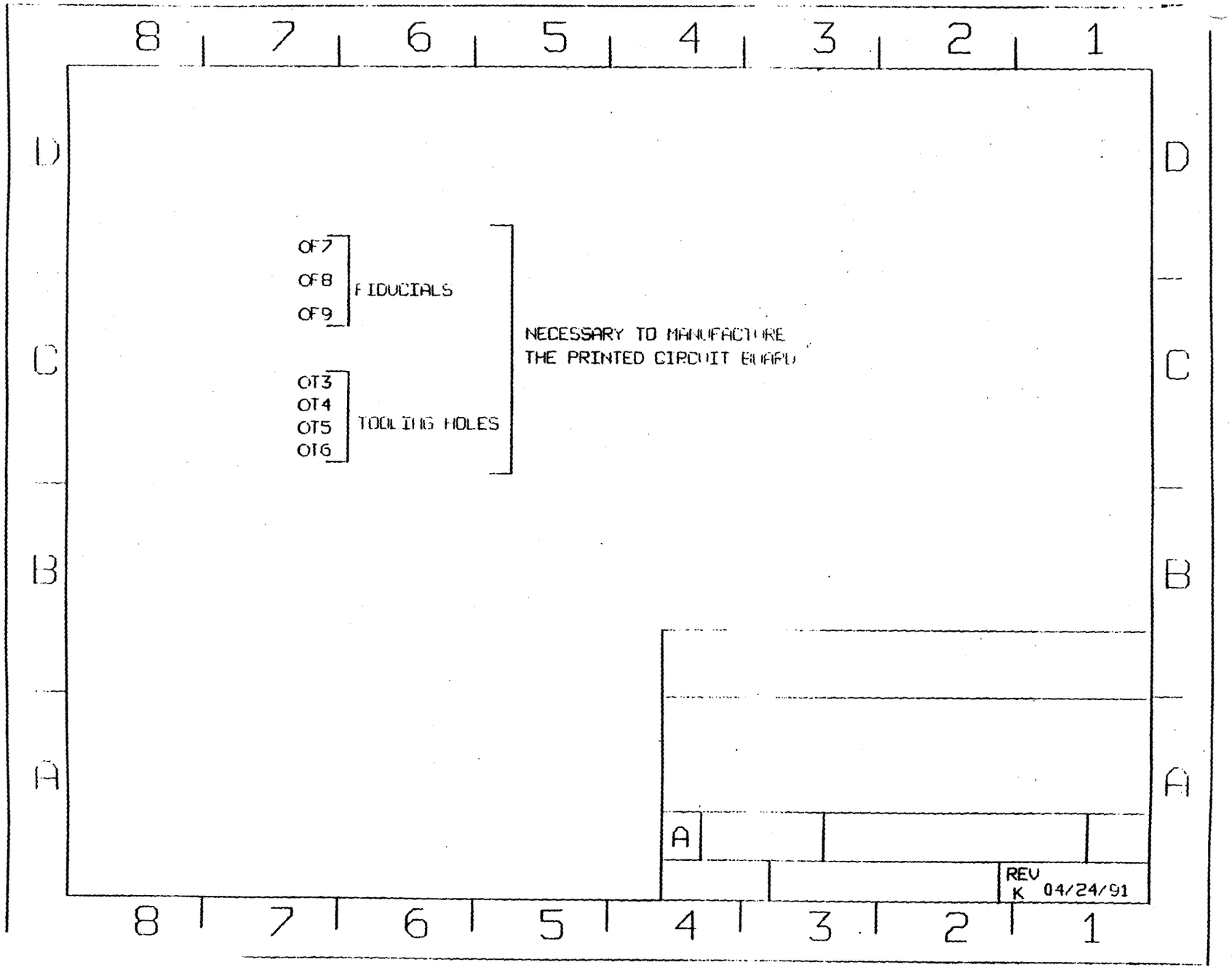
E771 DISCRIMINATOR
DISCRIMINATOR INPUTS
FROM PREAMP

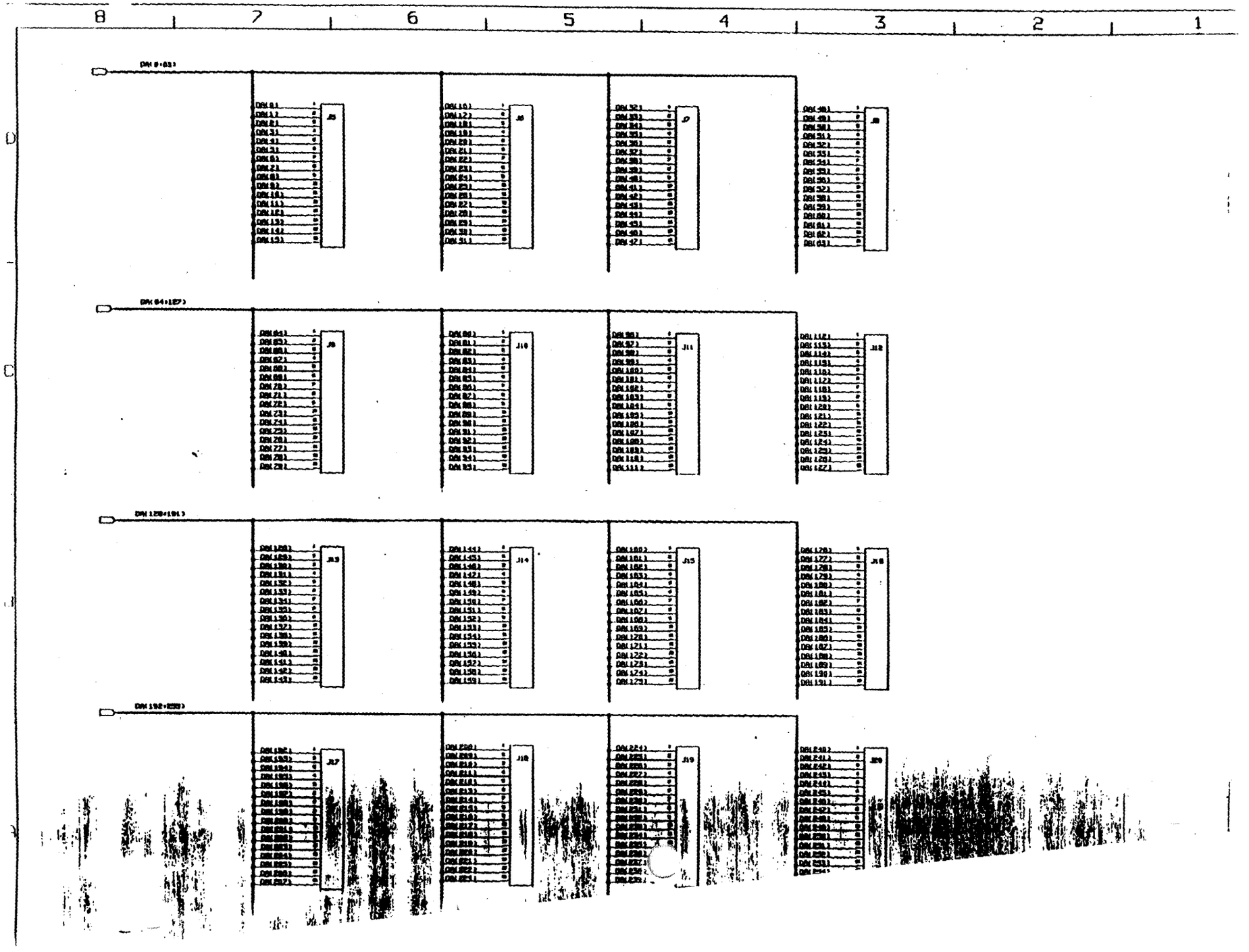
D


8
7
6
5
4
3
2
1
POST AMP COMPARATOR


E771 DISCRIMINATOR
FASTBUS INTERFACE
FASTBUS TRANSLATORS
FASTBUS INTERFACE
FASTBUS TRANSLATORS


FASTBUS INTERFACE
CONTROL LOGIC
SHEET #26

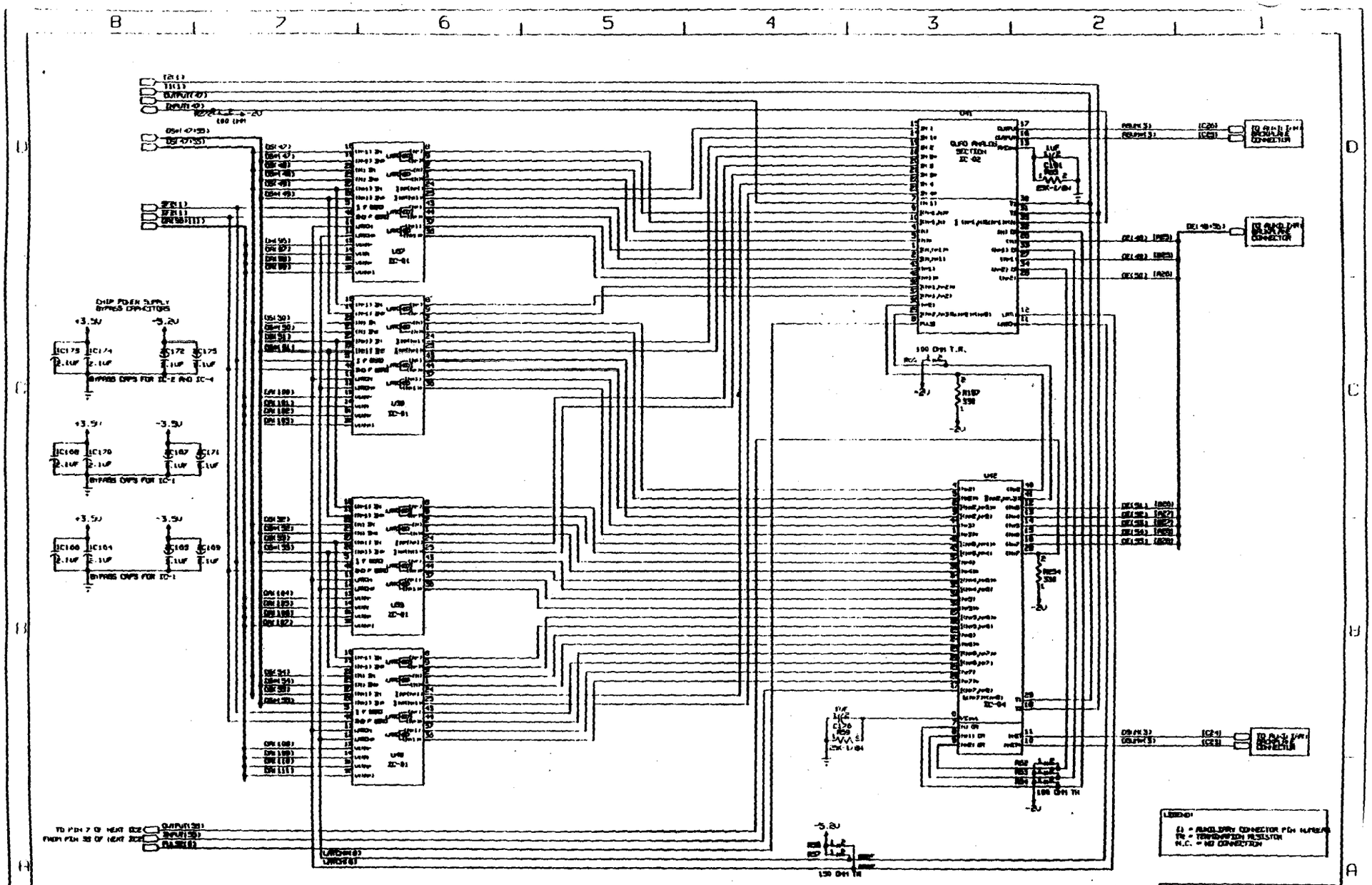

8 7 6 5 4 3 2 1
D
C
B
A
OF7
OF8
OF9
FIDUCIALS
OT3
OT4
OT5
OT6
TOOLING HOLES
NECESSARY TO MANUFACTURE
THE PRINTED CIRCUIT BOARD
A
REV
K 04/24/91


8
7
6
5
4
3
2
1
D
C
B
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
J16
J17
J18
J19
J20

VERSION	NOTES	SHEET #
A		
B		
C		
D		
E		
F	REVERSED INPUTS TO U192 AND CHANGED TO DAC READ	24
G	SWAPPED LABELS FOR E/B AUX CONN C14 & C15	21
H	REMOVED ANALOG GROUND FROM GROUND CONNECTIONS AND REMOVED GROUND FROM F/B AUX CONN C50 ADDED C10	25 21
I	ADDED GNDS C9,C30,C49,C50 C62,C63	21
J	ADDED DELAY CIRCUITRY AND ROTARY SWITCH MODIFIED LED DRIVER	24
K	CHANGED RESISTORS FROM 100 TO 50 OHMS AND MODIFIED BUFFER U186	1,5,9,13 26

E771 DISCRIMINATOR FASTBUS INTERFACE CONTROL LOGIC

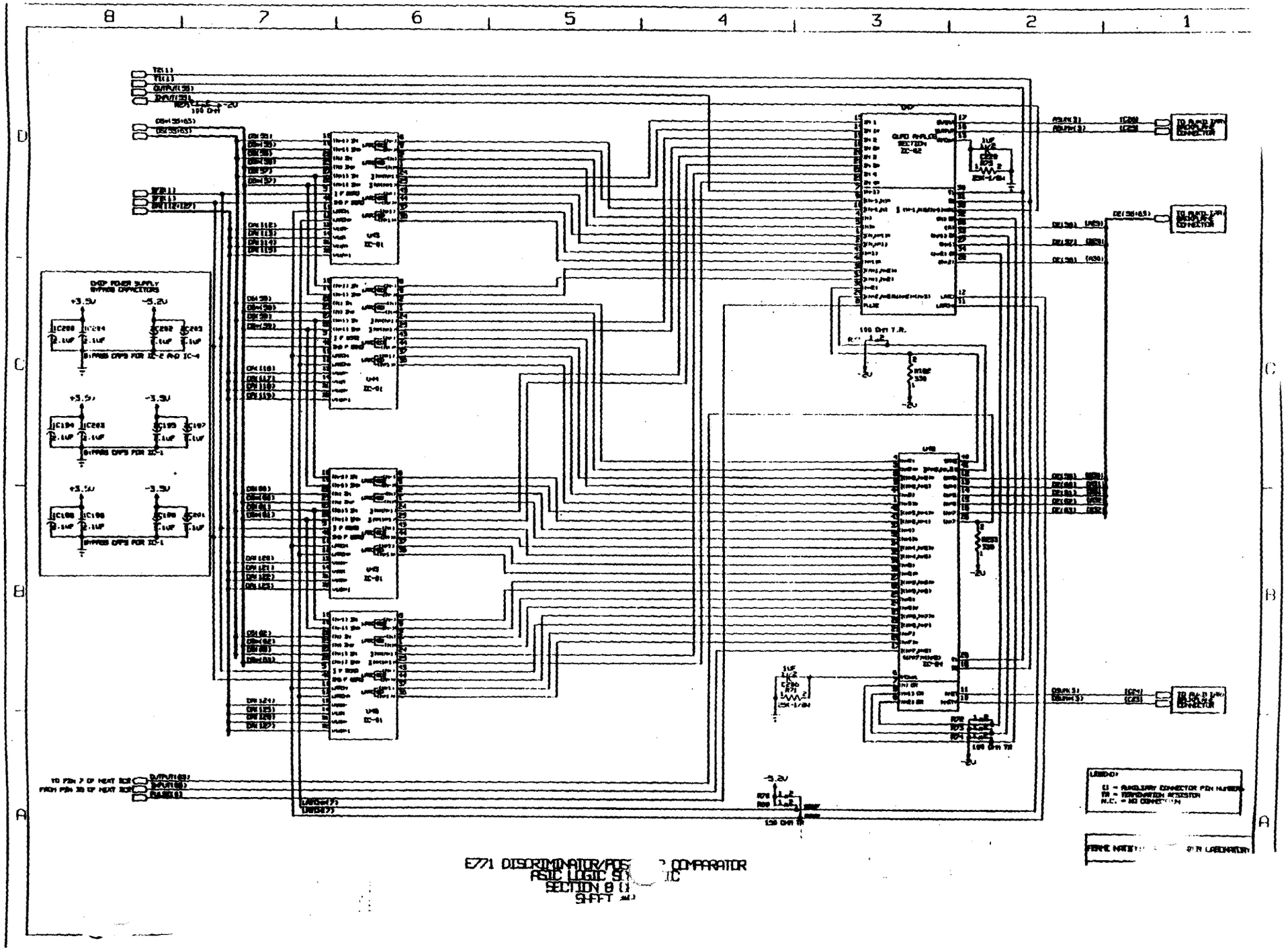
A	NEUMANN HALDEMAN		
			REV K 04/24/91



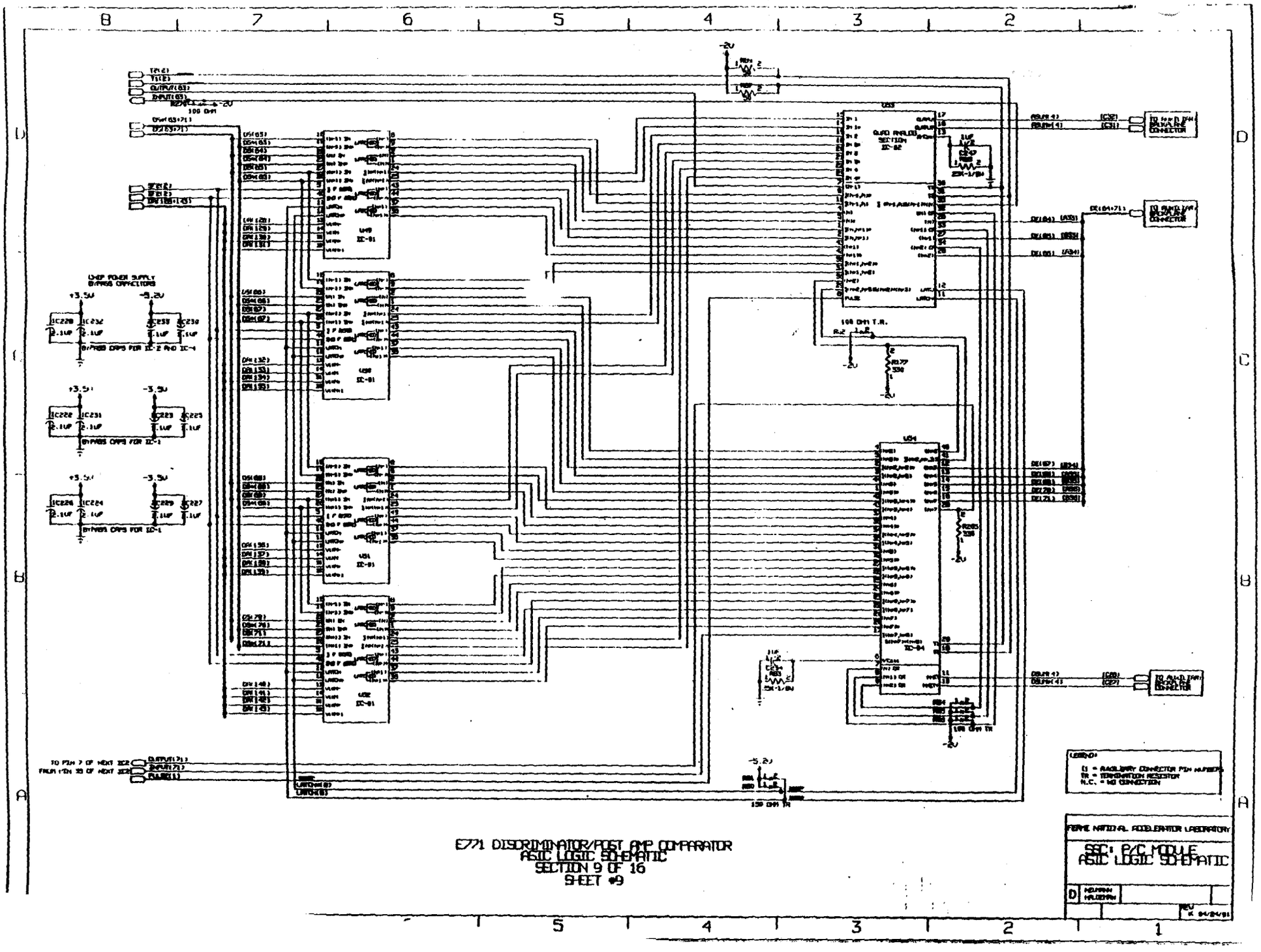
E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 7 OF 16
SHEET #7

FERMI NATIONAL ACCELERATOR LABORATORY

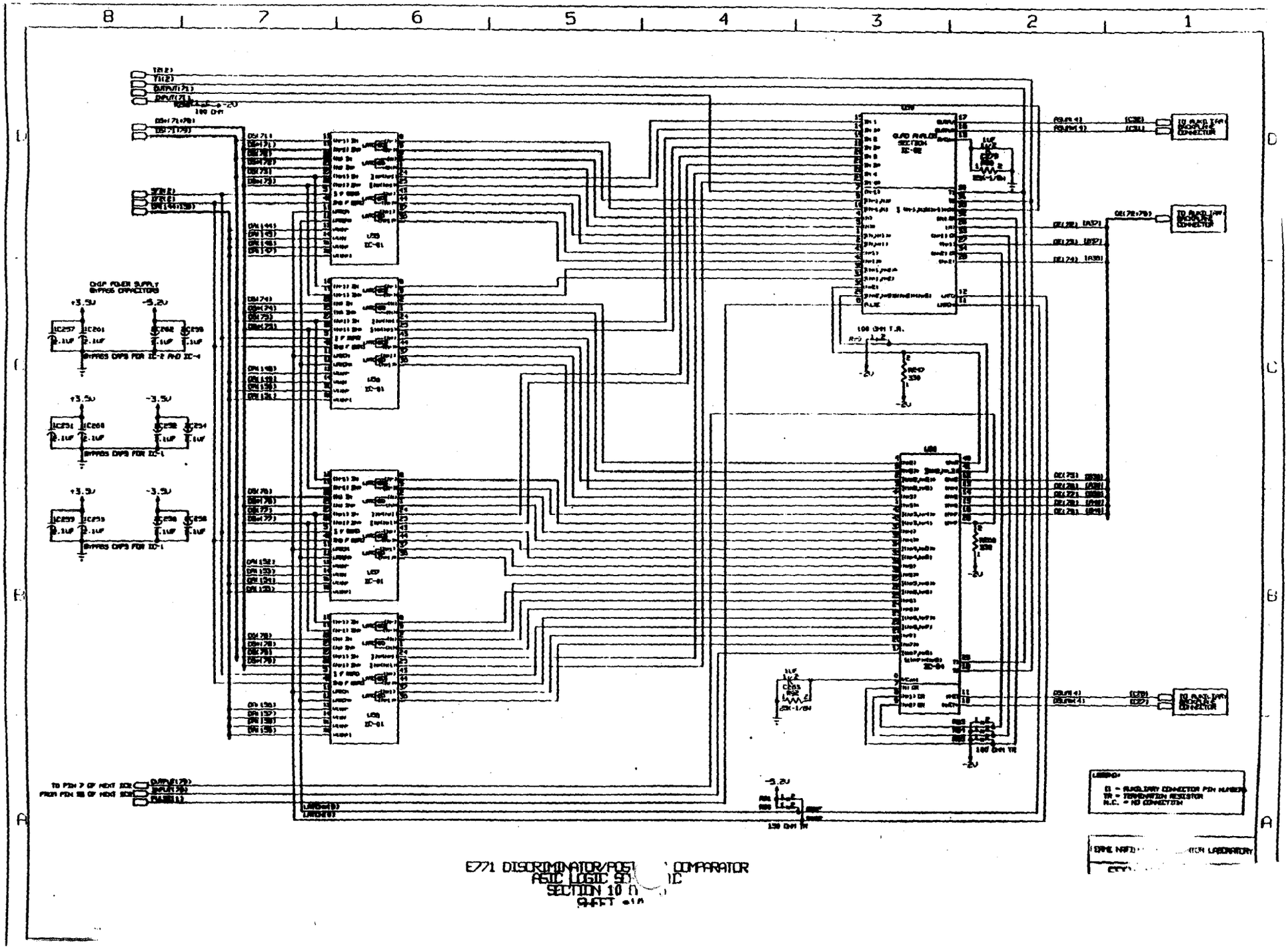
SSC: P/C MODULE
ASIC LOGIC SCHEMATIC



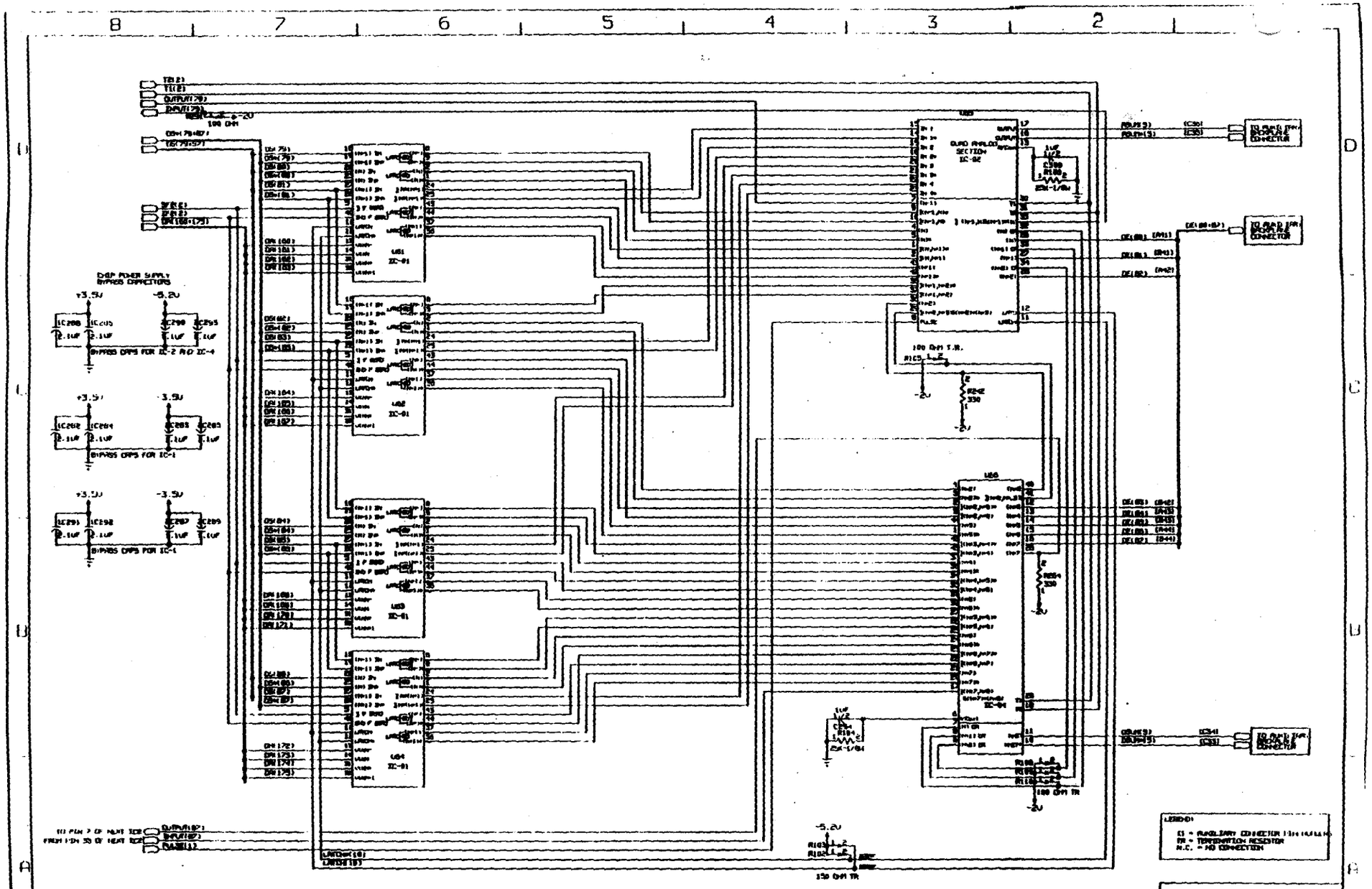
E771 DISCRIMINATOR/POS[illegible] COMPARATOR
ASIC LOGIC S[illegible]IC
SECTION 0 [illegible]
SHEET [illegible]



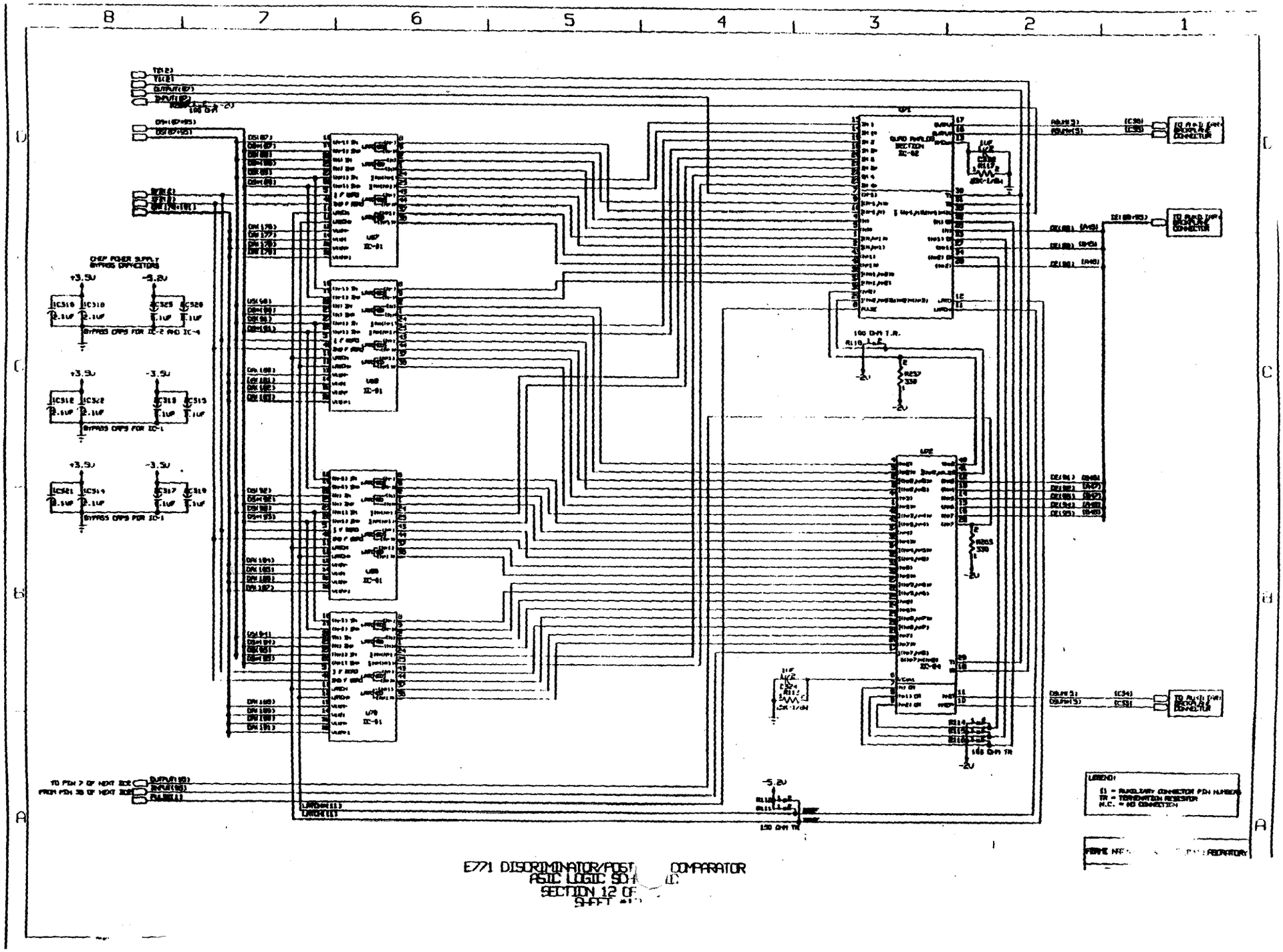
E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 9 OF 16
SHEET #9
FERME NATIONAL ACCELERATOR LABORATORY
SSC: P/C MODULE
ASIC LOGIC SCHEMATIC
LEGEND:
TO AUXILIARY BACKPLANE CONNECTOR



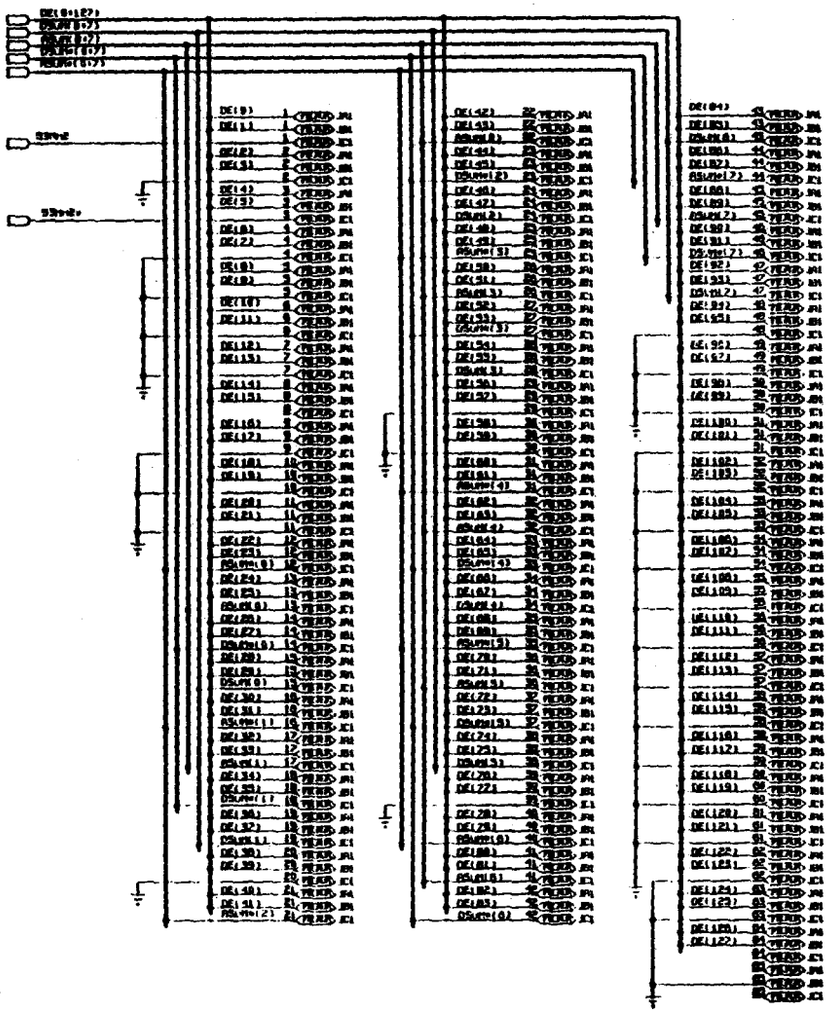
E771 DISCRIMINATOR/POST COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 10 OF
SHEET 10



E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 11 OF 16
SHEET #11

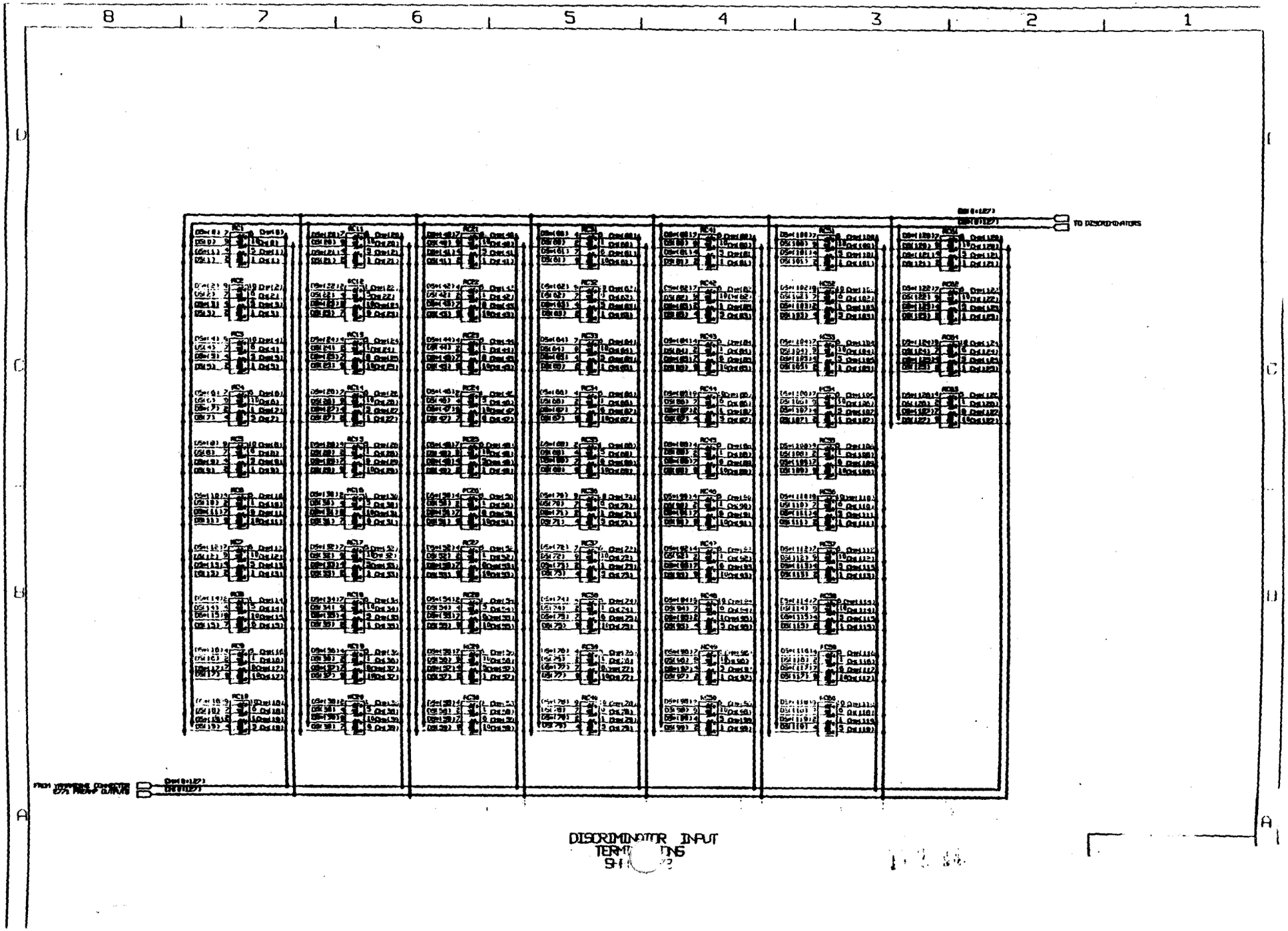


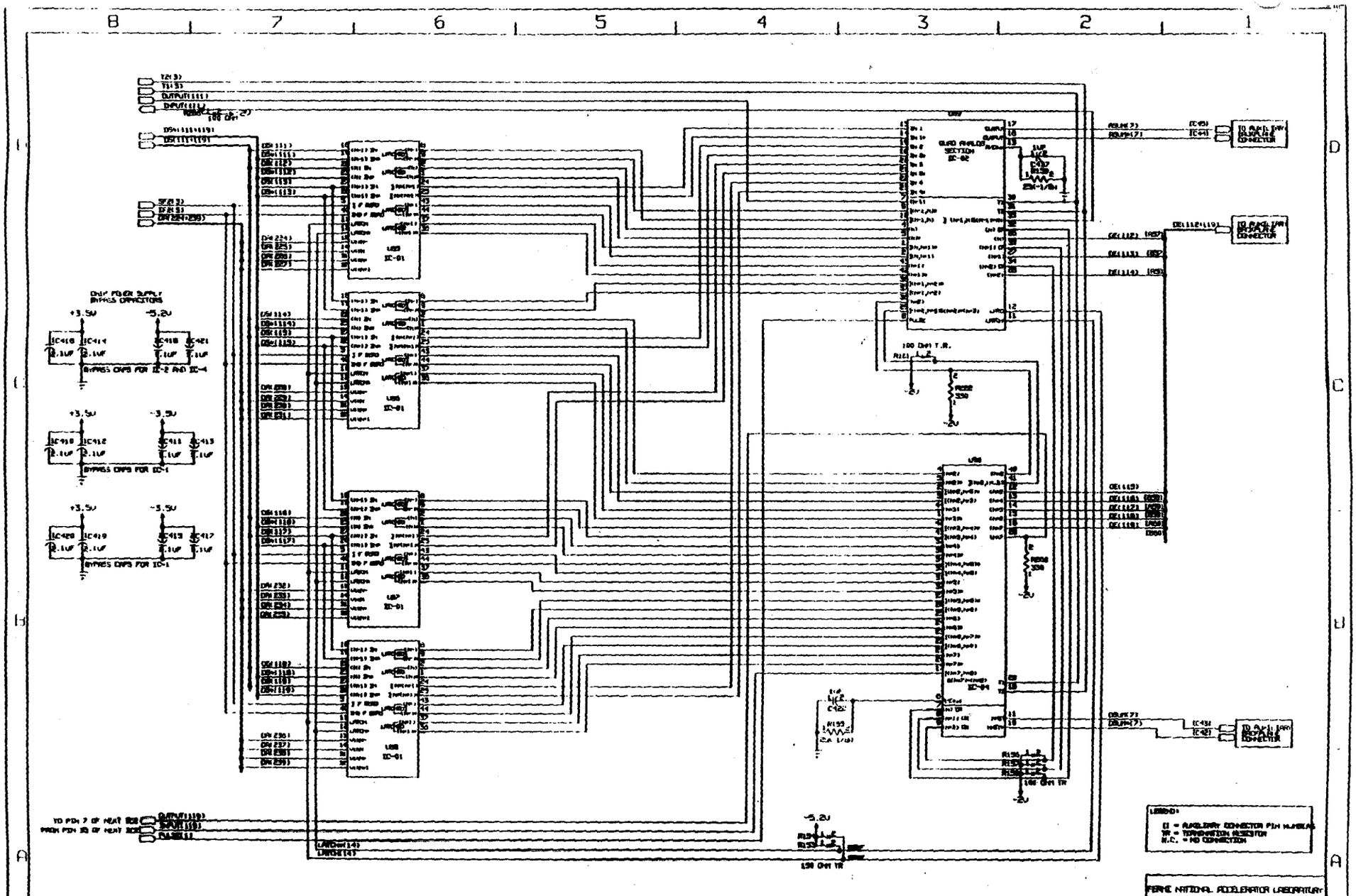
E771 DISCRIMINATOR/POST COMPARATOR
ASIC LOGIC SCH
SECTION 12 OF
SHEET

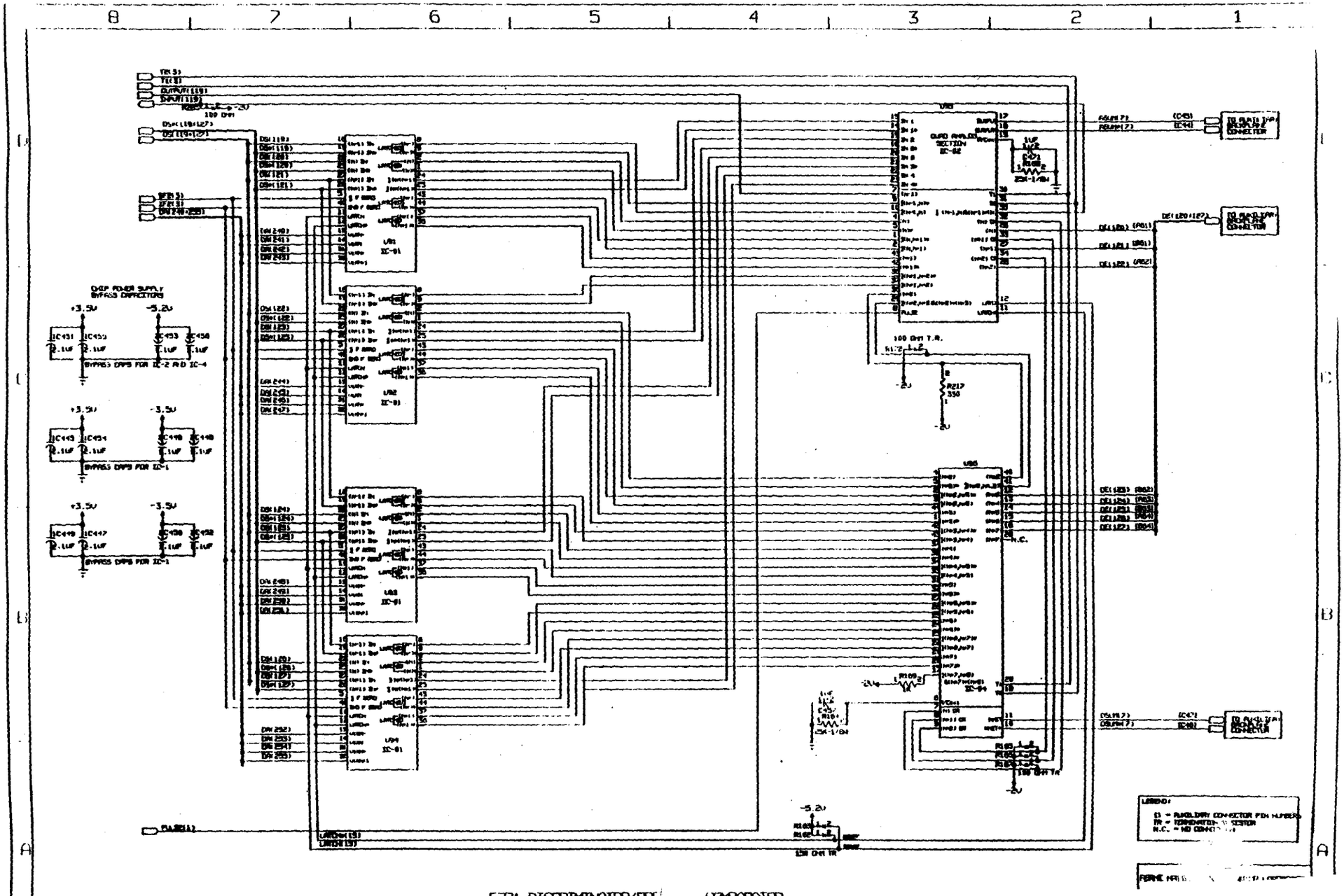


FASTBUS AUXILIARY CONNECTOR
SHEET #21

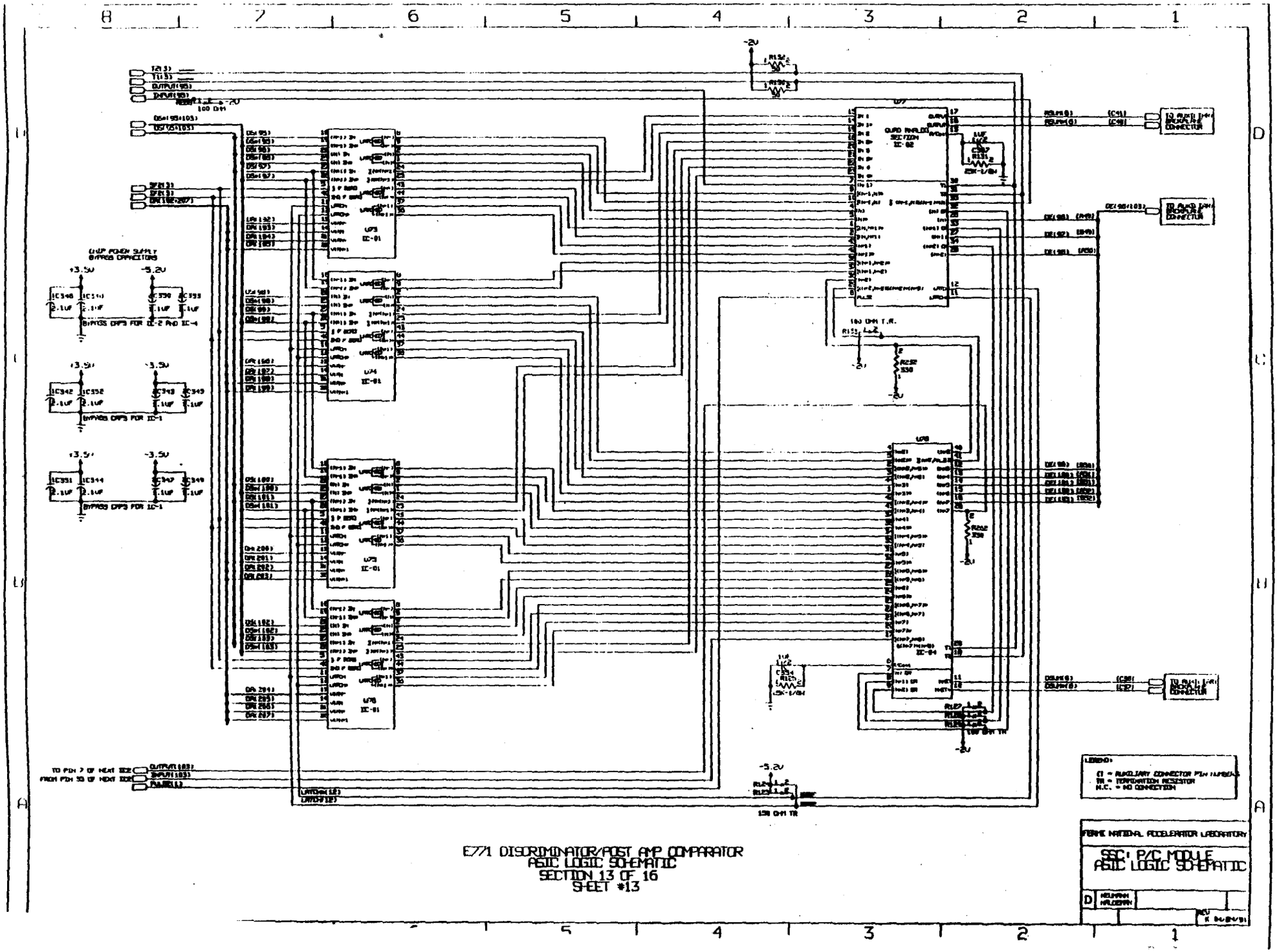
E771 DISCRIMINATOR
FASTBUS AUXILIARY CONNECTOR


8
7
6
5
4
3
2
1
D
C
B
A
TO DISCRIMINATORS
DISCRIMINATOR INPUT
TERMINATIONS

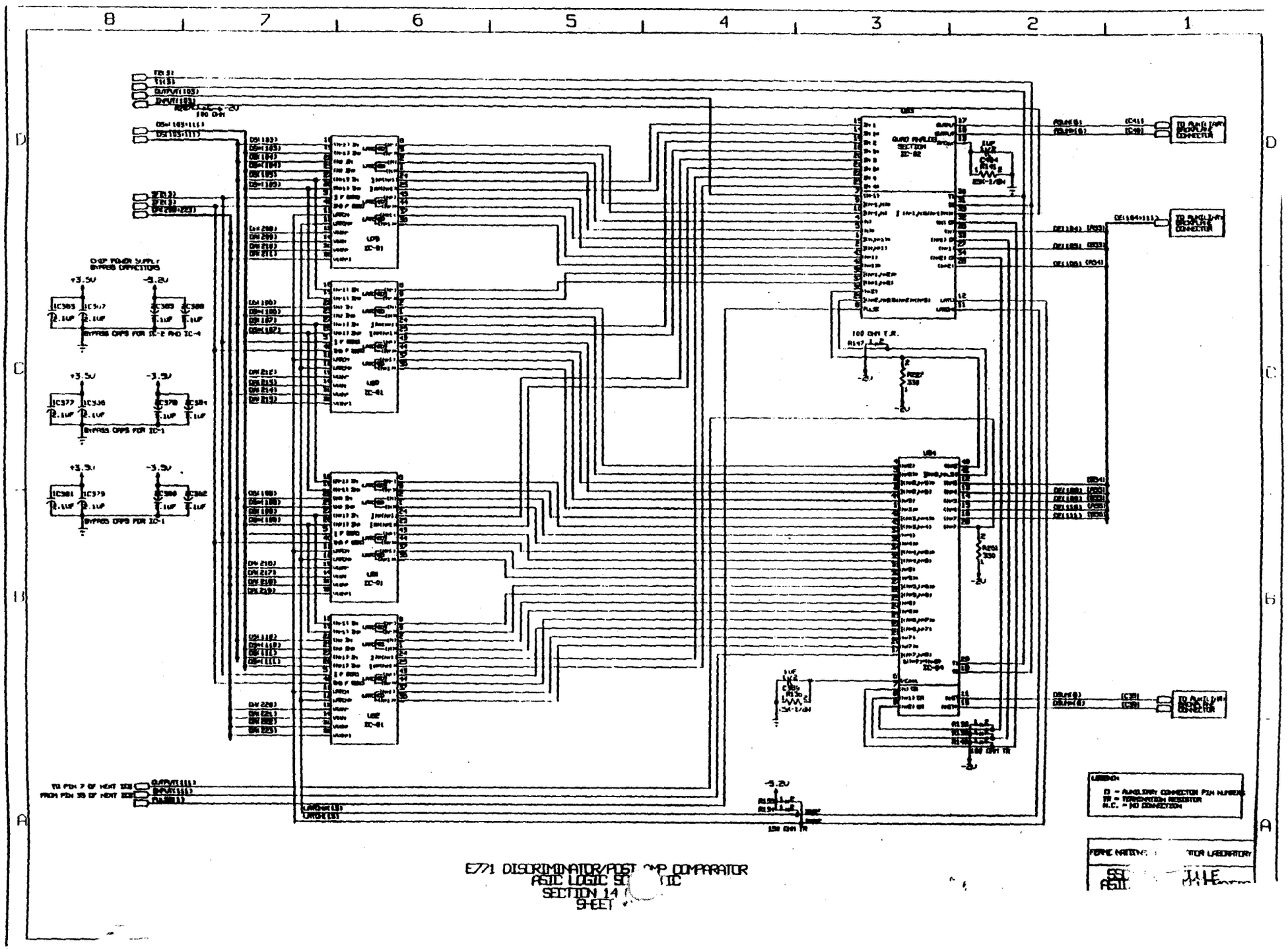

E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 15 OF 16
SHEET #15
FERMI NATIONAL ACCELERATOR LABORATORY
SSC: P/C MODULE
ASIC LOGIC SCHEMATIC



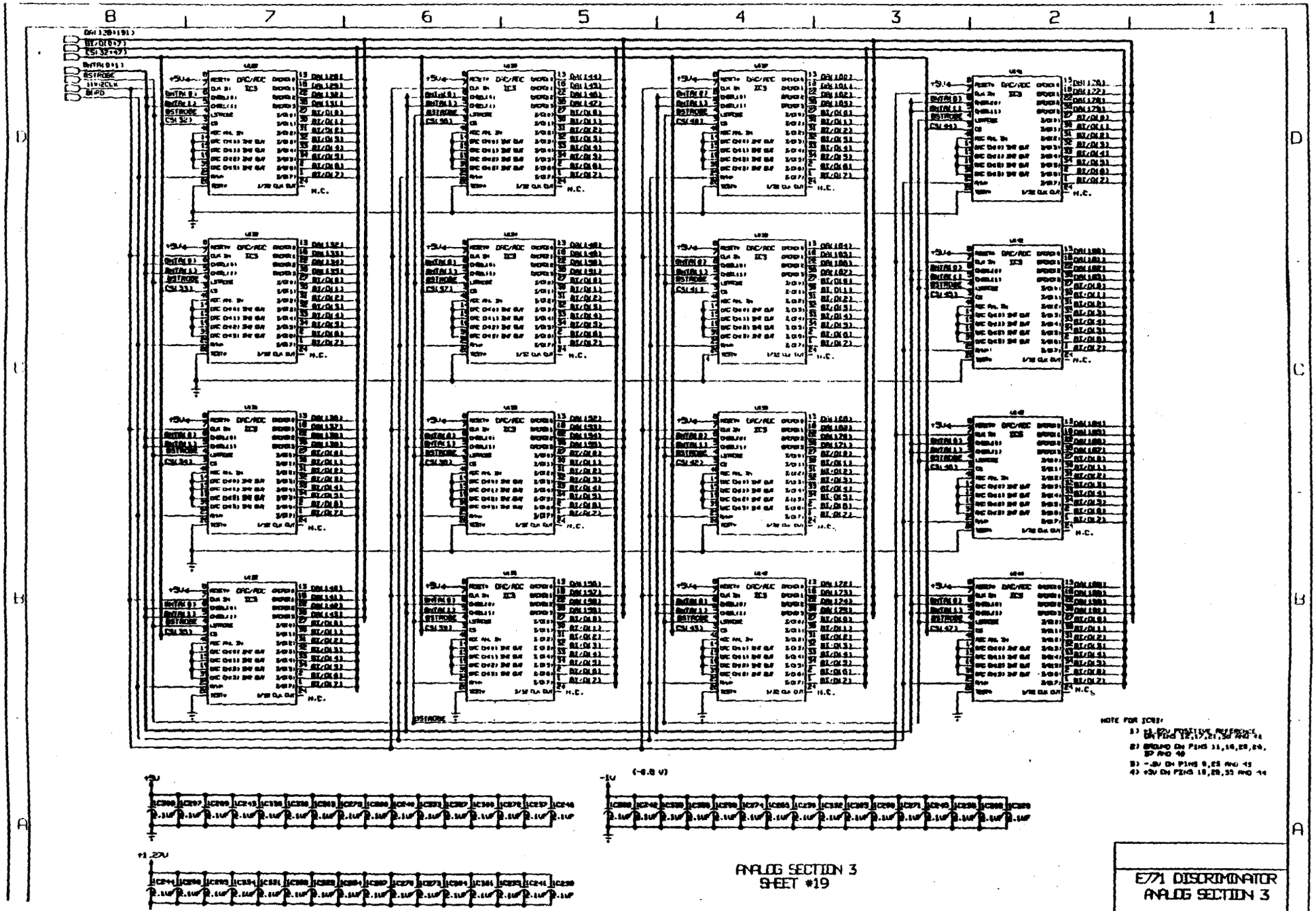
E771 DISCRIMINATOR/PUL[illegible] COMPARATOR
ASIC LOGIC SD[illegible] IC
SECTION 16 OF [illegible]



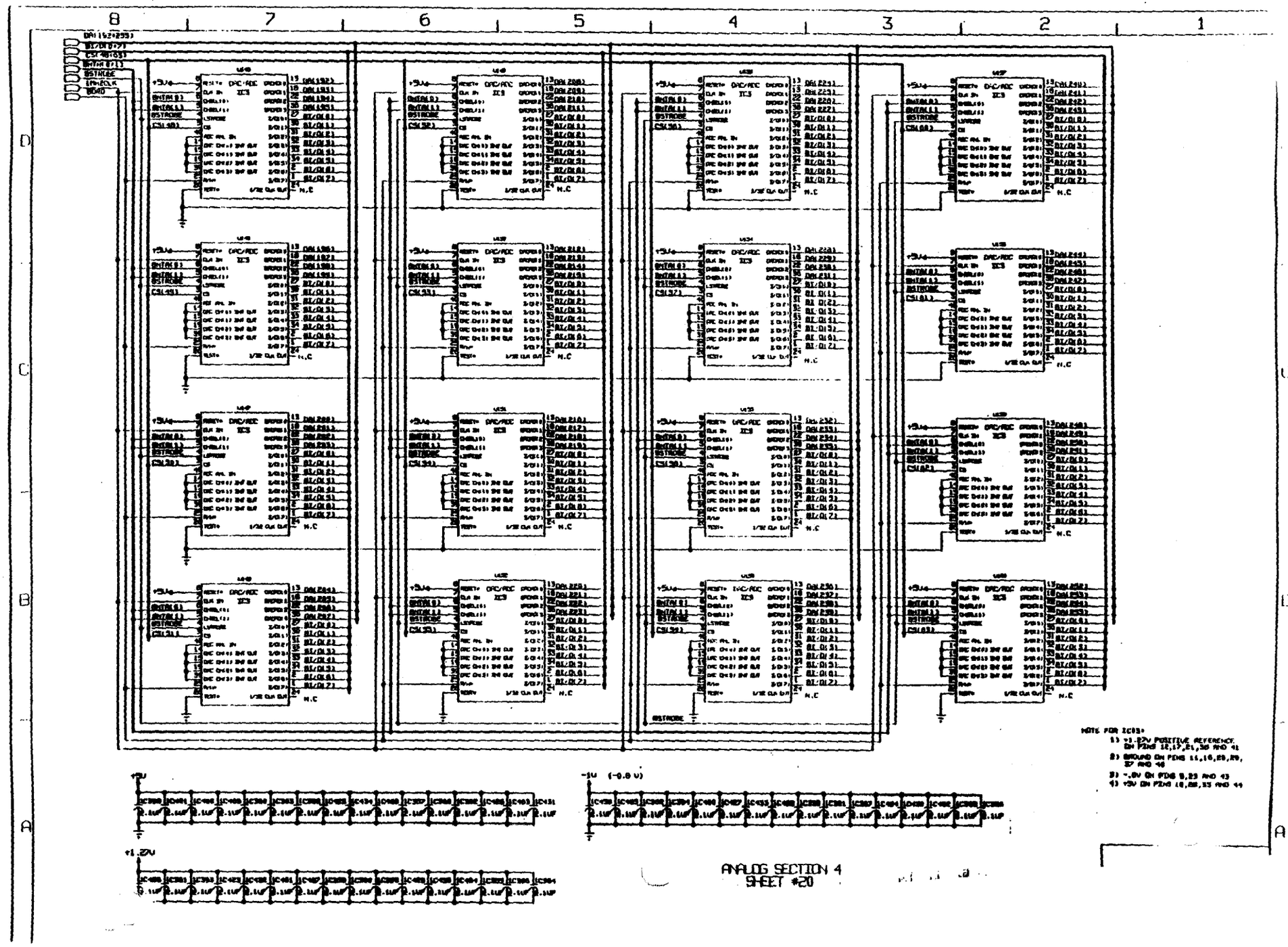
E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 13 OF 16
SHEET #13



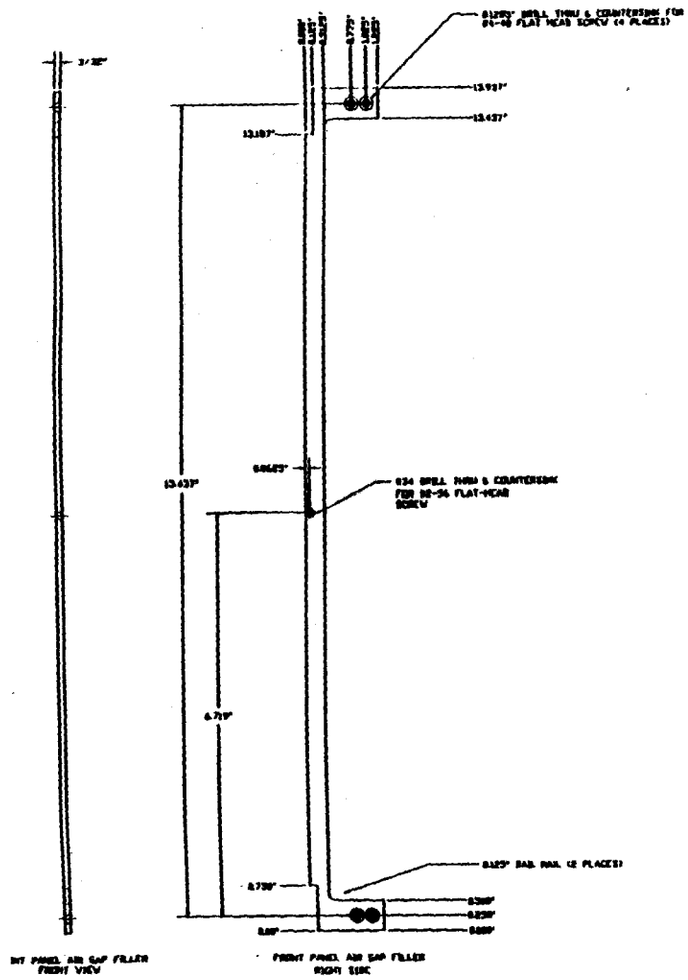
E771 DISCRIMINATOR/POST AMP COMPARATOR
ASIC LOGIC SCHEMATIC
SECTION 14
SHEET



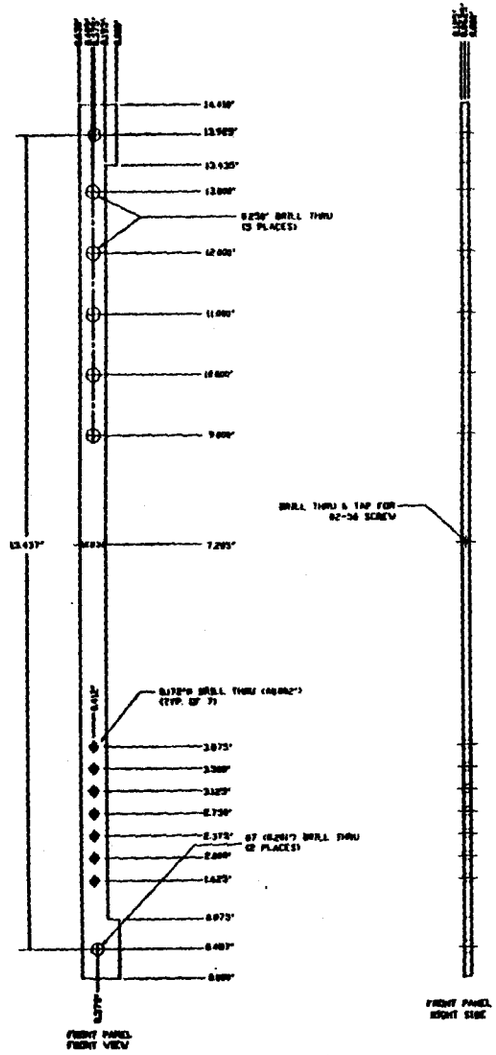
ANALOG SECTION 3
SHEET #19
E771 DISCRIMINATOR
ANALOG SECTION 3



ANALOG SECTION 4
SHEET #20



E771 - POST AMP COMPARATOR FRONT PANEL
AIR GAP FILLER



E771 - POST AMP COMPARATOR FRONT PANEL
DETAILS

D FRONT PANEL SILKSCREEN - 2563.000-MD-215753

ITEM NO.	PART NO.	DESCRIPTION OR SIZE
		PARTS LIST

DRAWN	J. HALBEKIAN	
CHECKED	J. HALBEKIAN	
APPROVED	J. HALBEKIAN	

2563.000-MD-215753

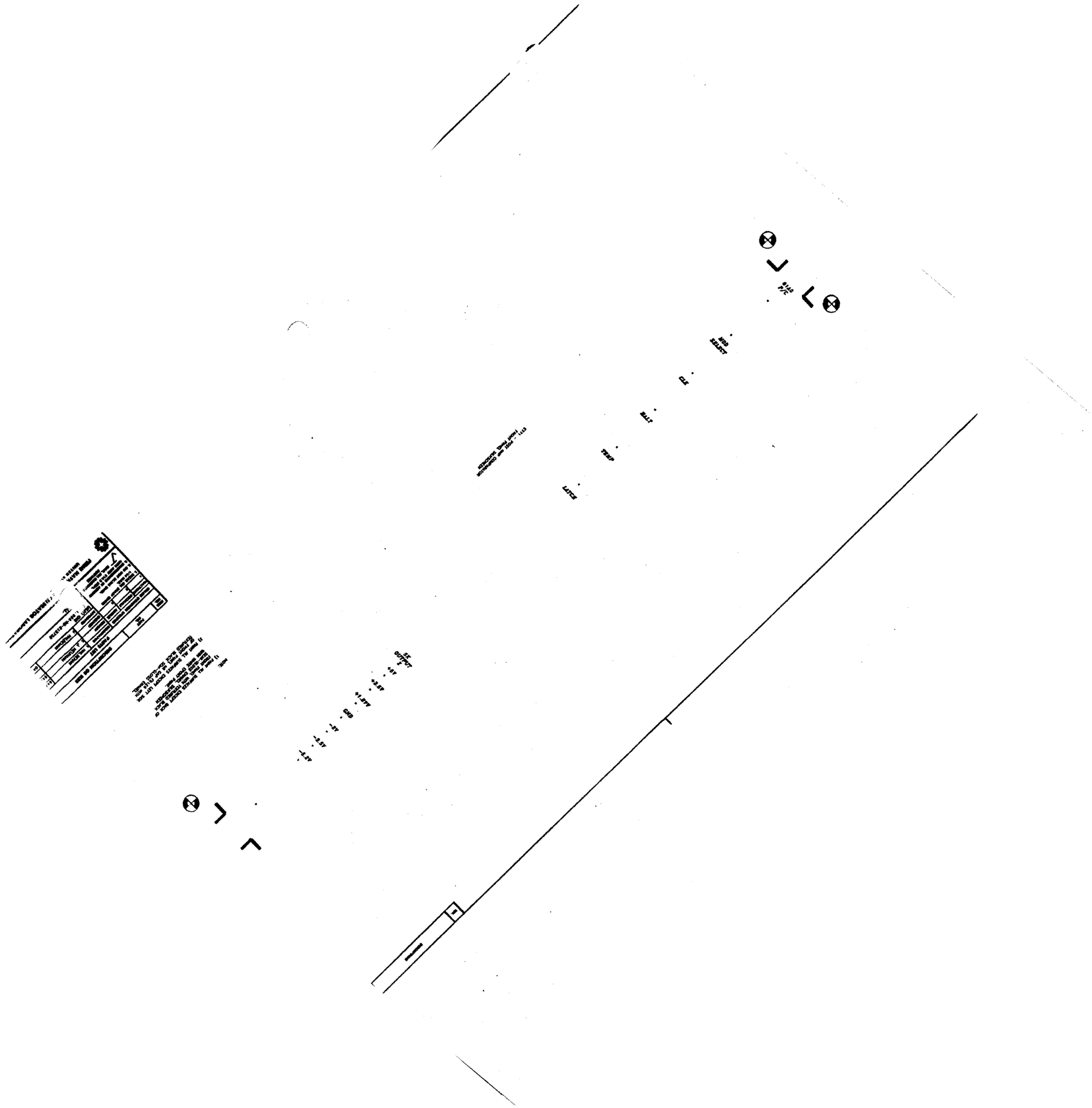
MATERIAL:
1/8" 6061-T6 ALUMINUM

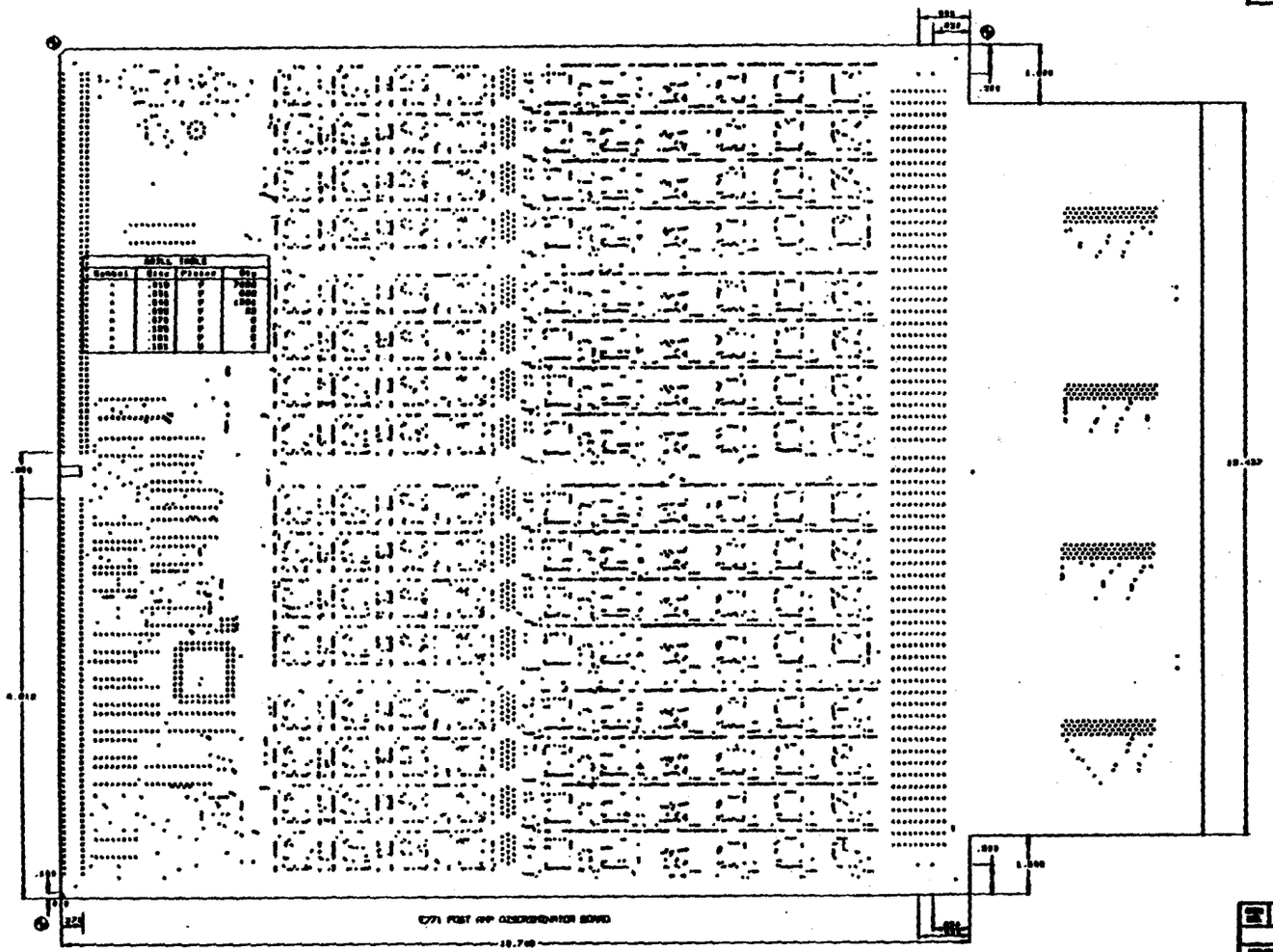
FERMI NATIONAL ACCELERATOR LABORATO
UNITED STATES DEPARTMENT OF ENERGY

EED

E771 - POST AMP COMPARATOR VER III
FRONT PANEL & FRONT PANEL AIR GAP FILLER

SCALE	SIZE	DRAWING NUMBER
1"=1"		2563.000-MD-215752



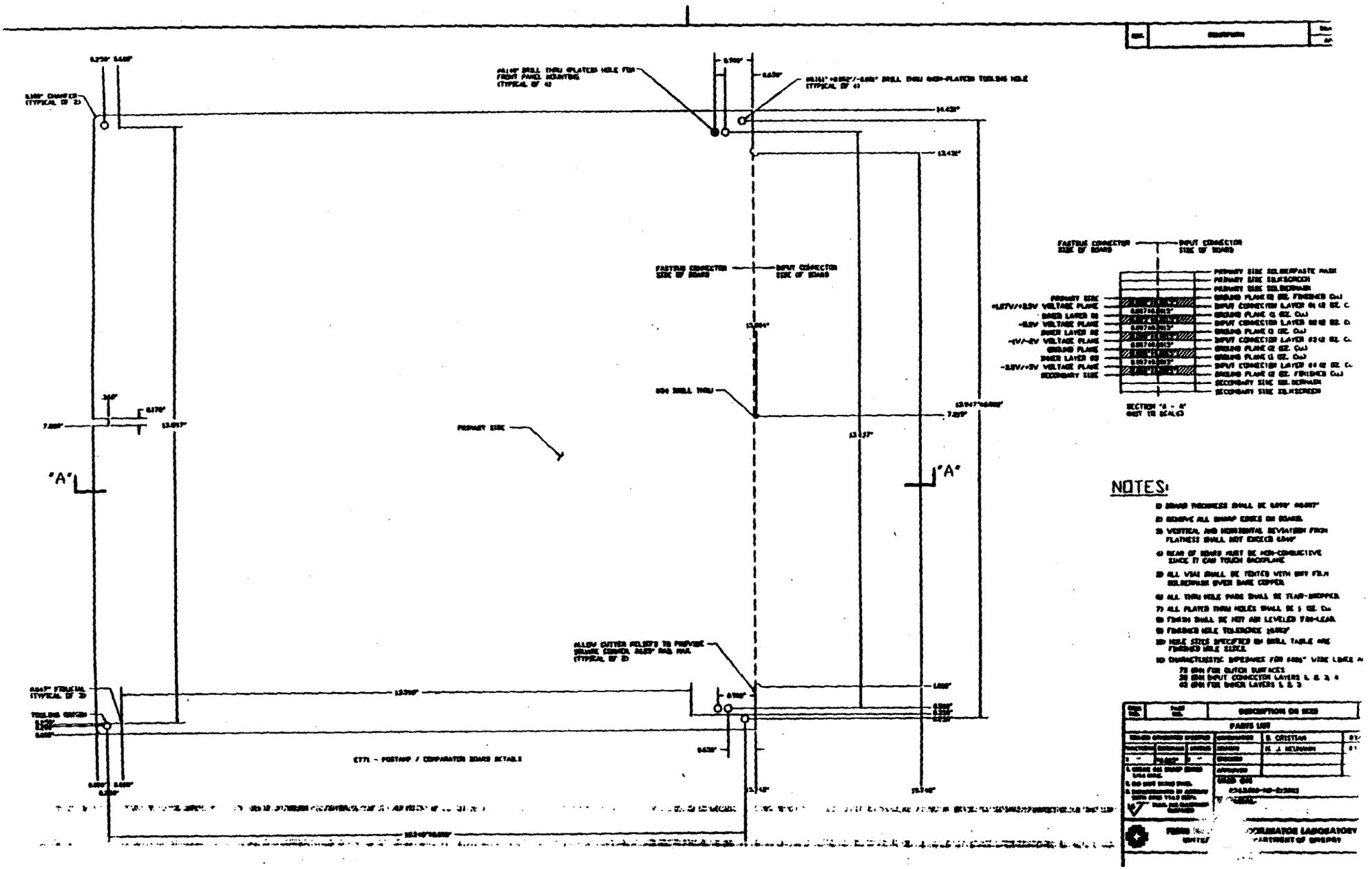


FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

BED
8271-POST AMP COMPARATOR VERSION III
DRILL DRAWING

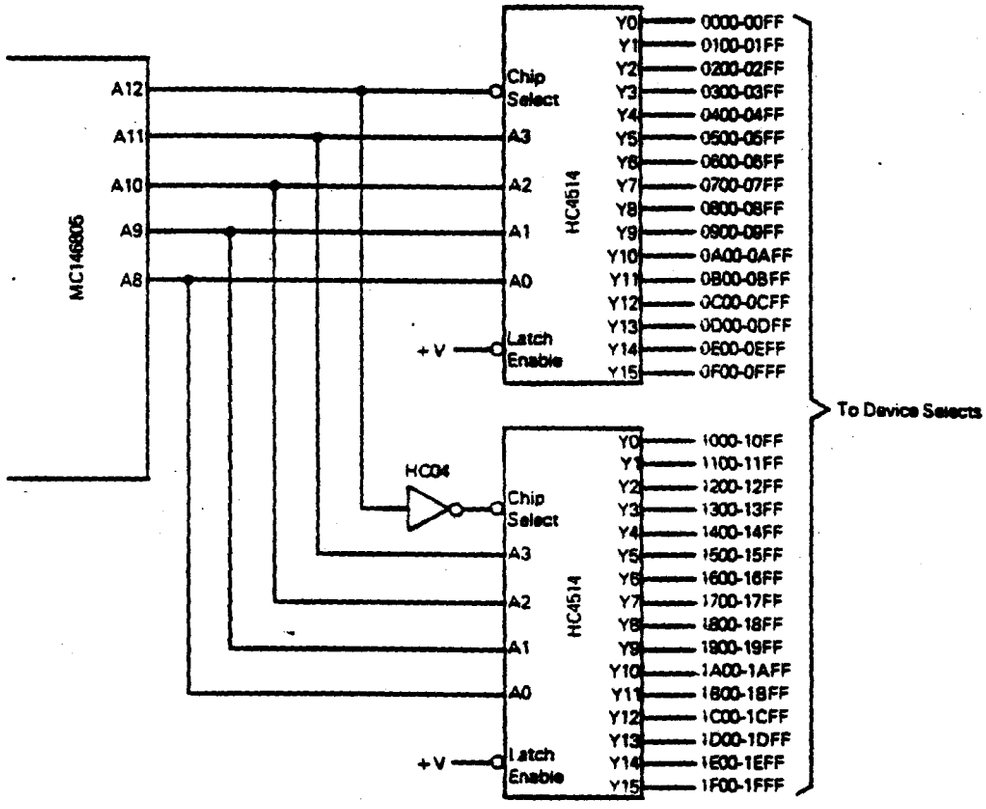
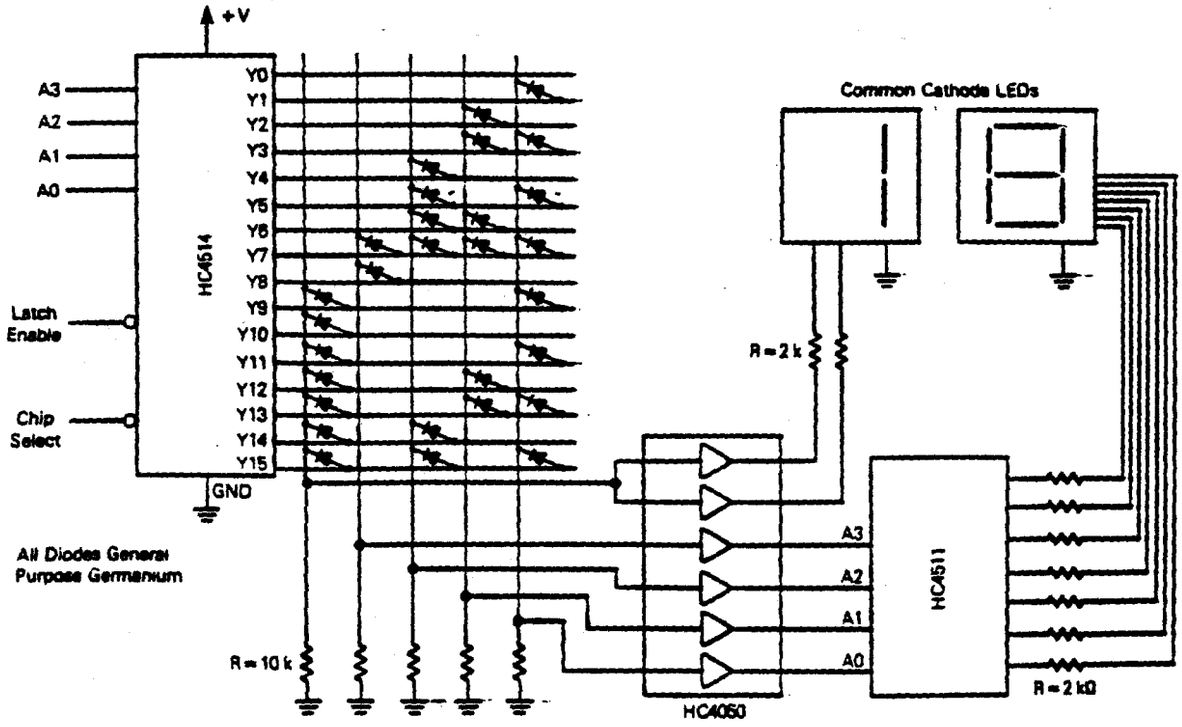
1.24

7512



FASTBUS CONNECTOR SIDE OF BOARD
INPUT CONNECTOR SIDE OF BOARD
PRIMARY SIDE
"A"
"A"
NOTES:
DESCRIPTION OR SIZE
PARTS LIST
S. CRISTIAN
H. J. NEUMANN

MICROPROCESSOR MEMORY DECODING



CODE TO CODE CONVERSION — HEXADECIMAL TO BCD