

CHAPTER 4

SEQUENCER SINGLE BOARD TEST

4.1 INTRODUCTION

The testing of the Sequencer is broken into three separate types of test. The initial low level test are simple peek and poke at FASTBUS registers to fix miswires or broken parts. The second set of test verify that the module works without errors for extended periods, that is test that loop and compare data. The third set of test are high level tests which involve system integration. These last test require that most of the hardware is working and that system test modules are present and working.

The following test are available as low level tests and as tests with looping and compare of data. The final higher level system tests are not described in this document.

4.2 TEST HARDWARE SETUP

The Sequencer stand alone test which are described here require that a sequencer test module be present and working. The Sequencer test module is composed of two parts.

4.2.1 Sequencer Fastbus Test Card

This card resides in a Fastbus slot and emulates the MTC interface for the sequencer and also provides control switches to control the auxiliary cards emulation of the Delay encoder.

Switches are present which select the start and stop strip pattern for generation of events. 4 switches to select a start pattern number and 4 switches to select a stop pattern number. There are also 12 switches which enable/disable which delay encoder channels will have hits. There is a set of 6 switches to select the event size. The last set of 8 switches selects the event address.

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There are buttons to generate sync errors, reset, manual or automatic address valid, write enable, sync, and a reset of the test card.

There are led for

1. ERR TO MTC. indicates that the sequencer has set the error signal.
2. WR ENBL. indicates that the sequencer has received and sent the write enable.
3. SYNC. indicates that the sequencer has received and sent the sync signal.
4. Reset. indicates that the sequencer has received and sent the reset signal.
5. ADR VAL. indicates that the sequencer had received and sent the address valid signal.
6. +5 power and -5 power. indicate presence of power to test card.
7. Error count. is a count of errors detected by the auto test hardware.
8. TEST count. is a count of transfers completed with or without errors.

4.2.2 Sequencer Auxiliary Test Card

This card resides on the SSD aux backplane. It received power from the backplane as well as from a cable to the fastbus backplane. This card emulates 12 delay encoders and also test the auxiliary interface. (See attachment for more detailed description.)

4.2.3 Cables

There are 5 cables which must be connected before testing can begin.

1. CLK 53MHZ. This is generated by the FASTBUS test card and a cable must be connected between the 53MCLK lemo of the test card and the 53MCLK lemo of the Sequencer.

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2. SYNC. This signal is generated by the FASTBUS test card and a cable must be connected between the SYNC lemo of the test card and the SYNC lemo of the Sequencer.
3. MTC interface 34pin ribbon. This cable must connect between the FASTBUS test card and the Sequencer. It has all the signals which are normally generated by the MTC. (ie. ev_adr(0:7), Write enable, address valid, reset, ...)
4. Test card interface. This 40 pin ribbon connects control signals and status between the FASTBUS test card and the Auxiliary test card.
5. Aux power. This cable provides additional power for the auxiliary test card for the standard fastbus backplane.

4.3 TEST PROGRAM FILES

The Sequencer test program is integrated into the SSD single board test program. The Sequencer test are part of a program SE_TEST.

There are a number of include files which must be present in SSD_DIAG libraries. The ones specific to the sequencer are:

4.3.1 SEERS.H

This is a definition of the error bit fields which get set during the test program operation. They are used to display status but are mainly for debugging difficult to understand errors.

4.3.2 SEREG.H

This is a definition of the sequencer register bit fields. Some of the fields are specific for building event data for checking errors. The bit field definitions simplify the test programs setting and clearing of bits and display of status.

4.3.3 SEQPAT.H

This is a definition of an array which contains fixed patterns which are present in the sequencer auxiliary test card

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for generation of delay encoder events.

4.3.4 CURCON.H

This is a definition of cursor control bit strings which simplify the cursor control commands.

4.3.5 CURCON.C

This is a set of basic cursor control commands. (i.e. clear screen and set cursor position.)

4.4 SEQUENCER ACCES THROUGH SINGLE BOARD TEST MENU

Before starting the tests the Sequencer should be located in slot 13 (D)

of the crate. Use the SET PRIMARY ADDRESS option of the Single Board TEST (SBT) menu to confirm the address value.

The sequencer test can be executed in automatic mode or in manual test mode. To enter automatic mode the test card switches must first be set to enable all encoder channels and generate 2 word events with start and stop pattern 0 and 1. Select the SBT option for Default test Menu to enter

auto mode. Set desired mode (ie. stop on error) then execute test. If errors occur the test program will return an error and stop or go to a test menu or continue.

To operate in manual mode select the SBT menu option for Sequencer menu.

You will receive the sequencer test menu.

4.5 SEQUENCER MENU

----- Sequencer Main Menu -----

- a) Single Transfer menu
- b) Block Transfer menu
- y) Sequencer Auto test
- g) Sequencer menu
- i) Set loop counter ,se nbr loops
- m) Set Primary Address (PAD) (hex value: *se_pad)

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- n) SAD (hex value: *se_sad)
- r) display read buffer
- s) load write buffer
- w) Map FASTBUS crate
- u) Show or reset Status Summary, TOTAL errors= se_ERS_total
- x) Exit Program

Enter se_command:

In response to the prompt select an option by typing the letter on the left. The response is not case sensitive. In some cases another submenu will be displayed.

4.5.1 I) Set Loop Counter ,se_nbr_loops

In the main menu display option I shows the value of se_nbr_loops which is the number of times a test will be executed. Select option I and you can change this value. The following prompt will be displayed.

Enter loop value (dec) :

If you type a value of 0 the tests will loop until a key is pressed to stop them.

4.5.2 M) Set Primary Address (PAD) (hex Value: *se_pad)

Main menu option M shows se_pad, which is the value of the FASTBUS primary address which will be used for the tests. The following prompt will be displayed.

Enter PAD (in hex):

4.5.3 N) SAD (hex Value: *se_sad)

Option N shows the value of the FASTBUS secondary address which will be used or was used. The following prompt will be displayed.

Enter SAD (in hex):

4.5.4 A) Single Transfer Menu

In response to the selection of option A the subprogram process_se_single_transfer(se_pad,envid,action) will be called

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and the following menu will be displayed.

----- Single Transfer Menu -----

- a) FRD
 - b) FWD
 - c) FRC
 - d) FWC
 - n) Print read data after every loop ,print_data
 - o) Inc SAD after each loop ,inc_st_sad
 - p) Inc write data after each loop ,inc_st_data
 - x) Exit this menu
- Enter se_command:

4.5.4.1 A) Single_transfer_read_data -

The FSCC will do a FASTBUS read of data space using the previously selected FASTBUS primary address (se_pad), secondary address (se_sad) and will loop for se_nbr_loop times. The data value read will be displayed each time. The option of incrementing data or secondary address toggled by option P or 0 respectively.

If errors are detected in the FASTBUS return status the following message will be printed if in GET_MENU mode.

FASTBUS error at PAD: se_pad SAD: se_sad

The following message will be printed with each FRD loop.

SAD (in hex): se_sad Value (in hex): se_read_data

4.5.4.2 B) Single_transfer_write_data -

Selecting the FWD option will provide the following prompt.

Enter data value (in hex):

The FSCC will do a FASTBUS write to data space using the previously selected FASTBUS primary address (se_pad), secondary address (se_sad) and will loop for se_nbr_loop times. The data value you select will be written each time with the option of incrementing data or secondary address selected by option P or 0 respectively.

If errors are detected in the FASTBUS return status the following message will be printed if in GET_MENU mode.

FASTBUS error at PAD: se_pad SAD: se_sad

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4.5.4.3 C) Single_transfer_read_control -

The FSCC will do a FASTBUS read of control space using the previously selected FASTBUS primary address (se_pad), secondary address (se_sad) and will loop for se_nbr_loop times. The data value read will be displayed each time. The option of incrementing data or secondary address toggled by option P or 0 respectively.

If errors are detected in the FASTBUS return status the following message will be printed if in GET_MENU mode.

FASTBUS error at PAD: se_pad SAD: se_sad

The following message will be printed with each FRD loop.

SAD (in hex): se_sad Value (in hex): se_read_data

4.5.4.4 B) Single_transfer_write_control -

Selecting the FWC option will provide the following prompt.

Enter data value (in hex):

The FSCC will do a FASTBUS write to control space using the previously selected FASTBUS primary address (se_pad), secondary address (se_sad) and will loop for se_nbr_loop times. The data value you select will be written each time with the option of incrementing data or secondary address selected by option P or 0 respectively.

If errors are detected in the FASTBUS return status the following message will be printed if in GET_MENU mode.

FASTBUS error at PAD: se_pad SAD: se_sad

4.6 U) SHOW STATUS DISPLAY

Option U in main menu shows se_ERS_total, which is the total errors which have already occurred. If selected STA_SUM(action,se_pad,envid) will be called and the following status display will be shown.

Summary Screen

PAD: se_pad SAD: se_sad

The Executing Test is in Reverse graphic

se_CSR000_tst errors : se_ERS_000

se_CSRC00_tst errors : se_ERS_C00

Block Word counter tests, se_CSRC10_tst errors :se_ERS_C10

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Clock delays tests, se_CSRC11 tst errors :se_ERS_C11
Overflow status register, se_CSRC12 tst errors : se_ERS_C12
Encoder event fifo, se_ECF_tst errors : se_ERS_ecf

read: %x write: %x\n",se_read_data,se_write_data);
se_data_rec: # se_ignore_rec: # se_rf_rec: # se_ovf_rec: #
se_strip_rec: # se_id_rec: #
Wd cnt exp: # rec: # Blk cnt exp: # rec: #
errors this test: # SubTotal tests : # Total data errors: %x
Total errors : se_ERS_total Total tests : se_TOT_tst
on last data error read: se_read_data write: se_write_data

Do you wish to reset the status? (Y) or (N):

4.7 W) MAP THE FASTBUS CRATE

Selecting this option will call the following program.
map_crate(action,se_pad,envid). The FSCC will sequentially
address each slot at CSR space with secondary address 0. Only
response with FASTBUS status FENORM will display the following:

Module with ID: se_read_data responds to PAD: *se_pad

When complete the FSCC will prompt with:

Press Q to return to menu

To this you must type a key followed by return to return to the
main menu.

4.8 R) SE_DISPLAY_READ_BUFFER()

This option will display the contents of the read buffer.
The following will be displayed

Last buff_loc used was : se_buff_loc
Enter starting offset (in hex):

The se_buff_loc is the last used read buffer location. You
select a buff location value to display. Then the following will
be printed.

%08lx %08lx %08lx %08lx %08lx

This is a block of values found at the selected buffer locations
followed by the following prompt.

Continue?

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If you type Y the display will again show more values starting at the next location. A N response will abort the display and return to the main menu.

4.9 S) SE_LOAD_WRITE_BUFFER()

Selection of option S will display the following menu.

```
----- Display Menu -----
a) Clear write buffer
b) Load write buffer with bit pattern
c) Load write buffer with ascending integers
d) Load write buffer with long words
e) Load write buffer with '55555555,AAAAAAAA'
f) Copy read buffer to write buffer
w) Display write buffer
y) Load write buffer with dataset[i] pattern
h) Load dataset[i] with write buffer pattern
x) exit
Enter se_command:
```

4.9.1 A) Clear Write Buffer

This option if selected will clear the write buffer from location 0 to se_buff_length as set by the global at beginning of the program.

4.9.2 B) Load With Bit Pattern

This option will produce the following prompt

```
Enter bit pattern (in hex):
```

The program will then fill the write buffer from location 0 to se_buff_length with the selected pattern.

4.9.3 C) Load Write Buffer With Ascending Integers

This option will load the write buffer with ascending values starting with location 0 with the value 0 until se_buff_length is loaded with value se_buff_length.

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4.9.4 D) Load Write Buffer With Long Words

This option will prompt with the following.

Starting offset (in hex):

You select the buff location then the following is displayed.

i : se_wrbuff(i) New value (exit with '.') :

Where i is the buff location and you select a value or type . to terminate this option. If a value other than . is selected the next location will be displayed and a new value can be entered.

4.9.5 E) Load Write Buffer With '55555555,AAAAAAAA'

Loads the write buffer with the pattern 55555555 to location 0 then AAAAAAAAAA to location 1 then repeats the sequence until se_buff_length is reached.

4.9.6 F) Copy Read Buffer To Write Buffer

Copies the contents of the read buffer to the write buffer.

4.9.7 Y) Load Write Buffer With Datasel[i] Pattern

Loads the write buffer with the datasel pattern which was previously set.

4.9.8 H) Load Datasel[i] With Write Buffer Pattern

Loads the datasel buffer with the contents of the write buffer. The datasel buffer is only a 16 location array which is used when checking for expected events. This is meant to duplicate the patterns which might be set by hardware test module sequences.

4.9.9 W) Display Write Buffer

To display the contents of the write buffer select option W. The following will be displayed

Last buff_loc used was : se_buff_loc

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Starting offset (in hex):

To this you select the buffer location which you wish to display and the following will be displayed

```
se_wrbuff[loc],se_wrbuff[loc+1],se_wrbuff[loc+2],se_wrbuff[loc+3]
```

After the array of data has been displayed the following prompt will be given.

Continue?

To this if you type Y more data will be displayed but if you type N the routine will be terminated and the program will return to the main routine.

4.10 Y) SEQUENCER AUTO TEST

This option in the main menu will call the following routine.

```
process_seqauto(action,se_pad,envid)
```

This routine will in turn call the following routines.

```
sqt_000(action,se_pad,envid);      /* Process CSRO tests */
sqt_C10(action,se_pad,envid);      /* Process CSR C0000010 tests */
sqt_C11(action,se_pad,envid);      /* Process CSR C0000011 tests */
sqt_C12(action,se_pad,envid);      /* Process CSR C0000012 tests */
sqt_ecf(action,se_pad,envid);      /* Process Encoder fifo tests */
```

4.11 G) SEQUENCER MANUAL TEST

This option in the main menu will call the following subroutine.

```
process_seqtst(action,se_pad,envid)
```

The following sub menu will be displayed.

```
----- Sequencer Manual test Menu -----
a) Geographic addressing
b) NTA load and increment
c) Set start and stop pattern dataset[i],se_start_pat,se_stop_pat
d) Set Valid Delay encoder channels dvs_number
f) Set Event data size se_ev_data_size maxbytes= se_maxbytes
h) CSRO tests
i) CSR C0000000-C000000B Ram tests
j) CSR C0000010 tests
```

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- k) CSR C0000011 tests
 - l) CSR C0000012 tests
 - m) Encoder fifo tests
 - o) Dump registers
 - p) Set ignore error flag %x \n#,se_ignore_err
 - q) Display error in compare read and write buffers
 - x) Exit this menu
- Enter se_command:

4.11.1 A) Geographic Addressing

Selection of this option will cause geographic data space addressing of the sequencer to be tested using the address selected by se_pad. The FASTBUS operation executed will be a primitive address cycle without a secondary address or a data cycle followed by a address cycle release if an AK was returned. The test will loop depending upon se_nbr_loop. The following messages will be printed if there are fastbus errors.

FASTBUS error at PAD: se_pad

If there is an error in the release of the FASTBUS the following message will be printed.

FASTBUS address release error at PAD: se_pad

4.11.2 B) NTA Load And Increment

This test will address the module at se_pad and perform a secondary address write followed by a secondary address read. When errors are found the following message will be printed.

FASTBUS error at PAD: se_pad SAD: se_sad

If the value read is not the value written to the NTA then the following message will be printed.

Bad NTA error at PAD: se_pad SAD: se_sad Read: se_bufspec

4.11.3 C) Set Start And Stop Pattern Datasel[i],se_start_pat,se_stop_pat

This option will allow you to change the value of the start and stop test pattern for the strip field when checking for events in the ECF test routine. The following messages will be printed.

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Starting pattern address (in hex):

Stop pattern address (in hex):

The normal response to these prompts is the switch setting of the Sequencer FASTBUS test card for the respective settings of start and stop pattern.

4.11.4 D) Set Valid Delay Encoder Channels Dvs_number

If selected this option will prompt for which encoder channels are enabled. This data will be used when checking incoming events for the correct data. The normal response to the prompt is the setting of the Sequencer FASTBUS test card setting for the individual channel enables 12 switches or values 0 to 4096. Each bit position is a separate channel enable. The prompt received is as follows.

Set encoded Valid Delay encoder channels:

4.11.5 F) Set Event Data Size Se_ev_data_size Maxbytes= Se_maxbytes

To set the size of the expected event select option F. The following prompt will be displayed.

Set Delay encoder event size:

The response should be the same setting as is on the Sequencer FASTBUS test card switch for event size. It is a byte count of each of the expected Delay encoder channels. Each channel will have the same byte count. Only one value will be expected. Total event size and byte count will be calculate using this number with the number of channels enabled and ignore words.

4.11.6 H) CSRO Tests

When option H is selected the following sub test will be executed. `int sqt_000(action,se_pad,envid)` This test will read and write patterns to the valid bits of CSRO and check if errors occur. If an error occurs the `int se_erinc(action,se_pad,envid)` subprogram will be called to increment the error count and then the following display programs will be called.

`int se_display_subtest(action,se_pad,envid)` Which will print the following message to the screen at a fixed screen line.

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errors this test: # SubTotal tests se_sub_TOT_tst: #

int se_display(action,se_pad,envid) Will then be called and the status summary of STA_SUM(action,se_pad,envid) will be displayed. The test will then terminate by calling int se_endtest(action,se_pad,envid) and prompting with the following:

Press return to exit:

To this prompt a key must be pressed followed by a return and the program will then return to the sequencer manual test sub menu.

4.11.7 I) CSR C0000000-C000000B Ram Tests

This test will execute as above in test H with the exception that tests will be performed on the CSRC locations of the Sequencer. By calling the int sqt_C00(action,se_pad,envid) test program.

4.11.8 J) CSR C0000010 Tests

This test will execute as above in test H with the exception that tests will be performed on the CSRC-10 locations of the Sequencer. By calling the int sqt_C10(action,se_pad,envid) test program.

4.11.9 K) CSR C0000011 Tests

This test will execute as above in test H with the exception that tests will be performed on the CSRC-11 locations of the Sequencer. By calling the int sqt_C11(action,se_pad,envid) test program.

4.11.10 L) CSR C0000012 Tests

This test will execute as above in test H with the exception that tests will be performed on the CSRC-12 locations of the Sequencer. By calling the int sqt_C12(action,se_pad,envid) test program.

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4.11.11 M) Encoder Fifo Tests

This test will execute as above in test H with the following exceptions. The tests will be performed on the data space 0 locations of the Sequencer. The program called will be `int sqt_ecf(action,se_pad,envid)`. This routine must be set up if not in `Stop_on_err` mode or `Get_menu_on_err` mode. The setup information comes from responses to prompts in this section of the program and those previously selected for configuring the event. The Sequencer FASTBUS test card and the Sequencer Aux test cards must be attached or these test might be confusing. The following prompt will be typed.

Do you want to reset the Sequencer (Y) :

If Y is selected routine `int sqt_rst(action,se_pad,envid)` will be called and the bit 30 (reset) will be set and written to CSRO of the sequencer at `se_pad`. If not selected Y then be careful about how the previous values of CSR registers were set.

Then the following will be printed.

Read event with single word transfers (Y) :

The program can read the Sequencer event data in block transfer mode or single transfers based upon this response.

After the above responses have been made the program will then call the `sqt_ecf_buff(action,se_pad,envid)` routine which will prompt for the following.

Do you wish to load ID ram with incrementing pattern? (Y) or (N):

This will load the ID ram of the Sequencer if Y is selected.

Do you wish to set the RF flag? (Y) or (N):

This will set the RF flag in the expected event if Y is selected.

Do you wish to disable the aux fifo? (Y) or (N):

Do you wish to disable the FASTBUS fifo? (Y) or (N):

The enable bits of the Sequencer buffers will be set depending on the response to the above prompts.

Events will now be read, when ready press G for go :

When ready to start taking events press G return. The test card should at this time be armed and data sent to the Sequencer. Pressing G will cause the program to read the Sequencer for the expected events and compare the data calling normal routines as in the previous routine H. That is status will be displayed with

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error checking.

4.11.12 0) Dump Registers

An additional status display is present which shows the registers. The option causes `int sqt_dr(action,se_pad,envid)` to be called which will read each register and display the status in the following format.

```
----- Sequencer Register dump -----  
  
CSRO errs: wr: # rd: # cmp: #  
CSRC00 errs: wr: # rd: # cmp: #  
CSRC10 errs: wr: # rd: # cmp: #  
CSRC11 errs: wr: # rd: # cmp: #  
CSRC12 errs: wr: # rd: # cmp: #  
  
CSRO : ID: # OT: # FEF: # AIF: #  
  
CSR10 : Blockcount: # Wordcount: #  
  
CSR11 : Clk1 delay: # Clk2 delay: #  
  
CSR12 : Sync err: # Encoder fifo overflow: #  
  
Valid Delay encoder channels #  
  
start and stop pattern dataset[i] # , #  
  
Event data size: # maxbytes: # maxwds: #  
Fastbus status:
```

The following prompt will then be given to select more event data display.

Display event info Y ?

If Y is the response then the following will be typed.

```
se_ev_idbuf:  
    se_ev_idbuf[i],se_ev_idbuf[i+1],se_ev_idbuf[i+2],se_ev_idbuf[i+3]);  
  
se_event_data.bit: FLAG: se_event_data.bit.flag  
SE_EVENT_DATA.bit: ID: # , strip: # , RF: #  
se_event_data.word: se_event_data.word  
se_event_last.bit.blockcount: se_event_last.bit.blockcount  
  
press key to return
```

In response to the prompt a key press followed by return must be

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pressed.

4.11.13 P) Set Ignore Error Flag ,se_ignore_err

Will prompt with the following.

Do you wish to ignore all errors?

If you answer Y the ignore errors will be selected and much display information will not be displayed errors will not be checked in sub programs. If you answer N then error checking will again be enabled.

4.11.14 Q) Display Error In Compare Read And Write Buffers

This routine will compare the read and write buffers for differences and display those differences. It will prompt of the starting location in the buffers to compare.

Starting offset (in hex):

Then it will display the data in the following format.

loc: i read: se_rdbuff[i] write: se_wrbuff[i]

After displaying a group of differences it will prompt

Continue?

A response of Y return will cause more compares to be done until all the buffer has be compared. Then the only valid response will be a N return.

4.12 B) BLOCK TRANSFERS

Selection of this main menu option will cause the process_se_block_transfer(se_pad,envid,action) subprogram to be called and the following submenu to be displayed.

----- Block Transfer Menu -----

- a) FRDB
- b) FWDB
- g) FIFO read enabled (%c) COPYEN (%c)\n",fifo_read,coen
- h) PIPElined read enabled (%c) : %d nsec\n",pipe_read,pipe_time
- i) Get number of bytes transferred (%d) \n",number_of_bytes
- j) Reset FIFOs
- l) Reset FIFOs in each loop (%c)\n",fifo_reset

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- o) EOBINT enabled (%c)\n",eoen
- p) Number of long words to transfer (dec value: %d)\n",se_maxwds
- n) Print read data after every loop (%c)\n",print_data
- x) Exit this menu

Enter se_command:

4.12.1 A) FRDB

Will initiate a block transfer loop which will repeat se_nbr_loop times. if errors occur they will be displayed as follows.

FASTBUS error at PAD: se_pad SAD: se_sad

Return data will be displayed if enabled by option N. with format:

PAD : se_pad SAD : se_sad

loc: i read: se_rdbuff[i]

When the test loops are complete the following prompt will be displayed.

Continue?

The only valid response is a key press followed by a return.

4.12.2 I) Get Number Of Bytes Transferred

Will display the number of bytes transferred in the last command.

Number of Bytes transferred : number_of_bytes

4.12.3 P) Process "set Number Of Words To Transfer" Commands

Sets the number of words to transfer in the block transfer command.

Enter maximum number of long words to transfer (in decimal):

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4.12.4 G) Process FIFO Command

Will select use of FIFO in FSCC and set copy flag for data compare.

Copy enabled (T/F) :

4.12.5 H) Process PIPE Command

Will select the pipeline transfer option for block transfers and set the speed parameter.

pipelined read (100/200/400) nsec:

For further information, please contact:

M. Larwill, B. Demaat

CHAPTER 5

MTC SINGLE BOARD TEST

5.1 TEST DEFINITION

5.1.1 Modes Of Operation (Ref. MTC HARDWARE DISCRPTION , October 19, 1990)

1. Test : External trigger requests are disregarded , triggers are generated by software (FB triggers). Write counter is shut down and the read address is controlled by the trigger offset (0 - trig. offset) Wait is always set in this mode.
2. Calibration : Each external trigger generates N (switch setable) consecutive read addresses. Address valid is generated independent of the presence of any error .
3. Run : Each external trigger generates a read address, which is stored in the FIFO if D/E READY is not present. The FIFO depth is programmable and WAIT is set if the number of FIFO stages is greater equal than that. If more triggers occur then FIFO OVERFLOW ERROR will be generated. If the read address (obtained by adding the offset determined by the calibration procedure to the reference D/E write counter of the MTC) is close by a programmable amount to the current write address in the D/Es a MEMORY OVERWRITE ERROR will be issued. Any of the above errors , or TRIGGER PHASE and DE errors will stop external triggers and FIFO reads (addr_valid) until it is cleared

5.2 FEATURES OF THE MODULE THAT ARE TESTED :

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1. Fastbus interface
2. Fifo read address
3. Fifo overflow
4. Clock phase adjustment
5. Memory overwrite
6. Wait
7. Calibration

5.3 HARDWARE REQUIREMENTS

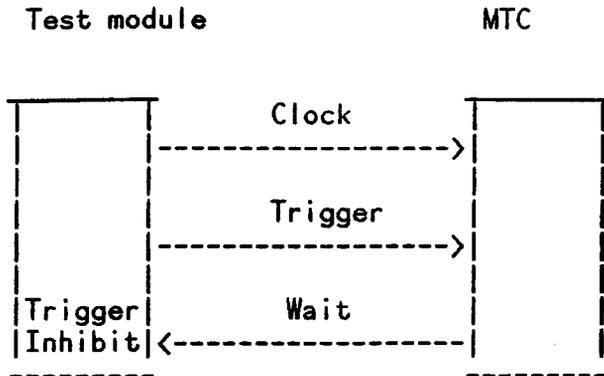
A standard Fastbus crate for the MTC and a standard NIM crate for the MTC test module. The test module provides the clock input and the external trigger input for the MTC. Since there are no external readings during the test, the module will issue a Memory Overwrite Error after (256 - Memory window set) clock cycles. The external trigger rate from the test module was chosen to be 1/6 clock cycles in order to fire enough triggers to test the whole FIFO depth before the error is issued. The triggers from the test module are inhibited with the WAIT output of the MTC, to prevent FIFO overflow error. The phase of the trigger must be adjusted to be synchronized with respect to the clock. This is done in the following way: the front panel provides a trigger monitor and a trigger window signals (NIM). The position of the leading edge of the trigger signal must be set in the middle of the trigger window delaying the external trigger with respect to the clock. Also, the window width can be adjusted from the front panel switch. A working module should not issue a trigger phase error (front panel led) when the write enable is set if the phase is properly adjusted (the write enable must be set to see a trigger phase error).

No more front panel connections are required and the presence

of an ENCODER READY from the ribbon cable connector will cause

the test to fail.

MTC SINGLE BOARD TEST



5.4 TEST DESCRIPTION.

According to a) , b) , c) the test procedures are defined :

1. Fastbus interface : Write and read to (from) CSR10 - CSR13 set and reset flags (bits) and read statuses of CSR0.

2. Fifo read address :

Reset
Error flag reset
Test mode
Write enable
Trigger address offset to 256 - N
FB trigger
FB encoder ready
Read CSR10
Compare
Reset

3. Fifo overflow :

Reset
Error flag reset
Test mode
Write enable
Set trigger pipeline depth to 7
While not overflow
 Set trigger address offset
 FB trigger
End While
Check number of triggers generated
Loop on trigger number
 Read back with Encoder Ready and
 check address

MTC SINGLE BOARD TEST

End Loop
Reset

4. Clock phase adjustment : Adjust clock phase and delay the trigger over a range of values , checking for trigger phase error (only in manual test , for automatic tests make sure that trigger remains in sync)

5. Memory Overwrite :

Reset
Error flag Reset
Test mode
Write Enable
Loop on the 255 possible read addresses
Error flag Reset
Set trigger address offset
Assert FB trigger
Check Memory Overflow
If not when address agrees with the Dip Switch
report it
Assert FB trigger
Read and compare address
End Loop
Reset

Here you have to set the switch to the hardcoded value 8 (see last MTC TESTS section) or you can change the default during the initialization time , to agree with your set value.

6. Wait :

Reset
Error flag reset
Loop over fifo depth
Set fifo depth
Set write enable
Loop until wait or error or timeout
When wait or error triggers(external) are inhibited
Set test mode
Assert Fb encoder ready until fifo is empty
Compare with depth or if error report
End Loop
Reset

7. Calibrate :

Reset
Error flag reset
Set trigger pipeline to 1 so wait will inhibit all but the first external trigger
Set calibration
Set Write enable

MTC SINGLE BOARD TEST

```
Loop until Wait
Set Test mode
Loop
  Assert Fb encoder ready
  Fill array
  Break if fifo empty
End Loop
Compare and check array, report errors
Reset
```

Test mode is required when reading back external triggers in Run mode in order to prevent the blocking of `addr_valid` due to Memory overwrite error. For the same reason `Reset` is required after every test completion. For every FB write the corresponding read is performed in order to check the FB interface. During the initialization the parameters that correspond to dip switches (memory overwrite window , number of calibration triggers) must be matched with the hardware values, from the main menu (option d).

Also depending on the mode of operation (interactive or auto) you can (or cannot in auto) alter the values of the parameter of each test (i.e trigger offset , pipeline depth) , to run on your preferred values.

5.5 SOFTWARE DESCRIPTION

MTC_TEST.C program compiles ,links and runs with the standard SSD procedures , under the control of SSD MAIN MENU , either on the VAX or on the 68020 of the FSCC (FNSSD1 node). The interface with SSD_MENU is via a call to the function : `mtc_test(*primary_address,*envid,*action)` where action is defined according to the SSD standard (section 1.3.11) , so you can either call the full test or the main menu of the test. The function returns the longword `MTC_er_log.word` , which is defined in the include file `ssd_diag$library:mtcdefn.h` (== PASS when everything is fine)

```
MTC_er_log; /* Used to pack error status */
```

Bits 0 - 11

```
Error Flag
Write Enable
Calibration Mode
Test Mode
Fifo Pipeline Depth
Trigger Address Offset
Clock
Fifo Read Address procedure
```

Fifo Overflow procedure
Calibration procedure
Wait procedure
Memory Overwrite procedure

5.5.1 Program Structure

There are 4 different types of functions according to the task they perform :

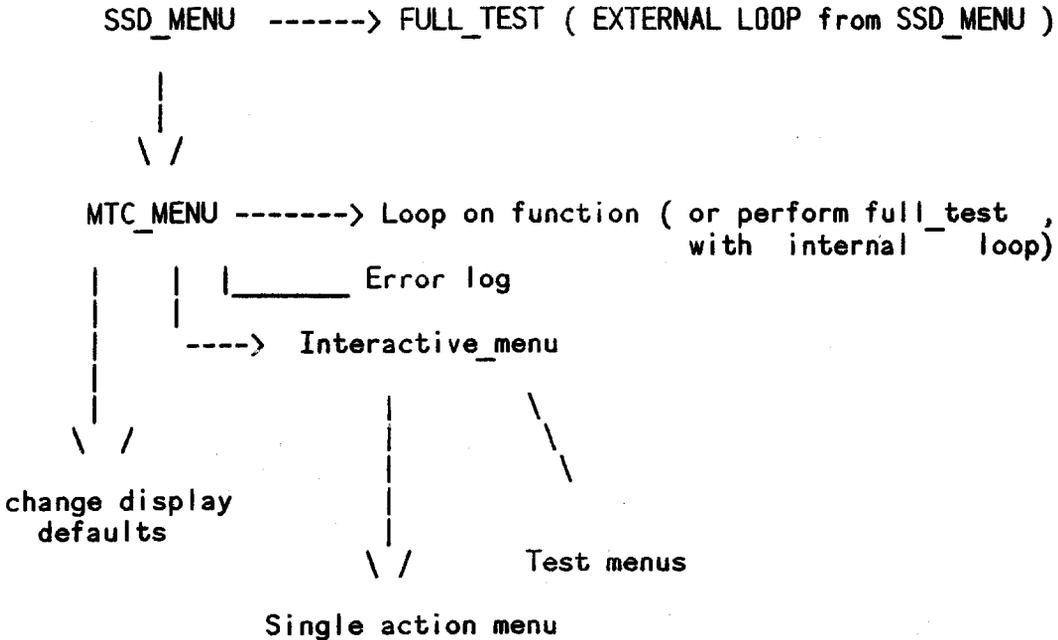
1. Single action
2. Test procedure
3. Menu
4. Display and error log.

The single action functions perform all the operations that are provided from the Fastbus Interface . In each of them succesfull completion is checked and a status is returned. In the test procedure functions the previous category functions are combined to perform the different module tests . The full test calls sequentially the test procedures and does the error logging.

The menus (see Appendix),give the capability to perform each test individually , if you enter mtc_test in menu driven mode , either interactively (step by step) or in a loop using the standard features of SSD_DIAG , stop or continue on error and log the errors.

The error log (and the corresponding display function) provides information in two levels :There is an error word bitfield that has a bit set corresponding to every error that occurs in each single action and a bit set for each test procedure error , then there are counters for each register and for every test procedure that give the multiplicity of each error .

MTC SINGLE BOARD TEST



5.5.2 Mode Description

The different modes of operation in the menu driven run of the test are ==>

1. LOOP mode :

You can choose to run the full test or any single task test in an infinite loop (until CR is pressed) or specifying the number of repetitions, aborting or continuing on error. Also for checking the output signals exists an infinite loop of setting and resetting particular bits on each register.

2. Interactive mode :

You can run each test step by step specifying the conditions by answering the on screen questions and having the status of the module after each action on screen. If an error occurs the control is passed to the FASTBUS interface menu. There is also the option of selecting a single action to activate, which gives the possibility to combine them to perform a test different from the defaults.

In each of the interactive submenus reset module ,reset

MTC SINGLE BOARD TEST

error flag and display register values items are provided.

5.6 SUMMARY - DEFAULT SETTINGS

A users application can call `mtc_test` via the standard Single Board Test action flags either to run the full test and decide pass or fail from the return value of the function or to enter it in the menu driven mode .

There are two parameters that must be matched in the software with the corresponding hardware values (switch setable) :

- 1) The memory window (MEMSW) -- default value 8
- 2) Number of triggers from calibration -- default 3 .

This values can be changed via the main menu item d) or one can set them on the module to the hardcoded software values via the dip switces.

APPENDIX A

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

After setting the MTC primary address in the top level menu and calling MTC_TEST in the mode GET_MENU, a typical test session could look like the following :

----- Main Menu -----

- e) Expert actions
- d) Display and change defaults
- a) Full test (1 time)
- l) Loop on function
- s) Check signals
- i) Display error summary
- c) Clear error summary and reset
- g) Registers display
- r) Reset module
- t) Reset error flags
- x) Exit Program

Enter command: d

default MEMSW is : 8
do you want to change it (1) :
default total fifo counts are : 9
do you want to change it (1) :
default wait set offs is : 1
do you want to change it (1) :
default extra trig is : 0
do you want to change it (1) :
default calibration length is : 3
do you want to change it (1) :

----- Main Menu -----

- e) Expert actions
- d) Display and change defaults
- a) Full test (1 time)
- l) Loop on function
- s) Check signals
- i) Display error summary

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

- c) Clear error summary and reset
- g) Registers display
- r) Reset module
- t) Reset error flags
- x) Exit Program

Enter command: l

ERRORS are not cleared by default

----- Loop Menu -----

AVAILABLE FUNCTIONS ARE

- f0) Full_TEST , burning test
- f1) Fbi0_test
- f2) Fbi11_test
- f3) Fbi12_test
- f4) Fbi13_test
- f5) RA test
- f6) Fifo test
- f7) Calibrate_test
- f8) Wait test
- f9) Mem_Ov_test
- x) Exit Menu

Enter command: f0

Infinite loop (0) or not (anything else) :0

Stop on error(0) or continue test(anything else) :0

----- Loop Menu -----

AVAILABLE FUNCTIONS ARE

- f0) Full_TEST , burning test
- f1) Fbi0_test
- f2) Fbi11_test
- f3) Fbi12_test
- f4) Fbi13_test
- f5) RA test
- f6) Fifo test
- f7) Calibrate_test
- f8) Wait test
- f9) Mem_Ov_test
- x) Exit Menu

Enter command: x

TEST COMPLETED , NO ERRORS DETECTED

----- Main Menu -----

- e) Expert actions
- d) Display and change defaults
- a) Full test (1 time)
- l) Loop on function
- s) Check signals
- i) Display error summary
- c) Clear error summary and reset

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

- g) Registers display
- r) Reset module
- t) Reset error flags
- x) Exit Program

Enter command: e

----- Main interactive Menue -----

- s) Set Primary Address (mtc_pa) (hex value)
- i) Fastbus Interface test menue
- f) Fifo test menue
- c) Callibrate test menue
- p) Clock Phase adjustment menue
- w) Wait test menu
- m) Memory overflow test menue
- a) Individuall action menue
- d) Display register
- r) Reset module
- t) Reset error flag
- x) Exit Menue

Enter command: r

Reseting MTC
CSR0 is set to : 1a20080
CSR10 is set to : 0
CSR11 is set to : 11
CSR12 is set to : 1
CSR13 is set to : 1f

----- Main interactive Menue -----

- s) Set Primary Address (mtc_pa) (hex value)
- i) Fastbus Interface test menue
- f) Fifo test menue
- c) Callibrate test menue
- p) Clock Phase adjustment menue
- w) Wait test menu
- m) Memory overflow test menue
- a) Individuall action menue
- d) Display register
- r) Reset module
- t) Reset error flag
- x) Exit Menue

Enter command: c

Set Calibration mode
CSR0 is set to : 1a200c0
and so the Calibration mode is : 1
Set Write Enable
Write enable : 1
Hopefully you are providing an external Trigger input

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

you expect to get back 5 consecutive read addresses
Read ERROR flag
CSR0 is set to : 1a208c5
and so the ERROR flag is : 1
Wait bit is : 1
Test mode set
TEST mode is : 1
CSR10 is set to : 9
and so the FIFO read address is : 9
Generate Fastbus Encoder Ready
CSR10 is set to : a
and so the FIFO read address is : a
Generate Fastbus Encoder Ready
CSR10 is set to : b
and so the FIFO read address is : b
Generate Fastbus Encoder Ready
CSR10 is set to : c
and so the FIFO read address is : c
Reset Calibration mode
CSR0 is set to : 1a20985
and so the Calibration mode is : 0

----- Main interactive Menue -----
s) Set Primary Address (mtc_pa) (hex value)
i) Fastbus Interface test menue
f) Fifo test menue
c) Callibrate test menue
p) Clock Phase adjustment menue
w) Wait test menu
m) Memory overflow test menue
a) Individuall action menue
d) Display register
r) Reset module
t) Reset error flag
x) Exit Menue
Enter command: w

Setting trigger address offset to 1 ...

----- Wait Test Menue -----
l) Loop over preselected values
i) Manual test
d) Display register
r) Reset module
t) Reset error flag
x) Exit Menue
Enter command: r

Reseting MTC
CSR0 is set to : 1a20080
CSR10 is set to : c

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

CSR11 is set to : 14
CSR12 is set to : 1
CSR13 is set to : 1f

----- Wait Test Menue -----

- l) Loop over preselected values
- i) Manual test
- d) Display register
- r) Reset module
- t) Reset error flag
- x) Exit Menue

Enter command: i

Enter Trigger Pipeline Depth (hex 3 bits) : 1

Triger Pipeline depth is : 1
Set Write Enable
Write enable : 1
Read ERROR flag
CSRO is set to : 1a20885
and so the ERROR flag is : 1
Wait bit is : 1
Test mode set
Assert first FB encoder ready, check for Fifo Status
Generate Fastbus Encoder Ready
Fifo status bit is : 1
Enc ready eq Pipeline Depth+1 Fifo must be empty
Enter 1 to assert another enc ready 0 to stop : 1
Generate Fastbus Encoder Ready
Fifo status bit is : 0
Enc ready eq Pipeline Depth+1 Fifo must be empty
Enter 1 to assert another enc ready 0 to stop : 0

Test completed

----- Wait Test Menue -----

- l) Loop over preselected values
- i) Manual test
- d) Display register
- r) Reset module
- t) Reset error flag
- x) Exit Menue

Enter command: x

----- Main interactive Menue -----

- s) Set Primary Address (mtc_pa) (hex value)
- i) Fastbus Interface test menue
- f) Fifo test menue
- c) Callibrate test menue
- p) Clock Phase adjustment menue
- w) Wait test menu
- m) Memory overflow test menue

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

- a) Individuall action menue
- d) Display register
- r) Reset module
- t) Reset error flag
- x) Exit Menue

Enter command: i

----- Fastbus Interface Menue -----

- l) Loop over preselected values
- i) Read Write register
- x) Exit Menue

Enter command: i

- i) Read module's ID
- c) Check flag setting resetting
- w) Write register (one of CSR10 11 12 13)
- r) Read register (one of CSR10 11 12 13)
- d) Display registers
- s) Reset MTC
- x) Exit Menue

Enter command: c

- e) Check error flag
- w) Check write enable
- c) Check Calibration mode set reset
- t) Check Test mode set reset
- r) Reset module
- f) Write Read FIFO read address
- p) Write Read Triger Pipeline depth
- a) Write Read Triger adres offset
- k) Check Clock phase ajustement
- d) Display registers
- x) Exit Menue

Enter command: r

Reseting MTC

CSR0 is set to : 1a20080
CSR10 is set to : 16
CSR11 is set to : 11
CSR12 is set to : 1
CSR13 is set to : 1f

- e) Check error flag
- w) Check write enable
- c) Check Calibration mode set reset
- t) Check Test mode set reset
- r) Reset module
- f) Write Read FIFO read address
- p) Write Read Triger Pipeline depth
- a) Write Read Triger adres offset
- k) Check Clock phase ajustement
- d) Display registers
- x) Exit Menue

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

Enter command: c

Set Calibration mode

CSR0 is set to : 1a200c0

and so the Calibration mode is : 1

Reset Calibration mode

CSR0 is set to : 1a20080

and so the Calibration mode is : 0

- e) Check error flag
- w) Check write enable
- c) Check Calibration mode set reset
- t) Check Test mode set reset
- r) Reset module
- f) Write Read FIFO read address
- p) Write Read Triger Pipeline depth
- a) Write Read Triger address offset
- k) Check Clock phase adjustement
- d) Display registers
- x) Exit Menue

Enter command: x

- i) Read module's ID
- c) Check flag setting resetting
- w) Write register (one of CSR10 11 12 13)
- r) Read register (one of CSR10 11 12 13)
- d) Display registers
- s) Reset MTC
- x) Exit Menue

Enter command: x

----- Fastbus Interface Menue -----

- l) Loop over preselected values
- i) Read Write register
- x) Exit Menue

Enter command: x

----- Main interactive Menue -----

- s) Set Primary Address (mtc_pa) (hex value)
- i) Fastbus Interface test menue
- f) Fifo test menue
- c) Callibrate test menue
- p) Clock Phase adjustment menue
- w) Wait test menu
- m) Memory overflow test menue
- a) Individuall action menue
- d) Display register
- r) Reset module
- t) Reset error flag
- x) Exit Menue

Enter command: a

----- Action Menue -----

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

- d) Display register
- e) Error Flag
- w) Write Enable
- c) Calibration mode
- s) Start Calibration
- t) Test mode
- f) Fifo address
- p) Trigger pipeline
- a) Trigger address offset
- l) Clock phase
- i) Read wait
- k) Read Fifo status
- b) Assert FB trigger
- y) Assert FB encoder ready
- r) Reset module
- x) Exit Program

Enter command: t

Enter 1 to set anything to reset :
Test mode reset

----- Action Menue -----

- d) Display register
- e) Error Flag
- w) Write Enable
- c) Calibration mode
- s) Start Calibration
- t) Test mode
- f) Fifo address
- p) Trigger pipeline
- a) Trigger address offset
- l) Clock phase
- i) Read wait
- k) Read Fifo status
- b) Assert FB trigger
- y) Assert FB encoder ready
- r) Reset module
- x) Exit Program

Enter command: x

----- Main interactive Menue -----

- s) Set Primary Address (mtc_pa) (hex value)
- i) Fastbus Interface test menue
- f) Fifo test menue
- c) Callibrate test menue
- p) Clock Phase adjustment menue
- w) Wait test menu
- m) Memory overflow test menue
- a) Individuall action menue
- d) Display register
- r) Reset module
- t) Reset error flag
- x) Exit Menue

TYPICAL SESSION WITH MTC_TEST PROGRAM IN MENU DRIVEN MODE

Enter command: x

----- Main Menu -----

- e) Expert actions
- d) Display and change defaults
- a) Full test (1 time)
- l) Loop on function
- s) Check signals
- i) Display error summary
- c) Clear error summary and reset
- g) Registers display
- r) Reset module
- t) Reset error flags
- x) Exit Program

Enter command: x

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A.1 ABBREVIATIONS

DE	Delay Encoder
FSCC	FASTBUS Smart Crate Controller
FSR	FASTBUS Standard Routines
MTC	Master Timing Controller
PC	Postamplifier/Comparator
RPX	Remote Procedure Execution
SE	Sequencer
SSD	Silicon Strip Detector
TSM	Test Stand Module

PN 436
Version : 1
15 April 1991

**Silicon Strip Detector (SSD)
System Test Software Guide**

**Wolfgang Kowald
Duke University, E771**

**Panagiotis Spentzouris
UOA, E771**

**Dave Slimmer
Online Support Department
Fermilab Computing Division**

**This is the reference guide for the SSD system
diagnostic part of the SSD product.**

KEYWORDS: Diagnostic, Fastbus, SSD, Silicon Strip Detector

**Systems Supported: pSOS, VMS V5.3
Software Version: V1.1**

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APPENDIX A PC TEST COUNTER PATTERNS

APPENDIX B STANDARD ERROR SUMMARY

CHAPTER 1

OVERVIEW

The primary goals of the SSD system diagnostic tests are to exercise as of much of the SSD hardware as possible and to exercise that hardware in a manner similar to the way it will be used in the experimental environment. The hardware includes a FASTBUS crate with SSD backplane, Postamp Comparator module (PC), Delay Encoder (DE), Sequencer (SE), and Master Timing Controller (MTC). A FSCC is used as the system control and data handling device as well as the processor running the diagnostic code.

Various hardware configurations involving test modules are used at the front end of the system in the system tests. There are three different front end test modules. Each of these provides an input to, or substitutes for, the PC module. FASTBUS test hardware modules include a Test Stand Module (TSM), and a Level Shifter Module (LSM). The TSM provides output patterns for the DE using the SSD backplane. Alternately, the TSM output can be used as input for the LSM module. The LSM then converts the TSM output to a level compatible with the front panel inputs of the PC. Note that tests using the TSM-LSM test module configuration produce results dependent on the TSM-LSM signals, which vary slightly from channel to channel in time, slope, and amplitude. An external test device, the Dave Christian's Card (DCC), can provide test pattern output directly to the PC inputs. A description of the hardware configurations is given in Hardware Note 102 (HN102).

The system test software is organized in a menu driven format with a tree structure. Top level menu items are generally concerned with FASTBUS environment settings. Lower level menus are concerned with either making special test initializations or selecting specific tests. Default values for all FASTBUS and test parameters are initialized immediately after the diagnostic is called to allow certain tests to be executed with minimal menu interaction. There is a default test provided as a "button test" which runs most of the individually selectable tests with default parameters.

OVERVIEW

Tests described by this document are meant to verify subsets of the total possible SSD system configuration. It is assumed that the appropriate single board tests for individual SSD modules have been successfully completed before these tests are attempted. Although the system tests provide error messages, problems should first be isolated by module substitution, and later by using single board tests to isolate a hardware fault. Because some of the single board tests do not test module I/O paths, the system tests may be needed to trouble-shoot an individual SSD module.

CHAPTER 2
ABBREVIATIONS SUMMARY

- o add - address
- o bkt - bucket
- o cntr - counter
- o corr - correction
- o DCC - Dave Christian's Card
- o DE - Delay Encoder
- o dec - decimal
- o encdr - encoder
- o [F] - False
- o FSCC - FASTBUS Smart Crate Controller
- o FSR - FASTBUS Standard Routines
- o horiz - horizontal
- o IC - (PC) Individual Channel
- o LSM - Level Shifter Module
- o MTC - Master Timing Controller
- o ovflw - overflow
- o PAD - FASTBUS Primary address
- o PC - Postamplifier/Comparator

ABBREVIATIONS SUMMARY

- o pln - plane
- o prev - previous
- o RPC - Resistive Plate Counter module (variant of PC)
- o RPX - Remote Procedure Execution
- o SC - (PC) Sum Channel
- o SE/SEQ - Sequencer
- o SSD - Silicon Strip Detector
- o stats - statistics
- o [T] - True
- o trig - trigger
- o TSM - Test Stand Module
- o vert - vertical

CHAPTER 3

SYSTEM TEST OPERATION FORMATS

The diagnostic can be run in a variety of ways, but the method with the fastest execution speed and most convenience is using the ROM version of the code. The ROM version of the diagnostic can be installed in FSCC ROM bank 2. (Copies can be made of the latest version in release from Computing Department master prom set.) If FSCC ROM bank 2 is not available, the diagnostic can be downloaded from the SSD DIAG\$tests product directory. (The logical SSD DIAG\$tests pointing to the SSD tests directory is defined by setting up the SSD product with the command \$ SETUP SSD_DIAG). Both the ROM version and downloaded version of the diagnostic run in FSCC RAM, so execution speed is the same. Downloading the diagnostic can take up to 10 minutes over a serial line, making this method far less convenient than using the ROM version. The diagnostic may also be run using remote procedure calls, using either the Ethernet or serial front panel ports on the FSCC. Although the Ethernet version is slightly faster, both methods have relatively slow execution speed due to the overhead associated with high numbers of small data transfers. Details of using the ROMed version follows. Please note that the commands are case insensitive, but are shown in capital letters for demonstration purposes.

3.1 ROM

The following sequence of commands copies the diagnostic code from FSCC ROM bank 2 to FSCC RAM, and starts the diagnostic.

{reset the FSCC manually with the front panel reset button}

\$ SET HOST/DTE ttnn:	(establish serial communications with FSCC)
pROBE> go 40000	(run EPROM to RAM copy program)
pROBE> gs	(start pSOS and do other board initializations)
pROBE> go	(start diagnostic)

SYSTEM TEST OPERATION FORMATS

3.2 SERIAL DOWNLOAD

This command sequence downloads the diagnostic from the SSD DIAG\$tests project area directly to FSCC RAM using the PORT_MGR product, and starts the diagnostic.

```
$ SETUP PORT_MGR                (if not done previously)

$ DOWNLOAD SSD_DIAG$root:[tests]ssd_diag.abs ttnn:
$ PTALK ttnn: (or alternately)  $ SET HOST/DTE ttnn:
PROBE> gs                (start pSOS and do other board initializations)
PROBE> go                (start diagnostic)
```

3.3 RPX ETHERNET

This sequence of commands downloads the server code to the FSCC through the serial port and starts the "boss" on a VAX. The diagnostic runs as if it were executing on the VAX, and uses the Ethernet connection to the FSCC for communications.

```
$ SETUP SSD DIAG                (setup appropriate products)
$ SETUP PORT_MGR
$ SETUP TRMB0

$ SET DEFAULT SSD_DIAG$TESTS    (diagnostic and command procedure directory)
$ @defrpx                       (defines logicals - must be tailored to
                                environment)
$ @boot_fscs_eth                (download server code and start boss - starts
                                boss with call to boss_eth.com. Both
                                must be tailored to environment)

$ RUN/NODEBUG SSD_DIAG          (start diagnostic)
```

3.4 RPX SERIAL

This sequence of commands also downloads the server code to the FSCC through the serial port and starts the "boss" on a VAX. The diagnostic then runs as if it were executing on the VAX, using the serial connection to the FSCC for communications.

```
$ SETUP SSD DIAG                (setup appropriate products)
$ SETUP PORT_MGR
$ SETUP TRMB0

$ SET DEFAULT SSD_DIAG$TESTS    (diagnostic and command procedure directory)
$ @defrpx                       (defines logicals - must be tailored to
                                environment)
$ @boot_fscs                    (download server code and start boss - starts
```

SYSTEM TEST OPERATION FORMATS

\$ RUN/NODEBUG SSD_DIAG

boss with call to boss.com. Both
must be tailored to environment)
(start diagnostic)

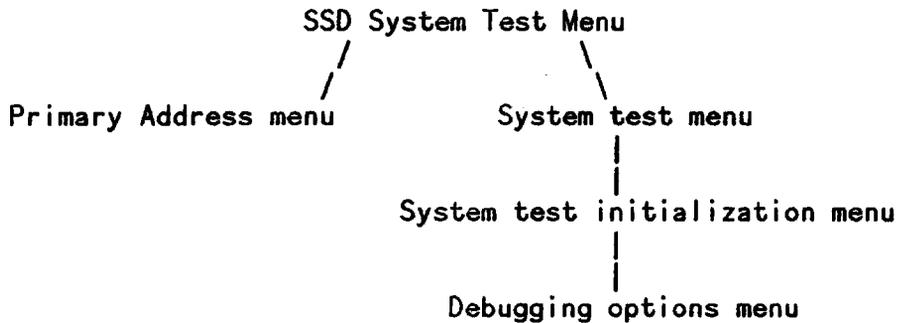
CHAPTER 4

SYSTEM TEST SOFTWARE HARDWARE CONFIGURATION

There are four general test configurations used in the system tests. They are the PC/s injecting test bit patterns, the TSM substituting for the PC, the TSM driving the PC through the LSM, and the DCC generating fixed pattern input to the PC. The only test allowing for multiple PC/DE pairs is the PC injecting bit pattern test. Other tests will typically be run with one of each type of SSD module required, appropriate test module/s, and the FSCC, all in the same FASTBUS/SSD crate. Reference HN102 for the appropriate hardware test configuration.

CHAPTER 5
SYSTEM TEST SOFTWARE DESCRIPTION

5.1 MENU STRUCTURE OVERVIEW



5.2 MAIN MENU

The top level menu provides information on the FASTBUS environment as well as options to tailor the FASTBUS environment. In addition, it provides access to lower level menus, and a means to end the test program. Several initializations occur automatically as the test is started to reduce the amount of menu interaction required. Initializations include those done by menu option Initialize FASTBUS, and initialization of the long timer. Primary addresses are set assuming one of each type of SSD system module. Note that it is not necessary for the system tests to have the FSCC arbitrate for bus mastership. Generally, the only menu interaction required is to check the Primary address initializations and to select the system test submenu. The main menu:

SYSTEM TEST SOFTWARE DESCRIPTION

SSD System Test Menu

- =====
- 1) Initialize FASTBUS
 - 2) Arbitrate (status = unknown)
 - 3) Release Bus
 - 4) Set Long Timer (297 usec)
 - 5) Set Short Timer (1500 usec)
 - 6) Set Primary Addresses
 - 7) System test menu
 - 99) Exit to pROBE

Enter Command:

5.2.1 Initialize FASTBUS

When the SSD System diagnostic is started, the FASTBUS environment is automatically initialized by the FASTBUS routines called by this menu option. Each FASTBUS Standard Routine that is part of this initialization is displayed in a banner above the top level menu. The initialization creates a FASTBUS environment ID that is passed to the module tests, so an error will occur if this menu option is called more than once before calling menu option Release Bus. The FASTBUS initialization routines are:

- o GPMINI - initialize interrupts and internal database
- o FBOPEN - open FASTBUS routines for use
- o FCIENV - allocate an environment ID and associated storage
- o FNPALL - allocate FASTBUS port for use
- o FBPSET(EG) - set environment parameter to enable geographic addressing
- o FBPSET(COEN) - set environment parameter to enable FSCC data FIFO to processor FIFO copy
- o FBPSET(EOBI) - set environment parameter to enable end of block interrupt

5.2.2 Arbitrate

The menu option shows the current arbitor status of the FSCC, one of either "Master", "Slave", or "unknown". If this option is chosen, the FSCC tries to arbitrate for bus mastership using the

SYSTEM TEST SOFTWARE DESCRIPTION

selected arbitration level. It is not necessary for the FSCC to be bus master to run these tests.

5.2.3 Release Bus

This option will release the bus and delete the current FASTBUS environment ID using the following routines:

- o FRLNV - releases system resources, environment ID becomes invalid
- o FBCLOS - deasserts any asserted FASTBUS port lines

5.2.4 Set Long Timer

The menu option displays the current environment value for the long timer. Selecting this option allows the long timer to be set to a new value. After selecting menu item Initialize FASTBUS, the long timer will always be reset to 5000000 usec.

5.2.5 Set Short Timer

Same as above, but the short timer can only be enabled or disabled. Selecting 1500 enables the timer and selecting 0 disables the timer.

5.2.6 Set Primary Address Menu

Set the primary addresses (slot number) for the SSD modules. The submenu displays the current values of the PADs.

	PAD (dec)
a) Postamp Comparator	21
b) TSM	17
c) Sequencer	13
d) Master Timing Controller	2
x) Go back to main menu	

Select module:

The DE module has no FASTBUS interface, and therefore no PAD.

SYSTEM TEST SOFTWARE DESCRIPTION

5.2.7 System Test Menu

In the process of bringing up the system test menu, an initialization is performed to allow the user to bypass the system test initialization submenu. The PC PAD displayed in the Primary address menu is written out to the SE as the PC's plane ID. All other PC plane IDs in the SE are set to zero. See the System test menu section for description of tests.

5.2.8 Exit To PROBE

In the ROM version, this option will terminate the SSD System tests with a pROBE break.

5.3 SYSTEM TEST MENU

A full description of each System test menu option follows.

- a) System test initialization menu
- b) TSM as PC test
- c) PC test counter test
- d) General readout loop
- f) CLK1/DAC scan
- g) PC channel quick tests
- h) PC channel characterization tests
- j) PC crosstalk test
- k) Default system tests
- l) Trigger address scan
- x) Go back to main menu

Select test:

5.3.1 System Test Initialization Menu

All tests, with the exception of the General readout loop, are setup to use some default values for test parameters. The purpose of System test initialization menu options is to allow system tests to be run in non-default ways. Although each of these menu options are given default values when the diagnostic first starts, subsequent changes will remain in effect. Each test description section contains a section named "Initialization Menu Options" that should be checked prior to running a test. The menu is logically divided so that menu options are associated with their respective SSD module. Additionally, there are several options at the end of the menu that are not specifically associated with one module.

SYSTEM TEST SOFTWARE DESCRIPTION

Several FASTBUS operations occur before the system test initialization menu scrolls onto the screen. The operations determine the current state (as displayed by the menu) of several selectable options for the SE and MTC. A detailed description of initialization menu options follows.

System test initialization menu with default states and options shown:

- PC: 1) PC PADs/pln encdr IDs 2) Define PC PADs
 3) Running Test Cntr [F] 4) Rolling Test Cntr [T]
 5) Set Test Cntr (FE hex) 6) PC latch mode [F]
 7) Set DAC buffer (100 dec) 8) IC Enable [F]
 9) DAC scan (230, 0, -1, F) 10) SC Enable [F]
- DE: 20) Accept prev bkt hit [T] 21) Loop on trig add (0 dec) [F]
 22) Set Trig Add Cor (-1 dec) 23) Trig add range (0 to 255 dec)
- SE: 30) Reset Sequencer 31) Define pln encdr IDs
 32) FASTBUS FIFO Enabled [F] 33) Aux FIFO Enabled [F]
 34) Set CLK1 (00), CLK2 (00) 35) Ovflw trunc Enabled [F]
 36) CLK1 scan (0,63, 1, F)
- MTC: 40) Reset MTC 41) Set trig pipe depth (0 dec)
 42) Write Enable on [F]

 50) Fill Buffer 51) Use RPC [F]
 52) One ch CLK1/DAC scan [F] 53) Print stats buf horiz
 54) FSCC Data FIFO enable [F] 55) Print stats buf vert
 66) Debugging options menu
 99) Exit menu

Enter Command:

- o PC PADs/pln encdr IDs

Displays a list of PC PADs and their associated SE plane IDs. Each non-zero PC PAD in the list indicates a PC used during subsequent tests. Note that only the PC test counter test can handle multiple PC's running simultaneously.

- o Define PC PADs

Allows creation of the PC PAD list. All previous PADS in the PAD list are set to zero. Each addition to the list is displayed. SE plane IDs should be redefined with the Define pln encdr IDs menu option.

- o Running Test Cntr [F]

Sets a flag. Pertains only to the PC test counter test. See the test description for more detail.

SYSTEM TEST SOFTWARE DESCRIPTION

- o Rolling Test Cntr [T]

Sets a flag. Applies only to the PC test counter test. See the test description for more detail.
- o Set Test Cntr (FE hex)

Sets a hex value in the range of 00 to FF (hex) which is passed to the PC test counter test. Pertains only to the PC test counter test. See the test description for more detail.
- o PC latch mode [T]

Sets a flag used by an internal PC initialization routine. In some tests this request may be overridden to establish the proper test conditions. The tests which automatically set this flag to the state shown in parenthesis include: PC test counter test (F), CLK1/DAC scan (T), PC channel characterization tests (T), PC channel quick tests (T), and PC crosstalk (T). This mode must be set to the desired state for the General readout loop test.
- o Set DAC buffer (100 dec)

Sets a 256 byte buffer with a single DAC value to be used by the PC. This value is used by tests which may not scan thru or initialize DAC values as part of the test. These tests include the General readout loop, PC channel characterization tests (CLK1 vs channel mode), and PC channel quick tests.
- o IC Enable [T]

Toggles a flag used by the PC initialization routine which enables or disables the PC Individual channel logic. This flag is automatically initialized to the appropriate state by the PC test counter test, the CLK1/DAC scan, the PC crosstalk test, the PC channel characterization tests, and the PC channel quick tests. This mode should always be set to the desired state for the General readout loop.
- o DAC scan (230, 0, -1, F)

Sets the DAC scan range for the following tests REGARDLESS OF THE INDICATED STATE OF THE FLAG: CLK1/DAC scan, PC channel characterization tests (in the DAC vs channel mode), and PC crosstalk test. The General readout loop uses the indicated DAC scan range only if the flag shows the scan function to be enabled. If the scan range is not enabled, the General readout loop uses

SYSTEM TEST SOFTWARE DESCRIPTION

the PC DAC value as set by the Set DAC buffer (ddd dec) menu option where "ddd" is a value between 0 and 255.

Because there are a fixed number of PC CSR bits (8), a DAC value request greater than 255 will always be truncated to 255. Tests using the DAC scan range end when the terminal value is reached. If the DAC increment or decrement is set so that the terminal value never occurs, the test will go into an infinite loop.

- o SC Enable [F]

Toggles a flag used by the PC initialization routine which enables or disables the PC Sum channel logic. This flag is automatically initialized to the appropriate state by the PC test counter test, the CLK1/DAC scan, the PC crosstalk test, the PC channel characterization tests, and the PC channel quick tests. This mode should always be set to the desired state for the General readout loop.

- o Accept prev bkt hit [T]

Sets a flag. If set, internal data checking routines will accept a hit occurring in the previous bucket that may or may not be present in the current bucket.

- o Loop on trig add (0 dec) [F]

If enabled, the selected test continues to loop on the beginning trigger address as set by the Trig add range menu option until a keyboard return is entered. This switch applies to the PC test counter test (fixed test counter only), TSM as PC test, and General readout loop.

- o Set Trig Add Corr (-1 dec)

Sets up a positive or negative value in the range of -255 to +255 which is used in the DE trigger address offset calculations in the following tests: PC test counter test, TSM as PC test, CLK1/DAC scan, PC crosstalk, PC channel characterization tests, General readout loop, and PC channel quick tests. Normally this value should be set to zero except for the PC test counter test. See the System test description section for more information.

- o Trig add range (0 to 255 dec)

Sets the range of DE trigger addresses to be read out. Used by the following tests: PC test counter test, TSM as PC test, and General readout loop. The beginning address only is used by the DAC/CLK1 scan, the PC

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crosstalk test, the PC channel characterization tests and the PC channel quick tests.

- o Reset Sequencer

Performs a FASTBUS write to SE CSR 0 to set the SE reset bit.

- o Define pln encdr IDs

Allows definition of plane IDs in SE RAM. Selecting this option will result in a query for all PC plane IDs. After the last PC plane ID is entered, the plane IDs are written to the SE. Then, the active PC PAD list and their corresponding plane IDs are displayed.

- o FASTBUS FIFO Enabled [T]

Switches state of SE FASTBUS FIFO by writing to SE CSR 0 and then checks if the bit is set. The flag following the menu option always reflects the enable state of the FIFO. The FASTBUS FIFO should be enabled for all system tests.

- o Aux FIFO Enabled [F]

Switches state of SE Auxiliary FIFO by writing to SE CSR 0 and then checks if the bit is set. The flag following the menu option always reflects the enable state of the FIFO. Having this FIFO enabled will cause overflow errors if there is no readout device attached to the SE auxiliary output port.

- o Set CLK1 (20), CLK2 (24)

Sets SE CLK1 with FASTBUS write to SE CSR space. The current value of CLK1 and CLK2 is read back and displayed by the menu. CLK2 is set by dip switches which are located on the SE module. The CLK1 value is important to tests that may not scan CLK1 values, such as the PC test counter test, the TSM as PC test, the General readout loop, the PC channel characterization tests, the PC channel quick tests, and the PC crosstalk test.

Because the CLK1 value is always read back after it is set; and, there are a fixed number of bits (6) allocated in the internal data structure for the CLK1 value, a CLK1 value request greater than 63 will always be truncated to 63.

SYSTEM TEST SOFTWARE DESCRIPTION

- o Ovflw trunc Enabled [F]

Switches the state of the SE overflow truncation function. When enabled, the SE truncates events after the SE FASTBUS FIFO is half full. This function should be disabled if more than one PC is used in the PC test counter test due to the amount of data produced by the PCs.

- o CLK1 scan (0,63, 1, F)

Sets the CLK1 scan range for the CLK1/DAC scan and the PC channel characterization tests REGARDLESS OF THE INDICATED STATE OF THE FLAG. The General readout loop is a special case and uses the indicated CLK1 scan range only if the flag shows the scan function to be enabled. If the scan range is not enabled, the General readout loop uses the SE CLK1 value indicated by the Set CLK1 (dd), CLK2 (dd) menu option where "dd" has a value from 0 to 63 and each unit is equal to 0.5 nsec.

Because the CLK1 value is always read back after it is set; and, there are a fixed number of bits (6) allocated in the internal data structure for the CLK1 value, a CLK1 value request greater than 63 will always be truncated to 63. Tests using the CLK1 scan range end when the terminal value is reached. If the CLK1 increment or decrement is set so that the terminal value never occurs, the test will go into an infinite loop - perhaps a useful feature in trouble-shooting.

- o Reset MTC

Performs a FASTBUS write to MTC CSR 0 to set the MTC reset bit. This reset also resets the other SSD modules. The SE auxiliary FIFO enable state, FASTBUS FIFO enable state, and overflow truncation enable state may need to be reinitialized after a MTC reset operation.

- o Set trig pipe depth (7 dec)

Sets the MTC trigger pipeline depth (0 to 7) to the requested value by a write to MTC CSR space. The current pipe depth is displayed by the menu option.

- o Write Enable on [T]

Switches state of MTC write enable, which when on allows DEs to accept data. The current state of write enable is displayed.

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o Fill Buffer

Calls submenu that gives options for filling the data buffer loaded to the TSM memory. (Data loaded into the TSM memory becomes the TSM output.) This option applies to the TSM as PC test and the General readout loop which do not initialize the buffer used by the TSM.

Other tests which do initialize the TSM input buffer, but may be overridden, include the CLK1/DAC scan, the PC channel characterization tests, and the PC channel quick tests. Entering "111" at the System initialization menu "Enter Command" prompt will toggle a flag that allows the user to change the default buffer initialization for these three tests. When menu responds to entering "111" with "use default hit_buffer [F]", the tests will use the buffer as initialized by the Fill Buffer menu option. When the menu responds to entering "111" with "use default hit_buffer [T]", the tests will use default buffer initializations.

The menu:

```
0 : fill selected position
1 : fill with row of pattern
2 : fill with 5555...
   AAAA...
3 : fill with FFFF...
   0000...
4 : fill with PC counter -fixed- pattern
5 : fill with PC counter -running- pattern
6 : fill with random pattern
7 : fill with repeated N raw pattern
   LLLL...
   WWWW...
   KKKK...
8 : display selected positions
99 : exit
```

Selection :

o Use RPC [F]

Sets a flag used by the TSM initialization routine. If set, this flag enables a variation on the scrambling routine used to setup the TSM data buffer which is specific to the RPC version of the PC. Assuming that only PCs are tested, none of the system tests require this flag to be set.

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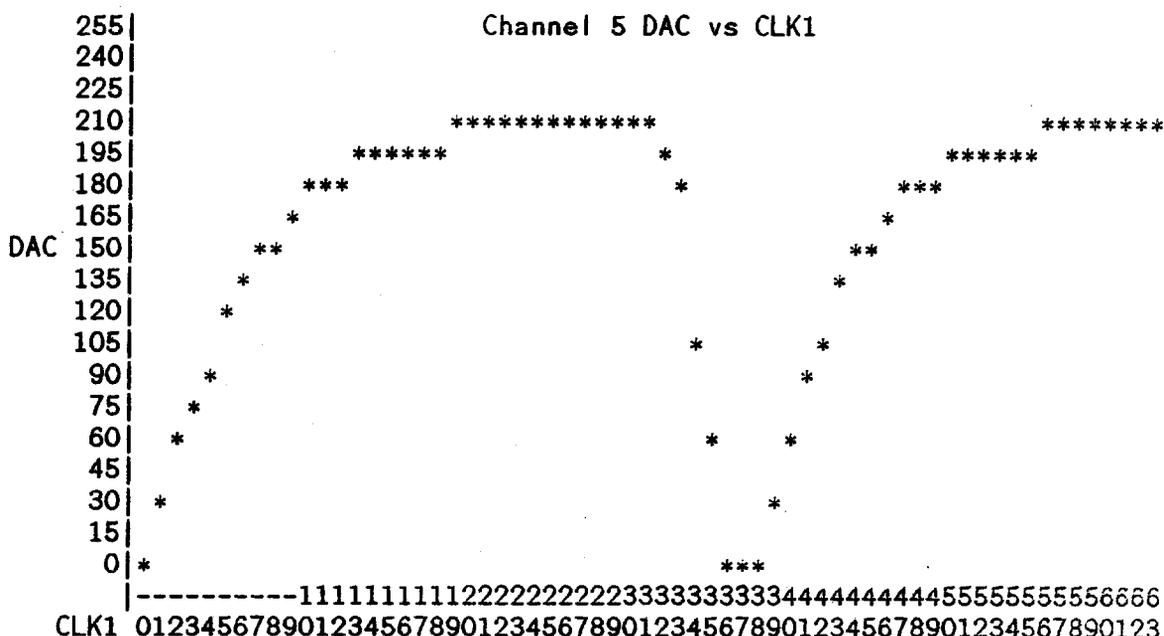
- o One ch CLK1/DAC scan [F]

This option, which only applies to the CLK1/DAC scan, allows one selected channel to be scanned, verses all 128 channels.

- o Print stats buf horiz

This menu option is for examining the CLK1/DAC scan data on individual channels. It allows selection of a single channel or range of channels for graphic display. If using the RPX version of the system tests, the graphs may be printed to an output file by enabling the Log errors to file switch in the Debugging options menu.

Example output:



The DAC values shown on the vertical axis represent the programmed DAC value. Actual DAC output is approximately equal to the programmed value multiplied by 5mV. CLK1 values on the horizontal axis also represent programmed value. The actual CLK1 value is equal to the programmed value multiplied by 0.5 nsec. Note that the graph displays the actual hit (the first pulse) and an extra hit, (the second pulse) which is provided by the DE. The extra hit provided by the DE is enabled by jumpers on the DE board.

- o FIFO block transfer enable [F]

This option allows use of the FSCC data FIFO. If enabled, data is also copied to the FSCC processor FIFO

SYSTEM TEST SOFTWARE DESCRIPTION

for checking. Enabling this option may slow test execution speed, and in some cases the FSCC data FIFO may overflow. This option, however, will allow data to be read out by an auxiliary device attached to the FSCC.

- o Print stats buf vert

This option allows a finer examination of the CLK1/DAC scan channel data. The display for each selected channel is distributed across several terminal screens.

- o Debugging options menu (default state on switches shown)

- a) Stop on error switch [F]
- b) Readout loop delay (0 dec) [F]
- c) Debugging mode switch [F]
- d) Stepping mode switch [F]
- e) Log errors to file switch (rpx only) [F]
- f) Log errors to banner switch [F]
- g) Print errors to terminal [F]
- h) Display Status
- x) Exit debugging options menu

Select option:

- o Stop on error switch [F] - Sets a flag. Applies to PC test counter test and TSM as PC tests only.
- o Readout loop delay (0 dec) [F] - Sets a flag and a delay value if enabled. Applies to PC test counter test and TSM as PC tests only. A delay count value of 3,000,000 produces a delay of about 1 second.
- o Debugging mode switch [F] - If enabled, sets a flag with test specific meanings as follows.

CLK1/DAC scan - display TSM input buffer, each CLK1 value used,
each DAC value used

PC crosstalk test - display first 5 TSM input buffer locations

PC channel characterization tests - display TSM input buffer, display
internally buffered data for graphi
display

PC channel quick tests - display TSM input buffer

- o Stepping mode switch [F] - Sets a flag. Internal routines for dynamic memory allocation, deallocation, PC initialization, MTC initialization, and SE initialization respond with a print statement indicating the next action to be taken, which must be initiated with a keyboard <Return>. The PC test counter test and TSM as PC test also use this flag in the same manner to indicate internal test

SYSTEM TEST SOFTWARE DESCRIPTION

actions.

- o Log errors to file switch (rpx only) [F] - This option tries to open a file with the name "syst.log" in the current directory. All tables and graphs output to the terminal are also written to this log file. Menus and other prompts do not appear in this file. The log file is always opened with the append option, so all data logged will go to the same file.
- o Log errors to banner switch [F] - Sets a flag. If enabled, the PC test counter test and TSM as PC test will have a banner displayed in inverse video along the bottom of the terminal screen indicating the current PC plane ID, DE address being read, total number of data errors, total number of word count errors, and total test iterations. Because of the frequent screen updates, use of this option will significantly reduce test execution speed.
- o Print errors to terminal [F] - If enabled, errors detected after each DE address read will be displayed in tabular form. An example:

```

=====> PC 21 <=====
-----
 0 ** | 1 * P | 2 ** | 3 * P | 4 ** | 5 * P | 6 ** | 7 *
 8 ** | 9 * P | 10 ** | 11 * P | 12 ** | 13 * P | 14 ** | 15 *
16 ** | 17 * P | 18 ** | 19 * P | 20 ** | 21 * P | 22 ** | 23 *
24 ** | 25 * P | 26 ** | 27 * P | 28 ** | 29 * P | 30 ** | 31 *
32 M | 33 M | 34 M | 35 M | 36 M | 37 M | 38 M | 39
40 M | 41 M | 42 M | 43 M | 44 M | 45 M | 46 M | 47
48 M | 49 M | 50 M | 51 M | 52 M | 53 M | 54 M | 55
56 M | 57 M | 58 M | 59 M | 60 M | 61 M | 62 M | 63
64 M | 65 M | 66 M | 67 M | 68 M | 69 M | 70 M | 71
72 M | 73 M | 74 M | 75 M | 76 M | 77 M | 78 M | 79
80 M | 81 M | 82 M | 83 M | 84 M | 85 M | 86 M | 87
88 M | 89 M | 90 M | 91 M | 92 M | 93 M | 94 M | 95
96 M | 97 M | 98 M | 99 M | 100 M | 101 M | 102 M | 103
104 M | 105 M | 106 M | 107 M | 108 M | 109 M | 110 M | 111
112 M | 113 M | 114 M | 115 M | 116 M | 117 M | 118 M | 119
120 M | 121 M | 122 M | 123 M | 124 M | 125 M | 126 M | 127
-----
Extra Ch. (E) : 0, Missing Ch. (M) : 96, Prev. Bucket Error (P) :
TA : 0, CLK1 : 20 Buffer [254] : FFFFFFFFFFFFFFFFFFFFFFFFFFAA
CLK2 : 24, DAC : 50 [255] : FFFFFFFFFFFFFFFFFFFFFFFFFF
Rec. : 32, Exp. : 128 ==> [ 0] : 000000000000000000000000
[ 1] : 000000000000000000000000055
  
```

The first "star" to the right of a channel number indicates that an expected channel was received. The second "star" to the right of a channel number indicates the expected previous hit flag was

SYSTEM TEST SOFTWARE DESCRIPTION

received. Single capital letters following channel numbers indicate errors as shown by the key at the bottom of the table.

- o Display Status - Selecting this option will cause a table of information to be printed to the screen which represents the current content of the SSD module CSR registers. An example display:

```
=====
MTC CSR0=01a20985 CSR10=00000100 CSR11=00000010 CSR12=000000fc CSR13=00
```

```
TRIG PHASE ERR=0 FIFO OVFL ERR    =0 MEM OVWR ERR=1 DE SEQ ERR
CLOCK MISSING =0 TEST_MODE        =1 ENC_READY   =1 CALIBRATION_MOD
WRITE_ENABLE  =1 FIFO_RA           =00 PRDPATH   =0 TOFFSET
CKPHASE       =00 ERROR_FLAG       =1 TRIG_WAIT   =1 FIFO_NOT_EMPTY
```

```
-----
SE CSR0=01a30040 CSRCx10=00000000 CSRCx11=040c0600 CSRCx12=00000000
```

```
OVERFLOW TRUNC    =0 LOAD_AUXILIARY =0 LOAD_FASTBUS    =1 BLOCK_C
WORD_COUNT        =00 CLK2_DELAY     =18 CLK1_DELAY     =00
ENCODER_ERROR STATUS =000 SYNC_ERROR_FLAG =0
PLANE_ENCODER_RAM : 00 00 00 00 00 00 00 00 00 00 00 00
```

```
-----
PC SLOT=15 CSR0=00000000 CSR1=00000000
```

```
1MHz_CLOCK    =X CLK1_ENABLE=0 SUM_CHANNEL =0 SINGLE_CHANNEL=0
MODE_RUN       =0 MOD_STATUS =X MODE1_STATUS=X MODE2_STATUS =X
TEST_COUNTER   =00
```

5.4 SYSTEM TESTS DESCRIPTION

The system tests can be broadly categorized as those using the PC front panel input and those that do not. The "PC test counter test" and the "TSM as PC test" are the two tests that do not use the PC front panel input path. All other tests in the menu do use the PC front panel input path. A full description of each test follows.

5.4.1 TSM As PC Test

In this test the TSM generates test patterns and outputs them via the backplane to the DE. The DE is read out by the FSCC from the SE FIFO. Bit patterns are verified by the FSCC. System triggers are generated by the MTC. Errors may be displayed while the test is running as with the PC test counter test.

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5.4.1.1 Test Pattern - The TSM input data buffer must be initialized before running the TSM as PC test with the Fill buffer menu option. There is no default initialization for the data buffer for this test.

5.4.1.2 Initialization Menu Options - (default state shown)

- o Loop on trig add (0 dec) [F]
- o Accept prev bkt hit [T]
- o Trigger add range (0 to 255 dec)
- o Aux FIFO Enabled [F]
- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o Set CLK1 (20), CLK2 (24)
- o Set Trig Add Corr (-1 dec)

5.4.1.3 Debugging Menu Options - The following options can be used for the TSM as PC test. The default state is shown.

- o Stop on error switch [F]
- o Readout loop delay (0 dec) [F]
- o Stepping mode switch [F]
- o Log errors to file switch (rpx only) [F]
- o Log errors to banner switch [F]
- o Print errors to terminal [F]

5.4.2 PC Test Counter Test

In this test the PC generates test patterns which are latched by the DE and read out by the FSCC from the SE. The PC test patterns are verified by the FSCC. System triggers are generated by the MTC. Errors may be reported during the test by enabling one of the debugging submenu options. An error summary is given

SYSTEM TEST SOFTWARE DESCRIPTION

at the end of the test. See appendix for standard error summary.
NOTE: the TSM and LSM modules should be removed from the crate during this test or spurious errors will occur. In addition, the trigger address correction should be set to 1 with the system test initialization menu option Set Trig Add Corr (d dec). This test will loop indefinitely until a keyboard <Return> is entered.

5.4.2.1 Initialization Menu Options -

5.4.2.1.1 Test Pattern -

1. Running Test Cntr [T], Rolling Test Cntr [F]

The DE is filled with patterns resulting from incrementing the PC test counter by one, 255 times. (See appendix for patterns.) Each input buffer pattern always corresponds to the same DE trigger address, i.e. first test counter pattern to DE trigger address 0, second test counter pattern to DE trigger address 1, etc. The initial test counter pattern is set with option Set Test Cntr (xx hex).

2. Running Test Cntr [F], Rolling Test Cntr [T]

The DE is filled with patterns resulting from incrementing the PC test counter by one, 255 times. After all PC test counter patterns are read out from the DE, the PC test counter patterns are rewritten to the DE, incrementing the test patterns relationship to DE trigger addresses by one. The PC test counter patterns are "rotated" through DE trigger addresses in this manner so that each test pattern is eventually read out from each possible DE trigger address. The initial test counter pattern is set with option Set Test Cntr (xx hex). This is the default mode for the PC injecting bit pattern test.

3. Running Test Cntr [F], Rolling Test Cntr [F]

With both options false, the entire DE memory is filled with the pattern resulting from the test counter value input with option Set Test Cntr (xx hex).

5.4.2.1.2 Other Options Affecting Test - (default state shown)

SYSTEM TEST SOFTWARE DESCRIPTION

- o Loop on trig add (0 dec) [F]
- o Accept prev bkt hit [T]
- o Trigger add range (0 to 255 dec)
- o Aux FIFO Enabled [F]
- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o Set CLK1 (20), CLK2 (24)
- o Set Trig Add Corr (-1 dec)

5.4.2.1.3 Options Set Automatically By Test - (to state shown)

- o PC latch mode [F]
- o IC Enable [F]
- o SC Enable [F]

5.4.2.2 Debugging Menu Options - The following options can be used for the PC test counter test. The default state is shown.

- o Stop on error switch [F]
- o Readout loop delay (0 dec) [F]
- o Stepping mode switch [F]
- o Log errors to file switch (rpx only) [F]
- o Log errors to banner switch [F]
- o Print errors to terminal [F]

5.4.3 General Readout Loop

This is a general readout routine which allows maximum flexibility in a test configuration using test modules like the TSM-LSM pair or the DCC to provide input for a single PC/DE pair of SSD

SYSTEM TEST SOFTWARE DESCRIPTION

modules. This flexibility is provided to allow creation of special purpose trouble-shooting loops. Data taken from this test is not saved, but the standard error summary is displayed when the General readout loop is stopped by keyboard <Return> or ends. There are no default parameters supplied by the test which requires that several parameters be setup in the System test initialization menu prior to executing the test. These parameters control DAC, CLK1 and trigger address loops. The input data buffer for the TSM must also be setup in the System initialization menu with the Fill Buffer menu option.

5.4.3.1 Required Initializations - (default state shown)

- o CLK1 scan (0,63, 1, F) - If the scan range is not enabled as indicated by the flag, the test will use the CLK1 value displayed by the Set CLK1 (dd), CLK2 (dd) menu option.
- o Set CLK1 (20), CLK2 (24) - Used if CLK1 scan function not enabled.
- o Fill Buffer
- o PC latch mode [T]
- o DAC scan (230, 0, -1, F) - If the scan range is not enabled as indicated by the flag, the test will use the DAC value displayed by the Set DAC buffer (ddd dec) menu option.
- o Set DAC buffer (100 dec) - Used if DAC scan function not enabled.
- o IC Enable [T]
- o SC Enable [F]

5.4.3.2 Optional Initializations - (default state shown)

- o Loop on trig add (0 dec) [F]
- o Accept prev bkt hit [T]
- o Trigger add range (0 to 255 dec)
- o Aux FIFO Enabled [F]

SYSTEM TEST SOFTWARE DESCRIPTION

- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o Set Trig Add Corr (-1 dec)

5.4.3.3 Debugging Menu Options -

- o Debugging mode switch [F]
- o Log errors to file switch (rpx only) [F]
- o Print errors to terminal [F]

5.4.4 CLK1/DAC Scan

This test produces a data base which contains the highest PC DAC value at which a channel is on for each SE CLK1 delay. The test is designed to take data on (1) or (128) channels through user selected ranges of DAC values and CLK1 delays. The channels may be read at a user selected DE trigger address. A table is provided at the end of the test which indicates the CLK1 value at the highest DAC value found for each channel. The criteria for finding a "higher" DAC value is that the DAC value must be 6 counts higher than the previous highest DAC value. This condition is imposed to try to find the highest DAC value in the actual hit instead of in the extra hit given by the DE. (In the graph displayed by the Print stats buf horiz menu option, the actual hit corresponds to the first pulse, and the extra hit given by the DE corresponds to the second pulse.) The average CLK1 value is a simple average of all CLK1 values displayed in the table below.

SYSTEM TEST SOFTWARE DESCRIPTION

| ch: CLK1 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 0: 23 | 1: 20 | 2: 16 | 3: 23 | 4: 18 | 5: 21 | 6: 22 | 7: 25 |
| 8: 15 | 9: 19 | 10: 15 | 11: 23 | 12: 15 | 13: 21 | 14: 14 | 15: 21 |
| 16: 58 | 17: 24 | 18: 17 | 19: 20 | 20: 15 | 21: 17 | 22: 18 | 23: 26 |
| 24: 14 | 25: 20 | 26: 16 | 27: 18 | 28: 17 | 29: 18 | 30: 13 | 31: 20 |
| 32: 15 | 33: 22 | 34: 16 | 35: 19 | 36: 18 | 37: 19 | 38: 14 | 39: 19 |
| 40: 16 | 41: 18 | 42: 10 | 43: 19 | 44: 15 | 45: 16 | 46: 10 | 47: 22 |
| 48: 13 | 49: 17 | 50: 13 | 51: 21 | 52: 18 | 53: 18 | 54: 10 | 55: 22 |
| 56: 15 | 57: 16 | 58: 8 | 59: 18 | 60: 18 | 61: 14 | 62: 12 | 63: 19 |
| 64: 21 | 65: 16 | 66: 12 | 67: 21 | 68: 17 | 69: 18 | 70: 16 | 71: 24 |
| 72: 16 | 73: 14 | 74: 15 | 75: 19 | 76: 22 | 77: 14 | 78: 19 | 79: 21 |
| 80: 18 | 81: 14 | 82: 14 | 83: 21 | 84: 16 | 85: 12 | 86: 15 | 87: 24 |
| 88: 19 | 89: 11 | 90: 14 | 91: 20 | 92: 16 | 93: 14 | 94: 15 | 95: 21 |
| 96: 0 | 97: 16 | 98: 10 | 99: 16 | 100: 16 | 101: 20 | 102: 14 | 103: 18 |
| 104: 20 | 105: 16 | 106: 10 | 107: 21 | 108: 18 | 109: 18 | 110: 16 | 111: 19 |
| 112: 19 | 113: 14 | 114: 8 | 115: 19 | 116: 19 | 117: 14 | 118: 15 | 119: 14 |
| 120: 18 | 121: 11 | 122: 9 | 123: 14 | 124: 22 | 125: 11 | 126: 16 | 127: 14 |

average CLK1 : 17
max CLK1 : 58
min CLK1 : 0

A error summary is also provided at the end of test. The system initialization menu options Print stats buf horiz and Print stats buf vert provide the means to examine individual channel data from the data base produced by the test. The data base contains valid data after the CLK1/DAC scan has completed, and retains that data until the CLK1/DAC scan is re-run, causing old data to be overwritten.

5.4.4.1 Test Pattern Input - The input data buffer for the TSM consists of (hex) A's and 5's. This data will produce a 50% duty cycle at the input of the PC. The buffer appears as follows:

```
[ 0] AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
[ 1] 55555555555555555555555555555555
[ 2] AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
[ 3] 55555555555555555555555555555555
.
.
.
[255] 55555555555555555555555555555555
```

5.4.4.2 Initialization Menu Options - (default state shown)

SYSTEM TEST SOFTWARE DESCRIPTION

- o Accept prev bkt hit [T]
- o Trigger add range (0 to 255 dec) - Uses beginng trigger address only.
- o Aux FIFO Enabled [F]
- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o CLK1 scan (0,63, 1, F)
- o Set Trig Add Corr (-1 dec)
- o DAC scan (230, 0, -1, F)
- o One ch CLK1/DAC scan [F]
- o Print stats buf horiz
- o Print stats buf vert

5.4.4.3 Options Set Automatically By Test - (to state shown)

- o PC latch mode [T]
- o IC Enable [T]
- o SC Enable [F]

5.4.4.4 Debugging Menu Options -

- o Debugging mode switch [F]
- o Log errors to file switch (rpx only) [F]
- o Print errors to terminal [F]

5.4.5 PC Channel Quick Tests

The "quick" tests for the PC front end use two TSM-LSM generated data patterns. The first pattern presented to the PC input is all 0's and should not generate PC output. If channels do

summary displayed at the lower left side of the graph.

5.4.5.1 Test Pattern Input - The input data buffer for the TSM consists of patterns selected via submenu to test either the PC individual or sum channel logic. When testing the individual channel logic, the sum channel logic is disabled and visa versa. The tests and corresponding input patterns are:

Whole buffer 0's, followed by:

- Individual channel
 - single 0's, F's
- Sum channel (3's)
 - single 0's, 3's
- Sum channel (6's)
 - single 0's, 6's
- Sum channel (C's)
 - single 0's, C's
- Sum channel (1's)
 - single 0's, 1's
- Sum channel (2's)
 - single 0's, 2's
- Sum channel (4's)
 - single 0's, 4's
- Sum channel (8's)
 - single 0's, 8's

A representative buffer for the Individual channel test:

```
[ 0] 00000000000000000000000000000000
[ 1] FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
[ 2] 00000000000000000000000000000000
[ 3] 00000000000000000000000000000000
.
.
.
[255] 00000000000000000000000000000000
```

5.4.5.2 Initialization Menu Options -

- o Accept prev bkt hit [T]
- o Trig add range (0 to 255 dec) - Only the beginning trigger address used.

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- o Aux FIFO Enabled [F]
- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o Set CLK1 (20), CLK2 (24)
- o Set DAC buffer (100 dec) - Depending on the combination of DAC value and input threshold used, adjacent sum channel responses indicated by "e"s on the graph may be present.
- o Set Trig Add Corr (-1 dec)

5.4.5.3 Automatic Initializatons -

- o PC latch mode [T]
- o IC Enable [T] - State depends on selected test.
- o SC Enable [F] - State depends on selected test.

5.4.5.4 Debugging Menu Options -

- o Debugging mode switch [F]
- o Log errors to file switch (rpx only) [F]
- o Print errors to terminal [F]

5.4.6 PC Channel Characterization Tests

Depending on the selected submenu option, this test does individual or sum channel characterization for the Postamp Comparator front end. The default test checks individual or sum channel response by scanning through a selected DAC range and recording where the channels respond less than 8 out of 8 reads and also where the channels respond 8 out of 8 reads. The fixed CLK1 value is user selected. The alternate test scans thru a selected CLK1 range using a selected, fixed DAC value. Selecting the DAC vs channel submenu option will toggle the test mode to CLK1 vs channel and visa versa.

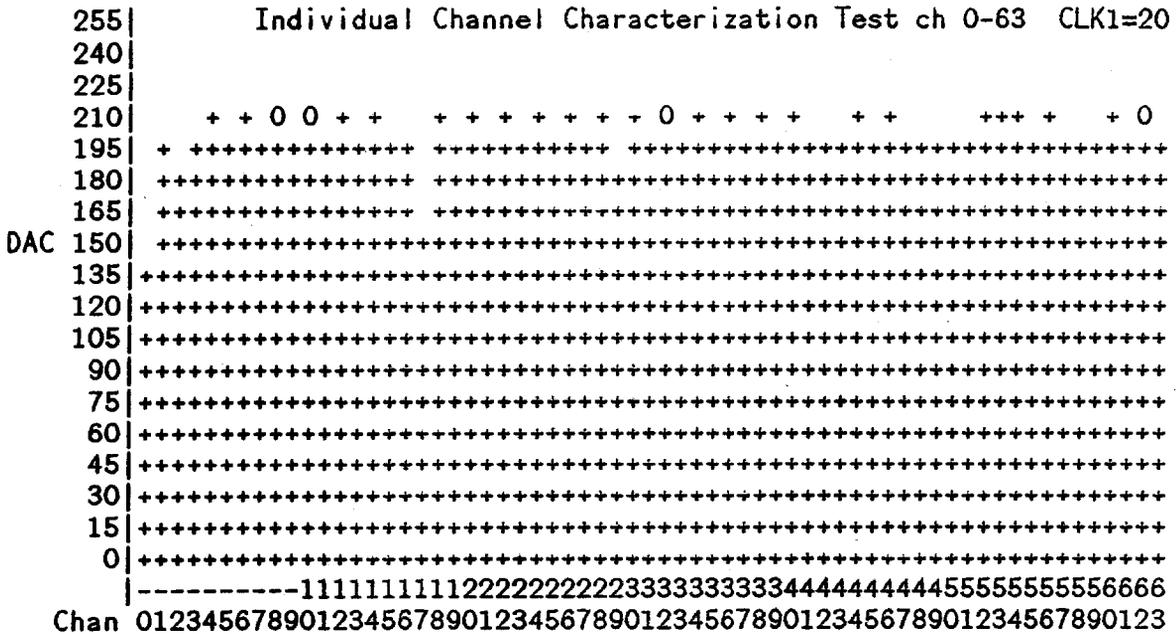
SYSTEM TEST SOFTWARE DESCRIPTION

Output is displayed graphically as follows:

```

no hits           = blank space
< 8 out of 8 hits = '0'
8 out of 8 hits  = '+'
    
```

Sample output for the DAC vs channel mode:



Output for this test is displayed in two terminal screens. The first screen displays channels 0 to 63, and the second screen displays channels 64 to 127.

SYSTEM TEST SOFTWARE DESCRIPTION

Sample output for the CLK1 vs channel mode:

```

68 |           Individual Channel Characterization Test ch 0-63  DAC=190
64 |
60 | ++++++0++++ ++++++ ++++++ ++++++
56 | ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++
52 | + ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++
48 | + + + + + + + + + + + + + + + + + + + + + + + + + + + + + +
44 | + + + + + + + + + + + + + + + + + + + + + + + + + + + + + +
CLK1 40 |
36 |
32 | + + + + + + + + + + + + + + + + + + + + + + + + + + + + + +
28 | + ++++++ + +0+ + + + + + + + + + + + + + + + + + + + + + +
24 | ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ +
20 | ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ +
16 | + ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ ++++++ +
12 | + + + + + + + + + + + + + + + + + + + + + + + + + + + + + +
8 | + + + + + + + + + + + + + + + + + + + + + + + + + + + + + +
4 |
0 | -----111111111122222222223333333333444444444455555555556666
Chan 012345678901234567890123456789012345678901234567890123

```

Output is also displayed in two screens as with the DAC vs channel mode.

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5.4.6.1 Test Pattern Input - The input data buffer for the TSM consists of patterns selected via submenu to test either the PC individual or sum channel logic. When testing the individual channel logic, the sum channel logic is disabled and visa versa. The tests and corresponding patterns are:

Individual channel

whole buffer F's, 0's
Sum channel (3's)
whole buffer 3's, 0's
Sum channel (6's)
whole buffer 6's, 0's
Sum channel (C's)
whole buffer C's, 0's
Sum channel (1's)
whole buffer 1's, 0's
Sum channel (2's)
whole buffer 2's, 0's
Sum channel (4's)
whole buffer 4's, 0's
Sum channel (8's)
whole buffer 8's, 0's

A representative buffer for the Individual channel test:

```
[ 0] FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
[ 1] 00000000000000000000000000000000
[ 2] FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
.
.
.
[255] 00000000000000000000000000000000
```

5.4.6.2 Initialization Menu Options - (defaults shown)

- o Accept prev bkt hit [T]
- o Trig add range (0 to 255 dec) - The beginning trigger address only used.
- o Aux FIFO Enabled [F]
- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o CLK1 scan (0,63, 1, F) - Used for the CLK1 vs channel mode.

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- o Set CLK1 (20), CLK2 (24) - Used for the DAC vs channel mode.
- o Set DAC buffer (100 dec) - Used for the CLK1 vs channel mode.
- o Set Trig Add Corr (-1 dec)
- o DAC scan (230, 0, -1, F) - Used for the DAC vs channel mode.

5.4.6.3 Automatic Initializations -

- o PC latch mode [T]
- o IC Enable [T] - State depends on selected test.
- o SC Enable [F] - State depends on selected test.

5.4.6.4 Debugging Menu Options -

- o Debugging mode switch [F]
- o Log errors to file switch (rpx only) [F]
- o Print errors to terminal [F]

5.4.7.2 Initialization Options -

- o Trig add range (0 to 255 dec) - Accepts beginning trigger address only.
- o Aux FIFO Enabled [F]
- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o Set CLK1 (20), CLK2 (24)
- o Set Trig Add Corr (-1 dec)
- o DAC scan (230, 0, -1, F)

5.4.7.3 Automatic Initializaton - (to state shown)

- o PC latch mode [T]
- o IC Enable [T]
- o SC Enable [F]

5.4.7.4 Debugging Menu Options -

- o Debugging mode switch [F]
- o Log errors to file switch (rpx only) [F]
- o Print errors to terminal [F]

5.4.8 Default System Tests

This test is a shell used to run several of the system tests. The system tests run with default parameters which are in effect only during the execution of this test. These tests include:

1. CLK1/DAC scan - Default parameters include a DAC scan range of 250 to 0 by steps of -1, and a CLK1 scan range of 0 to 63 by steps of 1.

SYSTEM TEST SOFTWARE DESCRIPTION

2. PC channel quick tests - This test is run with the (8) patterns which correspond to PC individual and sum channel modes.
3. PC channel characterization tests - The test is run in the DAC versus channel mode and CLK1 versus channel mode with PC individual logic enabled only.
4. PC crosstalk test - The default parameters for the DAC scan range are 230 to 20 by steps of -1.

5.4.9 Trigger Address Scan

This option is not a test, but uses the TSM-LSM pair in conjunction with a DE-PC pair to determine the DE address where TSM generated data should appear. The result suggests a value for the trigger address correction that should then be entered in the system test initialization menu. This routine scans through both CLK1 values and DE trigger addresses to find a TSM input pattern of 128 channels enabled. The CLK1 scan range and steps may be controlled by system initialization menu option, but the routine will always scan DE addresses 0 through 255. MTC module Trigger address offset calculation information and scan results are presented following the completion of the scan.

5.4.9.1 Initialization Menu Options -

- o Accept prev bkt hit [T]
- o Aux FIFO Enabled [F]
- o FASTBUS FIFO Enabled [T]
- o Ovflw trunc Enabled [F]
- o CLK1 scan (0,63, 1, F)

5.4.9.2 Debugging Menu Options -

- o Debugging mode switch [F]
- o Log errors to file switch (rpx only) [F]

SYSTEM TEST SOFTWARE DESCRIPTION

- o Print errors to terminal [F]

CHAPTER 6
REFERENCE DOCUMENTS

The following is a brief listing of supporting hardware and software product documents. Document HN102 contains a complete listing of SSD hardware documentation.

- o PORT_MGR - PN406
- o FSCC - HN96
- o RPX - PN384
- o FSR_FSCC (FASTBUS Standard Routines) - PN416

CHAPTER 7
RELEASE NOTES

7.1 SYSTEM TESTS V1.0

7.1.1 Hardware Versions

- o PC - Ver 2
- o DE - Rev 2
- o SE - Rev A
- o MTC - Rev C
- o TSM - July 1990
- o LS - June 1990
- o FSCC - PC2, PC3 with board revisions to date
- o SSD Backplane - Rev A

7.1.2 Executables

- o SYST.ABS - System Tests described by this document, PN436. The target for this executable is the FSCC.
- o SYST_RPX.EXE - Same as above, but built for execution on the VAX using Remote Procedure Calls over a serial or Ethernet connection to the FSCC.
- o SYST_RPX_DBG.EXE - Same as SYST_RPX.EXE, but built to enable VAX debugging.

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7.1.3 Remote Procedure Call Executables For FSCC

- o FSR.ABS - Serial communication version of FASTBUS Standard Routine server.
- o FSR_ETH.ABS - Ethernet communication version of FASTBUS Standard Routine server.

7.2 SYSTEM TESTS V1.1

7.2.1 Bug Fixes

- o Stop on error switch

This switch, which applies to the PC test counter tests and TSM as PC tests, caused test execution to stop after every trigger in V1.0. Initialization corrections allow this option to function as described in the section labeled "Debugging options menu" above.

- o TSM as PC tests

In version V1.0 TSM input data pattern scrambling was enabled. The scrambling function is disabled for version V1.1.

- o General readout loop

Several problems were corrected that caused this routine to loop incorrectly over CLK1 and DAC scan ranges.

- o Print errors to terminal

An initialization of an internal error counter was moved so that previous hit flag errors are now displayed if the Print errors to terminal Debugging menu option is enabled.

- o Default system tests

Trigger address correction is no longer set in this routine. The value used for the trigger address correction is the value displayed by the System initialization menu.

- o SYST_RPX

Several tests required additional calls to the

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SWITCH_CRATE routine to cover error and no error conditions.

7.2.2 New Features

- o Tigger address scan

This feature was added to facilitate determination of the correct trigger address correction for the TSM-LSM tests using the new SSD backplane. The trigger address correction for the PC test counter tests has been found to have the following relationship to the TSM-LSM tests trigger address correction value:

TAC = trigger address correction value

PC test counter tests TAC = ((TSM-LSM tests TAC) + 2)

- o PC test counter tests

This routine was modified so that the SE word counter is written prior to each MTC trigger with the two's compliment of the expected word count. This modification causes the SE word count to be zero under normal circumstances. A non-zero word count provides a real time trigger for SE module debugging purposes. This modification handles the case of multiple PC-DE pairs, but is not designed to handle the case of SE overflow truncation enabled.

7.2.3 Changes In Behavior

1. FSCC pre verify event

This routine will only print the message "defaulting to fscv_vfy_event" if the Debugging menu option Print errors to terminal is enabled.

2. Trigger address correction

This value was initialized to 0 in V1.0. It is now intialized to -1 to reflect timing differences between the current and previous versions of the SSD backplane.

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3. PC test counter - Stop on error

The print statements were removed that duplicate the display of the test counter value and the previous and current bucket PC output patterns.

4. Default System tests

The average CLK1 value determined by the CLK1/DAC scan is no longer passed to the PC Quick tests. The CLK1 value for the entire set of tests is taken from the value given by the System test initialization menu.

5. Set Primary Addresses

The TSM PAD is now initialized to slot 17 (dec).

6. Set DAC buffer

This System test initialization option for changing the PC DAC value shows the new initialization value of 100.

APPENDIX A
PC TEST COUNTER PATTERNS

PC tp bits	resultant PC output				#bits set in output
[0]	00000000	00000000	00000000	00000000	(0)
[1]	00000000	00000000	00000000	55555555	(16)
[2]	00000000	00000000	00000000	AAAAAAAA	(16)
[3]	00000000	00000000	00000000	FFFFFFFF	(32)
[4]	00000000	00000000	55555555	00000000	(16)
[5]	00000000	00000000	55555555	55555555	(32)
[6]	00000000	00000000	55555555	AAAAAAAA	(32)
[7]	00000000	00000000	55555555	FFFFFFFF	(48)
[8]	00000000	00000000	AAAAAAAA	00000000	(16)
[9]	00000000	00000000	AAAAAAAA	55555555	(32)
[10]	00000000	00000000	AAAAAAAA	AAAAAAAA	(32)
[11]	00000000	00000000	AAAAAAAA	FFFFFFFF	(48)
[12]	00000000	00000000	FFFFFFFF	00000000	(32)
[13]	00000000	00000000	FFFFFFFF	55555555	(48)
[14]	00000000	00000000	FFFFFFFF	AAAAAAAA	(48)
[15]	00000000	00000000	FFFFFFFF	FFFFFFFF	(64)
[16]	00000000	55555555	00000000	00000000	(16)
[17]	00000000	55555555	00000000	55555555	(32)
[18]	00000000	55555555	00000000	AAAAAAAA	(32)
[19]	00000000	55555555	00000000	FFFFFFFF	(48)
[20]	00000000	55555555	55555555	00000000	(32)
[21]	00000000	55555555	55555555	55555555	(48)
[22]	00000000	55555555	55555555	AAAAAAAA	(48)
[23]	00000000	55555555	55555555	FFFFFFFF	(64)
[24]	00000000	55555555	AAAAAAAA	00000000	(32)
[25]	00000000	55555555	AAAAAAAA	55555555	(48)
[26]	00000000	55555555	AAAAAAAA	AAAAAAAA	(48)
[27]	00000000	55555555	AAAAAAAA	FFFFFFFF	(64)
[28]	00000000	55555555	FFFFFFFF	00000000	(48)
[29]	00000000	55555555	FFFFFFFF	55555555	(64)
[30]	00000000	55555555	FFFFFFFF	AAAAAAAA	(64)
[31]	00000000	55555555	FFFFFFFF	FFFFFFFF	(80)
[32]	00000000	AAAAAAAA	00000000	00000000	(16)
[33]	00000000	AAAAAAAA	00000000	55555555	(32)

PC TEST COUNTER PATTERNS

[34]	00000000	AAAAAAAA	00000000	AAAAAAAA	(32)
[35]	00000000	AAAAAAAA	00000000	FFFFFFFF	(48)
[36]	00000000	AAAAAAAA	55555555	00000000	(32)
[37]	00000000	AAAAAAAA	55555555	55555555	(48)
[38]	00000000	AAAAAAAA	55555555	AAAAAAAA	(48)
[39]	00000000	AAAAAAAA	55555555	FFFFFFFF	(64)
[40]	00000000	AAAAAAAA	AAAAAAAA	00000000	(32)
[41]	00000000	AAAAAAAA	AAAAAAAA	55555555	(48)
[42]	00000000	AAAAAAAA	AAAAAAAA	AAAAAAAA	(48)
[43]	00000000	AAAAAAAA	AAAAAAAA	FFFFFFFF	(64)
[44]	00000000	AAAAAAAA	FFFFFFFF	00000000	(48)
[45]	00000000	AAAAAAAA	FFFFFFFF	55555555	(64)
[46]	00000000	AAAAAAAA	FFFFFFFF	AAAAAAAA	(64)
[47]	00000000	AAAAAAAA	FFFFFFFF	FFFFFFFF	(80)
[48]	00000000	FFFFFFFF	00000000	00000000	(32)
[49]	00000000	FFFFFFFF	00000000	55555555	(48)
[50]	00000000	FFFFFFFF	00000000	AAAAAAAA	(48)
[51]	00000000	FFFFFFFF	00000000	FFFFFFFF	(64)
[52]	00000000	FFFFFFFF	55555555	00000000	(48)
[53]	00000000	FFFFFFFF	55555555	55555555	(64)
[54]	00000000	FFFFFFFF	55555555	AAAAAAAA	(64)
[55]	00000000	FFFFFFFF	55555555	FFFFFFFF	(80)
[56]	00000000	FFFFFFFF	AAAAAAAA	00000000	(48)
[57]	00000000	FFFFFFFF	AAAAAAAA	55555555	(64)
[58]	00000000	FFFFFFFF	AAAAAAAA	AAAAAAAA	(64)
[59]	00000000	FFFFFFFF	AAAAAAAA	FFFFFFFF	(80)
[60]	00000000	FFFFFFFF	FFFFFFFF	00000000	(64)
[61]	00000000	FFFFFFFF	FFFFFFFF	55555555	(80)
[62]	00000000	FFFFFFFF	FFFFFFFF	AAAAAAAA	(80)
[63]	00000000	FFFFFFFF	FFFFFFFF	FFFFFFFF	(96)
[64]	55555555	00000000	00000000	00000000	(16)
[65]	55555555	00000000	00000000	55555555	(32)
[66]	55555555	00000000	00000000	AAAAAAAA	(32)
[67]	55555555	00000000	00000000	FFFFFFFF	(48)
[68]	55555555	00000000	55555555	00000000	(32)
[69]	55555555	00000000	55555555	55555555	(48)
[70]	55555555	00000000	55555555	AAAAAAAA	(48)
[71]	55555555	00000000	55555555	FFFFFFFF	(64)
[72]	55555555	00000000	AAAAAAAA	00000000	(32)
[73]	55555555	00000000	AAAAAAAA	55555555	(48)
[74]	55555555	00000000	AAAAAAAA	AAAAAAAA	(48)
[75]	55555555	00000000	AAAAAAAA	FFFFFFFF	(64)
[76]	55555555	00000000	FFFFFFFF	00000000	(48)
[77]	55555555	00000000	FFFFFFFF	55555555	(64)
[78]	55555555	00000000	FFFFFFFF	AAAAAAAA	(64)
[79]	55555555	00000000	FFFFFFFF	FFFFFFFF	(80)
[80]	55555555	55555555	00000000	00000000	(32)
[81]	55555555	55555555	00000000	55555555	(48)
[82]	55555555	55555555	00000000	AAAAAAAA	(48)
[83]	55555555	55555555	00000000	FFFFFFFF	(64)
[84]	55555555	55555555	55555555	00000000	(48)
[85]	55555555	55555555	55555555	55555555	(64)
[86]	55555555	55555555	55555555	AAAAAAAA	(64)

PC TEST COUNTER PATTERNS

[87]	55555555	55555555	55555555	FFFFFFFF	(80)
[88]	55555555	55555555	AAAAAAAA	00000000	(48)
[89]	55555555	55555555	AAAAAAAA	55555555	(64)
[90]	55555555	55555555	AAAAAAAA	AAAAAAAA	(64)
[91]	55555555	55555555	AAAAAAAA	FFFFFFFF	(80)
[92]	55555555	55555555	FFFFFFFF	00000000	(64)
[93]	55555555	55555555	FFFFFFFF	55555555	(80)
[94]	55555555	55555555	FFFFFFFF	AAAAAAAA	(80)
[95]	55555555	55555555	FFFFFFFF	FFFFFFFF	(96)
[96]	55555555	AAAAAAAA	00000000	00000000	(32)
[97]	55555555	AAAAAAAA	00000000	55555555	(48)
[98]	55555555	AAAAAAAA	00000000	AAAAAAAA	(48)
[99]	55555555	AAAAAAAA	00000000	FFFFFFFF	(64)
[100]	55555555	AAAAAAAA	55555555	00000000	(48)
[101]	55555555	AAAAAAAA	55555555	55555555	(64)
[102]	55555555	AAAAAAAA	55555555	AAAAAAAA	(64)
[103]	55555555	AAAAAAAA	55555555	FFFFFFFF	(80)
[104]	55555555	AAAAAAAA	AAAAAAAA	00000000	(48)
[105]	55555555	AAAAAAAA	AAAAAAAA	55555555	(64)
[106]	55555555	AAAAAAAA	AAAAAAAA	AAAAAAAA	(64)
[107]	55555555	AAAAAAAA	AAAAAAAA	FFFFFFFF	(80)
[108]	55555555	AAAAAAAA	FFFFFFFF	00000000	(64)
[109]	55555555	AAAAAAAA	FFFFFFFF	55555555	(80)
[110]	55555555	AAAAAAAA	FFFFFFFF	AAAAAAAA	(80)
[111]	55555555	AAAAAAAA	FFFFFFFF	FFFFFFFF	(96)
[112]	55555555	FFFFFFFF	00000000	00000000	(48)
[113]	55555555	FFFFFFFF	00000000	55555555	(64)
[114]	55555555	FFFFFFFF	00000000	AAAAAAAA	(64)
[115]	55555555	FFFFFFFF	00000000	FFFFFFFF	(80)
[116]	55555555	FFFFFFFF	55555555	00000000	(64)
[117]	55555555	FFFFFFFF	55555555	55555555	(80)
[118]	55555555	FFFFFFFF	55555555	AAAAAAAA	(80)
[119]	55555555	FFFFFFFF	55555555	FFFFFFFF	(96)
[120]	55555555	FFFFFFFF	AAAAAAAA	00000000	(64)
[121]	55555555	FFFFFFFF	AAAAAAAA	55555555	(80)
[122]	55555555	FFFFFFFF	AAAAAAAA	AAAAAAAA	(80)
[123]	55555555	FFFFFFFF	AAAAAAAA	FFFFFFFF	(96)
[124]	55555555	FFFFFFFF	FFFFFFFF	00000000	(80)
[125]	55555555	FFFFFFFF	FFFFFFFF	55555555	(96)
[126]	55555555	FFFFFFFF	FFFFFFFF	AAAAAAAA	(96)
[127]	55555555	FFFFFFFF	FFFFFFFF	FFFFFFFF	(112)
[128]	AAAAAAAA	00000000	00000000	00000000	(16)
[129]	AAAAAAAA	00000000	00000000	55555555	(32)
[130]	AAAAAAAA	00000000	00000000	AAAAAAAA	(32)
[131]	AAAAAAAA	00000000	00000000	FFFFFFFF	(48)
[132]	AAAAAAAA	00000000	55555555	00000000	(32)
[133]	AAAAAAAA	00000000	55555555	55555555	(48)
[134]	AAAAAAAA	00000000	55555555	AAAAAAAA	(48)
[135]	AAAAAAAA	00000000	55555555	FFFFFFFF	(64)
[136]	AAAAAAAA	00000000	AAAAAAAA	00000000	(32)
[137]	AAAAAAAA	00000000	AAAAAAAA	55555555	(48)
[138]	AAAAAAAA	00000000	AAAAAAAA	AAAAAAAA	(48)
[139]	AAAAAAAA	00000000	AAAAAAAA	FFFFFFFF	(64)

PC TEST COUNTER PATTERNS

[140]	AAAAAAAA	00000000	FFFFFFFF	00000000	(48)
[141]	AAAAAAAA	00000000	FFFFFFFF	55555555	(64)
[142]	AAAAAAAA	00000000	FFFFFFFF	AAAAAAAA	(64)
[143]	AAAAAAAA	00000000	FFFFFFFF	FFFFFFFF	(80)
[144]	AAAAAAAA	55555555	00000000	00000000	(32)
[145]	AAAAAAAA	55555555	00000000	55555555	(48)
[146]	AAAAAAAA	55555555	00000000	AAAAAAAA	(48)
[147]	AAAAAAAA	55555555	00000000	FFFFFFFF	(64)
[148]	AAAAAAAA	55555555	55555555	00000000	(48)
[149]	AAAAAAAA	55555555	55555555	55555555	(64)
[150]	AAAAAAAA	55555555	55555555	AAAAAAAA	(64)
[151]	AAAAAAAA	55555555	55555555	FFFFFFFF	(80)
[152]	AAAAAAAA	55555555	AAAAAAAA	00000000	(48)
[153]	AAAAAAAA	55555555	AAAAAAAA	55555555	(64)
[154]	AAAAAAAA	55555555	AAAAAAAA	AAAAAAAA	(64)
[155]	AAAAAAAA	55555555	AAAAAAAA	FFFFFFFF	(80)
[156]	AAAAAAAA	55555555	FFFFFFFF	00000000	(64)
[157]	AAAAAAAA	55555555	FFFFFFFF	55555555	(80)
[158]	AAAAAAAA	55555555	FFFFFFFF	AAAAAAAA	(80)
[159]	AAAAAAAA	55555555	FFFFFFFF	FFFFFFFF	(96)
[160]	AAAAAAAA	AAAAAAAA	00000000	00000000	(32)
[161]	AAAAAAAA	AAAAAAAA	00000000	55555555	(48)
[162]	AAAAAAAA	AAAAAAAA	00000000	AAAAAAAA	(48)
[163]	AAAAAAAA	AAAAAAAA	00000000	FFFFFFFF	(64)
[164]	AAAAAAAA	AAAAAAAA	55555555	00000000	(48)
[165]	AAAAAAAA	AAAAAAAA	55555555	55555555	(64)
[166]	AAAAAAAA	AAAAAAAA	55555555	AAAAAAAA	(64)
[167]	AAAAAAAA	AAAAAAAA	55555555	FFFFFFFF	(80)
[168]	AAAAAAAA	AAAAAAAA	AAAAAAAA	00000000	(48)
[169]	AAAAAAAA	AAAAAAAA	AAAAAAAA	55555555	(64)
[170]	AAAAAAAA	AAAAAAAA	AAAAAAAA	AAAAAAAA	(64)
[171]	AAAAAAAA	AAAAAAAA	AAAAAAAA	FFFFFFFF	(80)
[172]	AAAAAAAA	AAAAAAAA	FFFFFFFF	00000000	(64)
[173]	AAAAAAAA	AAAAAAAA	FFFFFFFF	55555555	(80)
[174]	AAAAAAAA	AAAAAAAA	FFFFFFFF	AAAAAAAA	(80)
[175]	AAAAAAAA	AAAAAAAA	FFFFFFFF	FFFFFFFF	(96)
[176]	AAAAAAAA	FFFFFFFF	00000000	00000000	(48)
[177]	AAAAAAAA	FFFFFFFF	00000000	55555555	(64)
[178]	AAAAAAAA	FFFFFFFF	00000000	AAAAAAAA	(64)
[179]	AAAAAAAA	FFFFFFFF	00000000	FFFFFFFF	(80)
[180]	AAAAAAAA	FFFFFFFF	55555555	00000000	(64)
[181]	AAAAAAAA	FFFFFFFF	55555555	55555555	(80)
[182]	AAAAAAAA	FFFFFFFF	55555555	AAAAAAAA	(80)
[183]	AAAAAAAA	FFFFFFFF	55555555	FFFFFFFF	(96)
[184]	AAAAAAAA	FFFFFFFF	AAAAAAAA	00000000	(64)
[185]	AAAAAAAA	FFFFFFFF	AAAAAAAA	55555555	(80)
[186]	AAAAAAAA	FFFFFFFF	AAAAAAAA	AAAAAAAA	(80)
[187]	AAAAAAAA	FFFFFFFF	AAAAAAAA	FFFFFFFF	(96)
[188]	AAAAAAAA	FFFFFFFF	FFFFFFFF	00000000	(80)
[189]	AAAAAAAA	FFFFFFFF	FFFFFFFF	55555555	(96)
[190]	AAAAAAAA	FFFFFFFF	FFFFFFFF	AAAAAAAA	(96)
[191]	AAAAAAAA	FFFFFFFF	FFFFFFFF	FFFFFFFF	(112)
[192]	FFFFFFFF	00000000	00000000	00000000	(32)

APPENDIX B

STANDARD ERROR SUMMARY

Total events read:	2	Data verify errors:	128
Events with errors:	2	Prev. bucket errors:	16
Sync errors:	0	Missing hit errors:	96
Word count errors:	2	Extra hit errors:	16