



Fermi National Accelerator Laboratory

FERMILAB-TM-1747

SSD Module Specifications and As-Built Hardware Descriptions

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April 1990

Introduction

This binder contains individual module specifications and as-built hardware description manuals for a Silicon Strip Detector (SSD) Readout System. The modules described herein have been assembled together as designed to provide a readout system for the E771 Silicon Strip Detector. The system was used to acquire data from the SSD during the Fermilab 1991 fixed target run.



Fermi National Accelerator Laboratory

April 11, 1990

TO: Distribution
FROM: Carl Swoboda 
SUBJECT: Silicon Strip Detector Readout System

The second edition specifications for all modules are included in this binder. The binder also contains papers that were submitted to the 1989 I.E.E.E. Nuclear Science Symposium. The system paper describes the overall system. Some specific details of the system have been improved since the paper was written but the paper does provide an accurate description of the proposed system implementation. The Preamplifier section contains papers specific to the detector mounted preamplifier system.

If you are interested in the detailed logic design of any of the modules listed in this binder please see Hector Gonzalez for logic schematics.

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A HIGH-RATE FASTBUS SILICON STRIP READOUT SYSTEM *

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Abstract

This paper describes a synchronous silicon strip readout system capable of zero deadtime readout at average trigger rates in excess of 1 MHz. The system is implemented in FASTBUS, uses pipelining techniques, and includes point-to-point fiberoptic data links to transmit detector digital data. Semi-custom ASIC chips are used to amplify, discriminate, and logically combine track data before encoding. This paper describes the overall system, each major FASTBUS module, and the functional aspects of the ASIC chips.

Introduction

Extracted beams at Fermilab retain the 53 MHz RF structure of the Tevatron accelerator. Events occur in well defined "buckets" of time which are approximately 1.5 ns long and occur every 18.9 ns. We are developing a silicon strip detector readout system capable of associating all of the information from an event with a single RF bucket and completely recovering within one or two buckets. The system operates synchronously with the 53 MHz Tevatron clock. A digital memory is used to provide a trigger delay, which is adjustable in one bucket steps to a maximum of 4.8 μ s.

The system consists of amplifiers mounted on the detector[1][2] and a set of FASTBUS modules that discriminate, delay, encode, and readout detector hit information.

System Overview

A block diagram of the system is shown in Figure 1. The detector signals are amplified by pre-amplifiers mounted near the detector. The amplified signals are connected to the FASTBUS data acquisition system by high density, .025 pitch, ribbon cables.

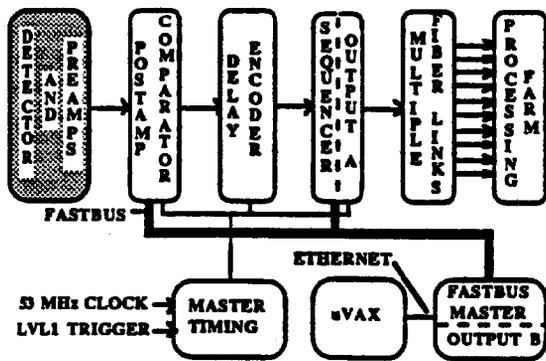


Figure 1: System Block Diagram

*This work performed under the auspices of the United States Department of Energy.

The Postamp/Comparator (P/C) modules discriminate the amplified signals. The discriminated signals are synchronously applied to the Delay/Encoder (D/E) modules in parallel where all channel data is delayed pending a Level 1 trigger signal. Upon the occurrence of a Level 1 trigger, the hit data propagating through the memories of the D/E modules is input to the encoders. Up to 12 D/E modules simultaneously pass encoded hit data to the Sequencer (SEQ) modules. Data can be readout through a FASTBUS Master in each crate (output B), or be transmitted directly out of the Sequencer modules (output A), over fiberoptic cable, to individual input ports of a NEVIS [3] [4] readout and processing system.

System Board Partitioning

The FASTBUS implementation of the system is based on 128 channel increments. Each fully loaded FASTBUS crate can process a maximum of 1536 channels. Each crate can contain 12 Postamp/Comparator modules, 12 Delay/Encoder modules, a FASTBUS Smart Crate Controller, and a Sequencer module. A crate implementation is shown in Figure 2.

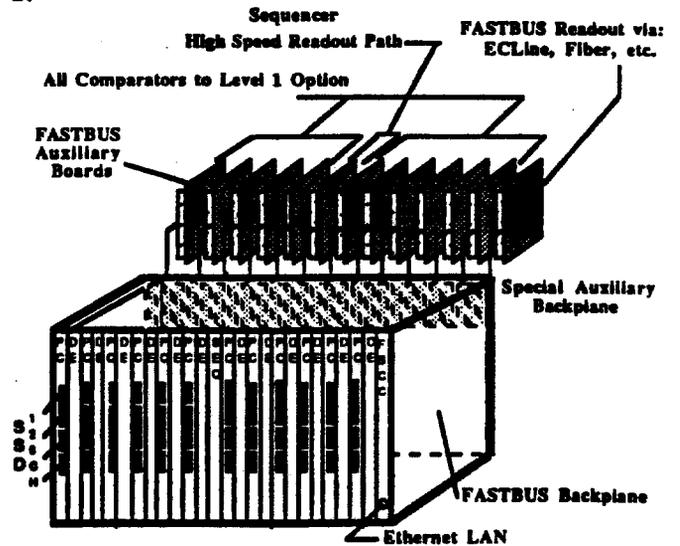


Figure 2: Crate Module Partitioning

Two different readout modes are user selectable. The FASTBUS readout path provides a relatively high bandwidth output to be used with FASTBUS, VME, or CAMAC buffers on the receiving end. The Sequencer output is intended to be used to feed optical links. In the fiberoptic link case, each crate transmits data to an independent receiver buffer that is part of a high speed event processor [4]. The Data transmission rate using the fiberoptic FASTBUS Auxiliary port is 40 MBytes/Sec/Crate.

System Modules

Preamplifier

A silicon strip amplifier which uses a Tektronix semicustom bipolar integrated circuit has been developed [2]. It has a fast impulse response (35 ns base to base) and high gain (17 mv/fc), and is able to directly drive a differential transmission line. The amplifiers are mounted in small custom leadless chip carriers, with 25 mil pitch in order to meet density requirements. Sixteen chip carriers, or 128 channels, are mounted on a double sided printed circuit board measuring 3.5 X 4.5 inches. Each board plugs into an edge connector mounted directly on the silicon strip detector Kapton fanout. Four 64 conductor, 25 mil-pitch flat cables connect each preamplifier card to Postamp/Comparator modules. Due to the high gain-bandwidth of the amplifiers, special attention must be given to grounding and shielding [1].

Postamp/Comparator (P/C)

The P/C module amplifies, discriminates and logically combines 128 channels of silicon strip hit data. A block diagram of this module is shown in Figure 3. The major portion of the analog and digital circuitry required on this board is implemented using bipolar Application Specific Integrated Circuits (ASIC) manufactured by Tektronix. The threshold setting Digital-to-Analog Converter is implemented as a CMOS ASIC.

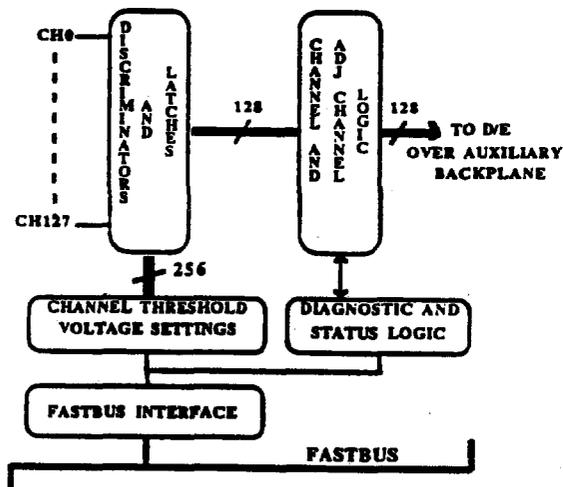


Figure 3: Postamp/Comparator Module

The following is a description of each ASIC contained on the P/C module.

ASIC 01: Two Channel Sum, Quad Latched Discriminator

A block diagram of this chip is shown in Figure 4. This ASIC receives low level linear differential signals from the preamplifiers mounted on the detector and produces analog sums of adjacent strip signals, discriminated digital signals of individual channels and discriminated signals of the analog summed adjacent channels. The analog sum block accepts the adjacent channel signals and provides an output proportional to the sum of its two inputs. The purpose of this block is to allow the discrimination of signals produced by particles which transverse the SSD midway between strips

causing the signal to be divided between two adjacent channels.

The discriminator block provides an output logic level for the duration that the input signal is above a threshold level. Each of the four discriminators has an individual threshold voltage control that allows individually set thresholds between 10 and 50 mV referred to the discriminator input. There is a built in hysteresis of 10 mV.

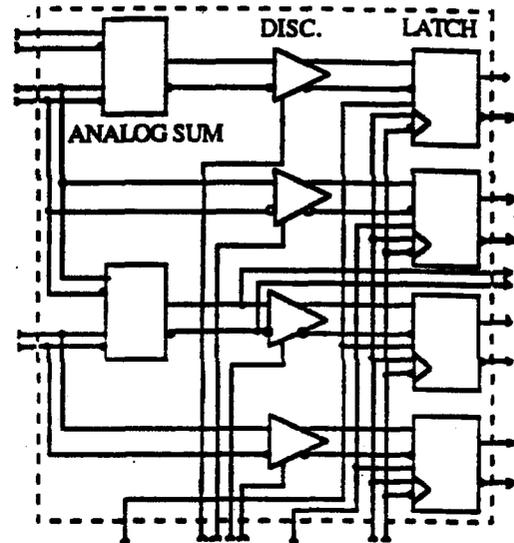


Figure 4: ASIC 01

The output of each discriminator drives a transparent latch, all four of which are controlled by a common 2.5 ns wide latch signal. In one state the latch is in the transparent mode, passing its input to the output. In the other state the output is latched ignoring input changes. There are also two Force Zero inputs, one for the individual signal latches and one for the summed signal latches that force the appropriate latch outputs to logical zeros.

ASIC 04: 5 Channel Logic and Octal NHU

The circuitry of ASIC 04 and ASIC 02 function jointly to logically combine 8 channels of track data. Block diagrams of the two ASICs are shown in Figures 5 and 6 respectively. They accept as inputs the outputs of 4 ASIC 01 chips (Two Channel Sum, Quad Latched Discriminators). If any individual channel input is above the threshold during the latch transition, a logical high is output on that corresponding channel. If two adjacent channels have signals both of which are below threshold but the sum of the two is above threshold, a logical high is output on those two corresponding channels.

The logic can be bit sliced at any channel boundary. Chip pinout limitations on the Tektronix linear arrays dictated that of a given set of 8 channels, the lower five would be processed by ASIC 04 and the upper three by ASIC 02. Thus 16 ASIC 04/ASIC 02 pairs are capable of processing all 128 channels as one logical unit.

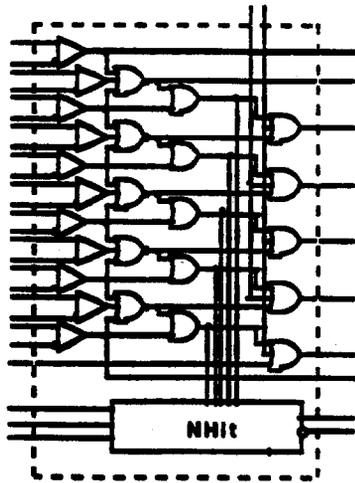


Figure 5: ASIC 04

The NHit circuitry provides a current output dependent on the number of channels hit. The output is approximately 100 μ A per strip hit. In the situation described above where individual signals are below threshold but the sum of the two is above, only 100 μ A is provided thereby treating it as a single hit.

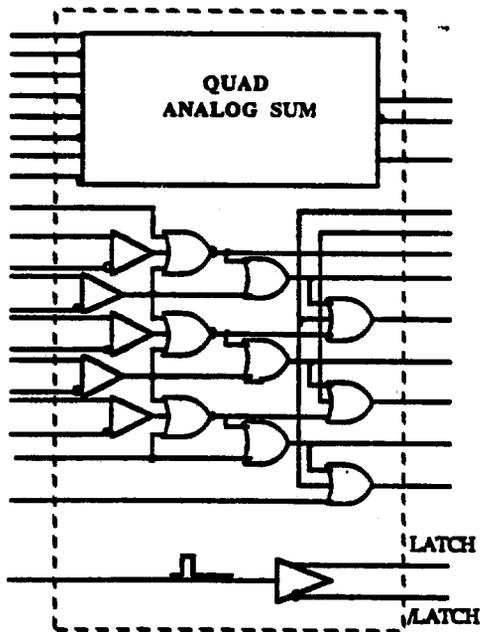


Figure 6: ASIC 02

ASIC 02: Quad Analog Sum and Latch Driver

The Quad Analog Sum circuit on ASIC 02 gets its inputs from analog sum outputs on ASIC 01 (two input sum circuits), thus producing an analog sum of eight adjacent channels.

The Latch Driver takes an ECL 2.5 ns pulse, converts it to a differential pulse which will then be used to drive the latch inputs of the four corresponding ASIC 01's.

ASIC 03: Digital to Analog Threshold Set and Readback

The chip shown in Figure 7 is a CMOS implementation of 4 D/A output channels and a single A/D readback channel. Writing and reading of this chip is accomplished through the FASTBUS system. To set a threshold for each channel and adjacent channel sum discriminator, 256 D/A outputs are required per 128 channel P/C module. 64 D/A chips are mounted on the P/C module in this case. It is optionally possible to feed more than a single channel discriminator with the same threshold level. Implementing this option minimally requires a single D/A chip with each output feeding 64 discriminators.

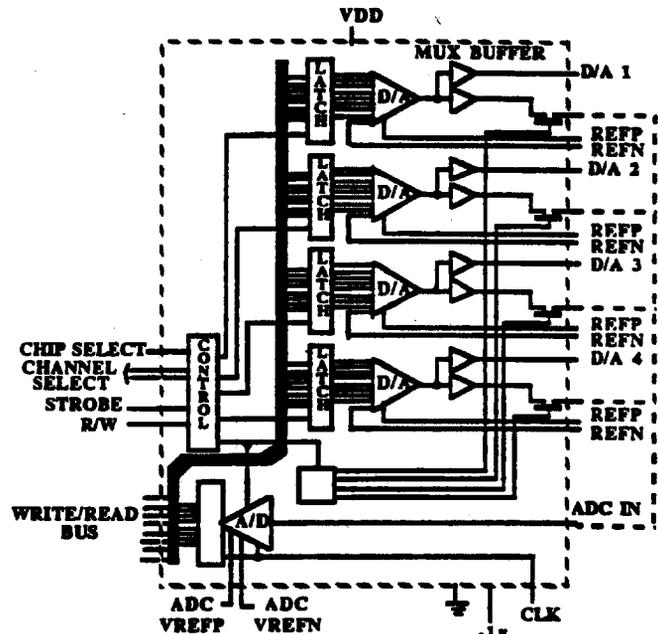


Figure 7: ASIC 03

Delay/Encoder (D/E)

The D/E module (Figure 8) accepts 128 channels of parallel data from the P/C every 18.9 ns and stores the individual channel data for up to 4.8 μ sec, while a level 1 trigger decision is made. The delay is implemented using high-speed ECL memory (10422-5). The 18.9 ns time between events is split into a write cycle and read cycle.

During each 18.9 ns RF cycle, a write address counter is incremented and data is written into the delay memories. During any cycle, stored data may be read from any memory location. No detector deadtime is generated by this readout.

When a level 1 trigger occurs, the MTC generates an address that corresponds to the location in the D/E memories holding data for the RF bucket in which the triggering event took place. This address is fanned out through the SEQ modules to all of the D/E's in the readout system. Data from the RF bucket containing the triggering event and data from the previous RF bucket in time are input to a pipelined priority encoder. It takes seven clock cycles to load the encoder pipeline. After this delay, the D/E outputs an ordered list of hit strips. The address of each hit strip is encoded in a seven bit number. An additional bit is used to flag strips which were hit in the RF bucket previous in time to the

triggering bucket. This bit identifies hits that are likely to have been caused by an event other than the triggering event.

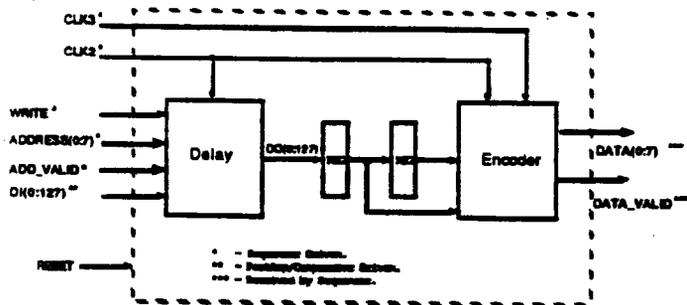


Figure 8: Delay/Encoder

Encoded data is transferred synchronously to the SEQ module over point-to-point connections on the FASTBUS auxiliary backplane. This transfer is data driven and occurs in parallel for all D/E's.

Sequencer (SEQ)

A block diagram of the SEQ is shown in Figure 9.

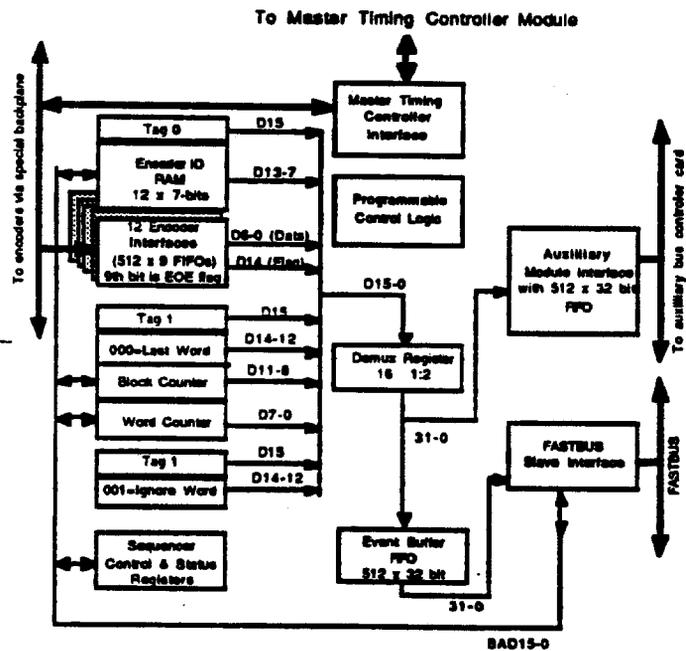


Figure 9: Sequencer Module

The SEQ module fans out triggers received from the MTC to the D/E's in the form of a hit address in the delay memories. It also accepts the conditioned 53 MHz clock from the MTC, delays it by a programmable amount, and fans out two versions of the 53 MHz clock and a 26.5 MHz clock derived from it, onto the FASTBUS auxiliary backplane. These clocks are used by the P/C to latch data, by the D/E to clock the high speed memory and the encoder pipeline, and to synchronize the data transfer from the D/E modules to the SEQ. The SEQ accepts data from the 12 D/E's in parallel and places it in 12 FIFO's. When a trigger is received, the SEQ

deasserts an "Encoder Ready" signal which is input to the MTC. As soon as all D/E data has been transferred to Sequencer input FIFO's, the "Encoder Ready" is asserted again and the readout system is ready to process another trigger.

The Sequencer reads data out of its input FIFO's in a fixed order. The 8 bits of data from each D/E are combined with 7 bits of D/E address and stored in a FASTBUS accessible memory. A high order zero is added to distinguish data from control information. The end of event is marked by control word containing a count of the number of data words and a 7 bit "event number" that may be used to insure synchronization across the entire readout system. The sequenced data is moved two 16 bit words every 73.4 ns into a "Event Buffer FIFO" that can be accessed from FASTBUS. The data is simultaneously output through the auxiliary connector to an optional high-speed fiberoptic link. When the fiberoptic port is used, the data may still be readout of the "Event Buffer FIFO" over FASTBUS and used to compile high statistics histograms in the FSCC without reducing the readout bandwidth.

FASTBUS Smart Crate Controller (FSCC)

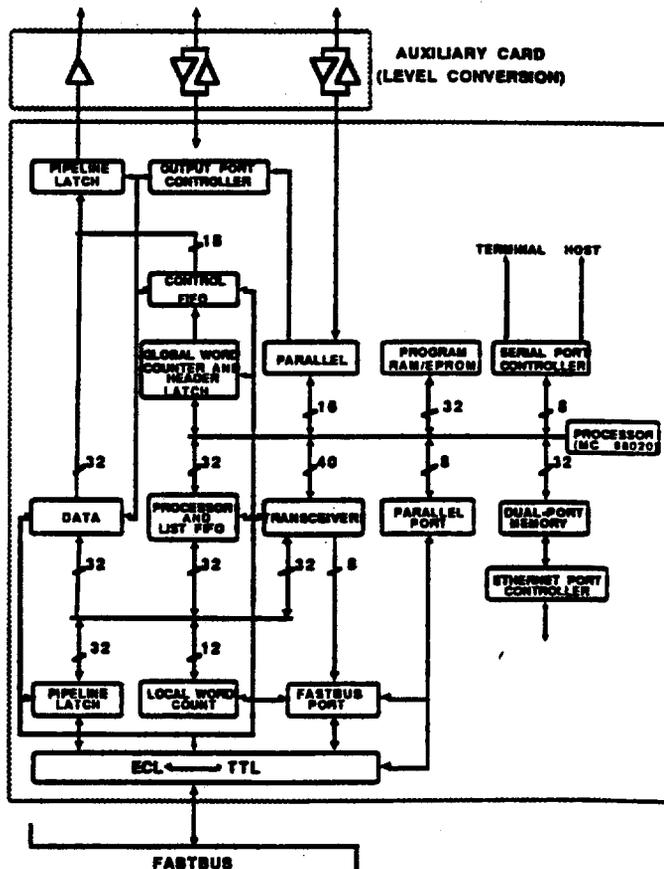


Figure 10: FSCC

The FSCC, shown in block form in Figure 10, is designed as a limited general-purpose readout device for low-occupancy front-end systems. It can execute most FASTBUS master operations directly from higher level software at normal 68020 processor speeds, typically a few hundred nsec p.

instruction, and also supports faster operation through microcoded list operations. The FSCC is dual-ported from FASTBUS to the auxiliary connector to allow 100 nsec block transfers on both ports through an intermediate FIFO buffer. This buffer is designed to store the data from a single crate of front-end modules and insert a leading word count or header. The output port connects to several standard formats using an auxiliary card level adaptor. In addition to the data ports, two RS 232 lines, an Ethernet interface and trigger I/O ports are provided. The FSCC runs the PSOS real-time OS kernel and is programmable in any combination of C, assembler or microcode depending on performance requirements.

Master Timing Controller (MTC)

The Master Timing Controller generates the system clock, controls system synchronization, and generates delay memory addresses upon the receipt of Level 1 triggers from the experiments Trigger system. A block diagram of the MTC is shown in Figure 11. The MTC receives the 53 MHz Tevatron

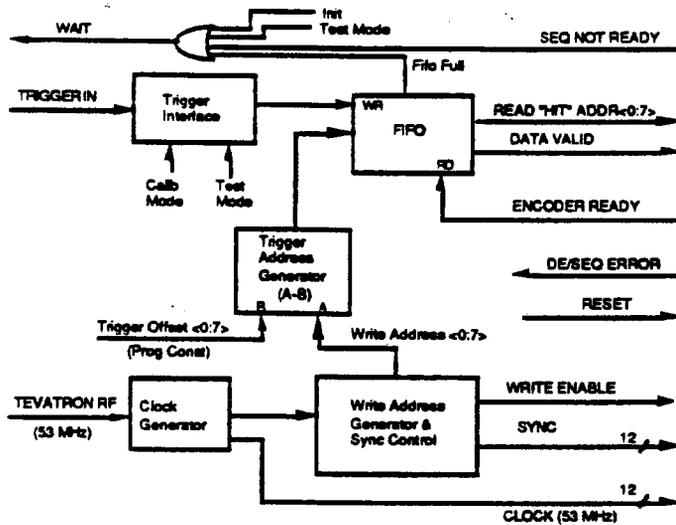


Figure 11: MTC

RF clock and establishes a 50% duty cycle clock whose phase is adjustable relative to the incoming RF. This CLOCK along with a SYNC pulse are distributed to each SEQ and eventually to all D/E's. D/E's use this clock and sync to determine write addresses for incoming data. Being synchronized, the MTC knows the current D/E write address and generates a read or "hit" address when a trigger is received. The hit address generated is offset from the write address based upon a calibration of the Trigger decision time. Hit addresses are placed into a high speed FIFO queuing up to eight trigger requests and can be accepted on successive RF buckets. The read or "hit" address output from the FIFO is broadcast to all D/E modules at a rate determined by the ENCODER READY signal summed from all D/E modules. The ability to pipeline triggers makes the system truly deadtimeless at trigger rates up to the readout bandwidth. With knowledge of the read address and the D/E's current write address, the MTC detects fatal DE memory overwrite errors. However, to prevent such a condition, the system is throttled by sending a WAIT signal to the Trigger system under appropriate conditions.

Project Status

All system module logical design is complete. The FSCC is in the second prototype stage. The P/C module board layout is nearing completion. The D/E and the MTC module prototype boards are due in February 1990. The SEQ module board design has started and will be completed in February. Prototype printed circuit boards of each of the system modules are expected to be available in early March for initial integrated testing.

Acknowledgements

The authors would like to thank Garry Moore, Betty Conrin, Rick Kwarciany, John Chramowicz, Rick Van Conant, Scott Holm, Bruce Merkel, and our tireless cooperative education student, Mike Kodner for the effort they expended on this project. Ruth Pordes and Mark Bennett of the Computing Division were instrumental in developing the software needed to make the FSCC a usable product.

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- [2] Tom Zimmerman, A High-Speed, Low Noise ASIC Preamplifier for Silicon Strip Detectors, 1989 Nuclear Science Symposium Proceedings
- [3] J.A. Crittenden et al., A Data Acquisition System for Elementary Particle Physics, IEEE Transactions on Nuclear Science, Vol. NS-31, No. 5, October 1984
- [4] W. Sippach, G. Benenson, B. Knapp, Real Time Processing of Detector Data, IEEE Transactions on Nuclear Science, Vol. NS-27, No.1, February 1980

A High Speed, High Gain Preamplifier System for Silicon Strip Detectors

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Abstract

A high speed, high gain amplifier system has been designed for silicon strip detectors. The amplifier has been designed using a semicustom bipolar linear array. This paper focuses on a practical integration of this amplifier into a working system. To maximize board density and reduce cost a new, relatively inexpensive custom chip carrier was designed. The design approach could be useful for other custom or semicustom chip designs. Insight into the design of a 128 channel preamplifier circuit board for low noise and low crosstalk using the new carrier is presented.

High channel density presents challenges in cabling. A relatively new high density cable with mass termination capability was used for transmitting signals from the preamp to the discriminator boards. As a part of the overall design, the approach taken for shielding of the detector, preamplifier cards, and output cables is discussed.

Introduction

The amplifier described in this paper is part of a high speed silicon strip detector readout system being developed at Fermilab [1]. This system will be used by two experiments, E-771 and E-789, in the 1990 fixed target run. Both of these experiments will operate at very high interaction rates with the goal of accumulating for study large samples of B particles. Each of these experiments will contain more than 10000 channels of silicon strip electronics. Although this paper is generally applicable to both experiments, the requirements for E-771 will be used as a specific example.

Front End System

The silicon strip detector for E-771 is comprised of 24 planes of silicon, each with 688 strips. Plane to plane spacing averages 0.5 inches. Signals from a silicon plane are fanned out over fine pitch circuitry on flexible Kapton to six high density connectors for preamplifier cards. Each preamplifier card has provision for 128 channels and has differential outputs for each of the channels. Thus there are 256 output signals per card. Outputs from a preamp card are transmitted over four fine pitch ribbon cables which are about 20 feet long to discriminator circuits housed in FASTBUS crates.

*Operated by the Universities Research Association under a contract from the U. S. Department of Energy.

The preamplifier packaging design was driven by a need to minimize the Kapton length and reduce the associated capacitance in order to improve the signal to noise performance of the system. Since the silicon planes are physically close together, a circuit board which could be mounted on nearly the same pitch as the silicon planes was designed. The size of the circuit board, the pitch of the pins on the preamplifier chips, the choice of input and output connectors, and choice of output cable were all driven by the desire to place the preamplifiers close to the silicon planes.

Another design criterion was that preamplifier cards be easily replaceable and repairable. These factors influence the type of input and output connectors used and the construction of the preamplifier board.

To achieve the desired goals, an integrated design of the front end electronics was implemented. The integrated design in this context means considering the chip design, chip packaging design, board design, heat dissipation, and shielding design all at the same time.

Preamplifier

The preamplifier response for a charge impulse is required to be 20 to 40 ns baseline to baseline and have an equivalent input noise of less than 1800 electrons RMS. To achieve the design in a physically small package with reasonably fast construction time, a semicustom, bipolar chip was designed using the Tektronix Quickchip 2S linear array. Four channels of the preamplifier are designed on a single die. The design and performance of this preamplifier chip is covered in another paper presented at the 1989 Nuclear Science Symposium [2].

The preamplifier chip was designed to maximize the isolation between input and output pads by locating the pads far apart and to make power supply busing across many chips easy. Figure 1 is a bonding pad diagram which shows that the inputs and outputs are on opposite ends of the chip to reduce feedback. Power supply connections are made on the sides of the chip to permit power busing under the chip. Identical power connections are made on each side of the die to facilitate the mounting of the chips in the chip carrier package which was chosen.

Chip Packaging

Each circuit board is to have 128 channels and thus 32 four channel dies mounted on it. To fit the chips onto the preamplifier board, the chips had to be mounted relatively

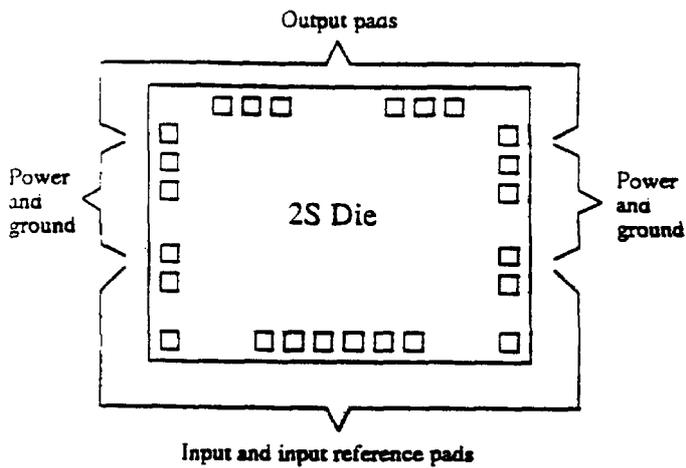


Figure 1 - Preamplifier Die Bonding Pads

close to each other. Chip on board (COB) mounting of the bare dies was considered to be impractical because of the large number of dies to be mounted. Secondly, COB does not readily permit replacement of a bad die after assembly. Thus a chip carrier was desired which would facilitate replacement of bad chips. To fit the required number of channels onto a board, a leadless surface mount chip carrier with a pitch of 25 mils was necessary. Standard packages which would meet the space requirements were not available. Therefore a custom package was designed.

The type of package designed is manufactured by Tectonic, Ltd in England and sold under the trade name of EPIC [3] by S A Communications of San Diego, CA. Advantages of the package in addition to full choice of package dimensions include ease of design, fast delivery, and relatively low cost. The primary disadvantages are that the package is not well sealed and replacement of a faulty device requires special care.

The EPIC chip carrier is made of B-T (bismaleimide-triazine) which is similar to the FR-4 material that is commonly used to make printed circuit boards. Thus, there is no temperature coefficient mismatch between the package and the printed circuit board to cause solder joint

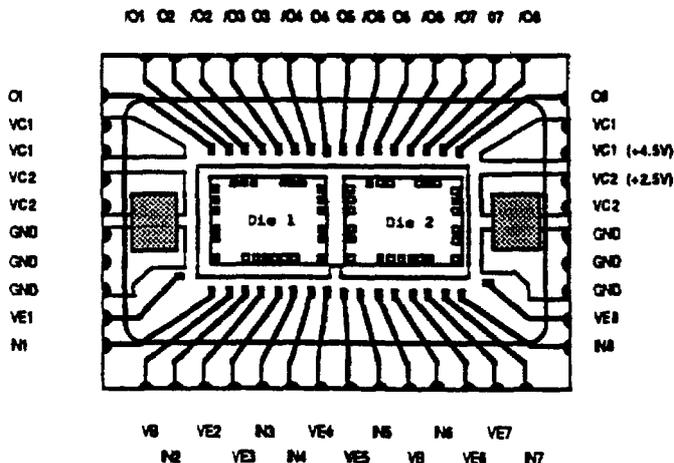


Figure 2 - Custom EPIC Chip Carrier Layout

failure problems. The glass transition temperature for B-T, however, is about 210°C, which makes it more suitable for gold ball bonding and surface mount reflow soldering.

To make most effective use of the space on the circuit board and reduce the packaging cost, the package was designed to have space for two dies (eight channels of preamplifier). The package was ordered by sending the layout shown in Figure 2 to the manufacturer's representative in the USA. Chip carriers were normally returned in about 4 weeks. As can be seen, provision was made inside the chip carrier for 2 internal bypass capacitors for critical power supply voltages. This feature was very helpful in preventing the output drivers on the chip from oscillating. Effectively, the assembled chip carrier becomes a mini hybrid with surface mount provisions. Figure 3 shows an assembled chip carrier with the lid removed.

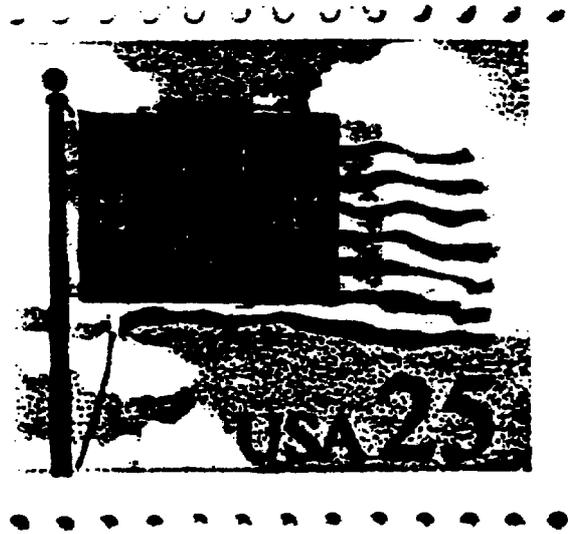


Figure 3 - Assembled EPIC Chip Carrier with Lid Removed to show 8 Preamplifier Channels.

The EPIC type of package has received only limited attention in the USA. However, the package has been extensively tested and used by British Telecom in the United Kingdom. Accelerated life tests performed by the manufacturer show the package to be highly reliable.

A preliminary measurement of the thermal impedance of the EPIC package to the circuit board described in the next section is about 80°C/watt. The preamplifiers dissipate about 350 mw per EPIC package.

Due to the inherent construction of the EPIC packages, they are not well sealed against moisture. To provide adequate protection, the chip surfaces must be coated or sealed to prevent contamination of the bonding pads. Two different materials have been tested on the preamplifiers. One is a polyimide surface coating (Rely-imide #210D) made by M & T Chemicals and the other is a glob top encapsulant (FP4323) made by Hysol for COB applications. Packages with both types of coating were thermally cycled. Packages with the coats of the polyimide material that covered the bonding wires (not recommended by the manufacturer) showed damage to the bonding wires after several days of thermal cycling. Similar

tests performed with thin coatings, 1-2 mils, and no coating of the bond wires showed no damage. The encapsulant material has shown no problems. Both materials when properly applied appear to be acceptable solutions to the moisture problem.

Initially, poor wire bonds to the package were encountered when using a gold wire bonder. This was apparently due to thin gold plating (8 to 15 microinches) inside the carriers. After ordering packages with a minimum of 32 microinches of gold, the problem disappeared.

Solder mounting and replacement of the EPIC packages requires special attention. Production assembly was accomplished with IR solder reflow techniques. Because of the fine pitch components, stencils rather than screens were used to deposit the solder paste. Special fine mesh solderpaste with low slump characteristics was necessary. Replacement of a single EPIC package by an experienced person requires about 10 minutes.

The EPIC package is relatively inexpensive for a custom package. Nonrecurring engineering charges are about \$1500 and the cost per package is \$1.06 for a few thousand pieces.

Board Layout

As has been mentioned, the printed circuit board and the chip carrier are an integrated design. Each printed circuit board which is 3.5 inches by 4.5 inches has 128 channels of preamplifiers. Seventy percent of the board space is devoted to input and output connectors. Eight chip carriers are mounted in a row on each side of the board. Power is brought into the center of the board with a cable and then distributed under the chips on each side of the board to minimize voltage drop. Power supply bypassing is done as close to the chip carriers as possible.

The circuit board has four layers. The center two layers are primarily ground plane, and act as a low impedance amplifier reference. They also provide impedance control for the output traces. Each channel of amplifier has a dedicated reference, or Vee, connection. Each four channel chip has a common ground connection for the output driver pulldown resistors on the chip. It is important that these all connect directly to the same low impedance reference, or ground plane, to reduce crosstalk. In fact, the common pulldown resistor ground connection is made through three parallel package pins to insure a low inductance connection to the board. Multiple vias are used to connect the chip ground pins to the ground planes in the center of the board. All bypassing is as tight as possible to the ground plane.

The ground plane layers also distribute the heat from the chips to the entire board. The board thus tends to act as a cooling fin. There are 144 circuit boards distributed over four sides of the detector. Forced air is used to cool the circuit boards.

Figure 4 shows an assembled card. Input signals are brought onto the card from the detector via an inexpensive, 132 pin 50 mil pitch card edge connector. This connector permits easy insertion and extraction of 128 channels of

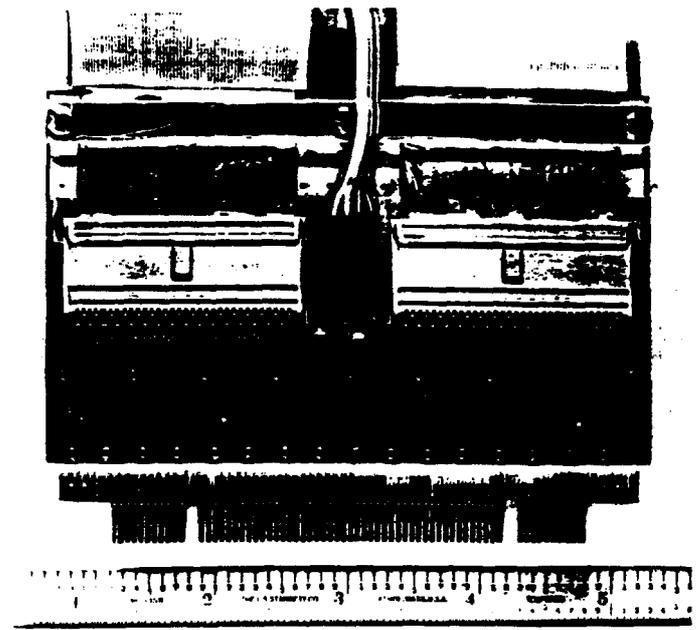


Figure 4 - 128 Channel Preamplifier Card With Connectors.

electronics with less than 10 pounds of force. Two 64 pin, high density connectors on each side of the card are used to send signals to the discriminator boards.

Shielding Design

A double RF shield is employed around the detector as shown in Figure 5. The inner shield encloses all of the silicon strip detector planes. Penetrations are made through the shield for the preamplifier cards to pass through and plug into connectors mounted on the detectors inside. Small beryllium copper RF gasketing strips are used to make contact from the shield to the exposed ground plane on the two sides of the preamplifier card near the card edge connector. See Figure 4. The RF shield is carried through the circuit card by means of a series of via holes located where the gasketing contacts the board. This arrangement maintains RF shield integrity which would have been reduced by the card slots. Also, this allows a very low impedance connection between the RF shield and the amplifier grounds. This was found to be absolutely essential in eliminating coupling between the preamplifier input leads coming from the detector and the higher signal level preamplifier outputs.

A second RF shield is placed around all of the preamplifier cards and the inner RF shield. Power supply leads for the preamplifiers are brought through the outer shield in four locations and then distributed. The outer shield eliminates pick up on the power distribution cables.

Preamplifier output cable bundles passing through the outer RF shield are shielded to reduce pick up on the cables. The bundle shields are terminated to the outer RF shield at the detector to effectively extend the outer shield to include the cables. The bundle shields are also connected at the receiving end to the FASTBUS crate racks.

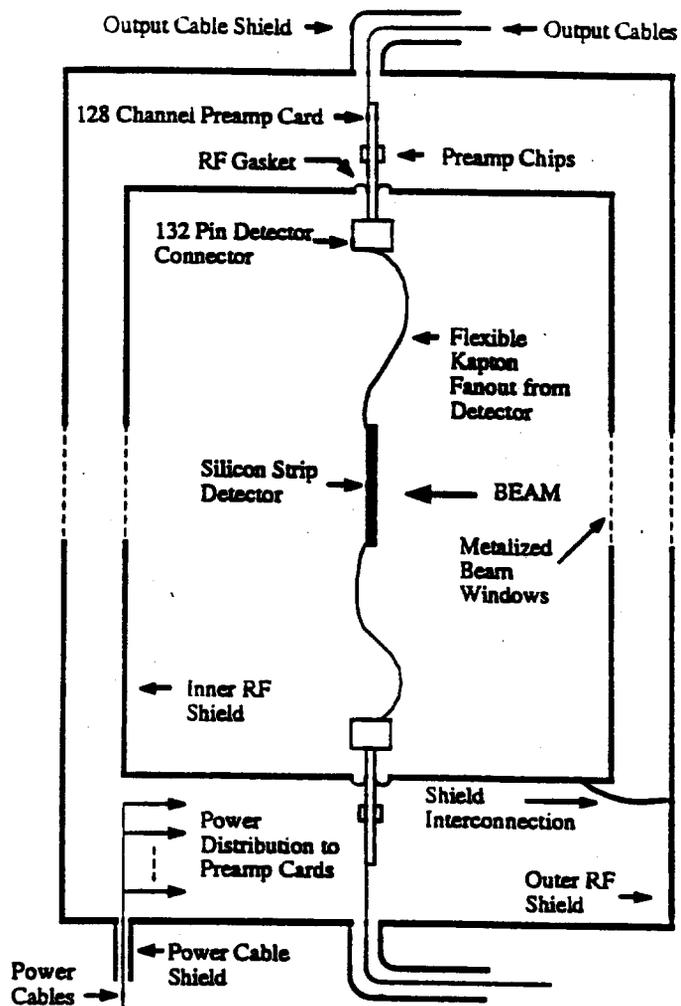


Figure 5 - Silicon Strip Detector and Pre-amplifier Card Shielding
Output Cables

A mass terminable, flexible, 64 conductor, 25 mil pitch ribbon cable was chosen to transmit the large number of signals at the output of each preamplifier card to the discriminator cards. The cable which is made by Spectra-Strip (#133-3013-064) has an embedded ground plane for impedance control and cross talk reduction. All wires in the cable are used as signal conductors.

Four of the cables are connected to each preamplifier card, for a total of 576 cables in the system. Each cable is relatively light weight, flexible, and stacks well into bundles for shielding.

For this application, pairs of conductors are driven differentially. The differential impedance of the cable is 100 ohms. Although the output signals are differential, the ground plane of the cable is connected to the preamplifier ground plane to provide a return path for imbalanced signals. Also, fixing each cable ground plane to the same reference reduces coupling which can cause oscillations. To make the connection to the preamp ground plane, the ground plane on the cable is folded back and wrapped with conductive adhesive copper tape and then clamped to the preamplifier ground plane as shown in Figure 4. In addition to making the ground connection to the

circuit board, the clamp also doubles as a cable strain relief.

At the receiving end, each signal conductor is AC coupled and terminated with 50 ohms to a common point which is connected to ground. Forward cross talk between adjacent conductor pairs in the cable is about 0.5% for a ten foot cable with 5 ns rise time pulse. This is quite acceptable for the silicon strip application.

Pre-amplifier Power

A "quiet power" source is provided for the preamplifier cards to eliminate noise injection from the power source. A separate double shielded transformer is used to provide AC power to the preamp power supplies. Only linear power supplies are used for the preamps. Power cables from the power supplies to the detector are shielded outside the RF shield and bypassed just inside the outer RF shield to stop any noise transmitted down the cables from entering the RF enclosure.

Once the Power supply voltages are brought inside the outer shield, they are distributed to the individual preamplifier cards by means of short ribbon cables. Each of the two power supply voltages on the ribbon cable to each card is fused. The fuses are located inside the outer RF shield. Easy access doors to the fuses are provided for maintenance purposes.

Summary

The front end electronics for the silicon strip detector is a packaging problem as well as an electrical design problem. Both factors needed to be considered in the early design stages of the project to build a system which not only meets the electrical design criteria, but is manufactureable and readily repairable. In completing the design, packaging ideas which should be applicable to other systems were developed.

Acknowledgments

The authors are particularly grateful for the help which Dan Graupman of the Research Facilities Group at Fermilab provided in laying out the preamplifier and various test boards. We would also like to thank Ted Bohn for his valuable assistance in assembling and testing various parts of the system.

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A High Speed, Low Noise ASIC Preamplifier for Silicon Strip Detectors

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Abstract

A first version Tektronix Quickchip semicustom ASIC preamplifier for silicon strip detectors was reported in Oct., 1988[1]. An improved version, QPA02, has been designed which incorporates laser trimming of nichrome resistors as a means of compensating for chip resistance process variations, which affected the response of the first version. This allows chips with randomly varying resistance values to be trimmed to have a standard output pulse shape. The QPA02 also has improved performance specifications. This paper describes the design philosophy and specifications of the QPA02, and the test results.

Introduction

The QPA02 is a high speed bipolar transimpedance amplifier built using a Tektronix "Quickchip 2S" semicustom linear array. It converts an impulse of charge to a fast voltage pulse. It was designed for use as a silicon strip amplifier for Fermilab E-771[2], but will be used in E-789 and may have other applications as well. E-771 requires an amplifier with a fast response to a charge impulse input, since the time between beam buckets is about 19 ns. The QPA02 has an impulse response that returns to baseline in less than 38 ns, or two beam buckets, for a detector capacitance of 20 pf. A high gain amplifier was designed (of order 15 mv/fc) so that output signals traveling over long cables could directly drive discriminators. This also reduces sensitivity to external noise pickup. A buffered differential output was necessary to drive flat cable with maximum noise immunity. E-771 space constraints forced a high channel density, which motivated an integrated circuit design.

The Tektronix Quickchip linear array was chosen for this design over other available high performance bipolar linear arrays because Tektronix markets its own design tools which facilitate accurate simulation and layout, and because custom laser trimmable nichrome resistors are available on Quickchip. A first prototype amplifier, QPA01, was designed, produced, and tested[1]. The response of the amplifier differed somewhat from the nominal simulations due to process variations in on-chip resistor values. This emphasizes one of the major challenges in analog integrated circuit design. Chip resistor values can vary widely from run to run and are unpredictable.

However, the designer can make use of the fact that on any given chip the resistors are matched to within 1%. The second version amplifier, QPA02, is designed to use a nichrome resistor laser trimming scheme to partially compensate for these resistance variations, resulting in a more standardized output pulse response.

The Quickchip Design Process

Designing with Quickchips is a well defined process. Normally a design is simulated and its performance understood by using TSPICE (a Tektronix proprietary enhanced version of SPICE 2G) before commencing layout. This is done using Tektronix supplied component libraries. Then a die selection is made from several available types. This is usually based on the number of components and I/O pads needed per chip. Layout is then performed using the QUICKIC (Tektronix version of KIC) layout editor. Two levels of metal are available to interconnect components. Sometimes layout constraints force component changes. This necessitates a return to TSPICE to verify any design changes. A design review at Tektronix checks the integrity of the design. Normally a prototype run of chips is made and performance checked before ordering production quantities.

Amplifier Design

The QPA02 is a two stage amplifier. A schematic is shown in Fig. 1. The first stage, or preamp, is a transimpedance feedback amplifier in the common emitter configuration to convert a charge input to a voltage output. The second stage is a differential voltage amplifier. Its function is to boost the gain, shape the preamp output, and provide differential outputs to drive a transmission line. A "reference" preamp stage, similar to the input stage, is used to provide DC tracking to the second stage. This is necessary since DC bias levels are somewhat uncertain due to process variations and temperature effects. This reference stage has no input capacitance and is bandwidth limited with a relatively large on-chip capacitor. Therefore it does not contribute significantly to the output noise.

Preamp

The preamp input transistor Q1 is a large area transistor to minimize noise due to base resistance. A cascode transistor, Q2, limits Miller capacitance at the input. The cascode base

*Operated by the Universities Research Association under a contract from the U. S. Department of Energy.

bias voltage is supplied by a simple diode string. An emitter follower, Q3, buffers the cascode collector to the second stage. A feedback resistor is connected from a variable attenuator (driven by the follower) back to the input.

This stage has two important open loop poles, one significantly higher than the other. The feedback resistor value is selected to give a slight overshoot in the impulse response. (This overshoot is smoothed out by the second stage shaper and causes the output to have a quicker return to baseline). The dominant open loop pole is formed by the capacitance at the input node (dominated by the detector capacitance C_d) and the input resistance R_{π} . This can be written as

$$f_1 = 1/2\pi R_{\pi} C_d = g_m/2\pi B C_d.$$

Since g_m is inversely proportional to I_c , and I_c is nearly proportional to the collector resistance R_c , f_1 is then proportional to $1/R_c C_d$, and is nominally around 2.5 MHz. The second pole is formed by the cascode collector node capacitance, C_c , and the collector resistor, and can be written as $f_2 = 1/2\pi R_c C_c$. Its nominal value is 65 MHz. The DC open loop transresistance is approximately βR_c . Without the cascode transistor, the amplifier would have only one important pole, formed by C_d added to the Miller capacitance of Q1. Such a configuration would be more sensitive to process variations in input transistor parasitic capacitance, and would have a longer impulse response fall time. By using the cascode, however, the response becomes more sensitive to

variations in input capacitance. Since detector capacitances should be relatively uniform channel to channel compromise is acceptable. The nominal design assumes 100 pf input capacitance, but other capacitances can be used. Supply voltage can then be used to adjust the impulse response if desired.

Since the two poles are widely separated, and the feedback is set such that the loop gain falls to one at about 25 MHz, the preamp closed loop bandwidth and phase margin are determined mainly by f_2 and R_{fb} . Thus process variations in resistance will affect the amplifier's response. Assuming fixed C_d , the value of R_c has little effect on the open loop gain at f_2 , since a change in R_c moves f_1 and the DC open loop gain in opposite directions, preserving gain bandwidth. In order to stabilize the response in the presence of process variations, the second pole frequency and the amount of feedback must be held constant. A scheme in which R_c and R_{fb} were formed from nichrome and then laser trimmed was considered. However, the values required were too large to be practically designed as nichrome trims. Also, there is no easy way of monitoring the resistance values while trimming to know when the correct value has been reached. Therefore, a method was developed which uses small value nichrome resistors as "fuses" which can be left in or cut out by laser. There are five different discrete configurations to which the amplifier can be "trimmed" by cutting different combinations of fuses. These configurations are assigned to evenly spaced portions range of possible chip resistance variation. A test resistor

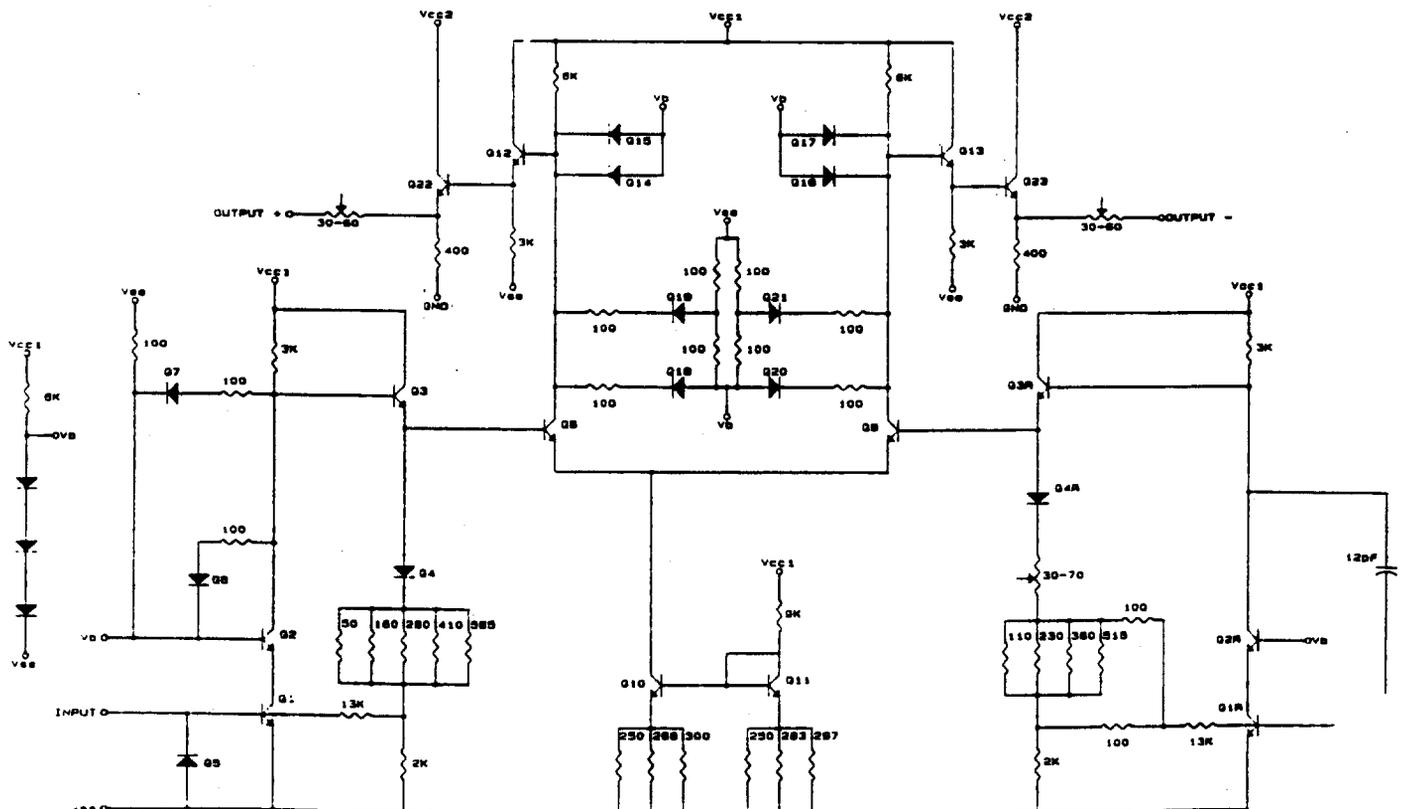


Fig. 1 - QPA02 Schematic

measurement determines which configuration is appropriate for any given chip. Nichrome laser cuts can then be made before the chip is powered up.

The frequency of the second pole is held at 65 MHz by changing the capacitance on the cascode collector node, based on the test resistor measurement. Two small capacitors in the form of back biased junctions are connected to this node through nichrome fuses. The value of one of these junction capacitors can be set to one of two levels by changing the value of back bias voltage via nichrome fuses. Thus a total of five different values of capacitance are available at this node. The amount of feedback is held at a constant value by trimming an attenuator which drives the feedback resistor (again, in discrete steps). This is done by cutting out four of five parallel nichrome resistors, based on the test resistor measurement. The response and phase margin of the preamp have been stabilized against chip resistance variation by using this technique.

The reference stage used for DC balance contains similar feedback attenuator trims, but the other trims are not necessary. A continuously trimmable nichrome resistor is added in order to remove any remaining DC imbalance due to transistor V_{be} or Beta mismatch. This is an active trim done by monitoring the DC output voltage while the device is powered.

Amplifier/Shaper

The second stage is a differential pair, Q8 and Q9, which is biased by a degenerated current mirror, Q10 and Q11. This stage provides an amplified differential signal at the collectors of the differential pair. Each collector is buffered in order to drive a transmission line. The output is bandwidth limited by adding capacitance to the collector nodes in the form of back biased junctions. This shapes the signal and limits the noise. The nominal shaped signal peaks at about 10 ns and is less

than 35 ns base to base. The first stage overshoot helps speed up the fall time at the output. Since the shaping depends on the RC time constant at the collector, the chip resistance value affects this. Therefore, a nichrome trim scheme similar to that used in the first stage is implemented here to trim the capacitance to one of five discrete values. Thus the shaping time constant will remain relatively constant.

The preceding scheme allows a standard output pulse shape over a range of chip resistance values. However, amplitude differences exist for the different cases since the resistance affects the gain. Therefore, the current mirror degeneration resistance in the second stage is formed from parallel nichromes of different values that were determined empirically using TSPICE. By cutting out two of the three resistors in each leg, the gain can be set such that the pulse height will be at a fixed value.

The output section of the second stage consists of small area emitter followers, Q12 and Q13, to buffer the collectors and drive larger output transistors, Q22 and Q23. An internal pulldown resistor is used to bias each output transistor at about 4 ma. An external pulldown may be added to increase the dynamic range if desired. A laser trimmable back termination is provided in series with each output.

QPA02 Layout

The Quickchip 2S die, the smallest available, was chosen for the layout since it contained the correct number of pads for four channels, and because the component layout was fortuitous. The pad assignments are shown in Fig. 2. The channels are laid out in columns, with input pads on the bottom and output pads on the top. Power supply pads are on either side. The preamplifier stages are on the bottom half of the chip, and the amplifier/shaper stages are on the top half. This arrangement maximizes isolation between inputs and outputs. Fig. 3 shows two chips bonded into a custom chip

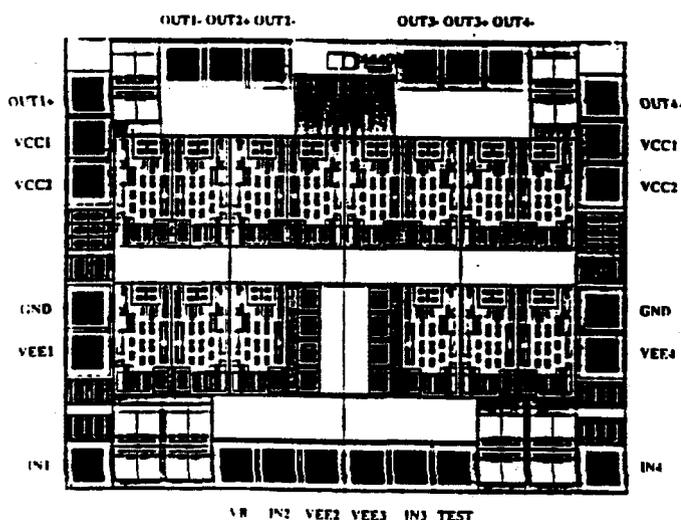


Fig. 2 - Quickchip 2S die with pad assignments

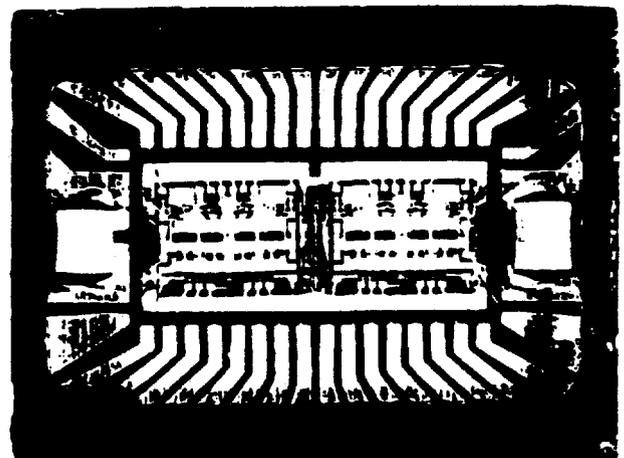


Fig. 3 - Two QPA02's in custom chip carrier

carrier. Small bypass capacitors for the output driver supply are also mounted inside the carrier.

A separate reference (VEE) pad is necessary for each channel to avoid common impedance crosstalk. Output driver pulldown resistors are included on the chip to avoid DC currents in output cables. These are all connected to a common point (GND). When using QPA02, GND and VEE pads should all be referenced to the same low impedance ground plane.

The output driver transistors are connected to a separate power pad, VCC2. This avoids the problem of high output currents coupling to the input circuitry. Also, this allows VCC2 to be independently adjusted. VCC2 should not be more than 2.0 volts lower than VCC1. For ease of use, VCC2 may be run at the same supply voltage as VCC1. However, this will result in increased power dissipation.

The cascode bias, VB, is shared between all channels on a chip. It is connected to a pad so that it can be externally bypassed. This is necessary to reduce crosstalk and to limit random noise components.

Since this amplifier has a large gain-bandwidth, it requires special care in grounding and shielding for practical use. This is the subject of another paper presented at these proceedings[3].

Performance and Test Results

Prototype chips were supplied by Tektronix for evaluation. Fig. 4 is a diagram of the test board used. For all tests, VCC1 was set at 4.5 volts and VCC2 at 2.5 volts. Response and noise measurements were made for a variety of input capacitances and compared to TSPICE predicted values. In all cases, the measured results closely matched the TSPICE values, proving the value of design simulation.

Fig. 5 is the measured impulse response for a charge input of 4 fc, taken at one output. This translates to a differential impulse gain of 17 mv/fc for $C_{in}=20$ pf. Fig. 6 illustrates how VCC1 can be varied to adjust the impulse response. In this case, VCC1 is used to keep the same pulse width for a variety of input capacitances. The QPA02 has a dynamic range of approximately 30 fc at the input before the

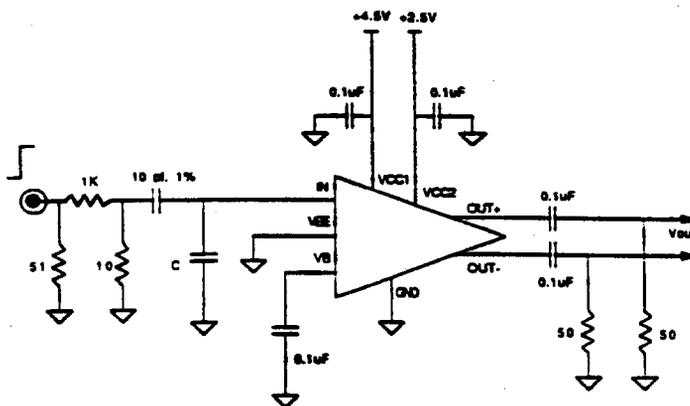


Fig. 4 - QPA02 test circuit diagram

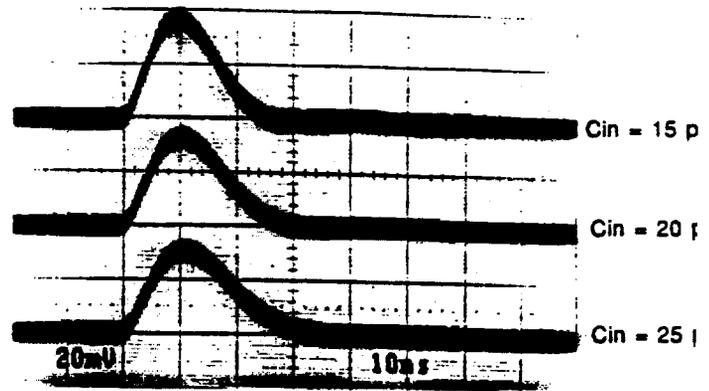


Fig. 5 - Impulse response

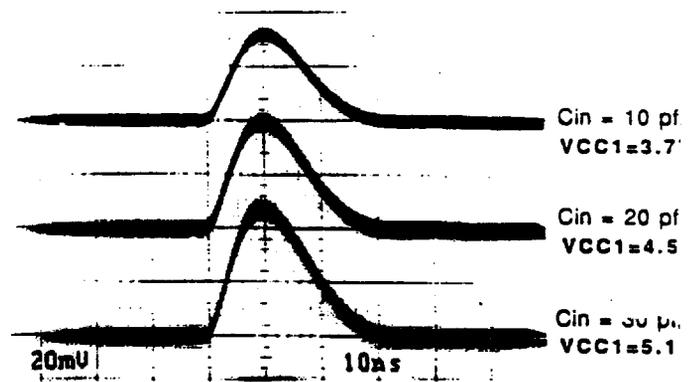


Fig. 6 - Impulse response adjusted with VCC1

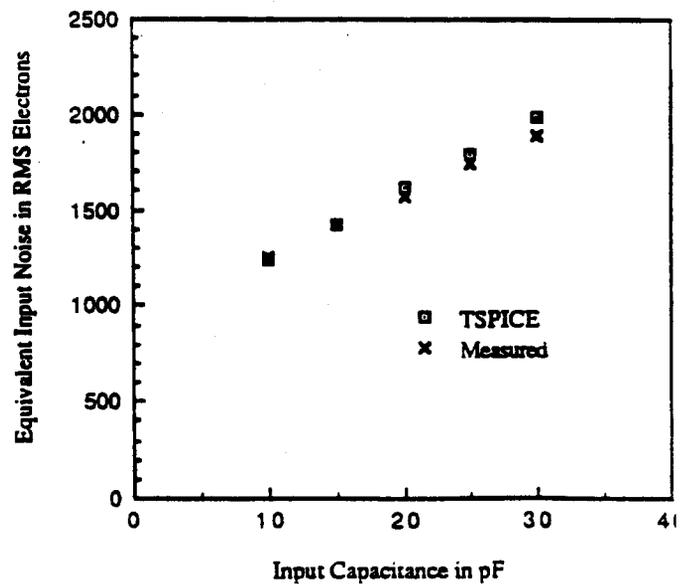


Fig. 7

outputs begin saturating. However, linearity is degraded above 10 fc.

The noise performance was measured using a LeCroy 620AL discriminator[4] and is shown in Fig. 7. The input noise is approximately 1570 electrons for $C_{in}=20$ pf.

The power consumption of the QPA02 is approximately 45 mw per channel. Channel to channel crosstalk is measured at typically 0.5%. The input impedance is approximately 200 ohms.

Conclusions

Semicustom linear arrays can be a fast and reliable way to produce integrated amplifiers for high energy physics. The QPA02 has been tested and demonstrated to be an effective silicon strip amplifier for high rate applications, performing as modeled. Other applications may exist which can use this amplifier or a modified version of this amplifier.

Acknowledgements

The author would like to thank Ray Yarema and Dave Christian for their frequent and sound advice. Mitch Newcomer of the University of Pennsylvania provided the foundation for the initial work. Also, Wink Gross of Tektronix provided helpful suggestions.

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THE DEVELOPMENT OF TWO ASIC'S FOR A FAST SILICON STRIP DETECTOR READOUT SYSTEM

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Introduction

A high speed, low noise readout system for silicon strip detectors is being developed for Fermilab E771, which will begin taking data in 1989. E771 is a fixed target experiment designed to study the production of B hadrons by an 800 GeV/c proton beam. The initial focus will be on events in which a B particle decays into a final state including a J/ψ , which subsequently decays into $\mu^+\mu^-$, and on events containing a single high transverse momentum muon. In order to accumulate the largest possible sample of B particles, the experiment will operate at a rate of up to 2×10^8 beam protons per second and 10^7 interactions per second. The experimental apparatus will consist of an open geometry magnetic spectrometer featuring good muon and electron identification and a 16000 channel silicon microstrip vertex detector. This paper will review the design and prototyping of two application specific integrated circuits (ASIC's), an amplifier and a discriminator, which are being produced for the silicon strip detector readout system.

A high rate system must be able to distinguish information corresponding to a desired event from information coming from other events occurring nearby in time. In order to be efficient, it must also recover from a measurement quickly. Extracted beams at Fermilab retain the 53 MHz RF structure of the Tevatron accelerator. This means that events occur in well defined "buckets" of time which are approximately 1.5 ns long and occur every 18.9 ns. The silicon strip detectors which will be used in E771 are 300 μ thick and will operate with a bias voltage high enough so that most of the signal will be induced in less than 10 ns, and all of the current will be induced in less than 20 ns. In order to preserve this resolution and memory time, an amplifier must be built which not only has high gain and low noise (the induced charge totals only 24000 electrons), but also has high bandwidth.

Technology

Recent developments in the micro-electronics industry have made it reasonable for the designers of large scale detector systems to consider the use of custom integrated circuits. A software base including reliable modeling and layout tools has been developed which eases the process of going from block diagrams and schematics to silicon. Fabrication costs have been reduced to the point that designers of systems with as few as 10000 channels may find the total cost of an ASIC less than that of a comparable discrete design. Meanwhile process technologies have been improved to the point that transistors fabricated on monolithic substrates can perform nearly as well as the best available discrete components. The obvious advantages of integrated circuit designs due to the reduction in interconnect capacitance and higher density packaging

are being exploited in the development of dense signal processing systems that physically could not be realized with discrete component designs.

Process Selection

The first choice a designer must make is what type of process to use. The readily available processes include CMOS, NMOS and silicon bipolar. Hybrid families are becoming available combining CMOS and bipolar but these are expensive and not yet accessible to small volume users. Our choice was based on an evaluation of the inherent noise performance, f_t , and power requirements of each family. A good guideline[1] is that if the desired signal rise time is greater than 50ns, MOS processes will be preferred over bipolar. This is due mostly to the fact that bipolar transistors require a bias current at the base which contributes a random noise proportional to the measurement time. MOS devices lose their advantage at high frequency where they require large terminal capacitance or large quiescent currents to equal the noise performance of their bipolar counterparts. We quickly decided to focus on bipolar processes for use in the E771 silicon system.

Since advanced bipolar processes require as many as 19 masks, full custom designs entail very large "non-recurring engineering" (NRE) costs. However, several companies now market arrays of uncommitted transistors and passive components. Most of the processing steps can be completed on an unlimited number of wafers using the same masks. The user customizes the array by specifying metal interconnect layers. This dramatically reduces the NRE costs and provides the user with a well characterized parts list that may be interconnected at will. The disadvantage is that the committed placement of components results in designs that have slightly higher stray capacitance and are much less efficient at the utilization of silicon area. The companies which market high performance bipolar linear arrays are AT&T, Gennum, Tektronix, and VTC. After consideration of the properties of the various arrays, and of the CAE & CAD tools available for each one, we decided to use the Tektronix Quickchip 2 for our ASIC's. Tektronix is the only vendor of the four listed that markets its own design tools. The Tektronix arrays are also the only ones which provide the option of customizing laser trimmable nichrome thin film resistors.

Amplifier

The configuration chosen for the E771 silicon strip amplifier is a common emitter transimpedance amplifier. The common base configuration was also considered, but was rejected for the following reason. The noise can be made approximately the same for both configurations if the standing current in the input transistor is the same[2]. However, in the common base configuration the standing current must pass through both a collector resistor and an emitter

* Fermilab is operated by Universities Research Association under a contract with the U.S. Department of Energy.

resistor, and both must have a large value to minimize noise. The result is that the common base configuration dissipates more power and uses more large resistors, which are in relatively short supply on the Quickchip arrays.

E771 SILICON STRIP DETECTOR ELECTRONICS
MULTIPLYING BIPOLAR PREAMP'S-APER/LINE DRIVER

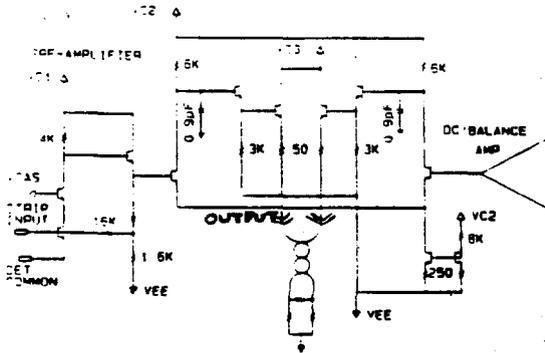


figure 1

A schematic of the E771 amplifier is given in figure 1. The first stage is a common emitter with cascode, buffered by an emitter follower. The open loop voltage gain, $g_m R_c$, is approximately 80. The cascode transistor eliminates Miller capacitance seen at the input, raising the frequency of the open loop dominant pole. This pole position is then determined mainly by the input (detector) capacitance and input impedance. For 20 pf input capacitance, the dominant open loop pole is at about 2 MHz. The cascode transistor introduces a second open loop pole at about 50 MHz. The value of feedback resistance was chosen to give a slight overshoot at the first stage output for an impulse input with an input capacitance of 20 pf. The first stage has a resultant closed loop bandwidth of about 50 MHz, with a 12 db/octave rolloff. The input impedance, given by $R_{in}/g_m R_c$, should be about 200 ohms. Computer simulation of the impedance, shown in figure 2, predicts a well behaved impedance of approximately 200 ohms, which falls off rapidly above the amplifier bandwidth frequency. The first stage is followed by a second gain stage which drives a differential output. The bandwidth of the second stage is limited with an RC pole at about 25 MHz to shape the pulse and reduce the output noise. The first stage overshoot causes the output of the second stage to return to baseline quickly. Since the response of the input stage is directly dependent on the value of the input capacitance, both stages are optimized for the 20 pf expected for the E771 silicon strip detectors plus fanout. The power dissipation of the full amplifier is less than 35 mw per channel.

E771 PREAMPLIFIER INPUT IMPEDANCE 11/08/88 14:37:38

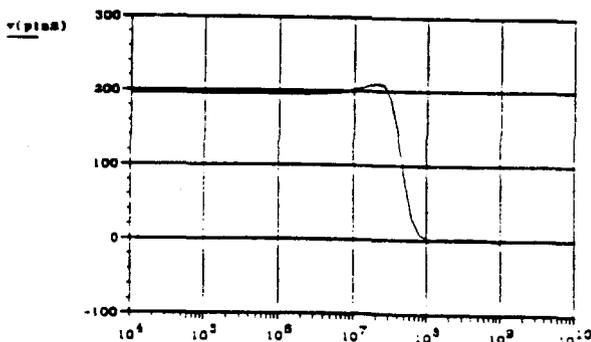


figure 2

In discrete or hybrid designs, key components can be specified with very tight tolerances. However, in integrated circuit design, this is generally not possible. Process variations cause large uncertainties in component values. For example, on a Quickchip 2 the value of active base implant (AB) resistance can vary by plus or minus 25% from nominal. Also, the temperature coefficient is quite high (1400 ppm/degree C). MOS capacitance can vary by 10% and MIM (Metal Insulator Metal) capacitance can vary by 30%. NPN β can vary by 50%. Most of these variations are uncorrelated with one another. However, these values represent maximums to be expected when comparing wafers processed in separate runs. Within a run the variations wafer to wafer are smaller. On a single wafer the variations are even smaller, and on a single chip the maximum variation is of order 1%. A good integrated circuit design must make use of this fact and rely on matching and differential configurations as much as possible. Laser trimmable nichrome resistors provide the option of specifying exact resistance values and are valuable in some circumstances.

Process variations have a fairly large impact on the first stage of the E771 amplifier. The pulse shape of its output depends on the value of the feedback resistor and of the resistor connected to the collector of the cascode transistor. The use of laser trimmable nichrome resistors was considered as a way of insuring a consistent response, but there are several problems with this approach. In general, the Tektronix nichrome resistors are best suited for use as small value (10-1000 ohm) resistors. A large value resistor must be split into a fixed resistance (with a large uncertainty) and a "trim tab." In order to cover the necessarily large trim range, the trim tab must be physically large. Even if there is enough free area on the chip to place the resistor, the large stray capacitance to the substrate associated with the large trim tab can become a problem. For example, a nichrome resistor trimmable to within 1% of 12K ohms requires a trim tab of about 22000 square microns, which has a stray capacitance of about 0.8 pf. The trimmed resistance of the tab may be very different for chips on different wafers. This means that the RC product associated with the fixed portion of the resistor and with the trim tab may also be different chip to chip. In addition, the parasitic capacitance also can vary significantly, and this is not correlated to the degree of trim required.

An acceptable solution for the amplifier first stage was arrived at which makes use of device matching. Active base resistors were used for both the feedback resistor and the collector resistor. If the collector resistor is lower than nominal, the second pole is higher in frequency. But the feedback resistor is also lower, changing the feedback and maintaining an approximately constant phase margin. The amount of first stage overshoot, and thus the output pulse shape, remains similar. The bandwidth of the amplifier does change and this results in a change in the output pulse width base to base. The overall pulse height can be maintained by trimming the gain of the second stage.

After studying the effects of process and temperature variation, it was evident that a differential second stage was required, with a "dummy" input amplifier to balance the DC output variations of the real input first stage. The dummy stage has no input capacitance and it also has a 6 pf feedback capacitor which kills its frequency response. Consequently, it does not contribute to the output noise. An added advantage of a differential second stage is that a

differential output is naturally provided. The configuration is basically a differential pair with resistive collector loads that are buffered by emitter followers to the outside world. A trimmable nichrome back termination resistor is placed in series with each output. A current mirror is used to bias the pair. The voltage gain of this configuration is relatively insensitive to process variations since it is proportional to the ratio of the collector resistance to the current setting resistance, and these are both the same type. A small nichrome degeneration resistor exists in each leg of the current mirror. These can be used to trim the voltage gain if desired. Shaping is performed by adding capacitance to each collector of the differential pair. An MOS capacitor is used, with a maximum process variation of $\pm 10\%$, a relatively small effect. Resistance variations do change the shaping time, and this effect tracks the change in the first stage output rather than cancelling it. For example, narrower pulses due to lower than nominal resistance have a smaller shaping time constant applied to them.

Measurements on the Prototype Amplifier

One of the major questions we had before our first experience with a Quickchip design was how good the computer models were. When prototypes were received, the AB resistance was measured (via an on chip test resistor connected between two power pins) and found to be an average of about 11% below nominal. TSPICE simulations were run at this resistance and the results compared to actual measured results. Figure 3 is the TSPICE predicted amplifier response to a 4fc impulse input for input capacitances of 15 pf, 20 pf, and 25 pf. Figure 4 is the actual measured response of a prototype amplifier with 20 pf. Within measurement accuracy, the simulated and measured responses are identical.

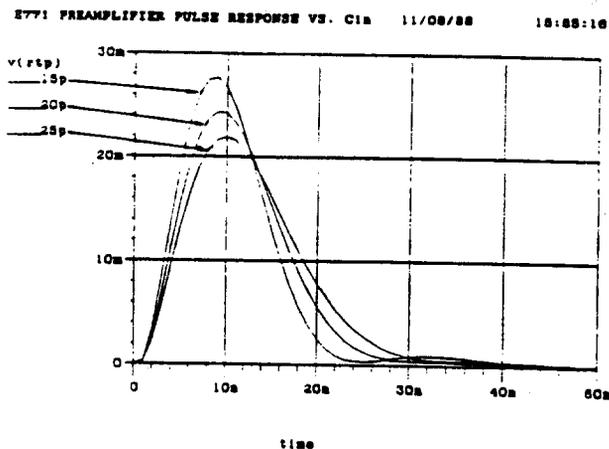


figure 3

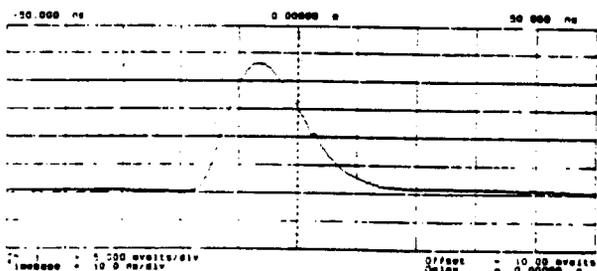


figure 4

* TSPICE is a Tektronix proprietary version of SPICE 2G. We found no significant differences between SPICE and TSPICE results.

The TSPICE predicted noise of the preamp was obtained by integrating the noise density over the full frequency range of the amplifier and then taking the square root. This gives an rms output noise voltage. This can then be referred to the input by dividing by the amplifier gain (mv/fc). The actual noise of the amplifier was measured using the technique shown in figure 5[3], and results are shown in figure 6 along with predicted values. Again, the two cases are almost identical. The noise at 20 pf is .27 fc.

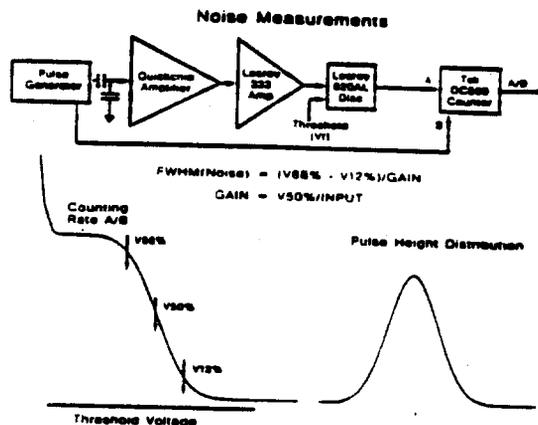


figure 5

Amplifier Noise

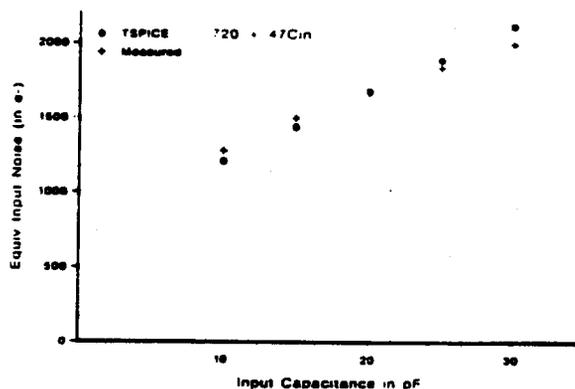


figure 6

Radiation Damage Measurements

Two prototype Quickchip amplifiers were exposed to a Co^{60} source in several steps at a dose rate of about 200 KRad per hour, for a total dose of 5.6 MRad. During irradiation normal bias voltages were applied to the amplifiers. The on chip test resistor (active base type) increased in value at a rate of about 2% per MRad. Nichrome resistors did not change in value. The only observed change in pulse shape was that which would be expected from the increase in the AB resistance. Transistor β decreased about 15%. Base-emitter voltage changes were not observed. Some channels developed a DC offset at the output, but none was large enough to change the pulse response. No significant change in the measured noise was observed.

Discriminator

The shaped preamplifier pulses will be sent over approximately 4 meters of ribbon cable, through a passive termination network, and into a second ASIC. This integrated circuit will provide a latched discriminator output for each strip and also a latched interpolation output derived by feeding the analog sum of two adjacent strips into a separate discriminator with an increased threshold. A fully differential prototype discriminator has been designed and fabricated using a Tektronix Quickchip 2S linear array. The circuit consists of a two stage differential amplifier/comparator with fully balanced hysteresis and voltage programmable threshold. The outputs are CML compatible or suitable for differential logic such as that planned for the latch. The present version requires about 15mw of power per channel (excluding output drivers that were added to the prototype) between supply rails of plus and minus 3 volts.

Circuit Description (see figure 7)

The input stage serves to provide signal gain and positive feedback nodes for threshold and hysteresis. This is accomplished using a cascoded differential input stage consisting of Q1-Q4. The approximate voltage gain of this stage is

$$A = IR_c / 2u_i \quad (u_i = kt/q; I = \text{current in } Q5)$$

The emitters of Q3 and Q4 have low input impedance and provide good feedback summing points without significantly reducing the bandwidth of the first stage. Using the expression for the gain given above, the effective input voltage due to a difference I_d in the currents in the collector resistors of Q3 and Q4 may be written as:

$$V_i = 2I_d u_i / I$$

The operation of both the threshold and the threshold hysteresis can be understood using this relationship. The output of the first stage is buffered with emitter followers and fed into the comparator stage formed by Q6 and Q7. The collector resistors in this stage are split into equal values and buffered with two sets of emitter followers. Q8 and Q9 provide a voltage divided output suitable for CML or differential logic stages. Q10 and Q11 feed a passive voltage translator to provide the hysteresis switch formed by Q12 and Q13 with suitable logic levels.

The function of the hysteresis is to reduce the effective input threshold during the time between when

the input goes over threshold and the time when it falls below the lowered threshold value. This helps to reduce the chance of repetitive triggering due to noise in the signal and has the beneficial effect of providing increased gain near the comparator switching point. Hysteresis has been implemented using a two step approach. A fast message that the output has changed state is sent to the input in the form of a charge. This is accomplished by the capacitor between the emitters of Q4 and Q10 and between Q3 and Q11. Switching logic levels across the capacitance C inserts charge into the summing node. This is almost immediately transferred to the collectors of Q3 and Q4 causing a voltage change proportional to the stray capacitance at that node. The only drawback to this form of feedback is the fact that the MIM capacitors used are subject to +30% process variations. This fast part of the hysteresis feedback is drained away by the resistors in the collectors of Q3 and Q4 in a few nanoseconds. Long term hysteresis is provided by switching a current controlled by Q12 and Q13. Since only 20µa of current in the collectors of Q3 and Q4 is required to shift the apparent input offset by 3mv, an unusually small current source needs to be established.

This has been accomplished using a normal current source transistor with the normal small valued P+ type emitter resistor replaced by a large valued AB resistor. This can lead to a 50% variation in effective hysteresis if AB and P+ resistor types go to opposite three sigma limits. SPICE simulation indicates that worst case variations in this current change the effective input threshold by 1.5 mv.

The threshold is set by adjusting the voltage difference between the base of Q14, referenced to ground and Q15, which is attached to a voltage divider network. The emitters of Q14 and Q15 connect to a common current source through equal valued resistors. A drop across these resistors created by the threshold voltage steers current from the emitter of Q14 to Q15. This differential current is referred to the input summing node through the collectors of Q14 and Q15. The effective input threshold may be approximated as:

$$THR = .67u_i (V_{th} / V_{ca})$$

where V_{th} is the input threshold setting and V_{ca} is the voltage across the current setting resistor. It should be noted that there are no process dependent terms to first order. On the prototype discriminator, a one volt change in applied threshold setting changes the effective threshold by about 16 mv.

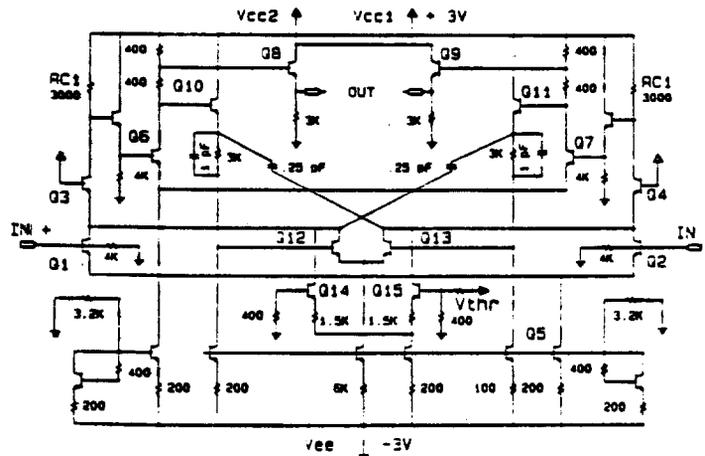


figure 7

Measurements on the Prototype Discriminator

The output of a prototype Quickchip amplifier was connected through eight meters of cable to the input of a prototype discriminator. Figure 8 shows a typical discriminator output pulse for a near threshold input pulse from the amplifier. We have set thresholds as low as eight millivolts and seen only random firing due amplifier noise. There is no hint of retriggering indicating that the hysteresis performs well. Figure 9 shows a snapshot in time taken of the discriminator output firing on amplifier noise at a threshold of about eight millivolts.

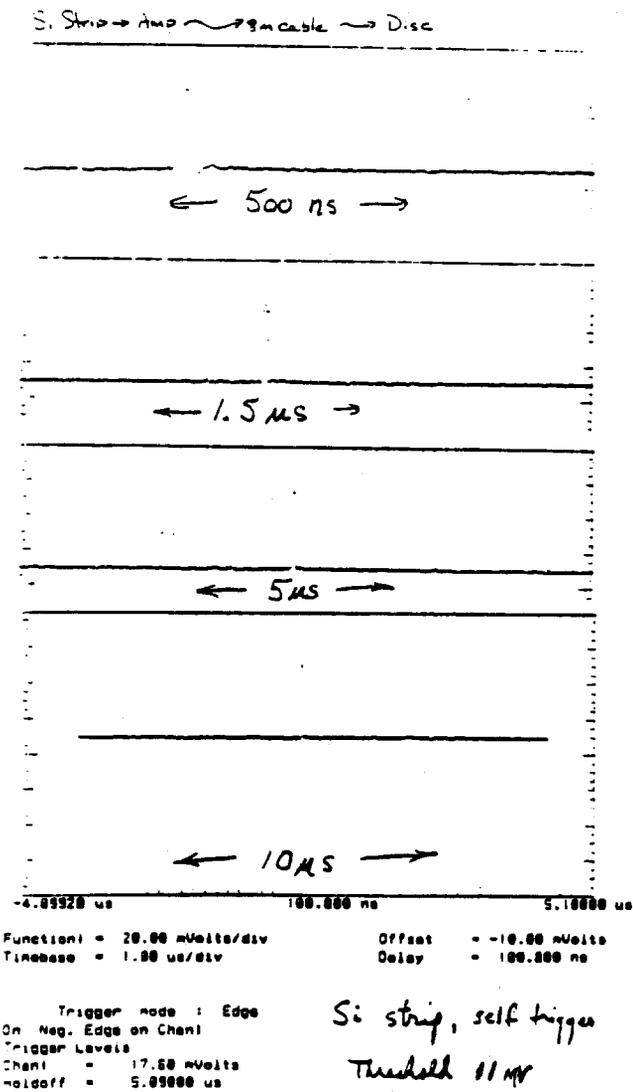


figure 8

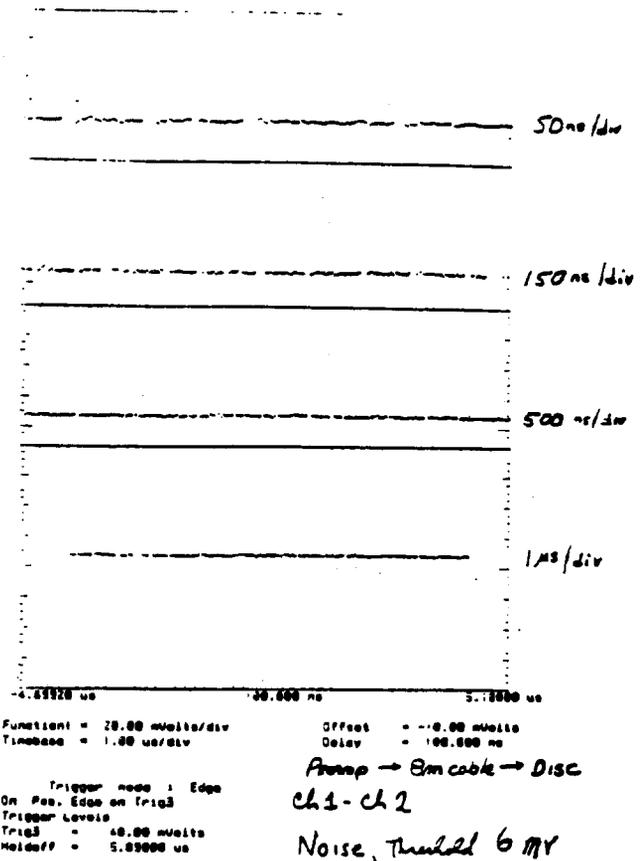


figure 9

Conclusion

We have designed and prototyped two bipolar ASIC's using Tektronix Quickchip 2 linear arrays. Measurements of the performance of the prototype devices agree very well with SPICE simulations.

References

- [1] V. Radeka, Annual Review of Nuclear and Particle Science, 1988
- [2] P. D'Angelo et al., NIM 193 (1982) 533-538
- [3] This method is described by P. Jarron and M. Goyot, NIM 226 (1984) 156-162

Acknowledgements

We would like to thank Jim McCreary of the Argonne National Laboratory Chemistry Department for permission to use the Cobalt source at Argonne to perform our radiation damage studies.



Fermi National Accelerator Laboratory

Postamp/Comparator

Hardware Description

HN100

**David Christian, Merle Haldeman
Scott Holm & Bruce Merkel**

Version 3.0

Revised 5-8-91

Word 4.0

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1.0 GENERAL INFORMATION

1.1 SSD READOUT SYSTEM (Overview)

The Postamp/Comparator (P/C) module was designed to work in conjunction with two other modules in the front end electronics for experiment E-771; a fixed target experiment. The two other modules; the Sequencer (Seq) and the Delay Encoder (DE) operate together with the P/C in a synchronous manner taking information from preamplifiers, mounted within a few inches of the Silicon Strip Detectors (SSD), repackaging it and sending it on for further repackaging and analysis.

SSD READOUT SYSTEM

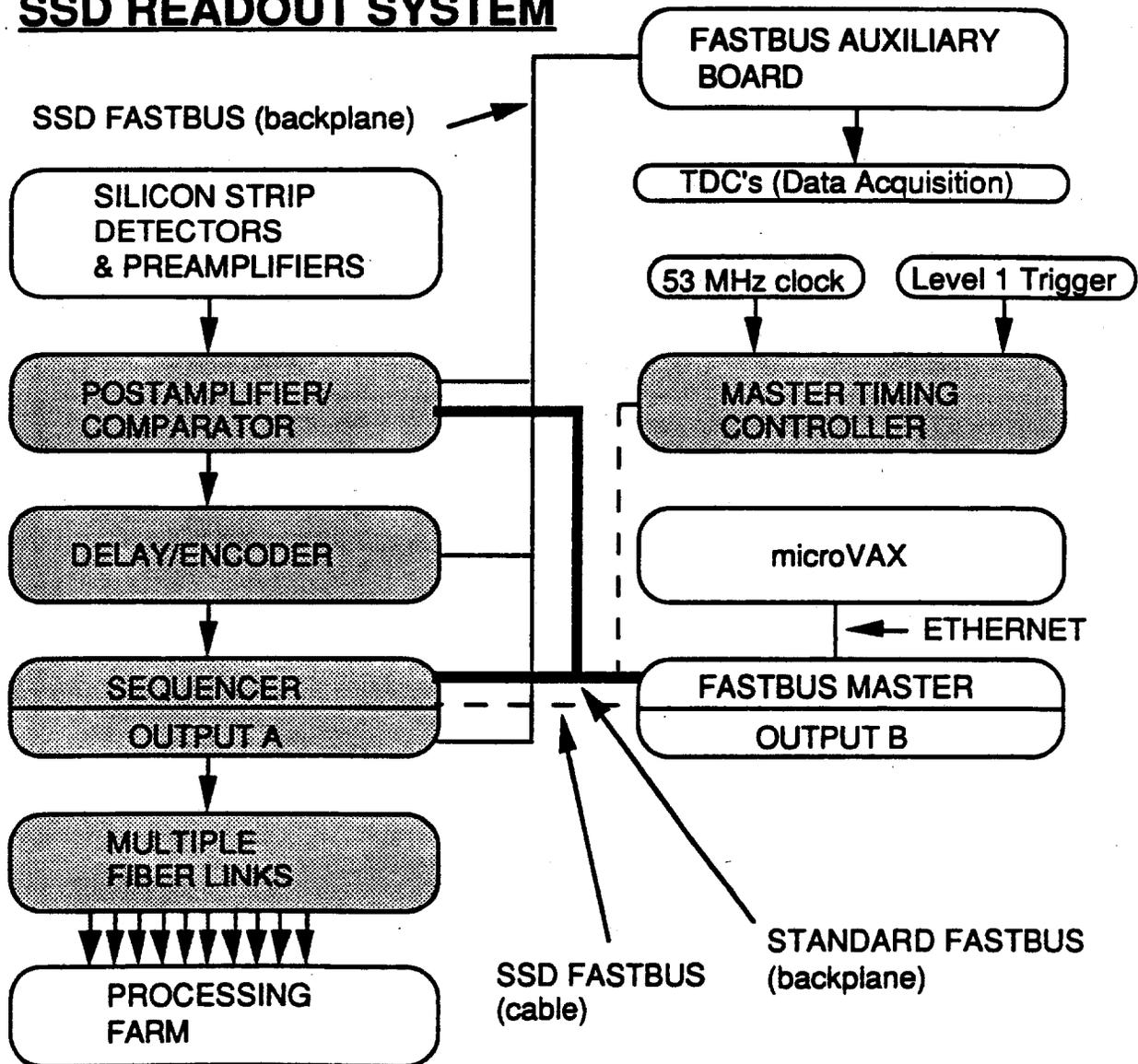


Figure 1: SSD READOUT SYSTEM

The purpose of the P/C module is to compare the voltage amplitude of its input pulses, to a programmable reference voltage (the threshold voltage) and to latch an ECL logic level output for each input pulse greater than its reference voltage. The latching of the logic levels is synchronized with a 53 MHz clock provided by the Seq module.

Differential input signals are received by each P/C from 128 SSD preamplifiers through four 64-conductor ribbon cable connectors mounted on the front portion of the P/C module. 128 ECL level output signals are sent, via a custom FASTBUS auxiliary backplane, to the DE module located in an adjacent slot in the FASTBUS crate. Eight fast analog sums and eight analog encoded digital sums intended for use by the prompt trigger logic, are constructed and output through FASTBUS auxiliary cards.

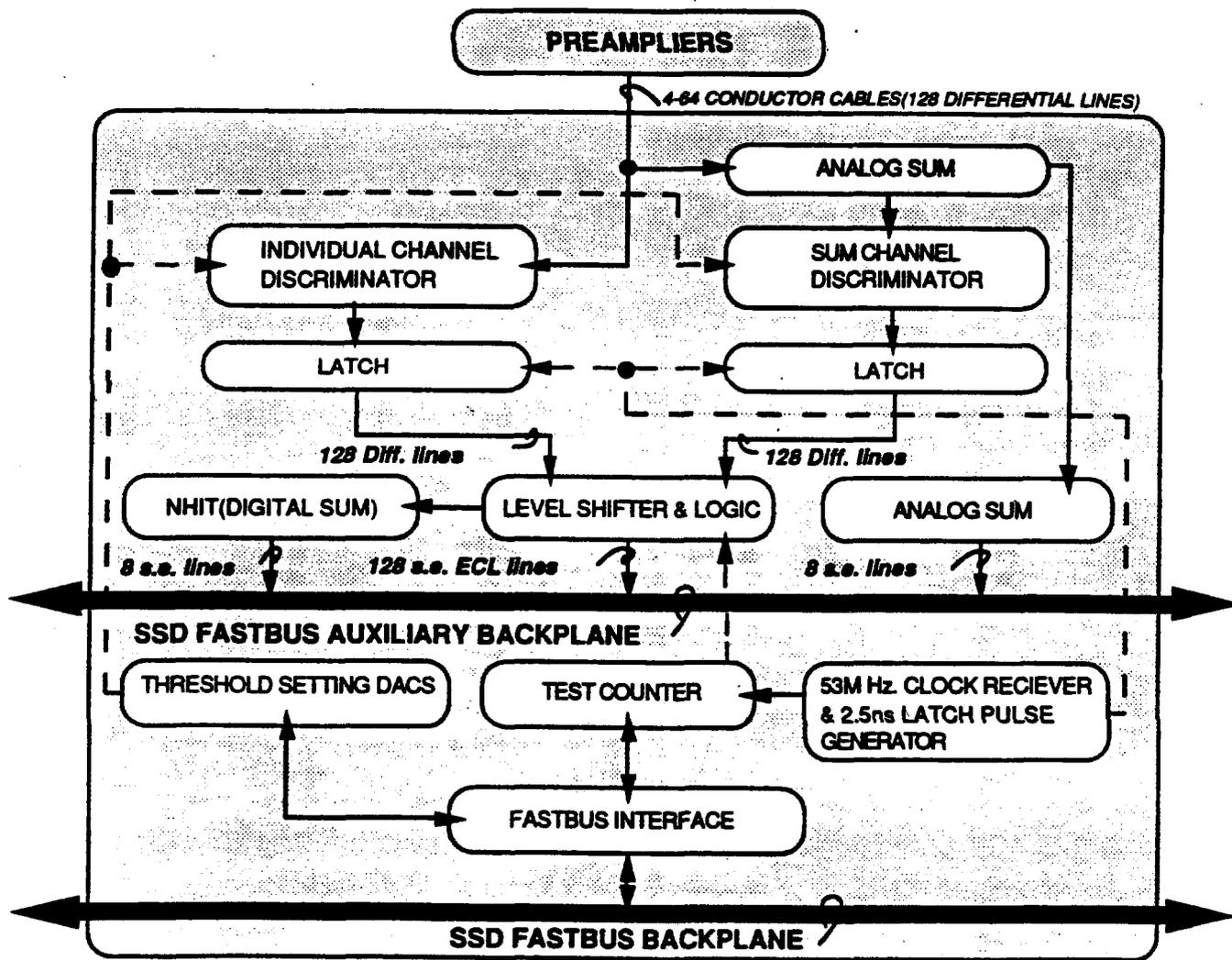


Figure 2: SSD POSTAMP/COMPARATOR

1.1.1 Standard Bus System

The P/C module is a FASTBUS slave module designed to be used together with a DE module in a FASTBUS crate equipped with a special SSD Readout auxiliary backplane. A diagram of an SSD crate with top, bottom and sides removed is shown below.

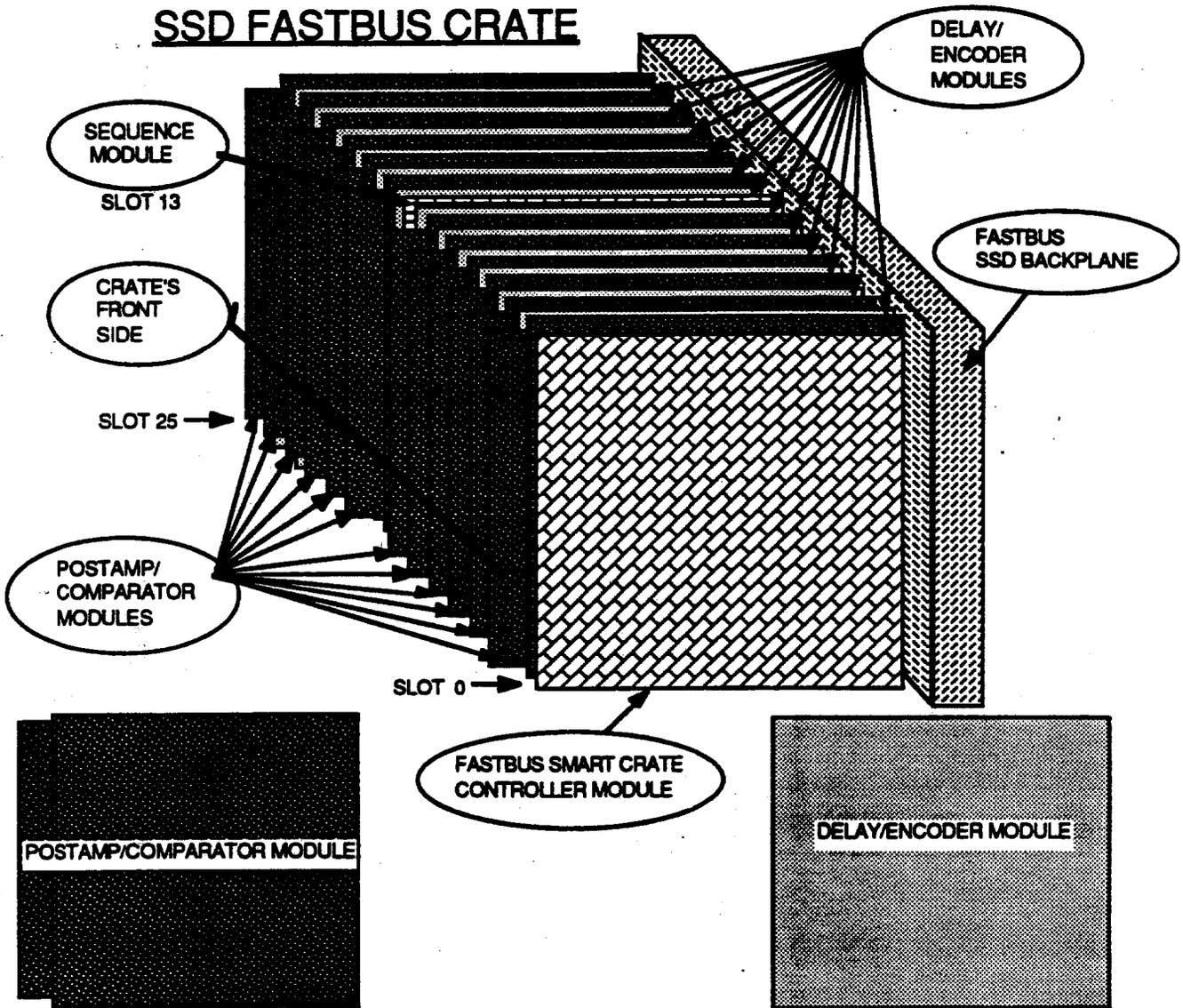


Figure 3: SSD FASTBUS CRATE

2.0 P/C MODULE - GENERAL INFORMATION

2.1 APPLICATION

This module was designed for use in the fast Silicon Strip Detector (SSD) readout system developed at FNAL for use by E-771. It is directly usable only in the context of this readout system.

2.2 PACKAGING

This board is a standard single width FASTBUS module(see ANSI/IEEE Std 960-1986) with the exception that the circuit board is extended through the front panel 3-7/8" and the FASTBUS segment connector uses pins B02 and B03 for -3.5V and pins B04, B05, and B40 for +3.5V.

2.2.1 Physical Size

The maximum board dimensions are 14.436 inches high by 19.747 inches deep, typical board dimensions are illustrated below. The board thickness is between 0.086 inches and 0.100 inches.

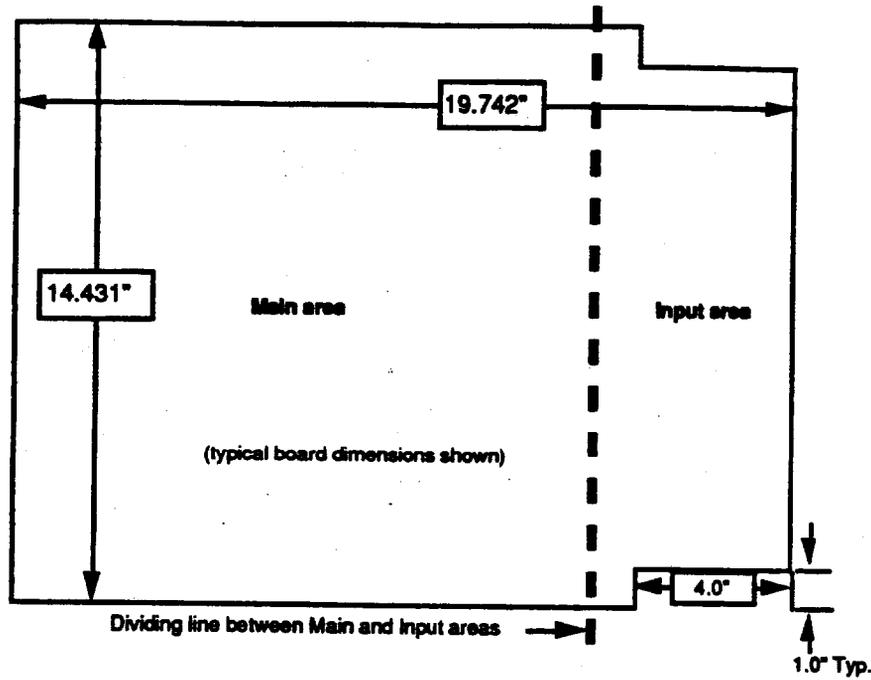


Figure 4: P/C Board Size

2.2.2 Layup

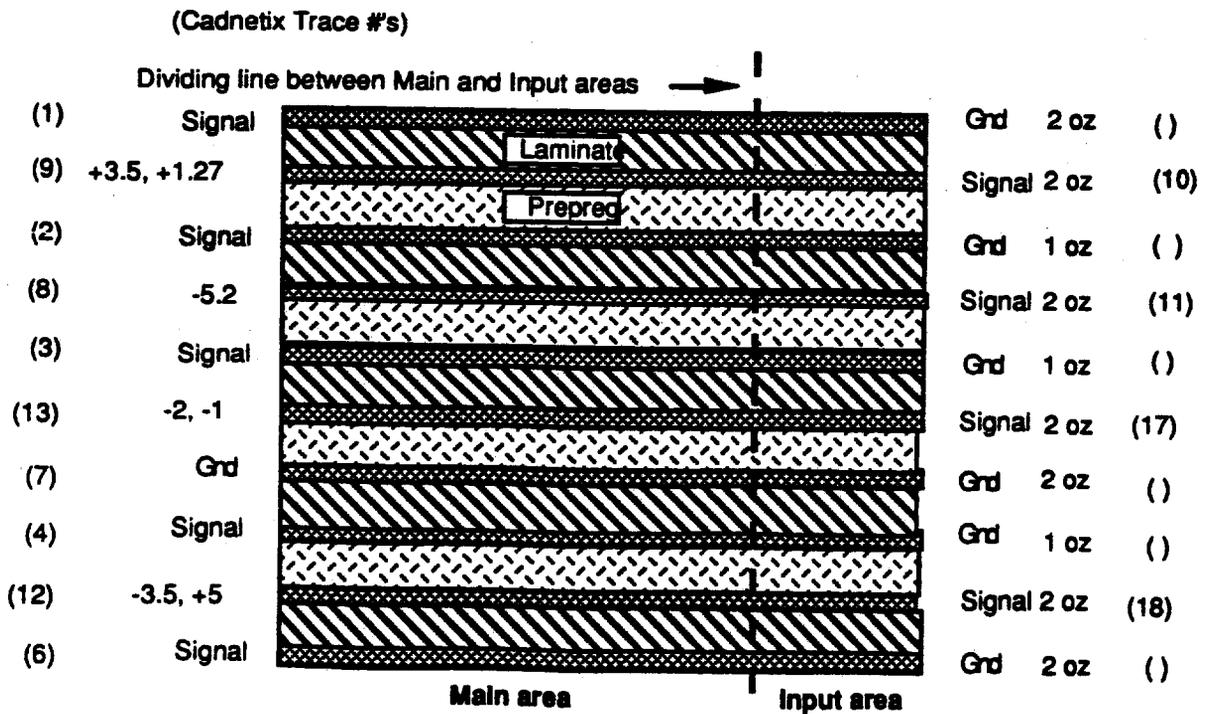


Figure 5: P/C Board Layup

2.2.3 Layout

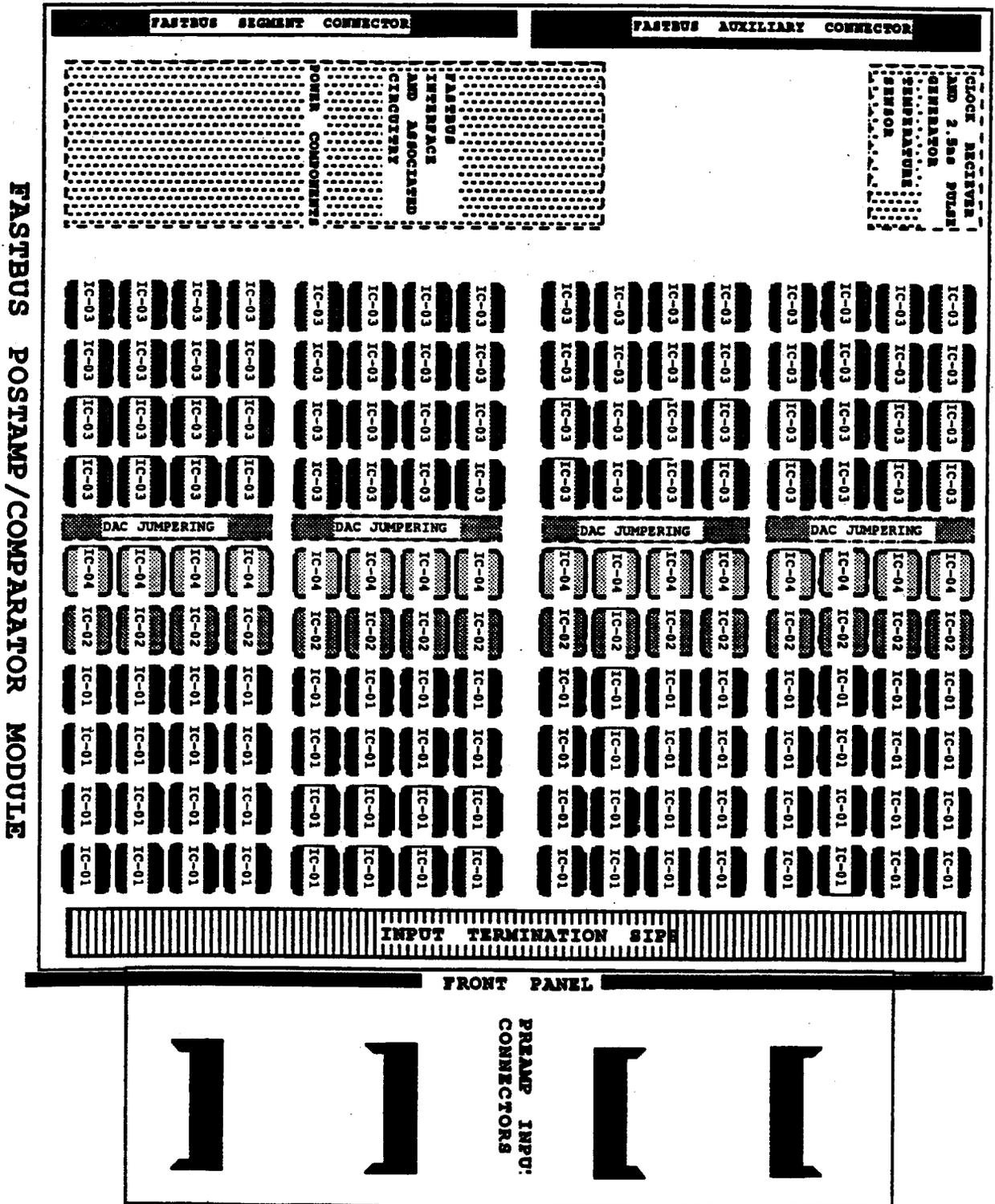
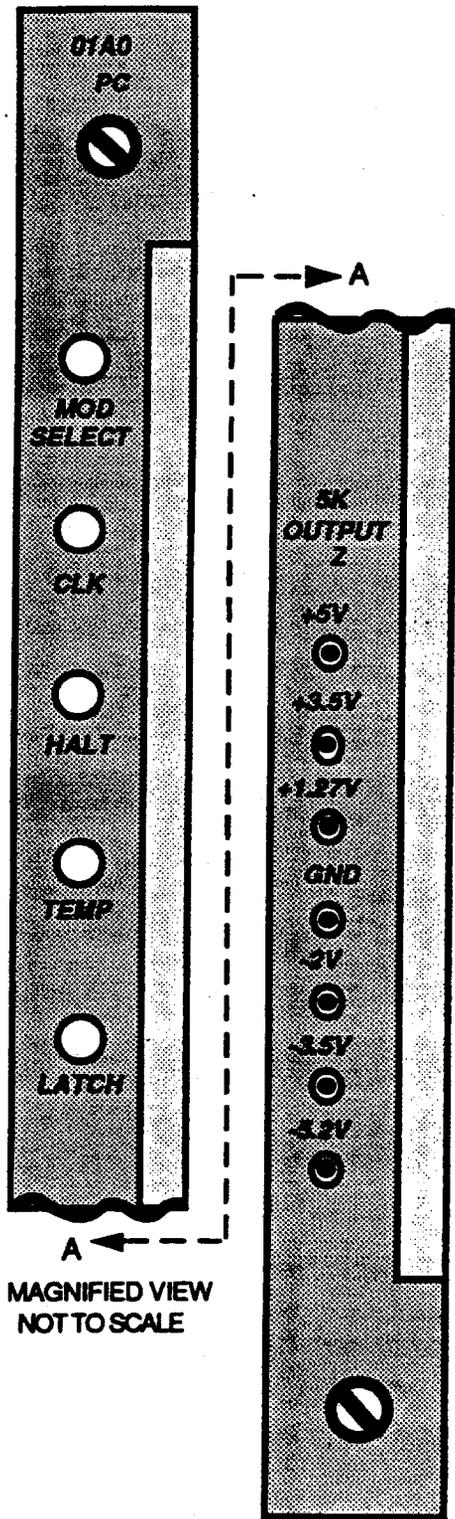


Figure 6: P/C Board Layout

2.2.4 Front Panel



MAGNIFIED VIEW
NOT TO SCALE

LED COLOR AND ENERGIZED MEANING		
MOD SELECT	Yellow	Module is being accessed by FASTBUS
CLK	Yellow	CLOCK (53M Hz.) is present
HALT	Red	Module is in TEST mode, Latches are in transparent mode.
TEMP	Red	Module temperature is >50 degrees celcius at the module top.
LATCH	Yellow	Module is in RUN mode, Latches are in latch mode.

VOLTAGE TEST POINTS
Voltage test points are in series with 5.1k ohm resistor.

Refer to Appendix G - Module Drawings
#2563.000-ED-215752 FRONT PANEL & FRONT PANEL AIR GAP DETAILS
#2563.000-ED-215753 FRONT PANEL SILKSCREEN

Figure 7: P/C Module Front Panel

2.2.5 Component List

#	MANUFACTURER	PART NUMBER	PART NAME	PART DESCRIPTION	PER	ONTY
					BD	
1	MOTOROLA	MC10109P	IC	DUAL 4-5-INPUT OR/NOR GATE	2	
2	MOTOROLA	MC10124P	IC	QUAD TTL TO ECL CONVERTER	2	
3	MOTOROLA	MC10125P	IC	QUAD ECL TO TTL CONVERTER	5	
4	MOTOROLA	CD74HC4514EN	IC	4 BIT LATCHED/4 TO 16 LINE DECODER	4	
5	BROOKTREE	BT501KC	IC	ECL/TTL OCTAL TRANSCIEVER/TRANSLATOR	2	
6	T.I.	NE555D	IC	555 TIMER SURFACE MOUNT	1	
7	MOTOROLA	MC10E016FN	IC	8-BIT SYNC BINARY UP COUNTER	1	
8	MOTOROLA	MC10E101FN	IC	QUAD 4-INPUT OR/NOR GATE	2	
9	MOTOROLA	MC10H115FN	IC	QUAD LINE RECEIVER	1	
10	MOTOROLA	MC10H188FN	IC	HEX BUFFER WITH ENABLE	1	
11	T.I.	SN74123	IC	RETRIGGERABLE MULTIVIBRATOR	1	
12	T.I.	SN10KHT5543FN	IC	OCTAL TTL-ECL TRANSLATOR W/OE	3	
13	T.I.	SN10KHT5541FN	IC	OCTAL ECL-TTL TRANSLATOR 3 STATE OUT	1	
14	ALTERA	EPMS128JC	IC	128 MACROCELL MAX EPLD	1	
15	FERMI	IC 01	IC	"SSD 2/CHAN SUM, DISCRIM AND LATCH"	64	
16	FERMI	IC 02	IC	"3/CHAN LOGIC, QUAD ANALOG SUM/CLK"	16	
17	US2	IC 03 DAC	IC	IC-3 CMOS DAC/ADC	64	
18	FERMI	IC 04	IC	SSD LOGIC AND NHIT	16	
19	TI	74ACT11245DW	IC	OCTAL BUS TRANSCIEVER 3/STATE OUTPUT	2	
20	TI	SN7404	IC	HEX INVERTER	1	
21	NATIONAL	LM311M	IC	LM311M SMT VOLTAGE COMPARATOR	1	
22	NATIONAL	LM35CZ	IC	LM35CZ TEMPERATURE SENSOR DEGREE C	1	
23	3M	268-6234-71-3877	IC	SOCKET 68 PIN FOR EPMS128JC	1	
24	LINEAR TECH	LT317AK	REG	POSITIVE VOLTAGE REGULATOR	1	
25	ELMEC TECH.	FDC 2510	DELAY	SIP ULTRA HIGH-SPEED FIXED DELAY LINE	1	
26	LITTELFUSE	251007	FUSE	FUSE PICO 7A	5	
27	GENERAL SEMI	5KP5.0A	DIODE	TRANSIENT SUPPRESSION TRANSZORB	5	
28	MOTOROLA	1N5401	DIODE	1N5401 DIODE	2	
29	MOTOROLA	1N4002	DIODE	1N4002 DIODE	1	
30	BEAU	85802	CONN	EUROSTYLE TERMINAL STRIPS STYLE B 90'	2	
31	DU PONT	68002-236	CONN	BERGSTICK II HEADERS (36 PINS) @ PINS	265	
32	E.F. JOHNSON	105-1041-001	CONN	TIP JACKS WHITE	3	
33	E.F. JOHNSON	105-1042-001	CONN	TIP JACKS RED	3	
34	E.F. JOHNSON	105-1043-001	CONN	TIP JACKS BLACK	1	
35	YAMAICHI	NFP-64A-0122	CONN	BOX HEADER 64 PIN 25mil PITCH	4	
36	AMP	2-532956-0	CONN	FASTBUS MODULE SEGMENT CONNECTOR	1	
37	AMP	534974-9	CONN	FASTBUS MODULE AUX CONNECTOR 195 PIN	1	
37A	SAMTEC	SNT-100-BK-G	CONN	2 PIN SAMTEC SHUNT	3	
38	BRADFORD	HCOZXX	SIP	50 OHM/.01uF CAP TERMINATING SIP	64	
39	MURATA/ERIE	GRM42-6X7R103K050BB	CAP	.01uF CAPACITOR SURFACE MOUNT1206	1	
40	MURATA/ERIE	GRM42-6X7R104K050B	CAP	.1uF CAPACITOR SURFACE MOUNT 1206	447	
41	MEPCO/CENT	49MC106C010KOASFT	CAP	10uF SMT POLARIZED CAP - CASE STYLE C	2	
42	MURATA/ERIE	GRM42-2Y5V105Z016B	CAP	1uF CHIP CAP 16 WVDC S.M. 1210	34	
43	MURATA/ERIE	GRM42-6X7R471K050B	CAP	470 pF 1206 SMT CAP	1	
44	MURATA/ERIE	GRM42-6COG500K050B	CAP	50 pF 1206 SMT CAP	1	
45	RCD	MC 1A 100Ω 5% B	RES	RESISTOR 100 OHM 1206 SMT	117	
46		5.1K Ω 5% 1/4 WATT	RES	RESISTOR 5.1K OHM	7	
47	RCD	MC 1A 1K Ω 5% B	RES	RESISTOR 1K OHM 1206 SMT	5	
48	RCD	MC 1A 220 Ω 5% B	RES	RESISTOR 220 OHM 1206 SMT	6	
49	RCD	MCR 1A 24.9K Ω 1% B	RES	RES 25K OHM 1206 SMT	32	
50	RCD	MC 1A 51 Ω 5% B	RES	RES 50 OHM 1206 SMT	12	
51	RCD	MC 1A 150 Ω 5% B	RES	RES 150 OHM 1206 SMT	32	
52	OHMITE RES	1 Ω 5% 45J1R0	RES	1 OHM 5 WATT	2	
53	RCD	MC 1A 330 Ω 5% B	RES	330 OHM 1206 SMT	34	
54	RCD	MC 1A 1.5K Ω 5% B	RES	1.5K OHM 1206 SMT	1	
55	RCD	MC 1A 3K Ω 5% B	RES	3K OHM 1206 SMT	1	
56	RCD	MC 1A 6.8K Ω 5% B	RES	6.8K OHM 1206 SMT	1	
57	RCD	MC 1A 13K Ω 5% B	RES	13K OHM 1206 SMT	1	
58	RCD	MC 1A 47K Ω 5% B	RES	47K OHM 1206 SMT	1	
59		120 Ω 5% 1/4 WATT	RES	120 OHM 1/4 WATT	1	
60	RCD	MC 1A 2.2 MEG Ω 5% B	RES	2.2 MEG OHM 1206 SMT	1	
61	RCD	MC 1A 4.3K Ω 5% B	RES	4.3K OHM 1206 SMT	1	
62	RCD	MC 1A 200 Ω 5% B	RES	200 OHM 1206 SMT	1	
63	MEPCO/CENT	ST4MA 501	RES	500 OHM POT SMT	1	
64	RCD	MC 1A 10K Ω 5% B	RES	10K OHM 1206 SMT	2	

#	MANUFACTURER	PART NUMBER	PART NAME	PART DESCRIPTION	QNTY PER BD
65	RCD	MC 1A 43 Ω 5 1/2 B	RES	43 OHM 1206 SMT	2
66	FERMI		BOARD	POST/AMP COMPARATOR BOARD	1
67	FERMI		BOARD	F/C CIRCUIT BOARD STUFFING	1
68	FERMI	0882-MB-199070	HRDWRE	"RAF 3/8"" HEX SPACER"	2
69	RAF	7039.SS MOD E =1/2	SCREW	SHOULDER SCREW	2
70	DIALITE	559-2301-001	LED	YELLOW LED	3
71	DIALITE	559-2101-001	LED	RED LED	2
72	FERMI	2563.000-MD-215752	PANEL	FRONT PANEL	1
73	FERMI	2563.000-MD-215752	PANEL	FRONT PANEL FILLER	1
74			SCREW	"4-40 x 5/16"" FLAT HEAD SCREW"	4
75			SCREW	" 2-56 x 3/8"" SS FLAT HEAD"	1
76	SECME	27 11008 23	SWITCH	TROPICAL VERSION ROTARY 8 POS. SWITCH	1
77	BELDEN CABLE	#9R28010	WIRE	28 GA. 10 CONDUCTOR RIBBON CABLE (IN)	27
78	OK IND		WIRE	PRE STRIPPED WIRE WRAP WIRE (IN)	240
79	DU PONT	68002-536	CONN	BERGSTIKII HEADERS STRAIGHT SINGLE ROW	96
80			SCREW	"6-32 x 3/8"" BINDER HEAD"	2
81			NUT	6-32 NUT	2
				TOTAL	1348

2.2.6 Connector Pinouts

2.2.6.1 FASTBUS Segment Connector

(Viewed From Front of Crate)

B01-GND	A01-GND
B02- -3.5V BUS	A02-AL00
B03- -3.5V BUS	A03-AL01
B04- +3.5V BUS	A04-AL02
B05- +3.5V BUS	A05-GND
B06- N/C	A06-AL03
B07- -5.2V BUS	A07-AL04
B08- -5.2V BUS	A08-AL05
B09- -5.2V BUS	A09-AR
B10-AK	A10-GND
B11-AI	A11-GK
B12-SS0	A12-DK
B13- -2V BUS	A13-AK
B14- +5V BUS	A14-WT
B15- +5V BUS	A15-GND
B16-SS1	A16-AS
B17-SS2	A17-DS
B18-RD	A18-MS0
B19-MS2	A19-MS1
B20-B20R	A20-GND
B21-EG	A21-AD00
B22- +5V BUS	A22-AD01
B23-SR	A23-AD02
B24-RB	A24-AD03
B25-BH	A25-GND
B26-B26R	A26-AD04
B27-GA00	A27-AD05
B28-GA01	A28-AD06
B29-GA02	A29-AD07
B30-GA03	A30-GND
B31-GA04	A31-AD08
B32- -2V BUS	A32-AD09
B33-DLA	A33-AD10
B34-DRA	A34-AD11
B35-DLB	A35-GND
B36-DRB	A36-AD12
B37-DAR	A37-AD13
B38-DBR	A38-AD14
B39-B39R	A39-AD15
B40- +3.5V BUS	A40-GND
B41-FP1	A41-TP
B42- -5.2V BUS	A42-A42R

(continuation)

B43-FP2	A43-PE
B44-FP3	A44-PA
B45-B45R	A45-GND
B46-TRO	A46-AD16
B47-TR1	A47-AD17
B48-TR2	A48-AD18
B49-TR3	A49-AD19
B50-TR4	A50-GND
B51-TR5	A51-AD20
B52- +5V BUS	A52-AD21
B53-TR6	A53-AD22
B54-TR7	A54-AD23
B55-URO	A55-GND
B56-UR1	A56-AD24
B57-TX	A57-AD25
B58-RX	A58-AD26
B59- -5.2V BUS	A59-AD27
B60- -5.2V BUS	A60-GND
B61- -5.2V BUS	A61-AD28
B62- -2V BUS	A62-AD29
B63- +5V BUS	A63-AD30
B64- +5V BUS	A64-AD31
B65-GND	A65-GND

Notes:

- 1.-5.2 Volts uses 7 pins
- 2.+5.0 Volts uses 6 pins
- 3.-2.0 Volts uses 3 pins
- 4.+3.5 Volts uses 3 pins
- 5.-3.5 Volts uses 2 pins
- 6.Ground uses 14 pins

2.2.6.2 FASTBUS Auxilliary Connector

(Viewed From Front of Crate)

C01-H53MHZ,Ø1 Clock	B01-Post./Comp. Ch.01	A01-Post./Comp. Ch.00
C02-GND	B02-Post./Comp. Ch.03	A02-Post./Comp. Ch.02
C03-L53MHZ,Ø1 Clock	B03-Post./Comp. Ch.05	A03-Post./Comp. Ch.04
C04-GND	B04-Post./Comp. Ch.07	A04-Post./Comp. Ch.06
C05-GND	B05-Post./Comp. Ch.09	A05-Post./Comp. Ch.08
C06-GND	B06-Post./Comp. Ch.11	A06-Post./Comp. Ch.10
C07-GND	B07-Post./Comp. Ch.13	A07-Post./Comp. Ch.12
C08-Reset	B08-Post./Comp. Ch.15	A08-Post./Comp. Ch.14
C09-GND	B09-Post./Comp. Ch.17	A09-Post./Comp. Ch.16
C10-GND	B10-Post./Comp. Ch.19	A10-Post./Comp. Ch.18
C11-GND	B11-Post./Comp. Ch.21	A11-Post./Comp. Ch.20
C12-Analog Sum 0*	B12-Post./Comp. Ch.23	A12-Post./Comp. Ch.22
C13-Analog Sum 0	B13-Post./Comp. Ch.25	A13-Post./Comp. Ch.24
C14-Digital Sum 0*	B14-Post./Comp. Ch.27	A14-Post./Comp. Ch.26
C15-Digital Sum 0	B15-Post./Comp. Ch.29	A15-Post./Comp. Ch.28
C16-Analog Sum 1*	B16-Post./Comp. Ch.31	A16-Post./Comp. Ch.30
C17-Analog Sum 1	B17-Post./Comp. Ch.33	A17-Post./Comp. Ch.32
C18-Digital Sum 1*	B18-Post./Comp. Ch.35	A18-Post./Comp. Ch.34
C19-Digital Sum 1	B19-Post./Comp. Ch.37	A19-Post./Comp. Ch.36
C20-GND	B20-Post./Comp. Ch.39	A20-Post./Comp. Ch.38
C21-Analog Sum 2*	B21-Post./Comp. Ch.41	A21-Post./Comp. Ch.40
C22-Analog Sum 2	B22-Post./Comp. Ch.43	A22-Post./Comp. Ch.42
C23-Digital Sum 2*	B23-Post./Comp. Ch.45	A23-Post./Comp. Ch.44
C24-Digital Sum 2	B24-Post./Comp. Ch.47	A24-Post./Comp. Ch.46
C25-Analog Sum 3*	B25-Post./Comp. Ch.49	A25-Post./Comp. Ch.48
C26-Analog Sum 3	B26-Post./Comp. Ch.51	A26-Post./Comp. Ch.50
C27-Digital Sum 3*	B27-Post./Comp. Ch.53	A27-Post./Comp. Ch.52
C28-Digital Sum 3	B28-Post./Comp. Ch.55	A28-Post./Comp. Ch.54
C29-GND	B29-Post./Comp. Ch.57	A29-Post./Comp. Ch.56
C30-GND	B30-Post./Comp. Ch.59	A30-Post./Comp. Ch.58
C31-Analog Sum 4*	B31-Post./Comp. Ch.61	A31-Post./Comp. Ch.60
C32-Analog Sum 4	B32-Post./Comp. Ch.63	A32-Post./Comp. Ch.62
C33-Digital Sum 4*	B33-Post./Comp. Ch.65	A33-Post./Comp. Ch.64
C34-Digital Sum 4	B34-Post./Comp. Ch.67	A34-Post./Comp. Ch.66
C35-Analog Sum 5*	B35-Post./Comp. Ch.69	A35-Post./Comp. Ch.68
C36-Analog Sum 5	B36-Post./Comp. Ch.71	A36-Post./Comp. Ch.70
C37-Digital Sum 5*	B37-Post./Comp. Ch.73	A37-Post./Comp. Ch.72
C38-Digital Sum 5	B38-Post./Comp. Ch.75	A38-Post./Comp. Ch.74
C39-GND	B39-Post./Comp. Ch.77	A39-Post./Comp. Ch.76
C40-Analog Sum 6*	B40-Post./Comp. Ch.79	A40-Post./Comp. Ch.78
C41-Analog Sum 6	B41-Post./Comp. Ch.81	A41-Post./Comp. Ch.80
C42-Digital Sum 6*	B42-Post./Comp. Ch.83	A42-Post./Comp. Ch.82
C43-Digital Sum 6	B43-Post./Comp. Ch.85	A43-Post./Comp. Ch.84
C44-Analog Sum 7*	B44-Post./Comp. Ch.87	A44-Post./Comp. Ch.86
C45-Analog Sum 7	B45-Post./Comp. Ch.89	A45-Post./Comp. Ch.88
C46-Digital Sum 7*	B46-Post./Comp. Ch.91	A46-Post./Comp. Ch.90
C47-Digital Sum 7	B47-Post./Comp. Ch.93	A47-Post./Comp. Ch.92
C48-GND	B48-Post./Comp. Ch.95	A48-Post./Comp. Ch.94
C49-GND	B49-Post./Comp. Ch.97	A49-Post./Comp. Ch.96
C50-GND	B50-Post./Comp. Ch.99	A50-Post./Comp. Ch.98
C51-GND	B51-Post./Comp. Ch.101	A51-Post./Comp. Ch.100
C52-GND	B52-Post./Comp. Ch.103	A52-Post./Comp. Ch.102
C53-GND	B53-Post./Comp. Ch.105	A53-Post./Comp. Ch.104
C54-GND	B54-Post./Comp. Ch.107	A54-Post./Comp. Ch.106
C55-GND	B55-Post./Comp. Ch.109	A55-Post./Comp. Ch.108
C56-GND	B56-Post./Comp. Ch.111	A56-Post./Comp. Ch.110
C57-GND	B57-Post./Comp. Ch.113	A57-Post./Comp. Ch.112
C58-GND	B58-Post./Comp. Ch.115	A58-Post./Comp. Ch.114
C59-GND	B59-Post./Comp. Ch.117	A59-Post./Comp. Ch.116
C60-GND	B60-Post./Comp. Ch.119	A60-Post./Comp. Ch.118
C61-GND	B61-Post./Comp. Ch.121	A61-Post./Comp. Ch.120
C62-GND	B62-Post./Comp. Ch.123	A62-Post./Comp. Ch.122
C63-GND	B63-Post./Comp. Ch.125	A63-Post./Comp. Ch.124
C64-N/C	B64-Post./Comp. Ch.127	A64-Post./Comp. Ch.124
C65-N/C	B65-GND	A65-N/C

2.2.6.3 Input Connector Pin Definitions

J1	J2	J3	J4	PIN #
CH0*	CH2*	CH125*	CH127*	1
CH0	CH2	CH125	CH127	2
CH4*	CH6*	CH121*	CH123*	3
CH4	CH6	CH121	CH123	4
CH8	CH10	CH117	CH119	5
CH8*	CH10*	CH117*	CH119*	6
CH12	CH14	CH113	CH115	7
CH12*	CH14*	CH113*	CH115*	8
CH16*	CH18*	CH109*	CH111*	9
CH16	CH18	CH109	CH111	10
CH20*	CH22*	CH105*	CH107*	11
CH20	CH22	CH105	CH107	12
CH24	CH26	CH101	CH103	13
CH24*	CH26*	CH101*	CH103*	14
CH28	CH30	CH97	CH99	15
CH28*	CH30*	CH97*	CH99*	16
CH32*	CH34*	CH93*	CH95*	17
CH32	CH34	CH93	CH95	18
CH36*	CH38*	CH89*	CH91*	19
CH36	CH38	CH89	CH91	20
CH40	CH42	CH85	CH87	21
CH40*	CH42*	CH85*	CH87*	22
CH44	CH46	CH81	CH83	23
CH44*	CH46*	CH81*	CH83*	24
CH48*	CH50*	CH77*	CH79*	25
CH48	CH50	CH77	CH79	26
CH52*	CH54*	CH73*	CH75*	27
CH52	CH54	CH73	CH75	28
CH56	CH58	CH69	CH71	29
CH56*	CH58*	CH69*	CH71*	30
CH60	CH62	CH65	CH67	31
CH64*	CH66*	CH61*	CH63*	33
CH64	CH66	CH61	CH63	34
CH68*	CH70*	CH57*	CH59*	35
CH68	CH70	CH57	CH59	36
CH72	CH74	CH53	CH55	37
CH72*	CH74*	CH53*	CH55*	38
CH76	CH78	CH49	CH51	39
CH76*	CH78*	CH49*	CH51*	40
CH80*	CH82*	CH45*	CH47*	41
CH80	CH82	CH45	CH47	42
CH84*	CH86*	CH41*	CH43*	43
CH84	CH86	CH41	CH43	44
CH88	CH90	CH37	CH39	45
CH88*	CH90*	CH37*	CH39*	46
CH92	CH94	CH33	CH35	47
CH92*	CH94*	CH33*	CH35*	48
CH96*	CH98*	CH29*	CH31*	49
CH96	CH98	CH29	CH31	50
CH100*	CH102*	CH25*	CH27*	51
CH100	CH102	CH25	CH27	52
CH104	CH106	CH21	CH23	53
CH104*	CH106*	CH21*	CH23*	54
CH108	CH110	CH17	CH19	55
CH108*	CH110*	CH17*	CH19*	56
CH112*	CH114*	CH13*	CH15*	57
CH112	CH114	CH13	CH15	58
CH116*	CH118*	CH9*	CH11*	59
CH116	CH118	CH9	CH11	60
CH120	CH122	CH5	CH7	61
CH120*	CH122*	CH5*	CH7*	62
CH124	CH126	CH1	CH3	63
CH124*	CH126*	CH1*	CH3*	64

2.3 TYPICAL CHARACTERISTICS

P/C Module: Typical Characteristics

Package	FASTBUS module P.C. board extended 3-7/8" through front panel
Power Supply Voltages	+5.0 Volts @ 0.6-2.74 A +3.5 Volts @ 4.27 A -2.0 Volts @ 2.42 A -3.5 Volts @ 4.08 A -5.2 Volts @ 4.45 A
Typical Power Dissipation	78 Watts
Required cooling air flow	400 ft/min. minimum
Required cooling air temp.	40 Degrees Celsius maximum entering module
Differential Input Signal Range	+/- 90 mV
Common Mode Signal Range	+/- 1 Volt
Input Impedance	50 Ω Transmission Line terminated with 0.1 μF in series with 50 Ω resistor.
Input Bias Current	0 A
Output Voltage	-1 to -1.8 Volts. Driving 100Ω termination to -2.0 V.
Propagation Delay	15.6 ns between input and output connectors measured with 80 mV differential input signal; DAC set for 250 mV (corresponds to 20 mV differential input signal).
Adjacent Channel Crosstalk	30 db
Hysteresis	10 mV
Triggering Uncertainty	0.5 mV
Ambient Temperature Range	0 to 40°C

3.0 P/C MODULE - THEORY OF OPERATION

3.1 BLOCK DIAGRAM

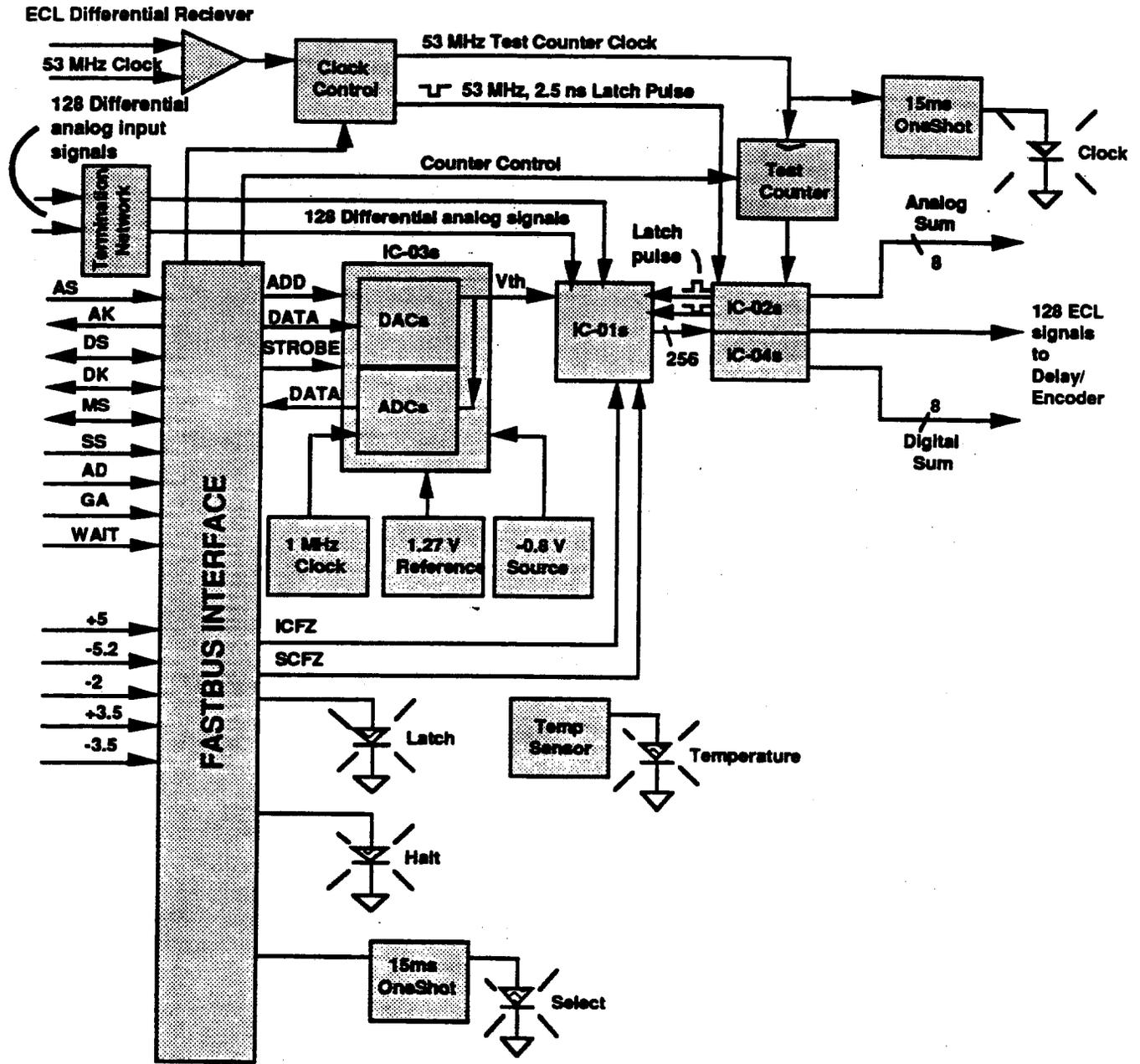


Figure 8: P/C Module Block Diagram

3.2 FASTBUS INTERFACE

The P/C Module is a FASTBUS slave. It responds to geographic addressing in control space only. It allows both single and block transfers and will respond with the following slave status responses. Information on the control space registers is found on pages 14 thru 18.

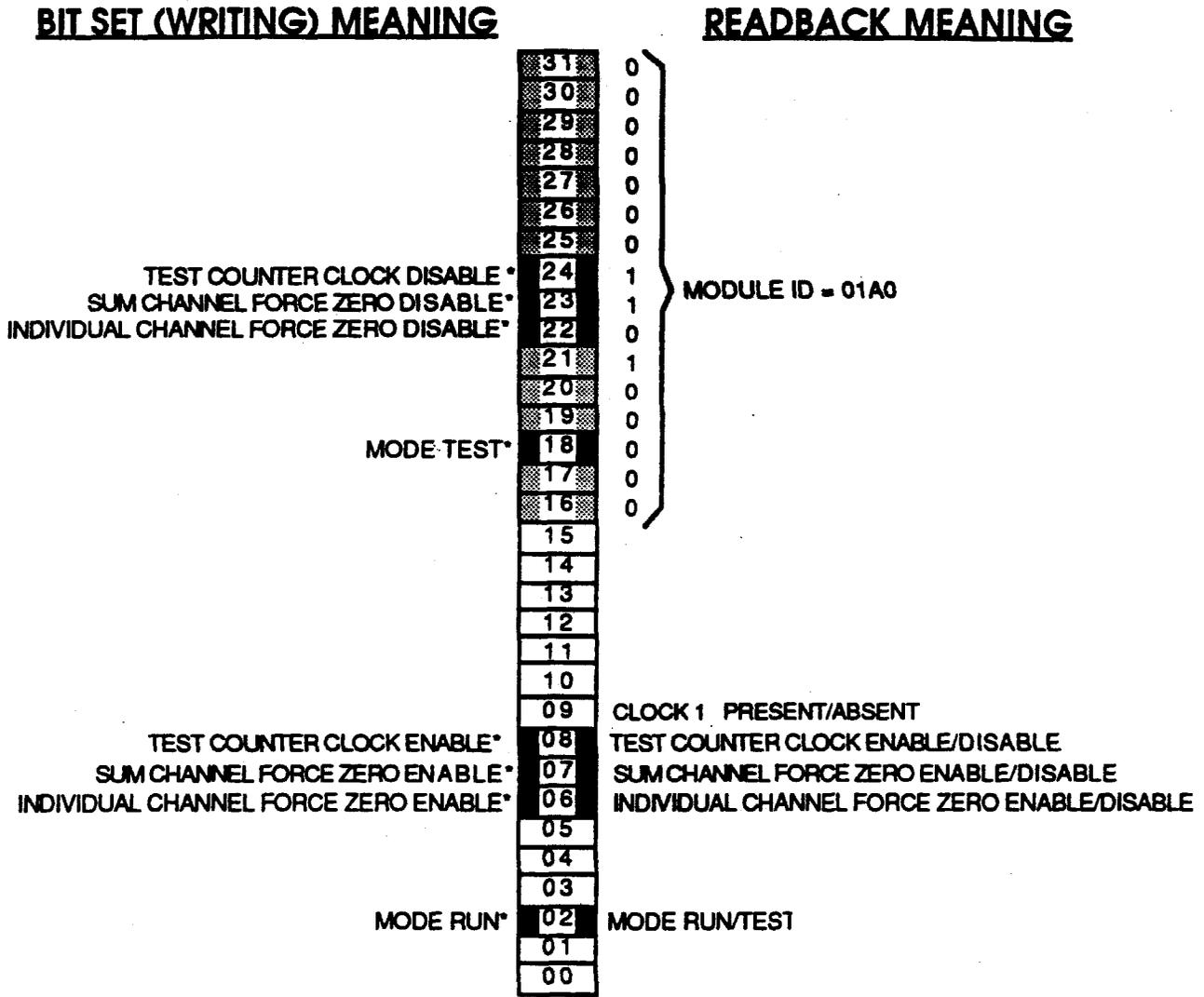
3.2.1 Slave Status Responses

The P/C Module asserts the following FASTBUS Slave Status (SS) Responses

- SS=2** for end of block on DAC, Read or Write block transfers.
- SS=6** for Reads or Writes to invalid addresses, or if an attempt is made to write to a DAC while the board is in the **RUN(LATCH)** mode.
- SS=7** for Reads or Writes to invalid secondary addresses.

3.2.2 CSR0

CSR0



* The corresponding bit displaced 16 bits away must have a zero written simultaneously.

Figure 9: Control Space Register-0

CSR0

This is the main control and status register. It is a selective set and reset register with the bit assignments shown on the next page:

CSRO Bit assignments:

- BIT 02 -- RUN** Writing a "1" to this bit puts the module in the **RUN(LATCH)** mode. A "0" must be simultaneously written to BIT 18. This bit is cleared by writing a "1" to BIT 18 thus putting the P/C in the **TEST(HALT)** mode.
- Reads a "1" back when in **RUN(LATCH)** mode or a "0" in **TEST(HALT)** mode.
- BIT 06 -- ICFZ__EN** Writing a "1" to this bit forces the outputs of the individual channel latches to a zero. A zero must be simultaneously written to bit 22
- BIT 07 -- SCFZ__EN** Writing a "1" to this bit forces the outputs of the Summed channel latches to a zero. A zero must be simultaneously written to bit 23
- BIT 08 -- CCLK__EN** When in the **TEST(HALT)** mode, writing a "1" to this bit **ENABLES** the 8-bit test counter which, if the 53 MHz clock is present, counts at the clock frequency. The test counter is disabled by setting bit 24; the count remains at the count it stopped at or was last preset to.
- While in the **RUN(LATCH)** mode, the eight output bits of the test counter are forced to zero.
- BIT 09 -- CLK1-ON** Reads a "1" back if 53 MHz. clock is present.
- BIT 18 -- TEST** Writing a "1" to this bit places the module in the **TEST(HALT)** mode. A "0" must be simultaneously written to BIT 02.
- BIT 22 -- ICFZ__DIS** Writing a "1" to this bit **DISABLES** the "Individual Channel Force Zero" feature and allows the latches to track the data in the latched or transparent modes. A "0" must be simultaneously written to BIT 06.
- BIT 23 -- SCFZ__DIS** Writing a "1" to this bit **DISABLES** the "Summed Channel Force Zero" feature and allows the latches to track the data in the latched or transparent modes. A "0" must be simultaneously written to BIT 07.
- BIT 24 -- CCLK__DIS** Writing a "1" to this bit disables the clock to the 8-bit test counter.
- BIT 16-31 -- DEVICE ID** The device ID (01A0) is read back on these bits.

3.2.3 CSR1

CSR1

BIT SET (WRITING) MEANING

READBACK MEANING

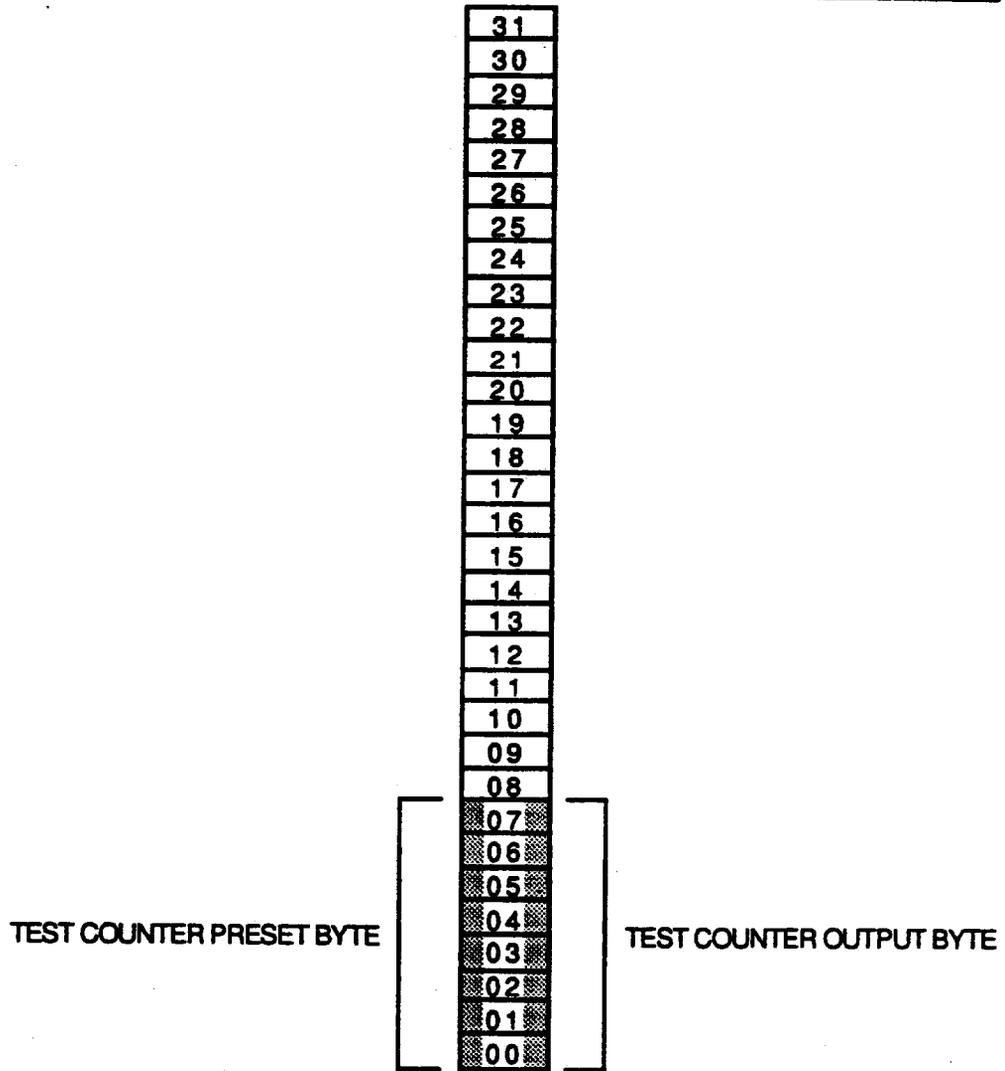


Figure 10: Control Space Register-1

CSR1

This register is used to write and read the 8-bit test counter. The counter is disabled and the outputs are forced to zero, when the P/C module is in the **RUN(LATCH)** mode.

BIT 00-07

Data to be written to or read back from the 8-bit test counter.

3.2.4 CSR10

CSR10

BIT SET (WRITING) MEANING

READBACK MEANING

31		
30		
29		
28		
27		
26		
25		
24		
23		
22		
21		
20		
19		
18		
17		
16		
15		
14		
13		
12		
11		
10		
09		
08		
07		
06	64	MSB
05	32	
04	16	
03	8	
02	4	
01	2	
00	1	LSB

IC-03 CHIP POPULATION

Figure 10: Control Space Register-10

CSR10

This register allows one to read back a value which indicates how this module is populated with IC-03 DAC/ADC IC's. The value read back is dependent upon the location of the three manually placed jumpers JU2, JU3 and JU4. Refer to section 3.5.2 CSR10 JUMPERS.

Although the bits have standard binary weighting, a "1" can exist in only one of the seven locations at a given time, thus one can only have IC-03 DAC/ADC populations of 1,2,4,8, 16,32 & 64, providing 4,8,16,32,64,128 & 256 DACs. A zero read back indicates a non-standard population.

3.2.5 CSR C000_0000 - C000_00FF

CSR C000_0000 through C000_00FF

BIT SET (WRITING) MEANING

READBACK MEANING

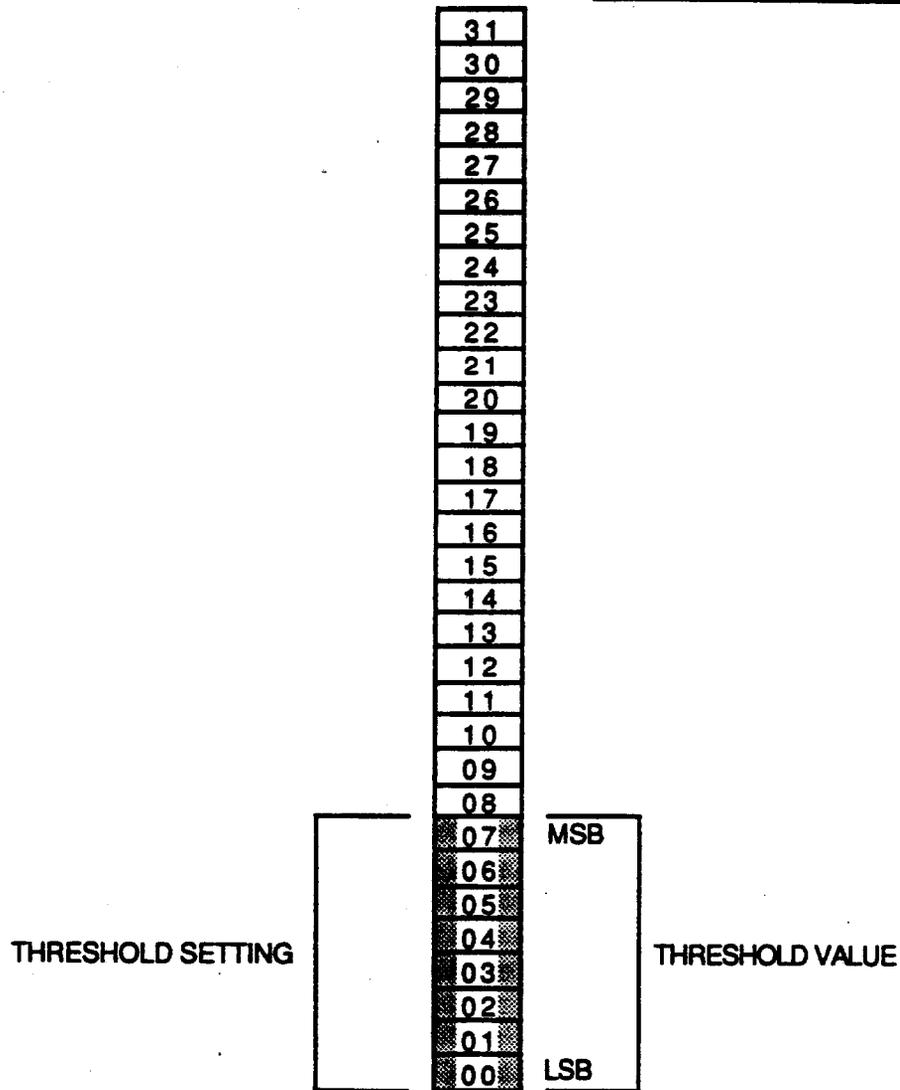


Figure 11: Control Space Register-C000_0000-C000_00FF

CSR C000_0000 - C000_00FF (Threshold Registers)

The 8 LSB of these 256 registers are used to write threshold settings or read threshold values from the IC-03 DAC/ADCs. These registers can be written only when the module is in the **TEST(HALT)** mode. If a write is attempted when in the **RUN(LATCH)** mode, the module returns an SS=6 error.

BIT 00-07 -- DATA

Data to write/read the DAC/ADCs.

3.3 MODES OF OPERATION

There are two general operating modes of the P/C module; "RUN(LATCH)" mode and "TEST(HALT)" mode. The "RUN(LATCH)" mode is used when data is being sent to the module through the input connectors and data is being latched. The "TEST(HALT)" mode is used when the module is being tested or is communicating with FASTBUS. The module mode is set via the FASTBUS control space register; CSR0(refer to section "3.2.2 CSR0").

3.3.1 RUN(LATCH) Mode Operation

In "RUN" mode, the module is set up to latch the 256 channels of data that is present at the discriminator outputs(refer to section "3.4.2 IC-01..."). The data is latched every 18.9 ns by the 2.5 ns LATCH pulse synchronized with the 53 MHz. clock. The 256 channels of latched data is passed to the logic of IC-02 and IC-04(refer to section "3.4.3 IC-02....") where it is reduced to 128 single ended channels of ECL level signals(to be passed via the FASTBUS Auxiliary backplane to the DE)as well as 8 differential analog sum signals and 8 differential NHIT signals, both also sent to the Auxiliary backplane for further processing.

During "RUN" mode the module is accessible by FASTBUS only to manipulate control space register CSRO so as to place the module into "TEST" mode, attempts to access other control space registers will result in an SS=6 error.

The LATCH LED on the front panel should be lit during "RUN" mode.

3.3.2 TEST(HALT) Mode Operation

"TEST" mode is used either to test the module via an 8-bit on board test counter(refer to section "3.4.6 Test Counter Circuit") or to manipulate FASTBUS controllable circuitry such as the control space registers or to change DAC threshold settings.

The HALT LED on the front panel should be lit while the module is in "TEST" mode.

3.4 CIRCUITRY OPERATION

3.4.1 Inputs

128 differential SSD preamplifier signals are received by the P/C module via four, 64-conductor ribbon cables. The input signal order does not correspond to the order of the silicon strips in the detector for reasons having to do with signal density on both the detector itself and the pre-amplifier cards connected to the detector. The input signal traces on the P/C module between the input connectors and discriminators are routed to restore the monotonic strip order of the detector. These differential signals are AC coupled through 0.1 μ F capacitors near the inputs of the IC-01 ASIC's, both sides of which are terminated through 50 Ω to ground. These termination components are housed in a custom 10-lead sip each of which will terminate two channels (4 wires) of the 128 channels; thus 64 sips per module.

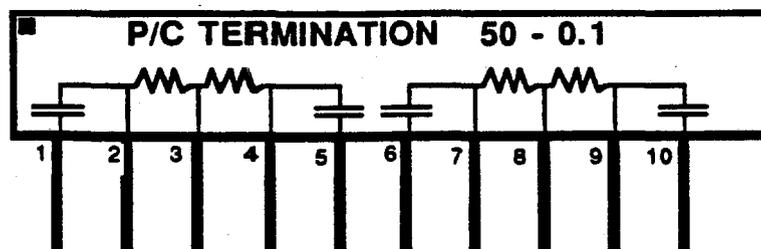


Figure 13: P/C Termination

3.4.2 IC-01 (Two Channel Sum, Discriminator and Latch)

IC-01 is a bipolar ASIC made using a Tektronix Quickchip 2K-130 linear array. It contains two linear summing amplifiers, four time-over-threshold discriminators(each with a 10 mV hysteresis and variable threshold setting capability), and four latches.

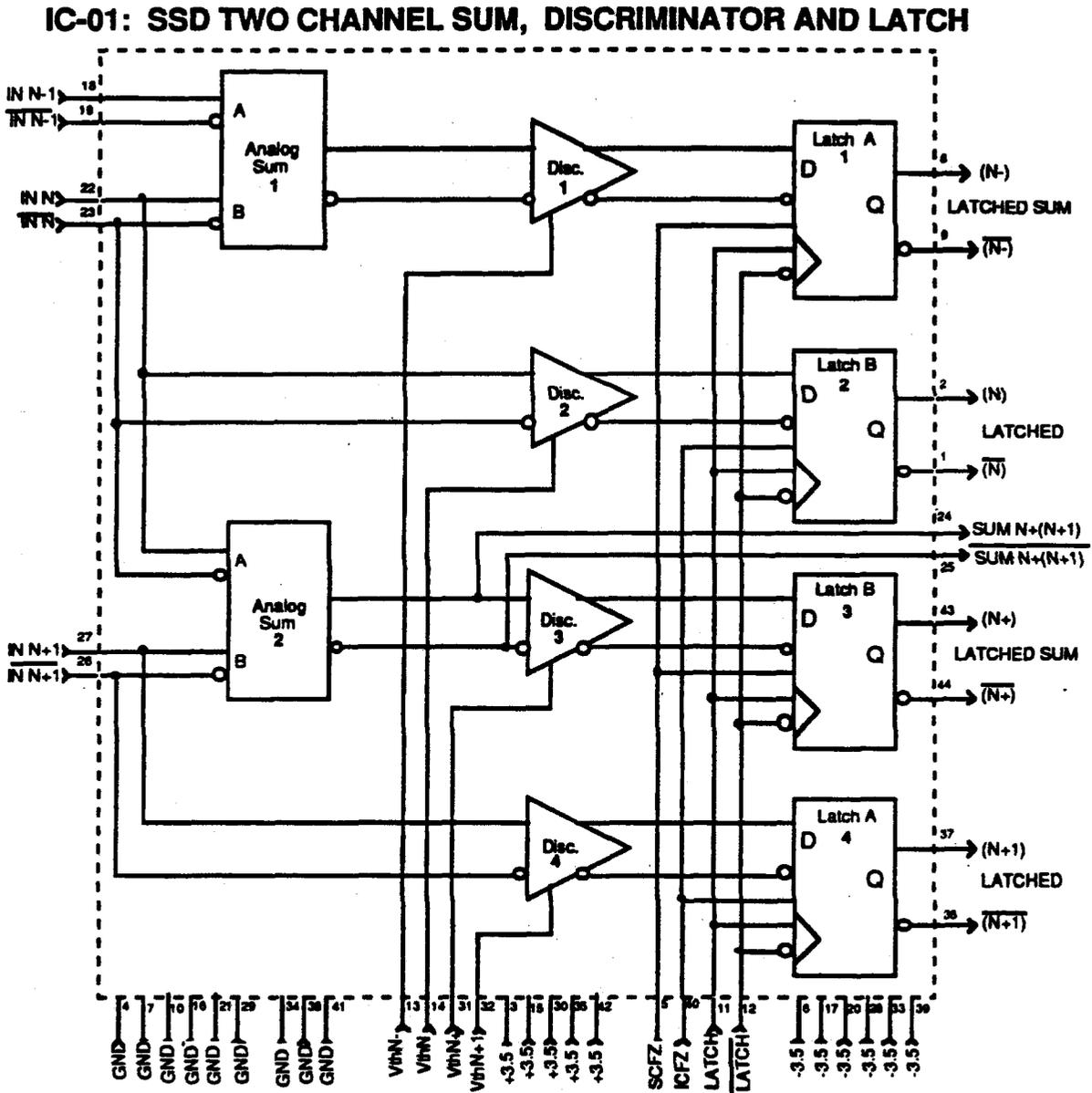


Figure 14: IC-01: Two Channel Sum, Discriminator and Latch

Each IC-01 (except for the units with the lowest and highest numbered channels on the board) receive signals from three consecutive silicon strips. The first and third signals are also input to neighboring IC-01 chips. Two linear sums are made; the first by adding the first and second inputs, and the second by adding the second and third inputs. The output of each of the two linear sums is input to a discriminator. The output of the second sum is also sent to IC-02 for additional summations. The second and third inputs are connected to the remaining two discriminators. The result is two pairs of discriminators, one pair discriminating individual strip signals (inputs two and three), and the other pair discriminating the two linear sum outputs. Each discriminator has a separate threshold setting input.

Typical Discriminator differential input voltage versus threshold voltage setting are shown in Appendix E (IC-01 ASIC data sheets). The 10 mV hysteresis band prevents the discriminators from following extraneous signals(white noise, cross-talk, overshoot, radiation noise, etc.) As the graphs show the discriminators are linear up to approximately 50 mV differential signals. The device has been characterized up to 90 mV differential.

The output of each of the four discriminators is sent directly to a latch (one per discriminator output) which is controlled by a differential, 2.5 ns wide LATCH pulse. This LATCH pulse, common to all four latches, controls the function of the latches, which can be thought of as digital sample-and-holds. When the LATCH pulse is present the latches are in the "transparent" state during which time the latch output follows the discriminator output. When the LATCH pulse is not present, the latches are in the "latched" state and the latch outputs remain unchanged.

In normal operation, an IC-02 located within four inches of it's associated IC-01's, provides this 2.5ns wide LATCH pulse. This LATCH pulse is synchronized to the 53 MHz CLK signal received from the Seq. This pulse switches the latch input from "latched" mode to "transparent" mode for a time equal to the width of the pulse (approximately 2.5 ns), and then returns it to the "latched" mode. The result is that the state of the discriminator is latched and held for one RF cycle less the width of the LATCH pulse(see diagram below). Two more control signals, called INDIVIDUAL CHANNEL FORCE ZERO and SUMMED CHANNEL FORCE ZERO, also effect the operation of the latches. INDIVIDUAL CHANNEL FORCE ZERO is connected to the two individual strip latches and SUMMED CHANNEL FORCE ZERO is connected to the sum latches. When FORCE ZERO is HI, the effected latches are forced to logical zero. This function is used to insure that no signal is received from an IC-01 chip while the P/C module is in the TEST(HALT) mode. It also makes it possible to disable either bank of discriminators while leaving the other bank operational.

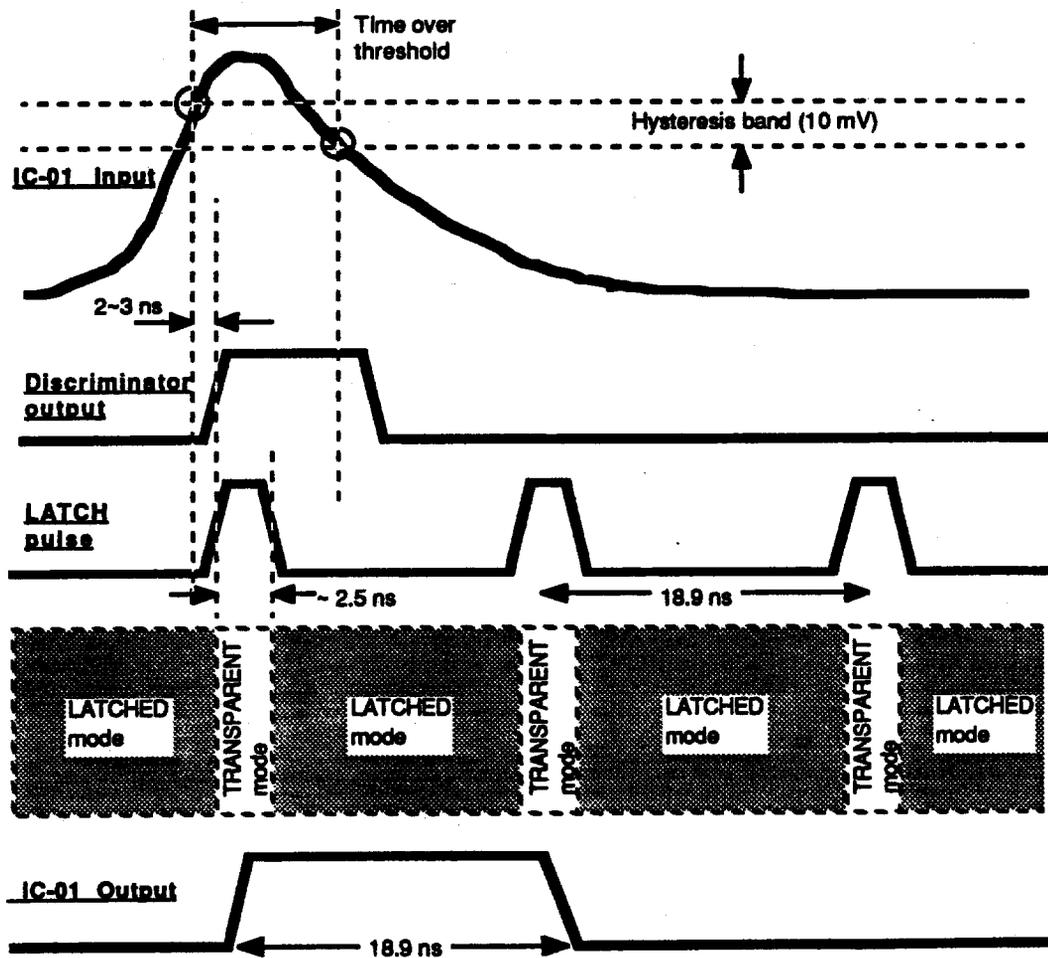


Figure 15: IC-01 Function Diagram

3.4.3 IC-02 (3-Channel Logic, Quad Analog Sum & Latch Driver) and IC-04 (5-Channel Logic & Octal NHIT)

The IC-01 latch outputs are input to two other bipolar ASIC's; IC-02 and IC-04 also made using Tektronix Quickchip 2K-130 linear arrays. These two chips as a group can be broken down into four functions: 1.)Logic, 2.)Quad ANALOG SUM, 3.)NHIT or DIGITAL SUM, and 4.)LATCH pulse buffer. The four functions will be discussed in order starting with the logic. Internal block diagrams of the two ASICs can be found on the following page as well as in Appendix E.

The logic functions as follows, the combination of these two chips accept inputs from four IC-01's (8 SSD channels), and produces eight ECL output signals which are sent, via the auxiliary backplane, to the DE module in the adjacent slot. Since the outputs of the latches of IC-01 are differential, the inputs to the logic on both IC-02 and IC-04 are differential receivers. The function of the receivers is three-fold; convert from differential to single ended, shift the level of the latch outputs to the level of the logic gates, and to switch input polarity by switching inputs to a receiver where a polarity change is necessary. The logic producing the eight ECL output signals performs in the following way: any given output channel (N) is set HIGH if the corresponding single strip latch (N) is set, or if one of the 2 summed-channel latches including strip N is set, but neither of the individual channel latches for the two channels contributing to the sum are set.

These logic signals are OR'ed with test inputs(t1 and t2) which sit at logical low levels while the module is in the RUN(LATCH) mode. Test signals are sent to these test inputs in the TEST(HALT) mode during which time the latch outputs are forced to a logical zero. The test inputs are implemented so that the adjacent DE module can be tested with a fixed or incremental pattern.

Recall that IC-01 supplied an output which was produced from the analog sum of two individual channel inputs, this output goes directly to one of the inputs of the quad ANALOG SUM of the IC-02. The four IC-01s(8 SSD channels) each supply the quad ANALOG SUM with an output which in turn the quad ANALOG SUM converts to an analog sum of the same eight strips used in the logic function above. The output current of the quad ANALOG SUM is a linear sum of the eight individual strip signals.

IC-04 is used to produce a signal known as NHIT or DIGITAL SUM which consists of a current, the magnitude of which is proportional (100 uA/strip hit) to the number of hit strips in the group of 8 SSD channels. The NHIT inputs are constructed by both IC-02 and IC-04 logic, forming a logical OR of a single strip signal and one of the summed channel signals which has that strip as one of its inputs. The result is that the output of NHIT will register a ONE if a hit is shared by two adjacent strips even though two bits (for two adjacent strips) are set in the DE.

The LATCH pulse buffer of IC-02 is designed to accept a narrow pulse (2.5 ns wide) and fan out a differential version of this pulse to the latch inputs of four IC-01 chips.

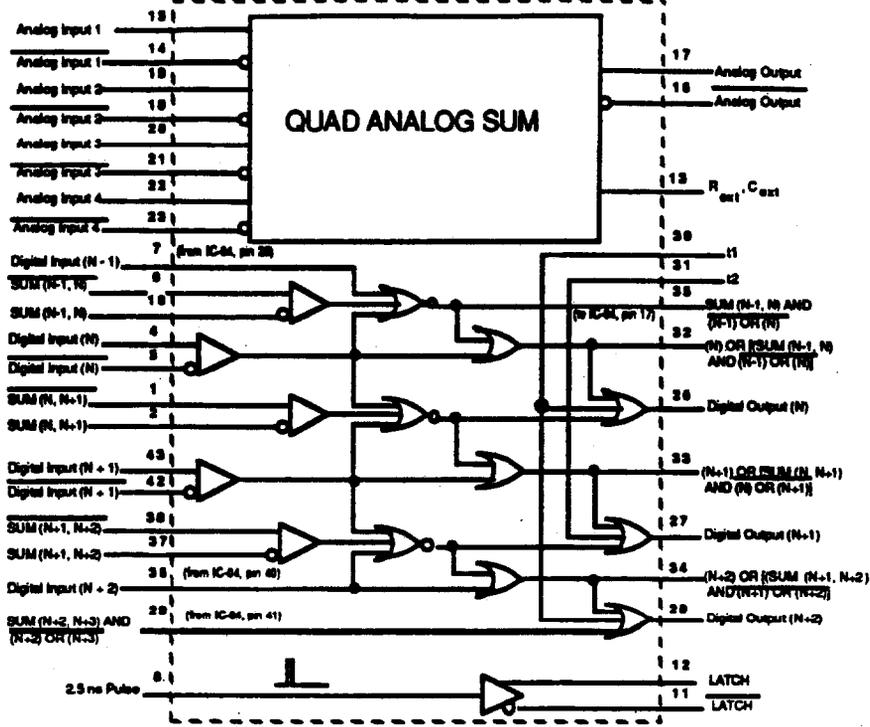


Figure 16: IC-02: Three Channel Logic, Quad Analog Sum & Latch Driver

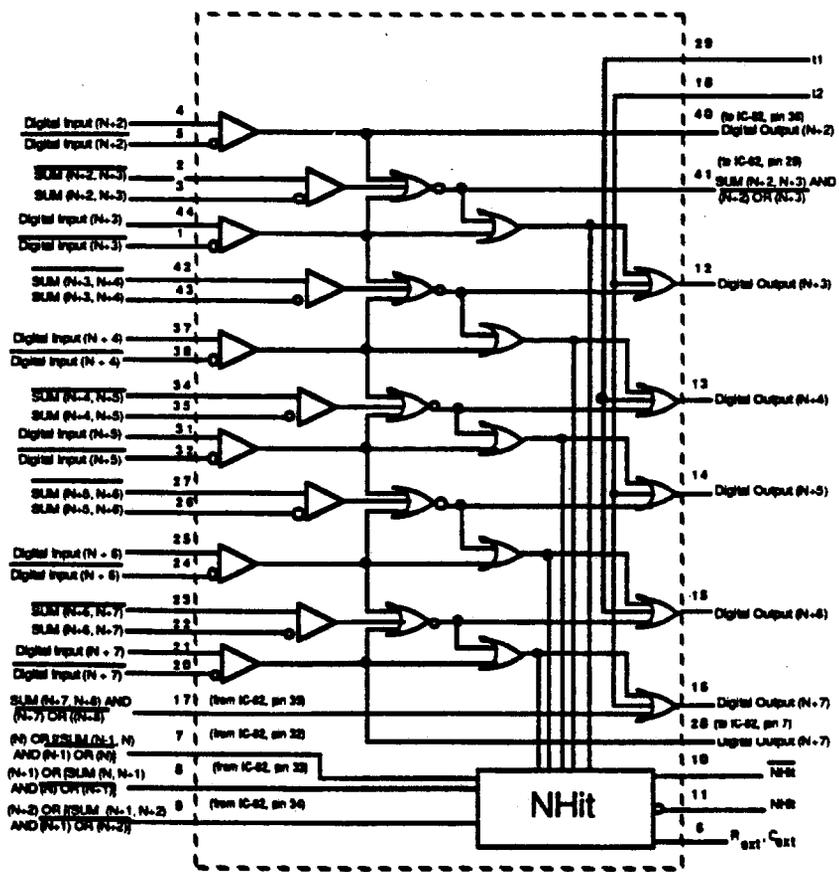


Figure 16: IC-04: Five Channel Logic and Octal NHIT

3.4.4 IC-03 DAC/ADC

Voltage levels are provided for the threshold voltage (V_{th}) inputs of the IC-01 (Sum, Discriminator and Latch) chips by a CMOS ASIC produced by United Silicon Structures. This chip contains four 8 bit D/A converters and one 8 bit A/D which requires an on board 1 MHz clock. An internal block diagram of IC-03 is shown below.

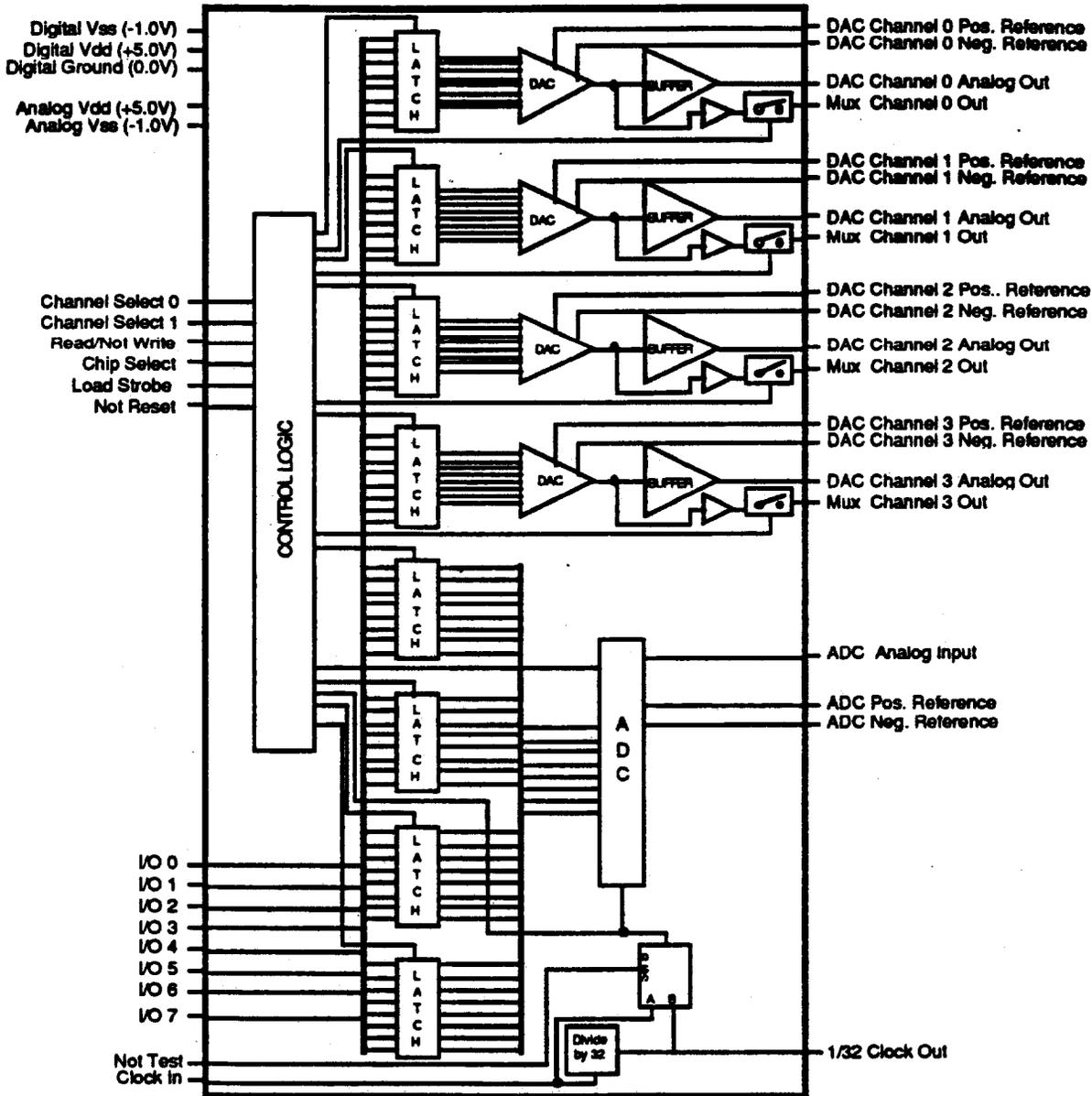


Figure 18: IC-03 Quad DAC/ADC

64 IC-03 chips may be mounted, providing individual control of all 256 discriminators, or DAC outputs may be jumpered together to allow the use of as few as one IC-03 chip to control all discriminators. The IC-03 chips share 8 bussed I/O lines and 4 control lines. Each chip has a separate select line. The DAC output range is from 0V to the reference +1.27V. The output impedance of these DACs varies between 10 and 30 Ω . Each chip requires power supply voltages of -0.8V, +5.0V, and a reference voltage of +1.27V.

Once a DAC has been written a value, one must wait for 32 counts of the 1 MHz clock before the data can be read properly.

3.4.5 2.5ns LATCH Pulse Circuitry

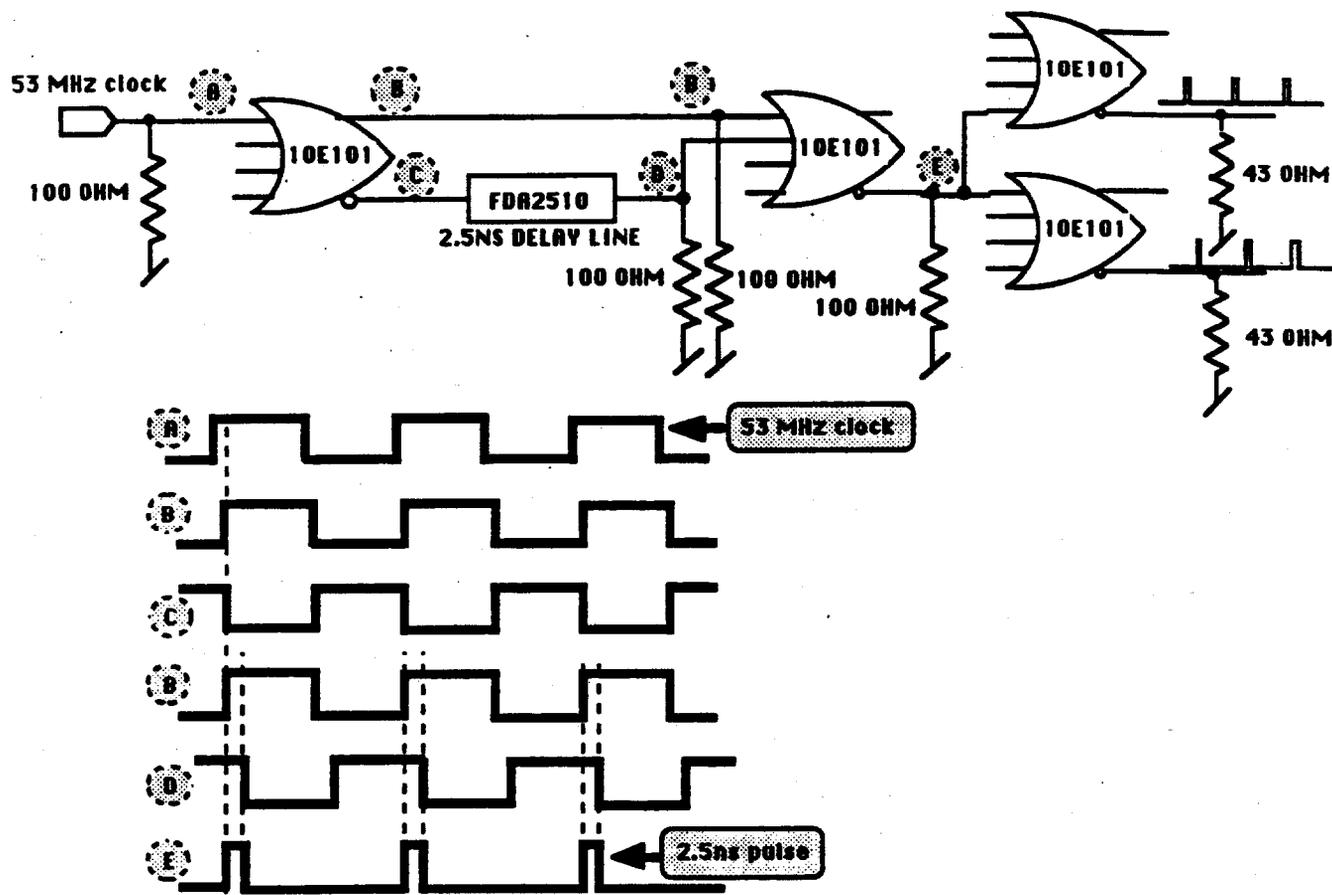


Figure 19: 2.5ns Latch Pulse Generation Circuit

3.4.6 Test Counter Circuit

A presettable 8 bit counter is included on the P/C module to provide a means of sending test data to the associated DE module. This counter is controlled via CSR0. The counter's outputs are reset (forced to zero) when the P/C module is in the RUN(LATCH) mode. When the board is in the TEST(HALT) mode, the counter may be set in the count or hold mode. In the hold mode, the counter output pattern can be altered by presetting the counter via CSR1. In the count mode, the counter is incremented by the CLK (53 MHz) signal. The control to and connection of outputs from the test counter is illustrated on the following page. This 8-bit counter provides 256 unique patterns which are sent to the DE module through the IC-02 and IC-04 test inputs(t1 and t2).

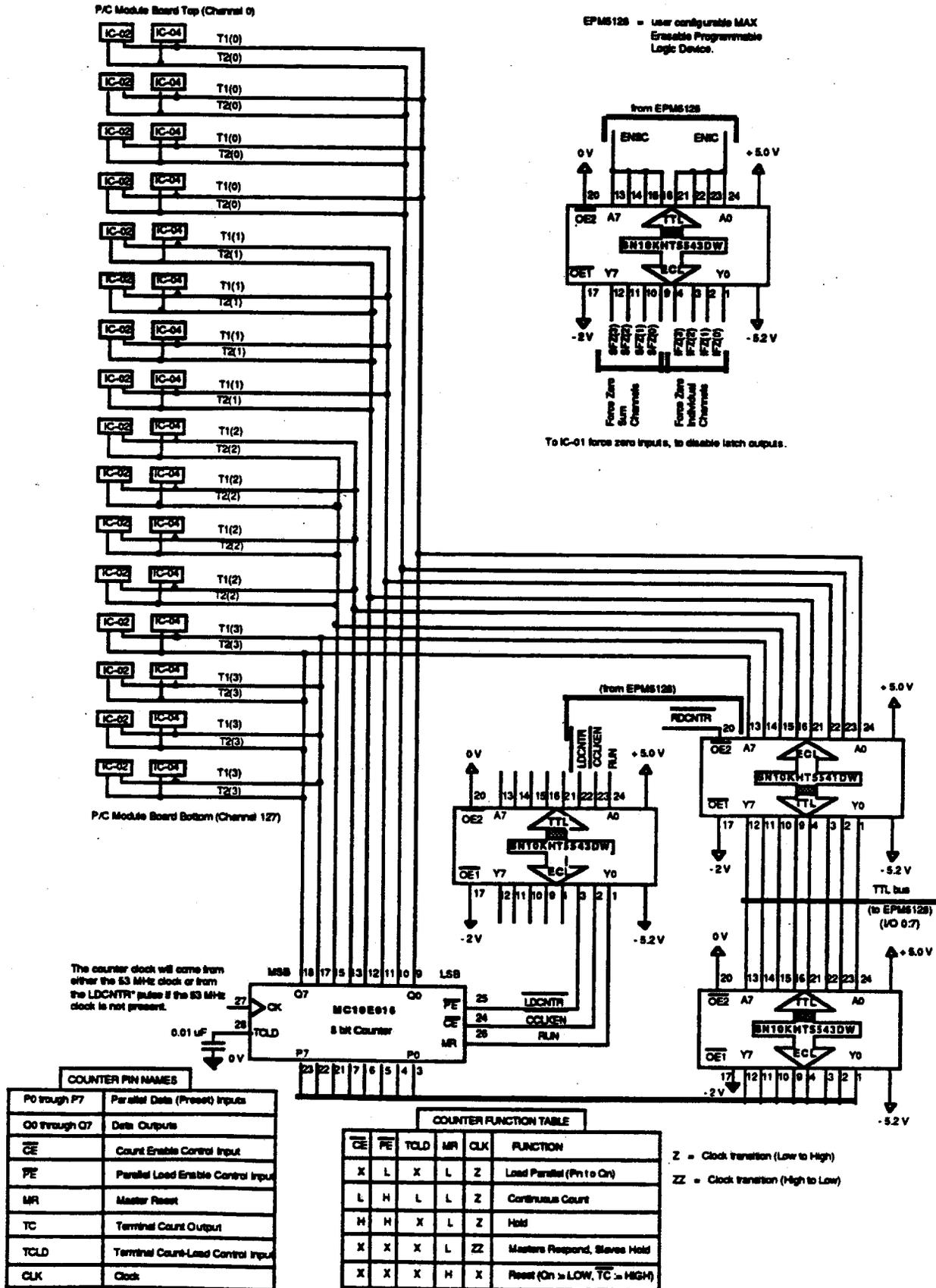


Figure 20: Test Counter Circuitry