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ABSTRACT

In order to improve the stability of the Fermilab Booster low level rf system, a numerically controlled oscillator system is being constructed. Although the system has not been implemented to date, the design is outlined in this paper. The heart of the new system consists of a numerically synthesized frequency generator manufactured by the Sciteq Company. The 3 GHz/sec rate and 30 to 53 MHz range of the Booster frequency program required the design of a CAMAC based, fast-cycling (1 MHz), 65K X 32 bit, digital function generator. A 1 MHz digital adder and 12 bit analog to digital converter will be used to correct small program errors by phase locking the oscillator to the beam.

INTRODUCTION

The Fermilab Booster is a 200 MeV to 8 GeV Proton accelerator. The machine has a 75 meter radius and a guide field that closely matches a 15 Hz biased sine wave. With harmonic number 84, the rf frequency sweeps from 30.2 to 52.8 MHz at a maximum of 2.9 GHz/sec. The low level rf system is described in [1] with some of the more recent work in [2]. The system uses a voltage controlled oscillator, or VCO, phase locked to the beam bunches to generate the rf drive signal for the accelerating cavities. This phase lock loop is limited to a closed loop bandwidth of 50 KHz due to cable delay and the finite bandwidth of the accelerating cavities, [3].

The VCO currently being used is described in [4] and is constructed with an ECL oscillator chip tuned with a varactor diode, or voltage controlled capacitor. It has some temperature drift due to the diode voltage drop, and generates a second harmonic which is 20 db below the fundamental. The frequency program is generated with two 12 bit A/D converters arranged in an amplitude-slope configuration and updated at 25 KHz, [5].

The requirements for an improved VCO for the Booster are described below. First the VCO must have a transfer function which is stable to 1 part per thousand or better over a reasonable temperature range and time period. This accuracy will allow the analytic rather than empirical generation of a frequency program. It must be able to track the 2.9 GHz/sec rate, and the modulation bandwidth should be large compared to 50 KHz. The noise level, including harmonics, must be sufficiently small to avoid exciting synchrotron oscillations in the beam.

NUMERICALLY CONTROLLED OSCILLATOR

The numerically controlled oscillator, or NCO, consists of a reference oscillator or clock, phase accumulator, sine wave lookup table, and digital to analog converter or DAC. It works by incrementing the phase accumulator by an adjustable amount each clock cycle. The most significant bits of the result are used to address the sine wave lookup table whose output programs the DAC. For an N bit accumulator the frequency output for a phase increment of m and clock frequency f_{ck} will be $f_{ck} * m / 2^N$. The NCO used was manufactured by the Sciteq Company and uses a 70 MHz clock generated from a precision 10 MHz oscillator, a

29 bit accumulator, an 8 bit lookup table, and an 8 bit DAC. The stability and precision of the NCO is tied to the reference oscillator which is roughly good to a few parts per million. According to Shannon's sampling theorem a frequency of 1/2 the clock, or 35 MHz, could be generated. A frequency doubler followed by a 30 to 53 MHz filter are used to generate the Booster's frequency range. The 29 bit digital input to the NCO provides a resolution of $70\text{MHz} / 2^{29} = .13$ Hz. The NCO can switch frequencies in a phase continuous manner with a transient response of less than 100 nsec.

Sources of error in the output include the amplitude quantization error of the DAC, DAC glitch error, and phase quantization noise. The phase quantization noise is determined by the size, or resolution, of the sine wave lookup table. These frequencies will mix with the clock harmonics producing lines at $f = f_{ck} * (n \pm m / 2^N)$. The amplitude of these lines will follow the familiar $\sin(\pi f / f_{ck}) / (\pi f / f_{ck})$ frequency dependence. Most of the unwanted frequency components can be filtered out, however, nonlinearities will cause some of the energy to be folded into the frequency range of interest. The amplitude of these spurious frequencies, for a good DAC, are typically the order of digitizing errors or 2^N times smaller than the fundamental. For the particular NCO in question they are measured to be less than -43 dbc.

There is some concern about exciting synchrotron oscillations with these spurious lines when the frequency coincides with one of the family of synchrotron lines. However, since the spurious lines sweep at different rates with respect to the fundamental the average energy given to any one synchrotron line should be much less than the -43 dbc number. In addition experiment has shown that, for the Booster, 10% modulation is required to excite the beam in a significantly short period of time.

DIGITAL FUNCTION GENERATOR

The design of a fast-cycling digital function generator has been a critical element in the realization of an improved Booster low level rf system. The generator, implemented as a one-wide CAMAC module, provides 128K x 16 bits of on-board, battery-backed, static RAM. For the Booster application, this memory is organized as a single 32 bit output function of up to 65K words in length with the output word updating at a 1 MHz rate.

The widely implemented 10 MHz Tevatron Clock, [6], is directly interfaced on the module. This clock, with its frequency servoed to the periodicity of the Booster, provides the update interval for the function record. Encoded clock events provide accurately referenced start times for the programmed function. Output words, with an update pulse, are generated in direct synchronization with the applied clock. The first point of the function table is available 1.9 usec (± 50 nsec) after recognition of a starting clock event. The end of function is realized by either the overflow of the program address or by recognition of a unique stop code in the output data.

A noteworthy property of the generator module is the ability to service CAMAC read and write operations

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to the memory while the module is actively providing a digital program. This is accomplished by a three-fold division of the 1 usec update interval. The first and second sub-intervals are dedicated to reading from memory the upper and lower 16 bit words of the 32 bit output. These words are loaded into internal holding registers. During the third sub-interval, CAMAC operations are processed. Also during this last interval, the contents of the holding registers are synchronously transferred to the output register for clocking to the external digital summation circuits.

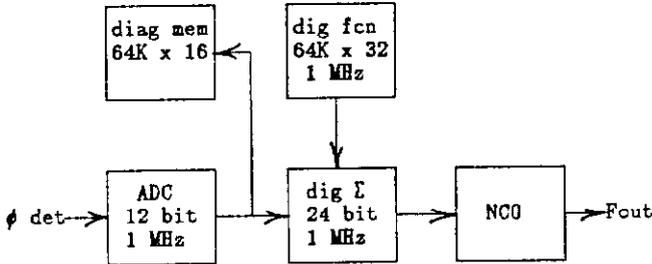


figure 1. Block diagram of NCO system.

IMPLEMENTATION

Tests done with the existing VCO indicate the frequency program is repeatable, assuming a perfect biased sine wave for the momentum, with an accuracy of 70 KHz. The program is repeatable, at least through a several hour period, to a few KHz. This allows the frequency range of the phase detector error to be less than the 20 MHz range of the program making it possible to use a 12 bit ADC.

The Sciteq NCO used has 29 bits of digital input providing a frequency resolution of .13 Hz. In an effort to balance the source of errors and to allow a reasonably sized program memory, only 20 bits are used. This provides a 66.8 Hz resolution. With the 12 bit error aligned on the least significant 12 bits of the program, the error range becomes ±137 KHz. If the digitizing error is approximated with a sine wave with the same amplitude, its effect can be estimated. For small amplitude FM modulation a close approximation of the sideband amplitude is $\Delta f/2f_m$, shown below.

$$\frac{1 \text{ 66.8Hz}}{2 \cdot 2 \cdot 1\text{MHz}} = -95.5 \text{ dbc} \quad (\text{resolution}) \quad (1)$$

$$\frac{1 \text{ 2.9GHz} \cdot 1\text{usec}}{2 \cdot 2 \cdot 1\text{MHz}} = -62.8 \text{ dbc} \quad (\text{program rate}) \quad (2)$$

A more rigorous approach using the fourier transform of the digitizing error would reveal sidebands at multiples of 1 MHz, however, the amplitudes of the first few are not significantly different from the above. These amplitudes should be compared to the measured -43 dbc worst case sideband amplitude of the NCO. Note that the frequencies will be multiples of 1 MHz from the fundamental compared to 25 KHz in the old system. The 1 MHz rate of the 12 bit ADC is faster than the 50 KHz bandwidth of the Booster frequency loop. However, the ADC will introduce an additional 1 usec delay which will reduce the stable bandwidth slightly.

IN THE FUTURE

The existence of the highly accurate frequency program in digital form, at the input to the NCO, can make improved diagnostic equipment possible. As an example, a digital signal processing chip could generate a program for a second NCO which tracks any rotation harmonic. This would allow real time measurements of the amplitudes of the coupled bunch instabilities. Two NCO's could be programmed in quadrature allowing much simplified circuitry to control the rf accelerating phase. In addition, a digital VCO opens the door for the use of DSP chips for the rest of the low level system. This would allow optimizing the loop bandwidths as a function of energy, passing through transition in more graceful ways, improving the capture of beam into bunches, and improved methods of phase locking accelerators. All of these functions could be cast in software making it possible to drastically change accelerating modes on a cycle by cycle basis. As these systems become cheaper to reproduce, it would be practical to have one at each rf cavity making it possible to increase the bandwidth of the frequency loop and possibly damp some of the higher order synchrotron oscillations or instabilities.

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