

**Fermilab**

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AMPLIFIER DISCRIMINATOR MULTIPLEXOR CARD

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## ADM CARD

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This T.M. describes the Amplifier-Discriminator-Multiplexor (ADM) card designed for the External Muon Identifier at the 15ft. Bubble Chamber. The E.M.I. consists of 5 planes of 1" square double-extrusion proportional tubes, very similar to the ones built by M.I.T. for E-594; these planes are typically 22 ft. long and 12 ft. high. They are located behind several feet of zinc, lead and iron, and serve to identify muons. They are designed to act as a hodoscope with a spatial resolution of about 1/2 an inch and with a time resolution of 1 micro-second. The spatial resolution is well matched to the multiple scattering suffered by muons produced in neutrino interactions in the Bubble-Chamber and the time resolution allows the one to two millisecond fast spill to be resolved into over a thousand time slices which, again, is quite adequate. The ADM card was largely designed by Sten Hansen.

The general scheme of the data read-out of the E.M.I. is based on the use of a master clock. The Time Digitizing System generates a 16Mhz TTL master clock which is sent (600 feet) to the E.M.I. The ADM card serves to amplify the signals from the proportional tubes, discriminate them, latch the signals in parallel into a shift register. The data is then shifted out serially to the Time Digitizing System, using the master clock.

1

Time Digitizing System, Nanometrics #N280

The shift registers are loaded, and the latches are reset once every sixteen cycles of the master clock. See fig. 1 for block diagram of the ADM Card. Each card serves 15 channels and multiplexing the data from several channels onto a single output cable reduced the number of signal cables between the chambers and the Time digitizing System by a factor of 15.

The fifteen channels of the ADM card can each be divided into 8 subsections. With the first 3 subsections making up the low level analog amplifier section, and the last five making up the high level digital section. The subsections from signal in to data out are:

Impedance Matching, Transistor Pre-Amp, Video Amplifier, Discriminator, Fast-OR, Set-Reset Latches, Parallel to Serial Data Conversion, and Line Driver and Signal Shaper.

## LOW LEVEL ANALOG AMPLIFIER SECTION

### INPUT IMPEDANCE MATCHING

The signal from the wire is capacitively coupled using a 3 kv 1000 pf capacitor. A 330 ohm resistor along with a 2N5770 as a common base amplifier, are then used to match the characteristic impedance of the wire. The 2N5770 carries a quiescent collector current of 0.4 ma. giving an  $R_{be} = \frac{25}{0.4} = 62$  ohms. A 1N914 diode is used for transient protection (Fig. 2). This section also performs as a highpass filter, see A, graph 1 for calculated frequency response.

2

P. 66 Horowitz and Hill; The Art Of Electronics.

### TRANSISTOR PRE-AMP

The signal then goes to a common emitter amplifier (fig. 2), which provides a voltage gain =  $-R_c/R_e$ , and inverts the signal. This 2N5770 carries a quiescent collector current of 1.05 ma, giving it an  $R_e$  of  $25/I_c(\text{ma}) \sim 23$  ohms. The  $R_c$  is frequency dependent and can be calculated according to fig. 3. The calculated gain as a function of frequency is represented by B, graph 1.

### VIDEO AMPLIFIER

The signal is capacitively coupled with a 0.1 uf capacitor to a differential input video amplifier (LM733C), to isolate the input of the LM733C from the dc bias of the transistor pre-amp. (fig. 2). This capacitor, along with the 1.2k and 2.2k resistor, the 1000 pF capacitor, and the input resistance of the LM733C, also functions as part of a bandpass filter, see C, graph 1. The 1000 pf capacitor to ground was added in the field to help reduce noise pickup from the TTL logic section of the card. The LM733C with the 10k pf capacitor across pins 11 and 4, provides a gain response which also varies with frequency (D, graph 2). At high frequencies, the gain is nominally 400, although the specs for the LM733C vary from 250 to 600. The differential output is capacitively coupled using 0.1 uf capacitors, again to remove the possible differences in the DC biasing levels between the outputs of the LM733C and the inputs of the NE521.

The overall calculated gain of the low level analog section as a function of frequency is represented by E, graph 3. The gain

reaches a maximum of  $\sim 850$  at about  $0.35$  Mhz and falls to  $1/2$  its peak values at  $0.102$  Mhz and  $0.9$  Mhz.

## HIGH LEVEL DIGITAL SECTION

### DISCRIMINATOR

$1/2$  of an NE521 is used as a differential comparator (discriminator). The threshold voltage, after a division of 11 on the card, is set typically to  $-1.3$  volts, which corresponds to  $2.6$  mv input voltage or  $6$  ua peak input current. The output (TTL bar) goes to both the Fast-OR section and the Set-Reset Latches section.

### FAST-OR

A fast-OR is built into the system to allow the E.M.I. to be used as a trigger (for example, for the laser holography flash).

$1/4$  of a 74LS09 is used as an "OR GATE" for negative logic. The open collector output enables it to be wire-ored with the other 15 channels. The data is then converted from TTL bar to NIM for the fast OR output (fig. 4A). A jumper is used to connect to one of the 4 possible FAST-OR output connections on the 50 pin card edge connector.

### SET-RESET LATCHES

The data to be sent to the time digitizing system is stored in the Set-Reset Latches. The Latch consists of  $1/4$  of a 74LS279 which inverts and stores the data for the Parallel To Serial Data Converter. After the data is loaded into the Parallel To Serial

Data Converter, a TTL bar pulse resets the latches . Since the pulses from the discriminator have a minimum width of 200 ns, the fact that data received by the latches during the Load and Reset pulse (50 ns) is ignored does not matter.(figure 5.)

#### PARALLEL TO SERIAL DATA CONVERTER

Two 74LS165'S are used to convert the parallel data from all 15 channels to a serial data stream of 16 bits. Pin 6 on U29 (bit 16) is tied high to provide a fiducial . This fiducial is crucial and is used to check that the serial data has the correct phase at the T.D.S. The data is loaded from the 15 data channels into the shift register when the load pulse is received (TTL bar). The data out of the shift registers is TTL (fig. 5).

#### DATA LINE DRIVER AND SIGNAL SHAPER

The data stream then goes to a transistor pair line driver. A single pole high pass filter is used to shape the signals, to compensate for the dispersion in the 600 feet of RG58 between the E.M.I. and the counting room. (fig. 6).

The data pulses are ~60ns wide. After transmission down 600 feet of RG58, their shape is badly distorted. (See photo 1).A more serious problem is the dc pile-up proportional to duty cycle (%on time). This offset makes it impossible to restore the signal at the receiving end with a simple discriminator. A

3

The TDS is designed to normally ignore the 16th bit of data. on each cycle - thus avoiding the problem of filling its buffers with the fiducial pulse. Any phase error results in a vast number of fiducials appearing in the data and immediately is signalled by an excessive number of apparent hits in the EMI.

threshold that functions properly for a 10% duty cycle pulse would be on continuously for a 50% duty cycle pulse.

The cable losses which are a function of frequency can be approximated by a single pole low pass filter. A single pole high pass filter is therefore used as compensation at the output. This compensates nicely for the frequency dependence of the transmission cable, and effectively eliminates any duty cycle dependent dc offset. (See photo 2).

#### GROUND PLANES

The ADM card essentially has two ground planes. The low level analog ground plane (fig. 7a), and the high level digital ground plane (fig. 7b). The ground planes were separated to isolate the low level analog section from the ground noise characteristic of the TTL circuits. The low level analog ground plane is connected by copper mesh and four screws to structural ground. The high level digital ground plane is connected to the power supply ground through the 50 pin card edge connector. While the two ground planes are separated for high frequencies, they are connected in one place to ensure the dc potentials are the same.

#### POWER AND CONTROL SIGNALS DISTRIBUTION

The power and control signals are bussed along the top of the E.M.I. extrusions. The power, ground and threshold are on 1/2 inch brass buss bars. The clock, load and reset and fast-or outputs are carried along a pc board buss, which was made on the gerber machine in lab 8. The power and control signals are

supplied via a cross-over card and 50 pin card edge connector and cable.

+8V and -8V are supplied through the 50 pin card edge connector. +8v goes to two 7805 voltage regulators, and -8v goes to two 7905 voltage regulators, which supply +5v(a) and (b) and -5v(a) and (b). The +/- 5v(a) supplies power for the low level analog section, while the +/-5v(b) supplies power for the high level digital section.

CLOCK, LOAD, RESET, and THRESHOLD are provided via the 50 pin card edge connector (fig. 4). The CLOCK, LOAD, and RESET signals are TTL bar signals, which are buffered on the ADM board with transistor pair line receivers. Fig. 4b is an example of one set of line receivers. The CLOCK and LOAD signals go to the Parallel to Serial Data Converter section. The RESET signal goes to the Set-Reset Latches section (fig. 5). THRESHOLD is a voltage level, controlled from the experiment counting room which is applied to the Discriminator section.

#### SUMMARY

I have described the Amplifier Discriminator Multiplexor used on the new E.M.I. About 2300 channels were used in the last run. Apart from some noise pick-up in the field - we had not seen in the lab - the board functioned reliably. In particular the multiplexing scheme worked well and allowed a considerable savings in cables and cabling complexity.

ADM BLOCK DIAGRAM

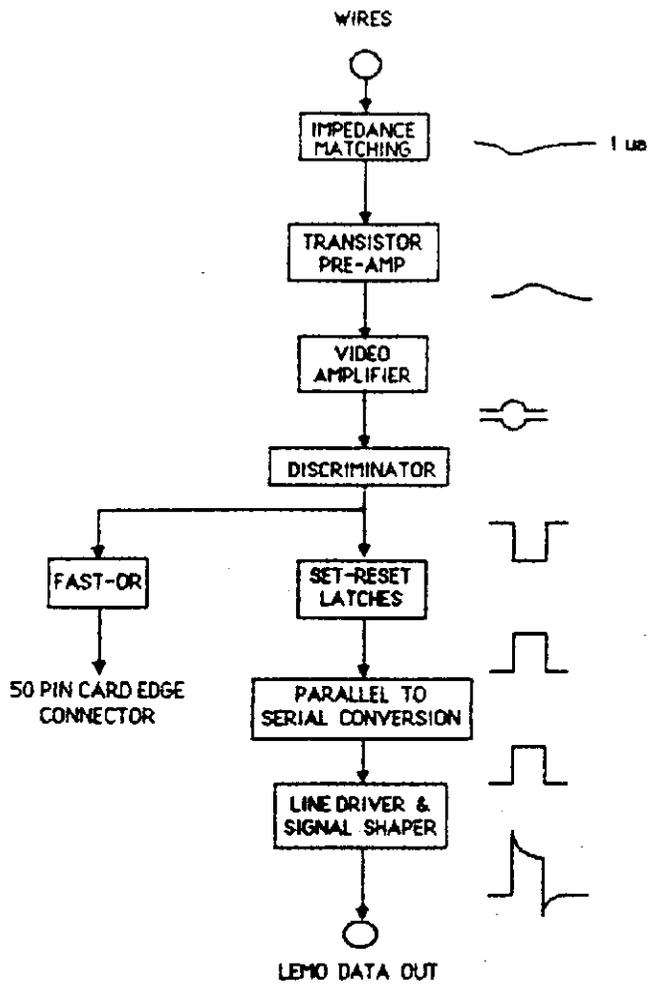
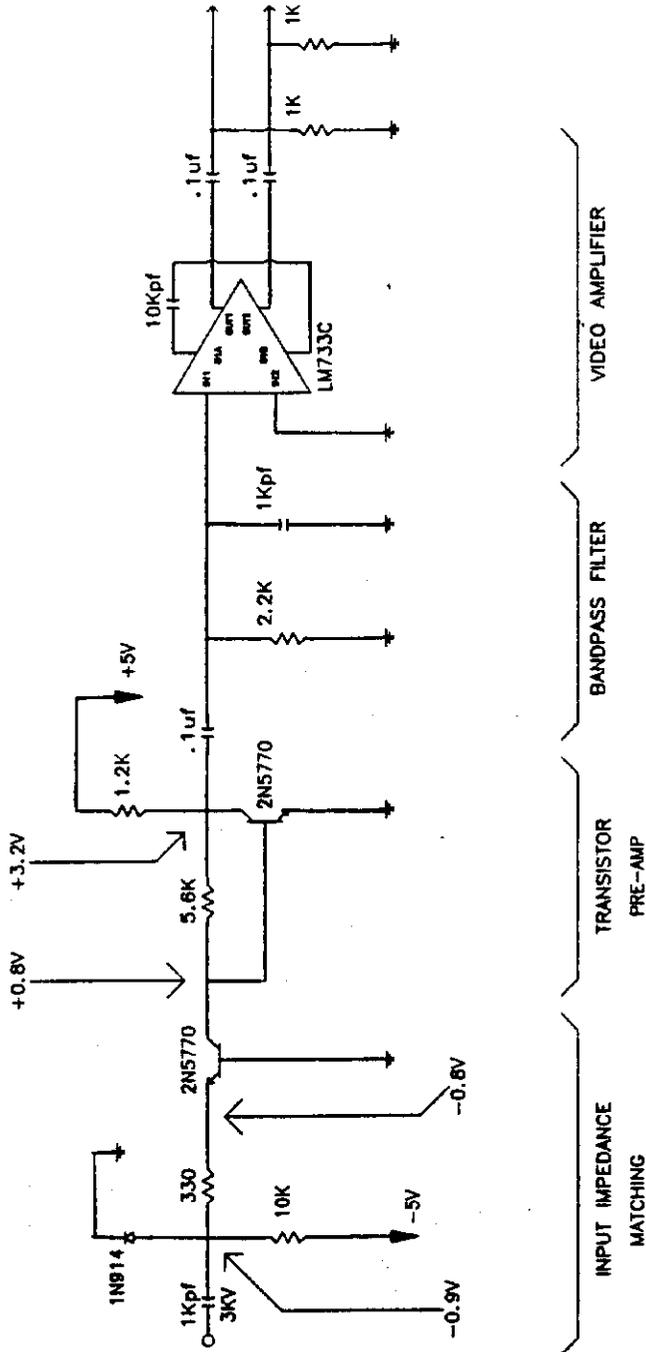


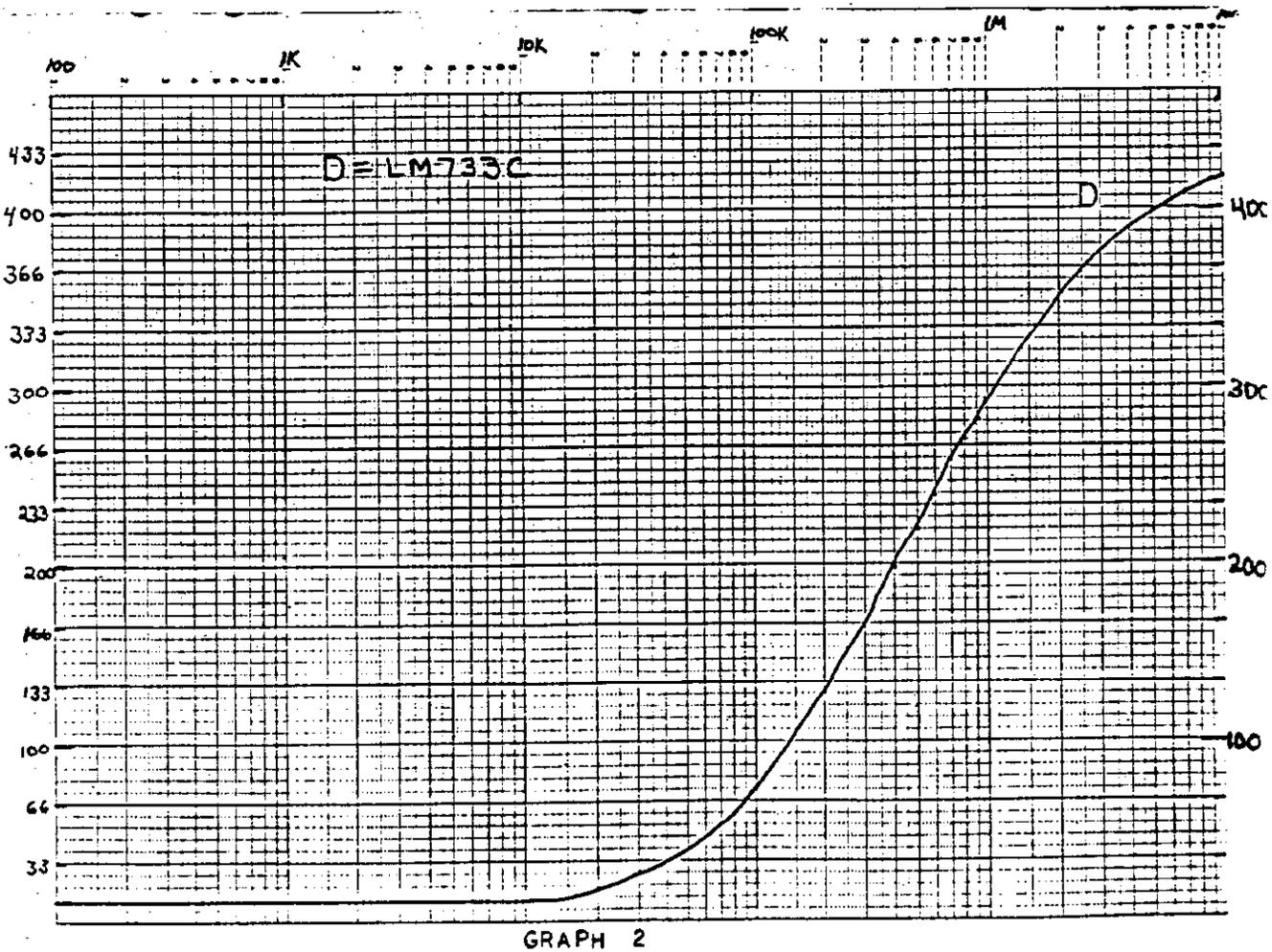
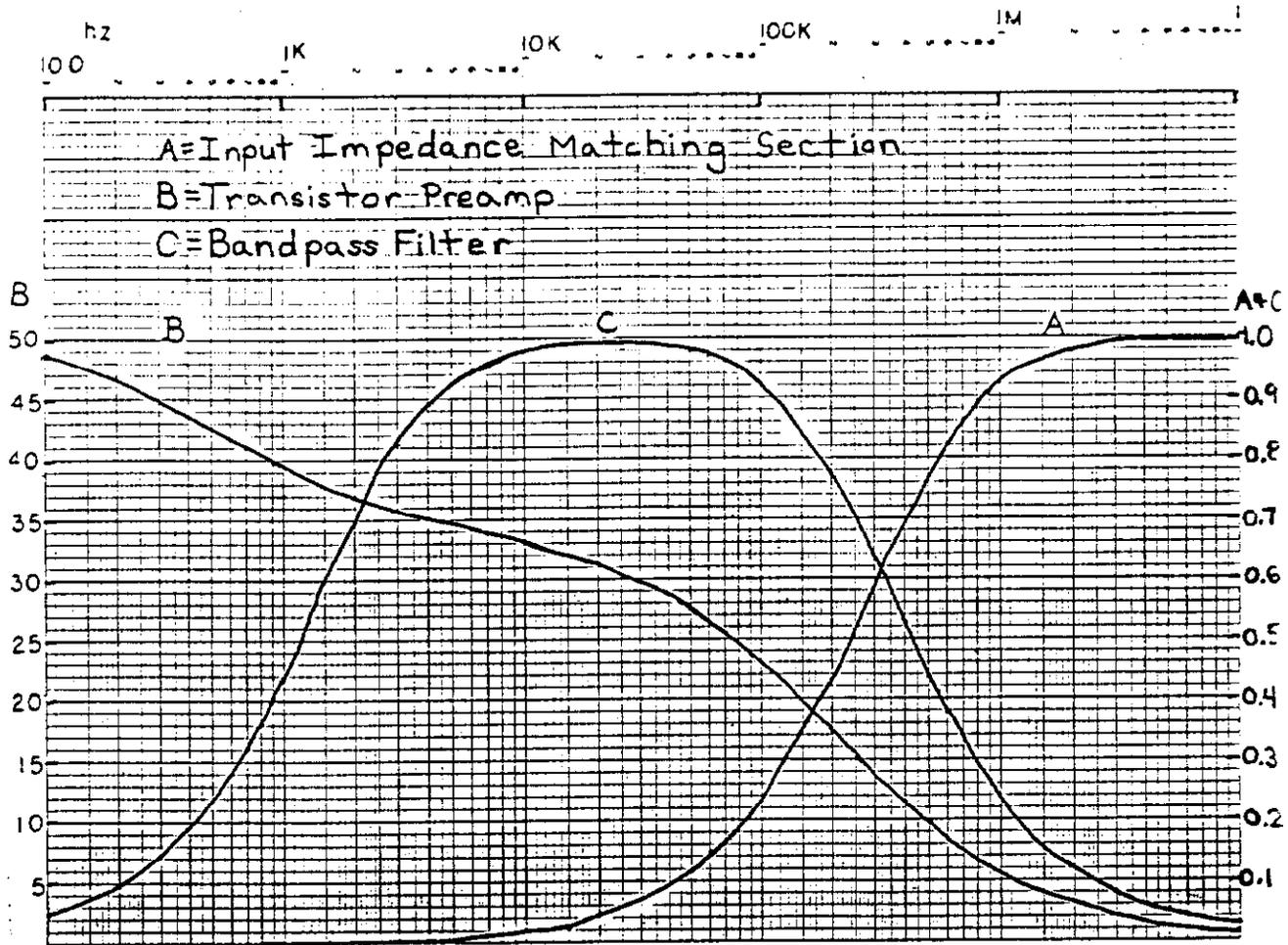
FIG. 1



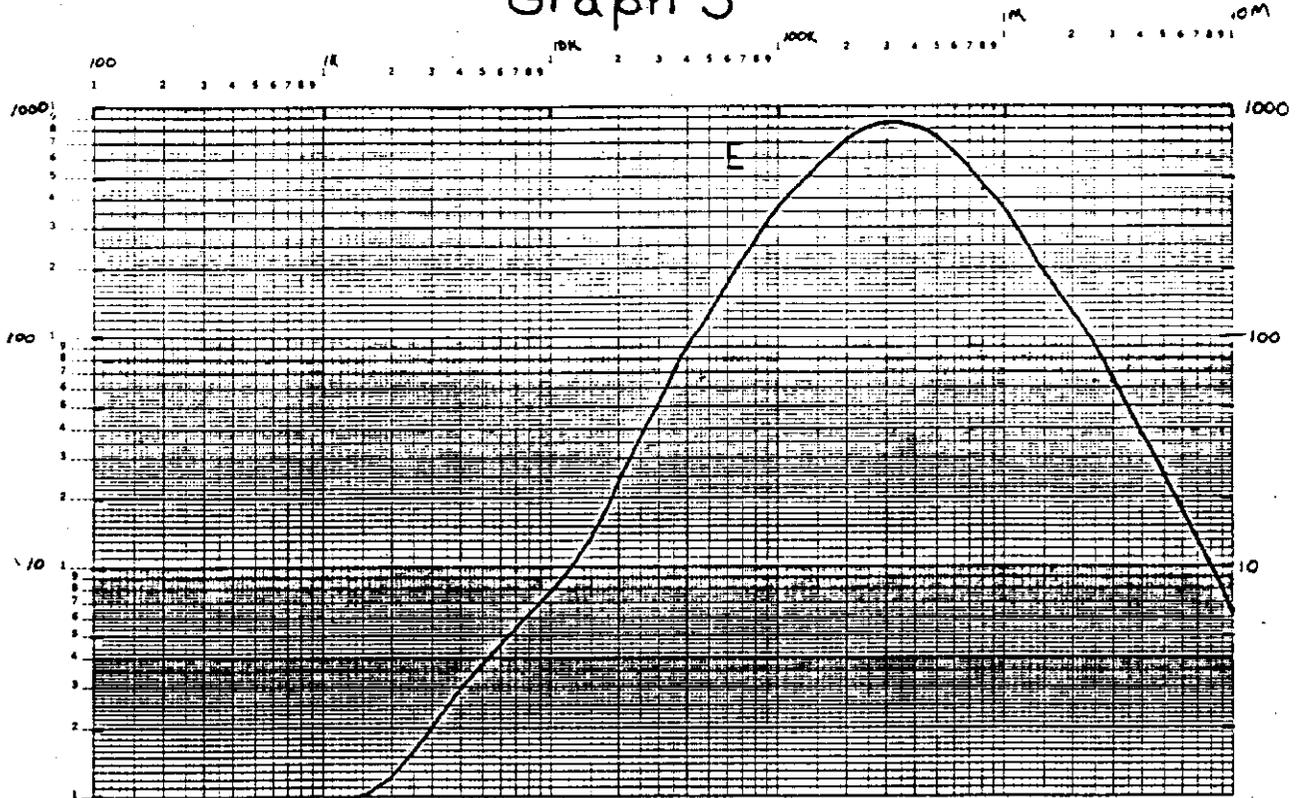
9

ORIGINATOR	STEN HANSEN
DRAWN	D. GRAUPEMAN
CHECKED	
APPROVED	
	
FERMI NATIONAL ACCELERATOR LABORATORY UNITED STATES DEPARTMENT OF ENERGY	
EXPERIMENTAL AREAS DEPT. (FSG) EMI AMPLIFIER DISC. MULTIPLEXER CARD (FRONT END)	
SCALE	DRAWING NUMBER
	REV

Fig.2



# Graph 3



**CALCULATED GAIN vs FREQUENCY for LOW LEVEL ANALOG SECTION**  
**AxBxCxD=E**

Fig. 3

### Input Impedance Matching Section

$$A = \text{Gain} = \frac{\omega RC}{[1 + (\omega RC)^2]^{\frac{1}{2}}} \quad \begin{matrix} C = 1Kpf \\ R = 384\Omega \end{matrix}$$

### Transistor Pre-Amp Section

$$B = \text{Gain} = \frac{R_c}{R_E} \quad \begin{matrix} R_E = \frac{25}{I_c(ma)} \\ I_c \approx 1.05 ma \end{matrix}$$

$$R_c = \frac{1}{\frac{1}{1.2K} + \frac{1}{\omega 1Kpf + \frac{1}{2.2K}} + \frac{1}{\omega 0.1\mu F}}$$

### Bandpass filter

$$\text{Highpass Gain} = \frac{\omega RC}{[1 + (\omega RC)^2]^{\frac{1}{2}}} \quad \begin{matrix} C = 0.1\mu F \\ R = 776 \end{matrix}$$

$$C = \text{Lowpass Gain} = \frac{1}{(1 + \omega^2 R^2 + C^2)^{\frac{1}{2}}} \quad \begin{matrix} C = 1Kpf \\ R = 650 \end{matrix}$$

### Video Amplifier Gain (LM733C)

$$D = \text{Gain} = \frac{1.4 \times 10^4}{\frac{1}{\omega C} + 32} \quad C = 10Kpf$$

### Overall Gain for Lowlevel Analog section

$$\text{Gain} = A \times B \times C \times D$$

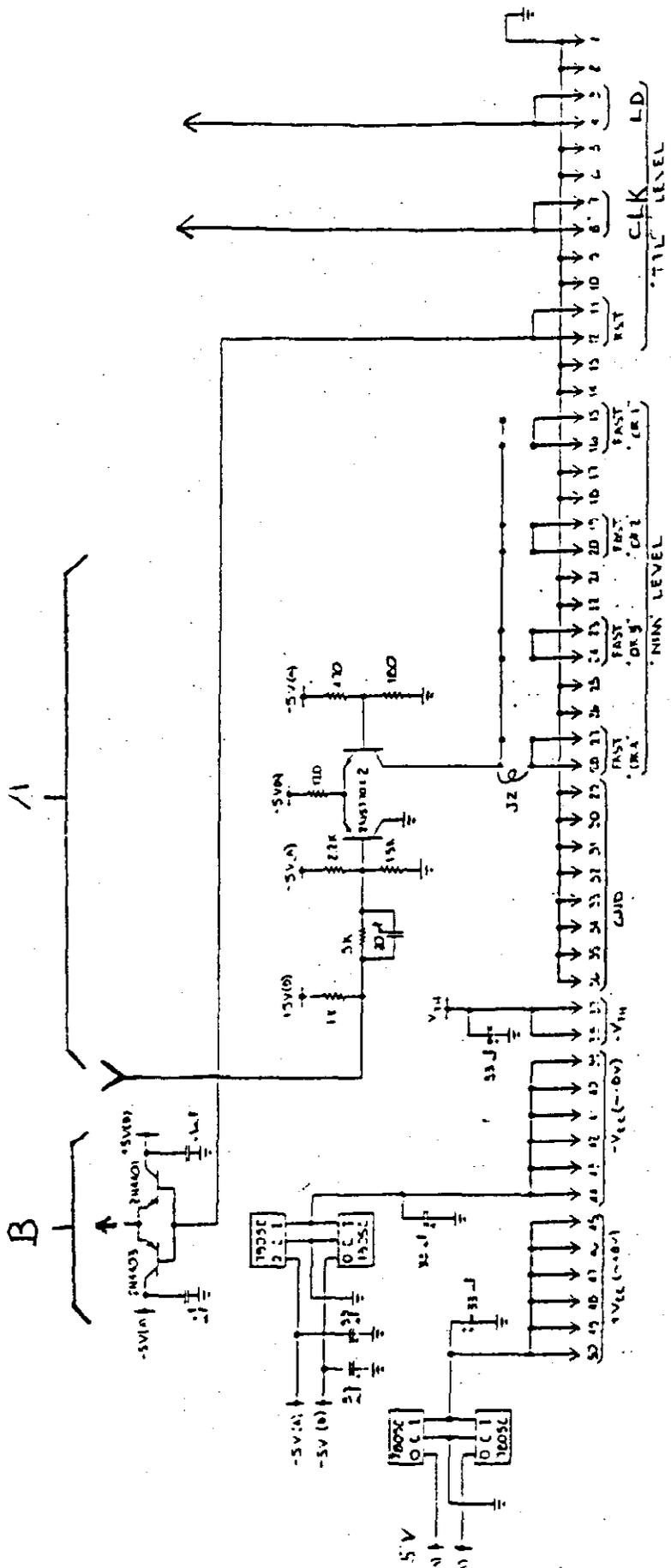
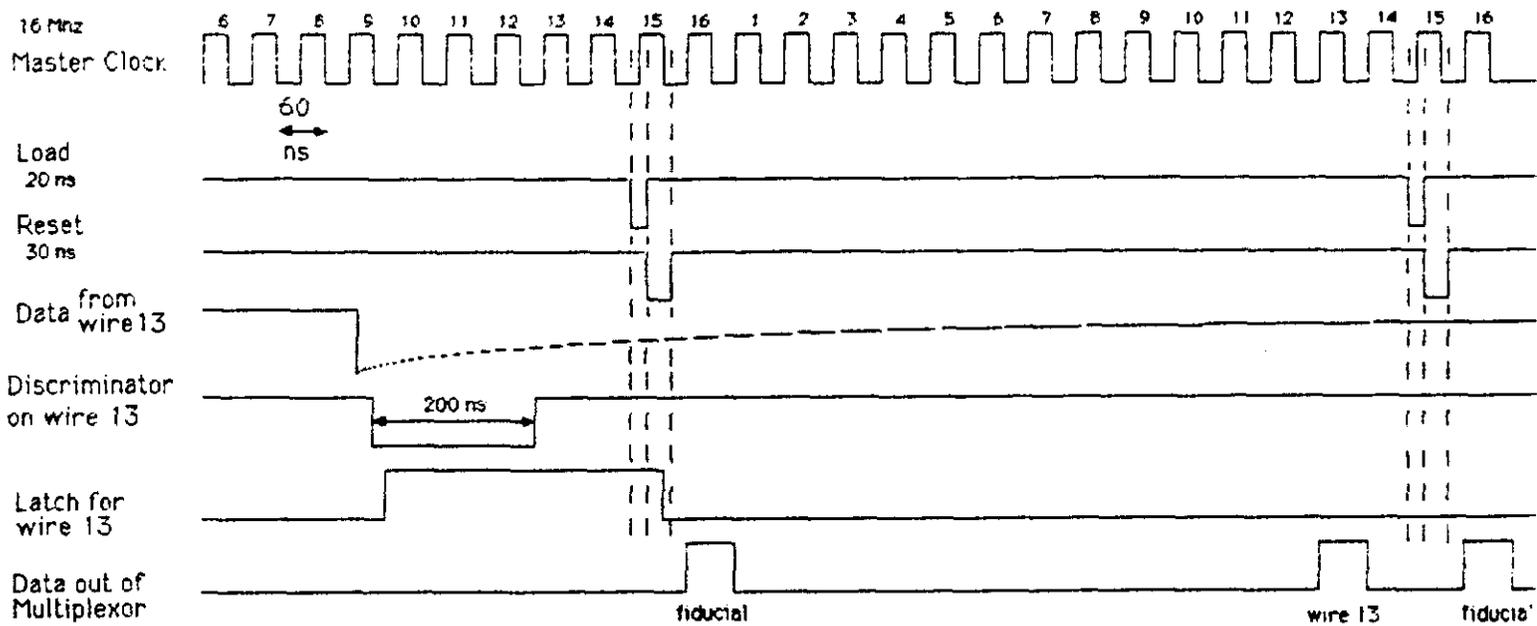


Fig. 4



AMPLIFIER DISCRIMINATOR MULTIPLEXOR

DATA TIMING

FIG. 5

# ADM CARD SIGNAL DRIVING

74LS165 SHIFT REGISTER OUTPUT

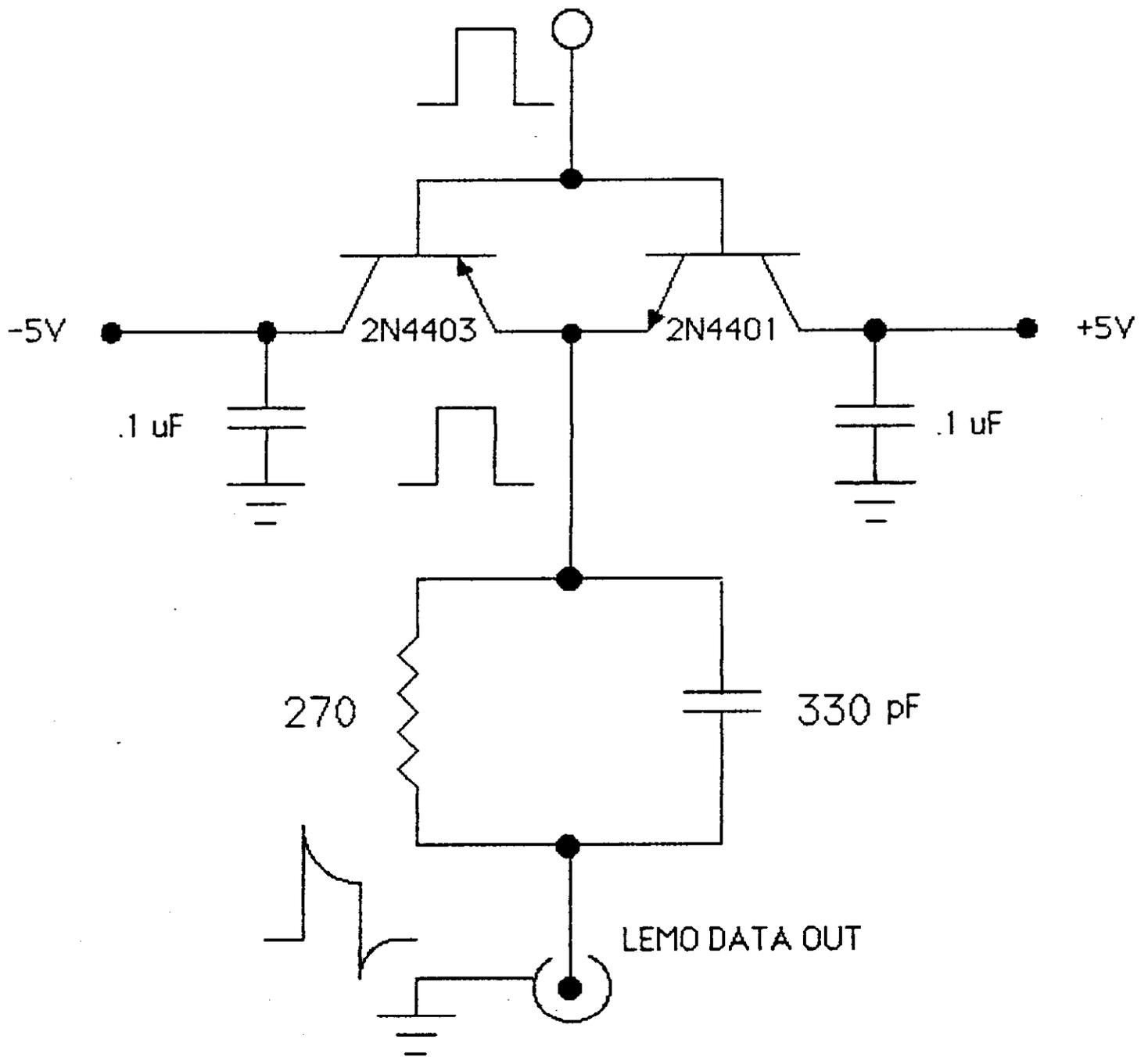
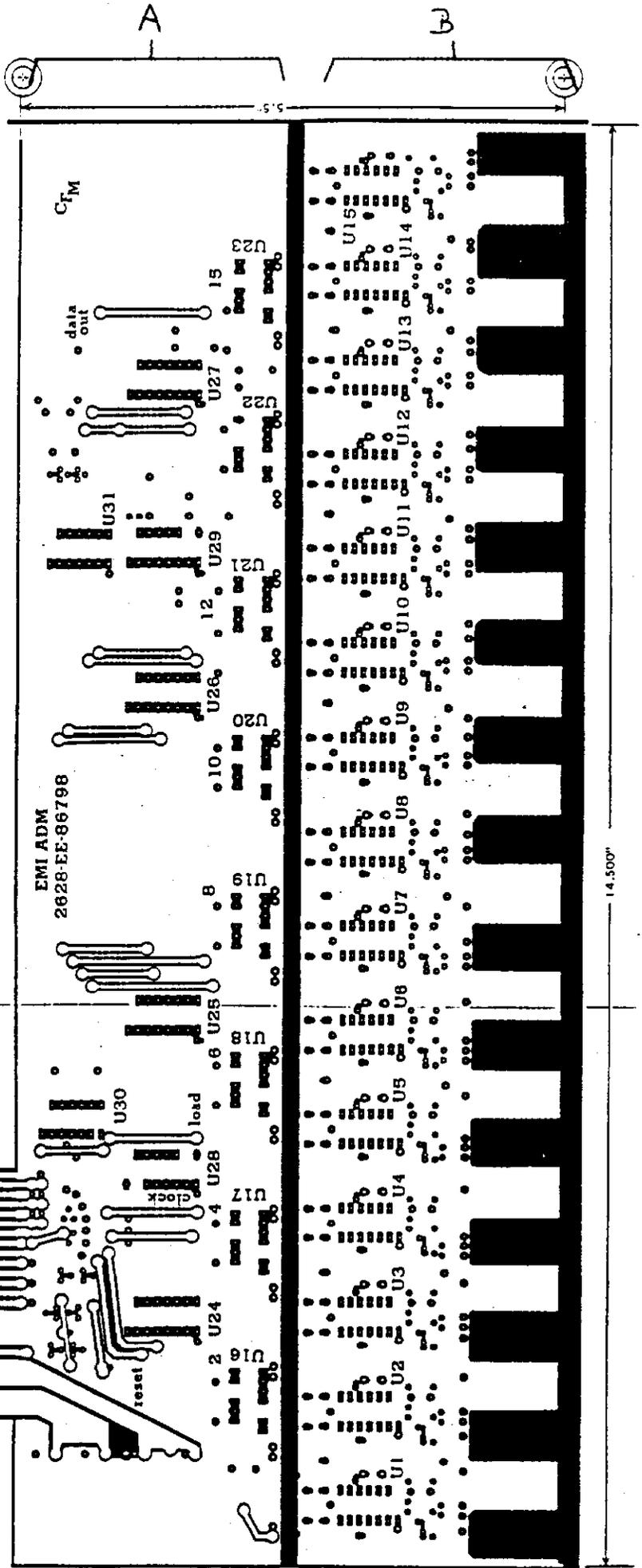


FIG. 6

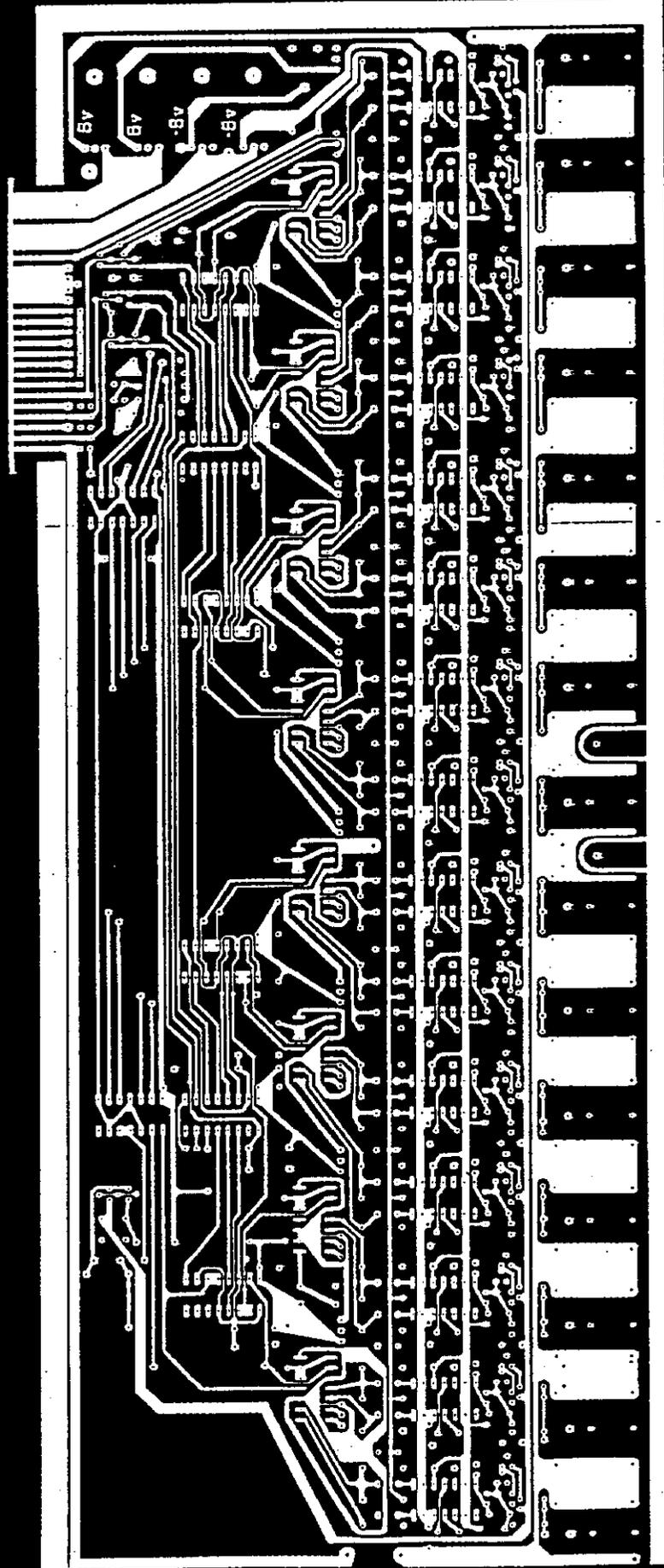
Fig. 7



Top Positive

14.500"

Page 16 of 18



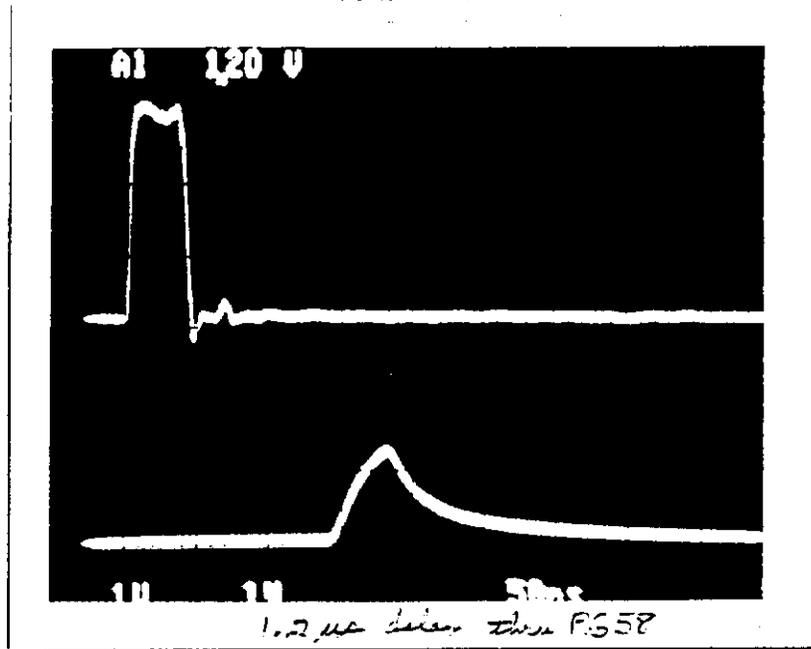


Photo 1

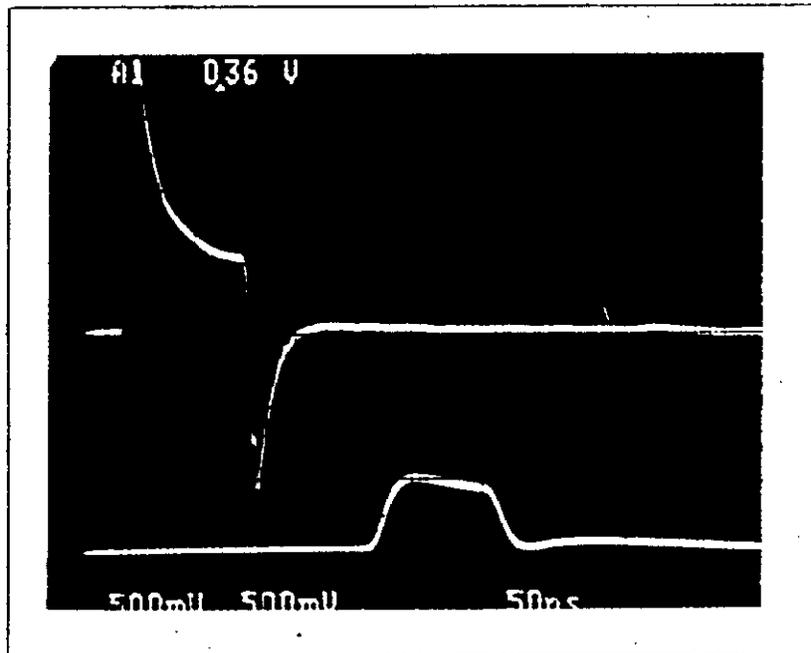
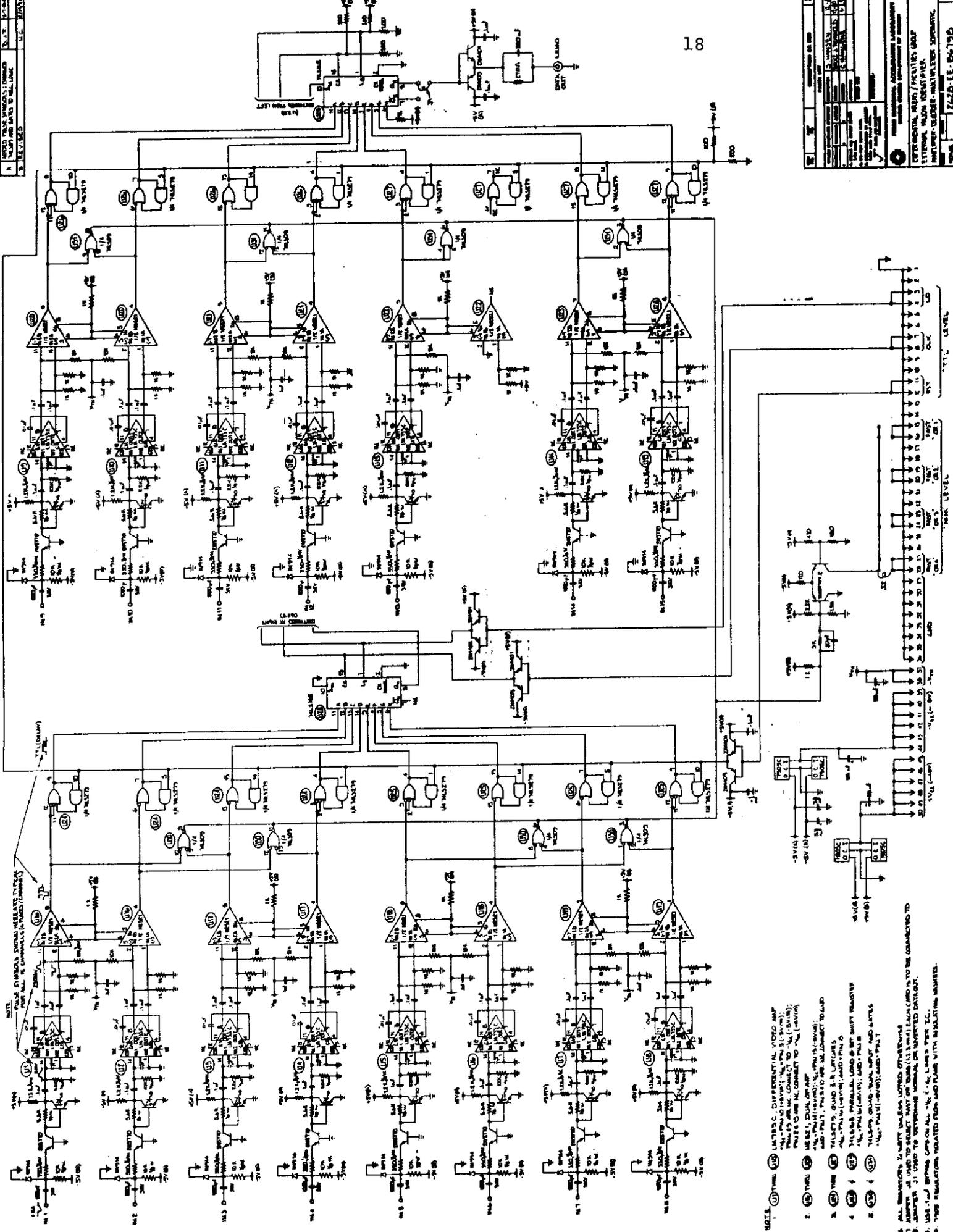


Photo 2

REV	DATE	BY	CHKD
1	10/1/68	J. L. JONES	J. L. JONES
2	10/1/68	J. L. JONES	J. L. JONES
3	10/1/68	J. L. JONES	J. L. JONES

PROJECT	2420-11-00-190
DATE	10/1/68
DESIGNED BY	J. L. JONES
CHECKED BY	J. L. JONES
APPROVED BY	J. L. JONES
LABORATORY	GENERAL TESTS / ANALYSIS GROUP
TEST ROOM	STRONG HALL, COMBUSTION
TEST NO.	2420-11-00-190
TEST DATE	10/1/68
TEST ENGINEER	J. L. JONES
TEST TECHNICIAN	J. L. JONES



- NOTE: PIN SYMBOLS SHOWN HEREIN ARE FOR ALL COMMONALC (MIL/COMM)
1. ALL INVERTERS: 2. W/RY UNLESS NOTED OTHERWISE
  3. JUMPER: 3. USED TO SELECT THAT OR "BANK" (1, 2, 3, 4) EACH CHIP IS TO BE CONNECTED TO
  4. JUMPER: 3. USED TO TERMINATE NORMAL OR INVERTED DRIVER.
  5. USE 1.0 OHM CAPS ON ALL "1" & "0" LEADS PER I.C.
  6. "0" LEADS: TERMINATION RELATED FROM AND NAME WITH INSULATING TAPE.
1. (1) TRIMMER (2) UNITS: 3. DIFFERENTIAL WORD AMP  
 4. 1.0 OHM CAPS ON ALL "1" & "0" LEADS PER I.C.  
 5. USE 1.0 OHM CAPS ON ALL "1" & "0" LEADS PER I.C.  
 6. "0" LEADS: TERMINATION RELATED FROM AND NAME WITH INSULATING TAPE.