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ELECTRONICS FOR DAMPING TRANSVERSE INSTABILITIES FOR THE FERMILAB BOOSTER SYNCHROTRON

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Introduction

Transverse instabilities are controlled by an active beam damper which corrects the orbit of individual proton bunches in the Fermilab booster synchrotron. The corrective signals, which are in reality processed versions of the beam pick-up data, are applied to the beam via power amplifier/deflector electrodes approximately one turn after sensing the bunch position. The electronic systems of the damper are configured as a closed-loop feedback arrangement wherein the beams dynamical quantities act as the systems input while the output is produced by active signal processing of input data by the damper electronic components.

A unique feature of the described damping electronics is that the feedback loop delay time is continuously adjusted such that the arrival time of the deflector signals correspond on a one-to-one time basis with the specific bunches needing orbit correction. Control of the loop delay throughout a machine β variation of 0.57 - to - 0.99 is achieved with 2.7 ns resolution over a 1400 ns variable delay range. A 9 bit digital delay controller adjusts the delay during each machine cycle.

The described beam damper operates with beam intensity variations of 30 dB, repetition rate variations approaching one octave (30-to-53 MHz), and with bunching related beam pulse half-width variation of 12-to-2 ns.

This paper presents a brief outline of the overall damper system configuration and contains a description of the beam position detector, coaxial cable delay system, and data receiver.

Information relative to other damper sub-systems is contained in separate papers[1].

Damper System Configuration

The booster damper block diagram is shown in Figure 1 with its sub-system elements. The control loop signal processing begins at the position pick-up electrodes, S, while the principal processing (synchronization, sampling, holding, normalization, and scaling) takes place in the position detector. Signals developed by the position detector are transmitted through the coaxial cable delay system, power amplifiers and terminate at the output end of the stripline deflector electrodes, TD, Figure 1.

A one turn delay, DL, is included in the data transmission path to permit the deflector signals to be time correlated with corresponding beam data at the deflectors. The fields of the deflection electrodes, TD, are polarized to force off axis bunches to return to the beampipe axis. The power amplifiers, PA, have a bandwidth of ~150 MHz, can deliver as much as 160 V-PK per pair to the deflectors and are ac coupled permitting the equilibrium orbit to move about somewhat without significantly reducing the control loop dynamic range.

The delay control logic signals are developed from a single input, the boosters low-level rf signal. The logic and control signal serves two functions in the control loop, (1) it controls nine series connected rf switches in a coaxial delay system and (2) it activates two transmission gates in the loop, each designed to discriminate against spurious transients and noise. These transmission gates, TG, can also be controlled by external application of TTL, or NIM logic format control signals for diagnostic and test purposes.

The damper feedback loop of Figure 1, automatically becomes active (closed loop) when the beam bunch signal at, S, exceeds a 300 MV peak threshold level. This threshold and the associated processing sensitivity of the position detector, permits the damping process to begin early in the booster cycle - adjust after injection and during the early phases of beam bunching. Damping occurs over 98% of the booster cycle for the 300 MV thresholding level.

At extraction, the beam input signals drop below the position detector threshold causing the damping loop to open and the damper awaits subsequent beam injections to force the above process to repeat.

The loop forward gain, between position detector output and deflection electrodes is 46 dB maximum, and is adjustable over a wide range. The adjustable gain feature aids in establishing total loop gain,(including the per turn contribution) which in turn sets the closed loop damping rate and stability characteristics. The damping time constant is typcially less than 200 μsec at maximum gain.

The data transmission path utilizes rf signals to convey the position information through the delay system and to the power amplifiers. An Amplitude Modulation, Double Side Band, frequency division multiplex scheme is used for data transmission. The frequency band between 50 and 850 MHz is used for this purpose. Transverse displacement position data is transmitted on a carrier wave frequency of 250 MHz. Significant sideband energy covers the spectrum between 50 and 450 MHz. The position sense (polarity) data is transmitted on a separate carrier centered at 675 MHz. Significant polarity sidebands extend throughout the 500-to-850 MHz part of the spectrum. A small but important guard band 450-to-500 MHz provides sufficient spectrum width for practical fiters and multiplexers to separate the signals. A signal spectrum, showing the distribution of signal power with frequency for a typical position signal is shown in the photograph of Figure 2.

At the receiver, RCVR, the data is recovered by demultiplexing, demodulation, and amplification. The resultant signals are applied in complimentary form to the power amplifiers and thereafter to the deflectors.

The rationale which requires the rather complex transmission scheme outlined is that the position detectors output signal fidelity must be preserved if bunch-by-bunch operation is to be achieved. The rf carrier technique permits a dc-to-175 MHz position signal spectrum to be transmitted without serious fidelity impairment. In contrast, if baseband transmissions were made over moderate distances, say 600 meters, as is required for delay control and via "moderate cost", 7/8" dia. semirigid coaxial cables, the signal risetime would be degraded beyond 6 ns,[2] the value considered the practical upper boundary for the Booster bunch-by-bunch corrections.

Digital delay and optical storage techniques offering excellent pulse transmission fidelity and delay resolution are equally as feasible as the rf carrier coaxial cable schemes discussed but there were judged significantly more complex and more costly to develop and implement than the described system.

Position Detector

A set of two coplanar signals representing the vertical and radial beam displacements respectively, are developed by the beam bunches and the pick-up electrode assemblies. The position detectors, one required for each plane, receives one set of coplanar electrode voltages and each detector produces two output voltages. These voltages are proportional to beam displacement but neither is functionally related to intensity, rep rate, or beam signal pulse width over the ranges mentioned. One of the developed outputs is used to transmit the magnitude part of the transverse displacement while the second output transmits displacement sense (polarity) data. Figure 3 shows the block diagram of the detector with its four major functional parts, (1) bunch synchronizer, (2) beam sampler, (3) rf processor/normalizer, and (4) output scale factor amplifier.

The bunch synchronizer is designed to keep the gate driver sampling pulses timed to the peak of corresponding beam pulses regardless of the pulse width/rep rate variations. In addition, the synchronizer provides sufficient amplitude limiting and amplification to allow normal operation over a 33 dB beam intensity range. This value represents a 40% margin beyond the design limit specified for the damper electronics. The synchronizer inputs are derived from beam pulse wideners made from hybird junctions and configured as transversal filters. These wideners increase the effective beam width by a factor of two. The wideners aid in minimizing sensitivity effects due to jitter, and in conjunction with the summer, Σ, helps minimize amplitude modulation effects and maintain limiting during intervals of low beam intensities.

Tracking the beam pulse peak is achieved by the adaptive delay control, ADC, which is part of the synchronizer. This circuit is activated by a frequency discriminator driven by the boosters low-level rf and is functionally a variable delay in the sample pulse train path which controls the diode gates, A_G and B_G. Adaptive control of the delay is continuous over a 6 ns range. The ADC circuit keeps the sampling pulse train optimized with respect to the peak of the beam pulses within 0.5 ns throughout the entire range of damper system input variables encountered in the boosters acceleration cycle.

The diode sampling gates, A_G and B_G, together with associated circuitry peak detect and hold the level of each beam pulse for one rf repetition interval, $1/f_{BOOSTER}$ sec. The gates allow bipolar transmission and consist of a matched six diode array, 4 diodes in a bridge configuration for switching and 2 for current steering and switching control. The developed sampled and held versions of each beam pulse linearly modulate separate 317 MHz rf oscillators, effectively converting the peak value of the beam pulses into pulsed rf signals each having about 5 rf wavelets per beam bunch. These rf signals, M_A and M_B, have amplitudes proportional to the peak beam signal obtained by the pick-up electrodes. The signals are processed by the rf processor/normalizer. In the rf processor/normalizer portion of the position detector, the amplitude ratio of the input rf signals, M_A/M_B, is developed and subsequently the phase deviation associated with this ratio is produced by the rf processor. The phase deviations are insensitive to beam intensity variations through a 30 dB range and correctly define the beam position in terms of a phasor which is proportional to displacement. A double balanced mixer configured as a phase detector is used for demodulation and produces the normalized, displacement quantity Vn, at baseband frequencies - dc-to-175 MHz. A more detailed description of a similar rf processor is contained in reference 3.

The beam position detector sensitivity is set by the output scale factor amplifier, X24. This amplifier provides a nominal gain of 24 in the dc/175 MH region, provides a minimum of 20 dB attenuation for harmonious of the 317 MHz processor rf signals, and sets the sensitivity at 0.5 V/mm displacement.

Coaxial Cable Delay System

The damper feedback delay time is adjusted continuously during the acceleration cycle as is required by the changing revolution time of the proton bunches. The method used to secure the variable delay is shown in Figure 4. A group of 9 semirigid, medium diameter, coaxial cables is connected to a group of 9 solid state fast transfer rf switches. These "three legged" switches are designed to connect the applied rf signals which contain the position data directly through the short direct path, In-to-Out, or through alternative paths via any or all of the cables, S_0-to-S_8. The short direct path gives a maximum delay of 10 ns for the 9 switches. As much as 1410 ns can be selected in 2.73 ns increments for alternative routing through the cables. In conjunction with ≈1200 ns of fixed delay provided by a 7/8" diameter coaxial cable, the total delay is sufficient to keep the deflector signals in step with the proton bunches for all conditions of machine acceleration.

The rf switches have 30 dB isolation between any selected signal ports, VSWR <1.5, switching speed <30 ns, switching transients <15 MV peak, insertion loss <2 dB, and power handling capability to 50 MW/50 Ω. In addition, the rf switches provide double 50 ohm back terminations, BT, for the cable ports when the switching control commands the straight-through connection. The back terminations dissipate trapped signal energy in the relatively hi-Q cables quickly and without multiple reflections. A Π pad, E, Figure 4, internal to each switch, provides straight-through path amplitude equalization. The attenuation characteristics of the cable and straight-through paths are equalized to <0.5 dB at the 250 MHz displacement channel frequency for all delay states. The increase in cable loss at the 675 MHz polarity carrier prevents equalization to the same degree and results in some amplitude modulation as delay is varied. This effect is insignificant, however, since the polarity signal is threshold detected at a value much lower than obtained when the largest modulation index exists due to delay programming.

An important feature of the described delay technique is that the spurious intermodulation signal level is at least 30 dB below the peak level of the applied rf signal. This is considered an important achievement since there are 36 diode gates (more than 100 diodes) included in the switching delay path and the transmitted signal components are distributed over an 800 MHz range.

Digital control of the switches is achieved through an 18 line, 100 ohm twisted pair dataway and fan-out. The interface with control logic is through standard ECL logic devices, MC10101 (transmitter) and F9582 (receiver).

Data Receiver/DEMUX

Delayed position information in the form of an AM-DSB frequency division multiplexed wave of 4V P-P amplitude is applied to the data receiver/DEMUX. The block diagram is shown in Figure 5. The DEMUX, consisting of rf hybrid splitters, hi-pass and lo-pass filters separate the input signal spectrum into the displacement and polarity channels as indicated. A short fixed delay, DL, 8 ns nominal, is included in the displacement channel to correct for time skew between the two separated signal paths. Skew correction maintains corresponding displacement and polarity data alignment within 0.5 ns. The displacement signal is processed by splitting it into two equal amplitude components and thereafter switching one or the other component through a detector and to a differential amplifier. Balanced mixers, Π, configured as SPST switches control signal flow to the detectors, AM DET, and to the complimentary differential amplifier, CDA. The switch outputs are applied to linear detectors for full-wave demodulation.

The polarity of the output signals at ports 1 and 2, is dependent on whether the CDA has the input at its + or its - terminal. The CDA input condition is in turn related to which rf switch is commanded closed by the polarity channel signals. For a detected polarity signal above the threshold, V_T, switch A is closed switch B open and detected signals of +, 0, as shown in Figure 5 are applied to the CDA. When the polarity signal is absent due to the beam being on the opposite side of the axis, the detected signal is below, V_T, and the complimentary conditions apply at the input to the CDA. The threshold level, V_T, is set well below the point where amplitude skew can influence the small displacement properties of the displacement channel.

The CDA gain is adjustable, allowing a transmission path of unity gain to be established between the position detector output ports and receiver output port. The bandwidth of the receiver is dc-to-200 MHz. The displacement signal polarity can be switched in less than 3 ns, allowing the receiver output data to follow the individual bunch data developed by the position detector. The overall measured 10-90% rise and fall time, position detector included, for position data is 4 and 4.4 ns respectively, dynamic range is 30 dB, and linearity is better than 5% BSL.

Figure 6 shows a typical position detector signal, 18 bunches at booster operating frequency of 38 MHz (TOP) and the corresponding CDA output signal after delay (BOTTOM). Time skew in this photo is caused by scope cabling under test conditions.

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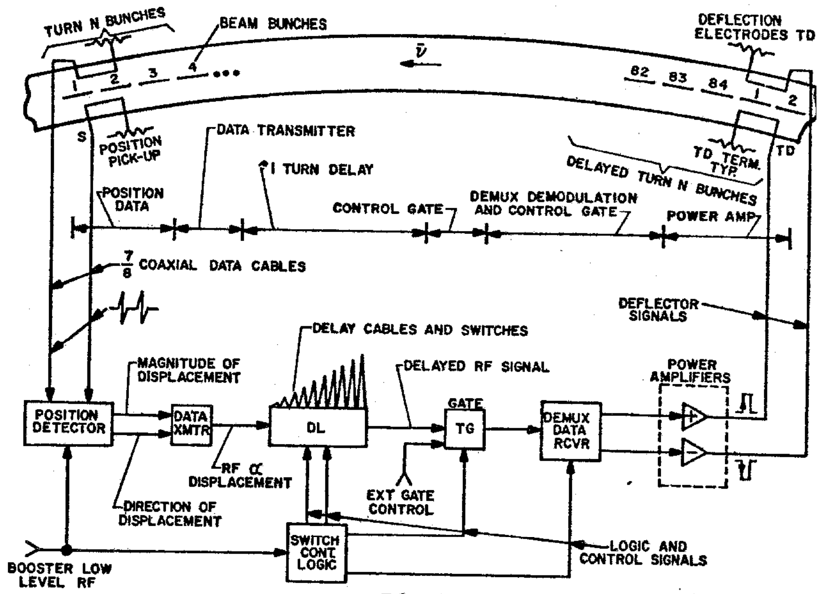

FIGURE I
BOOSTER DAMPER BLOCK DIAGRAM

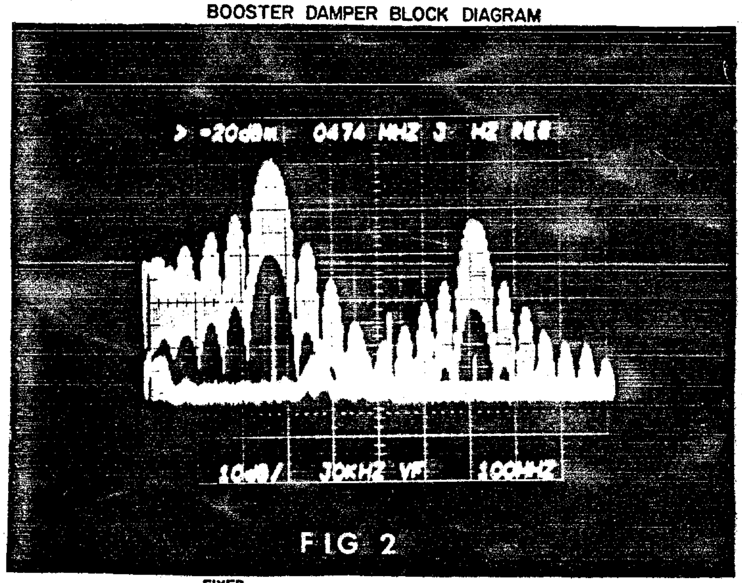

FIG 2

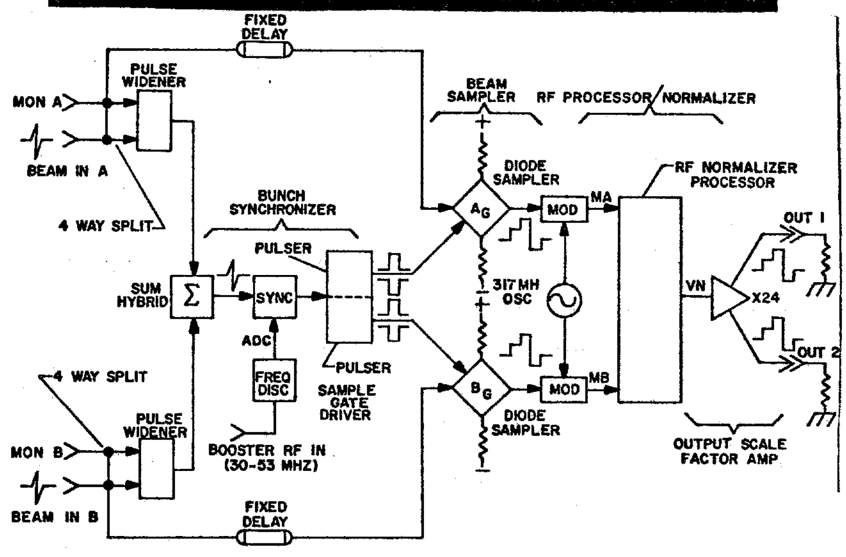

FIGURE 3
POSITION DETECTOR BLOCK DIAGRAM

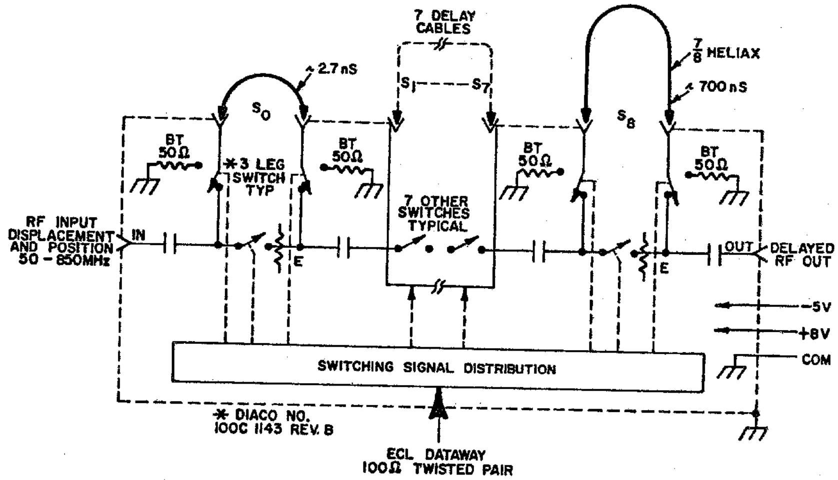

FIGURE 4

SIGNAL DELAY CONTROL RF SWITCH ASSEMBLY

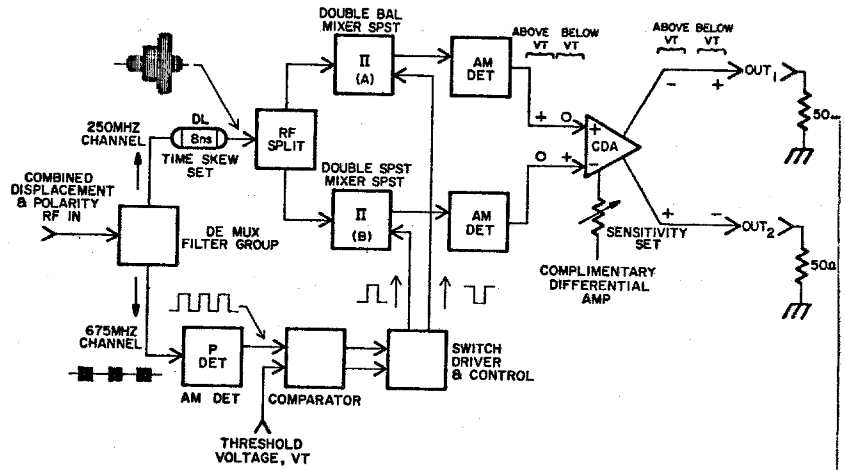

FIGURE 5

DATA RECEIVER/DE MUX BLOCK DIAGRAM

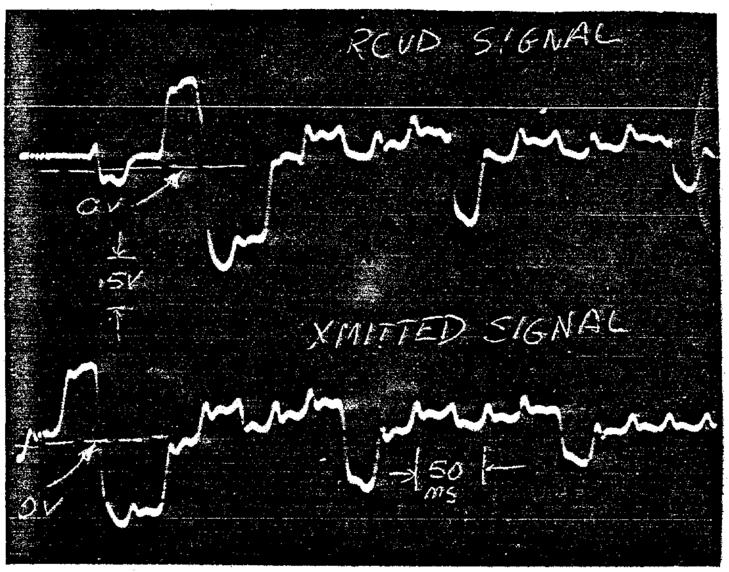

FIG 6