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THESIS

"Design and Performance Characteristics of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector"

Submitted in satisfaction of the requirements for the Ph. D. in Physics with Specialty in Optoelectronics

NOW 17

Presented by

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TABLE OF CONTENTS

INTRODUCTION

Chapter one

BTeV experiment at Fermilab **1**

1.1 BTeV Requirements for the vertex detector 5
1.2 Fermilab Pixel Chip (FPIX chip) 7
1.2.1 FPIX1 pad description 9
1.3 Multi-chip Module (MCM) 12
1.4 Conclusions 15

Chapter two

Performance of VCSELs and PIN photodiodes **16**

2.1 Single VCSELs and single PIN photodiodes 16
2.1.1 DC test on single VCSELs and PIN photodiodes 16
2.1.2 Radiation hardness on Mitel and Honeywell single VCSELs 21
2.1.3 AC test on single VCSELs and PIN photodiodes 23
2.2 Performance VCSEL and PIN arrays 24
2.2.1 AC test on an optical link array 27
2.3 Conclusions 31

Chapter three

Designing a 106Mbps digital optical link **32**

3.1 VCSEL driver 32
3.2 PIN receiver 34
3.3 Schematic 35
3.4 Conclusions 36

Chapter four

Designing a Biphase-Mark Encoder and Decoder **38**

4.1 Altera FPGAs 39
4.1.1 Programming the Altera FPGAs 40
4.2 Biphase-mark Encoder 42
4.3 Biphase-mark Decoder 44
4.3.1 PLL used to recover the command and clock signals 46
4.4 Conclusions 52

Chapter five

1.06 Gbps Digital Optical Link **53**

5.1 Gigabit Rate Transmit/Receive Chip Set HDMP-10XX 53
5.2 Finisar optoelectronic modules 58
5.3 1.06 Gbps optical Link 62
5.4 Radiation Hard CHFET Serializer 65
5.4.1 Optical G-Link transmitter based on the CHFET serializer and the Honeywell HFE4080 VCSEL 72
5.5 Conclusions 74

Chapter six

Optical Readout and Control Interface for the BTeV Pixel Vertex Detector **75**

6.1 First prototype of the Optical Readout and Control Interface (ORCI) for the BTeV Pixel Vertex detector 75
6. 2 The command and control link transmitter 76
6.3 The command and control link receiver 77
6.4 The readout optical link transmitter 78
6.5 The readout optical link receiver 80
6.6 Performance of the first prototype of the ORCI 80

6.7 Tests of the ORCI with the MCM 84
6.8 Conclusions 87

GENERAL CONCLUSIONS **88**

REFERENCES **90**

INTRODUCTION

High-energy physics is the science of the fundamental nature of matter. Studying subatomic particles and forces gives us a key to understanding the simple physical laws that govern the universe. In 1965, the United States Joint Committee on Atomic Energy (JCAE) and the National Academy of Sciences (NAS) approved a frontier high energy physics project to design and build a 200 GeV Accelerator. In 1967, Robert R. Wilson was chosen by URA (Universities Research Association, Inc) as the first Director of the National Accelerator Laboratory (NAL). In 1974, the Laboratory was renamed in honor of Enrico Fermi as Fermi National Accelerator Laboratory (Fermilab). Physicists use accelerators of higher and higher energy to probe deeper and deeper inside the nucleus. Like more powerful microscopes, the higher and higher energy accelerators enable the investigation of smaller and smaller distances, by now distances inside the proton. Higher energy accelerators also enable the production of heavier and rarer particles.

The search for new particles using the Fermilab accelerator produced a discovery in 1977, the first evidence for the bottom quark was observed. Following that a second accelerator using superconducting magnets was constructed in the same tunnel. This was called the Tevatron, because the design energy was 1 TeV. Later additional components were built to create a beam of antiprotons that allowed the Tevatron to be operated as a proton-antiproton collider. The beam of particles begins as negative hydrogen ions in the Cockcroft-Walton accelerator. They continue to the Linac (Linear accelerator). As the beam of negative hydrogen ions enters the third accelerator, the circular Booster, both electrons are stripped off leaving a proton beam. Finally the protons are injected into the Main Ring. The antiproton source was essential to produce the proton's opposite particle. These antiprotons could then be steered into collision with protons and observed in specially designed detectors. The energy of these collisions would be close to 2 TeV in the center of mass. In 1985 the beam reached 800 GeV, and the first collisions of protons and antiprotons (combined energy of 1.6 TeV) were observed at the Colliding Detector at Fermilab (CDF). With the highest energy get achieved the most powerful superconducting accelerator in the world began the search for the most exotic particle within reach: the top quark. Two specialized detectors were constructed by large teams of experimenters at CDF and at DZero. In 1995 both the CDF and DZero teams announced the top's discovery.

Under the command of John Peoples until 1999 and now under Michael Witherell the most powerful particle accelerator on earth, Fermilab's Tevatron, gives scientists from all over the United States and the world the opportunity to work together on experiments to try to understand the laws of nature. The Tevatron accelerates protons and antiprotons in a giant underground ring. When proton and antiproton collide at close to the speed of light, they make a tiny fireball of pure energy as intense as that at the big bang, when the universe was a trillionth of a second old. Some of the energy turns into matter, according to Einstein's famous equation, $E = mC^2$, yielding sprays of particles that may hold answers to our questions about the laws and origin of the universe.

As the program at Fermilab moves forward the particle physics field focuses inside the quark and beyond. Fixed-target and colliding-beams experiments continue their searches on the frontier. In order to contribute to a deeper understanding of the heavy quarks, bottom and charm, Fermilab has approved the BTeV experiment, E897. The new Fermilab's Tevatron will produce more than 400 billion b-flavored hadrons per year and 10 times as many c-flavored hadrons per year. A hadron is a particle made of strongly-interacting constituents (quarks and/or gluons). These include the mesons and baryons. Such particles participate in strong interactions. The heavy-flavored b and c hadrons will be an excellent resource with which to investigate CP violation, quark/anti-quark mixing and rare decays. BTeV will be well positioned to answer the most crucial questions in heavy flavor physics. BTeV will use a powerful magnet, called SM3, which already exists at Fermilab. The other important parts of the experiment include the pixel vertex detector, the RICH detectors, the EM calorimeters, and the muon system.

The BTeV pixel vertex detector will be a multi-plane pixel device that will sit inside the beam pipe and has been proposed to be used in the first level trigger of the BTeV experiment. Thus, the BTeV pixel vertex detector will be central to the capability of the experiment. The major components for the pixel vertex detector system will be the sensor, readout chip, sensor-to-readout-chip connection, mechanical support and cooling, high-density interconnection between the readout chips and the control chips on the detector plane peripheries, and the multiplexing and data transmission to the first-level trigger.

The silicon pixel detector will be composed of 62 pixel planes of 100x100mm each, divided into 31 stations with 2 planes each, and it will be placed perpendicular to the colliding beam and installed a few millimeters from the beam. VLSI pixel readout chips containing front-end electronics for every pixel sensor will be bump-bonded to the detector. The particle interaction will cause scattering, which will increase the error in the reconstruction of the trajectories of the particles. Since this detector will be employed for on-line track finding for the lowest level trigger system, the pixel chip will have to read out all detected hits. The pixel chip development involves a succession of steps and submissions toward a chip that meets the BTeV requirements. VLSI chips with pixel unit cells of the same dimensions have been designed and built to instrument the sensors. The chips resulting from these steps have been dubbed FPIX0, FPIX1, and so on. The FPIX1 represents the first step towards the final pixel readout architecture. The FPIX1 chip that is a column-based pixel chip with $50\mu m \times 400\mu m$ pixel cells arranged in an array of 160 rows by 18 columns for a total of 2880 pixel cells. The BTeV experiment and the Large Hadron Collider (LHC) experiments will be the firsts using bidimensional pixel arrays. Previous experiments at CERN, Fermilab and another laboratories have been used Silicon strip detectors, which are linear pixel arrays only.

Since each pixel readout chip has 2880 channels and it there will be about 13000 chips. This means a total of 3.8×10^7 channels receiving data from proton-antiproton collisions every 132ns. To send the commands to program each chip on the planes we will use an optical link of 106 Mbps per half plane. To read out all the data generated by the pixel detectors it was decided to use between 2 and 4 optical links of 1Gbps per half plane. Both the emitters of the 1Gbps optical links and the receivers of the 106 Mbps optical links will be about 7cm from the beam since they will be mounted on the detector planes. A very important constraints associated with

this planes is their mass, they must be resist about 1Mrad of radiation, they must operate inside the beam pipe in vacuum at -5^0C and the place to put all the optoelectronics for the optical links is very small, about $4cm^2$. Other solutions, which place the optical circuits outside of the vacuum vessel about 25 cm from the detector, are being studied.

The former parameter is the most critical, since it influences many elements in the final capability of BTeV: separation of decay vertices from interaction vertices, trigger efficiency and enrichment, signal to background levels, proper time resolution, and sensitivity to multiple interactions per crossing. The mass resolution is also important, but mostly influences just the signal to background quality of BTeV data. Current FPIX1 prototypes have sensitive areas of $7.2mm \times 8mm$ ($57.6mm^2$).

The subject of my thesis work is:

"Design, build and characterize the first prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector"

The first prototype of the Optical Readout and Control interface was made using commercial parts and modules manufactured by different companies.

In Chapter one we explain briefly the BTeV experiment. We describe the future spectrometer being built for the BTeV experiment, including the BTeV Pixel Vertex Detector. We explain that this Detector will use 62 half-planes of 5 cm X 10 cm. Each half-plane will contain the MCMs, which are linear arrays of FPIX chips connected in daisy chain. We also discuss the requirements of the BTeV Pixel Vertex Detector. One of the requirements is the high bandwidth required for the readout. An option to solve this issue is to use 1.06 Gbps digital optical links to readout the data generated in the half-planes. A second type of optical links operating at 106 Mbps could be used to send the command and control signals to the FPIX chips form the counting room to each detector half-plane.

In chapter two we present the performance test results of the Mitel single VCSELs, the Honeywell single VCSELs, the Mitel VCSEL and PIN array 4-channels, and the Mitel single PIN photodiode. With these results we conclude that the Mitel VCSELs and PIN photodiodes manifest the better performance with rise and fall times of only 250 ps, jitter peak-peak of only 50 ps and cut bandwidth of 1.18 GHz. All the Mitel VCSELs had a linear relationship between the optical power and the forward current.

In Chapter three we present the design for the VCSEL driver and show the advantage of driving the VCSELs with voltage instead of the traditional current. This reduces the optical power variation between different Mitel VCSEL from 80 % to 25%. Also we present the PIN receiver circuit based on a PIN photodiode used in photovoltaic mode, which makes our PIN receiver an inherently low noise circuit.

In Chapter four we show the Biphase-Mark code used to maintain the DC line balance. We present the design of the Biphase-Mark Encoder/Decoder using FPGAs to implement them.

Also we describe the PLL used in the PIN receiver to recover the command and clock signal. With the VCSEL driver and the PIN receiver we built the prototype 106 Mbps digital optical.

In Chapter five we describe the implementation of one 1.06 Gbps digital optical link based on the G-Link chip set HDMP-1032/1034 and the Finisar optoelectronic modules. Also, we present the tests performed on a preliminary version of the CHFET serializer. The results showed that this preliminary version has errors in the first four data bits. This means that the chip does not work very well. But we can conclude that if a future version works correctly then a G-Link transmitter based on the CHFET serializer would be a very good option.

In Chapter six we present the first prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector, which has been designed, built, and tested at Fermilab. The 104 Mbps optical link contained in this first prototype provides high accuracy transmission of information in a very wide range of optical power as is evident from the low BERs measured. Also the 1.04 Gbps optical link show a very good performance. A very important test was the results that we obtained when we connected the Optical Readout and Control Interface Board with the MCM. The noise and threshold uniformity test results with and without using the Optical Readout and Control Interface are seen to be the same within errors.

With the first prototype of the Optical Readout and Control Interface for the BTeV pixel vertex detector we are contributing to develop the first prototype of the half pixel plane for the BTeV Pixel Vertex Detector.

The final version of the 106 Mbps and 1.06 Gbps optical links can be used in another applications involving a radiation exposure, e. g. in the space, satellite communications, another high energy physics experiments, etc..

With this work we did the follow presentations and publications:

1. S. Vergara, M. Sheaff, M. A. Vargas, "High Speed Radiation Hard Optical Links", poster presentation, SOMI XIV CONGRESO DE INSTRUMENTACION, Tonanzintla, Puebla, MEXICO. 1999.
2. G. Cancelo, S. Vergara, A. Vargas, "Fiber Optic based readout for BTeV's Pixel Detector", poster presentation, LEB Sixth Workshop on Electronics for the LHC experiment, Cracow, Poland, September, 2000.
3. S. Vergara, M. Sheaff, M. A. Vargas, "High Speed Radiation Hard Optical Links", Proceedings SOMI XIV CONGRESO DE INSTRUMENTACION, pp. 790-794, Tonanzintla, Puebla, MEXICO. 1999.
4. G. Cancelo, S. Vergara, A. Vargas, "Fiber Optic based readout for BTeV's Pixel Detector", Proceedings, LEB 2000 Sixth Workshop on Electronics for the LHC experiments, pp. 502-506, Cracow, Poland, October, 2000.
5. S. Vergara, G. Cancelo, M. Sheaff, M. A. Vargas, "Optical Readout and Control Interface for the BTeV Pixel Vertex Detector", Fermilab Preprint FERMILAB-PUB-00-246E, November 2000, submitted to NIMA on September 2000.

Chapter One

BTeV experiment at Fermilab

The main goal of the BTeV experiment, proposed for the Fermilab Tevatron is to study the physics of the charm and bottom quarks. The experiment will use the Fermilab Tevatron. The accelerator will produce more than 400 billion b-flavored hadrons per year and 10 times as many c-flavored hadrons per year. These particles participate in residual strong interactions. The heavy flavored hadrons will be an excellent resource with which to investigate CP violation, quark/anti-quark mixing and rare decays. With all the results expected from the experiment. BTeV will be well positioned to answer the most crucial questions in heavy flavor physics.

Today the atom is known to contain many more elementary particles inside. The structure within the atom [1] is shown as Fig. 1.

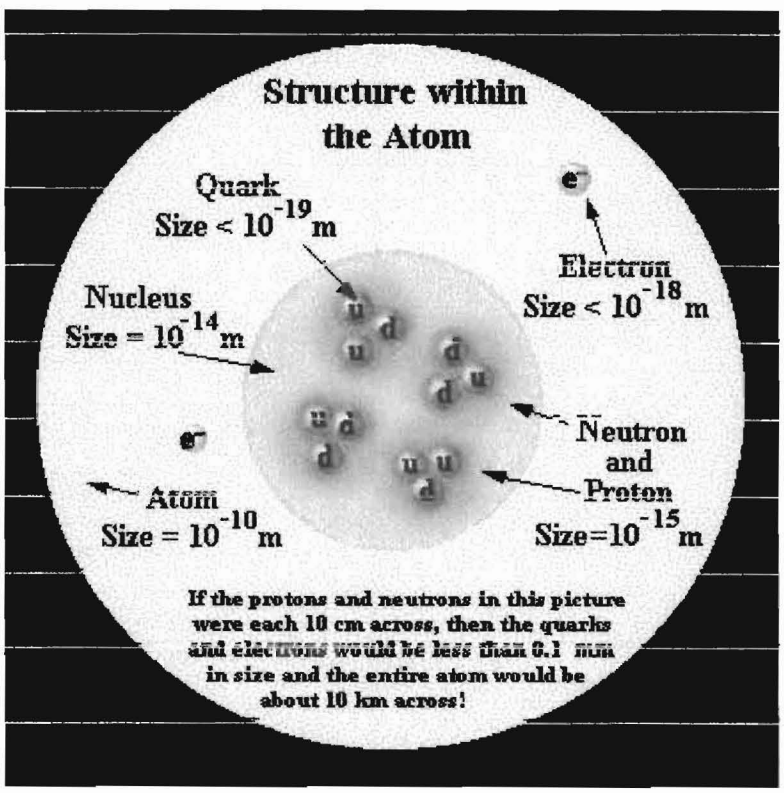


Figure 1: The structure within the atom (this picture is a conception of an artist in a work made for Fermilab).

We can see that the neutrons and protons contain quarks. Also, inside the atom there are leptons. The elementary particles and force carriers [1] are shown in Fig. 2.

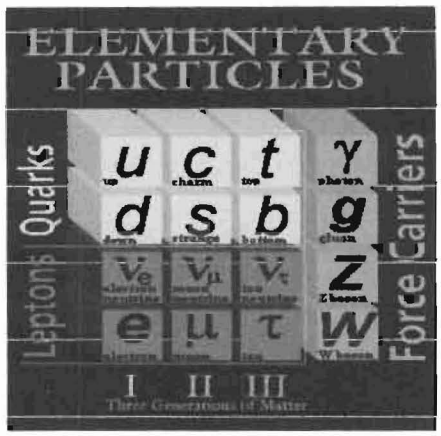


Figure 2: Elementary particles.

The BTeV experiment will use a powerful magnet, this magnet will generate a integrated dipole field of 5.2 T-m. The other important parts of the experiment include the vertex detector, the RICH detectors, the EM calorimeters and the muon system [2]. A sketch of the future apparatus is shown as Fig. 3.

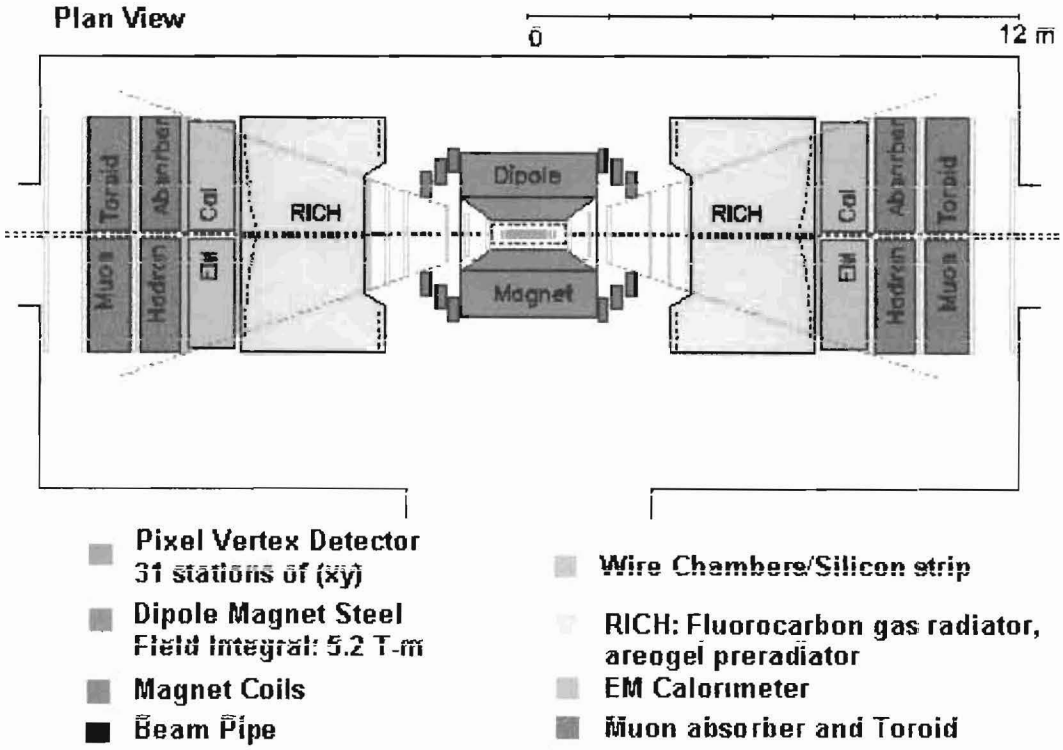


Figure 3: Sketch of the future BTeV spectrometer, this figure is not to scale, and it is only to illustrate.

The vertex pixel detector will provide the high resolution space points near the interaction, which are used both online and offline to reconstruct tracks and associate them with their parent vertices. In designing the vertex tracking system, one must consider the long interaction region (IR) of the Tevatron, which has a $\sigma_Z = 30cm$.

The BTeV experiment is going to use silicon pixel detectors because they provide high precision space points and they are quite radiation hard. Radiation hardness will allow the detector elements to be placed very close to the beam (~6 mm, in vacuum, separated from the beam only by a thin RF shield). The measurements of space points, with very little noise, provides superior pattern recognition, allowing the experiment reconstruct tracks and vertices in real time, and trigger on events containing reconstructable heavy flavor decays. The long interaction region forces one to have a rather long vertex detector with many pixel planes.

The pixel vertex detector will contain about thirty million rectangular pixels, each 50 μm X 400 μm. Each pixel sensor is read out by a dedicated electronics cell. The pixel sensors elements are arranged in a bidimensional array of unit cells of the same size as the sensors in the Fermilab pixel chip (FPIX). The two are connected by bump-bonds. The basic building block of the pixel vertex detector is a hybrid assembly called the Multi-Chip Module (MCM) which of a linear array of FPIX readout chips connected in daisy chain, bump-bonded to a sensor and wire-bonded to a flexible printed circuit which carries I/O signals and power.

The baseline pixel vertex detector consist of a regular array of 31 "stations" of "planar" pixel detectors distributed along the interaction region [3], see Figure 4.

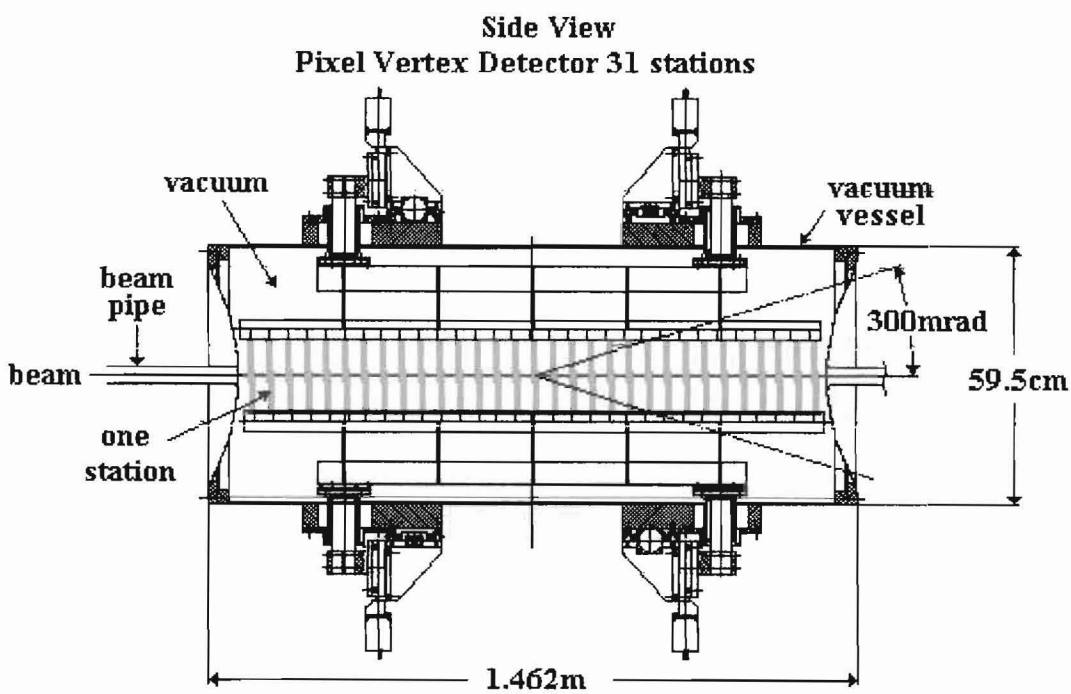


Figure 4: Side view of the future Pixel Vertex Detector, including the vacuum vessel and its mechanical support.

Each station will contain one plane with the narrow pixel dimension vertical, and one with the narrow dimension horizontal, and will be composed of two 5 cm X 10 cm halves. The half stations will be mounted above and below the beam and are arranged so that a small square hole is left for the beams to pass through [3]. Two diagrams showing how the MCMs will be arranged on the pixel planes are shown in Fig. 5 and Fig. 6.

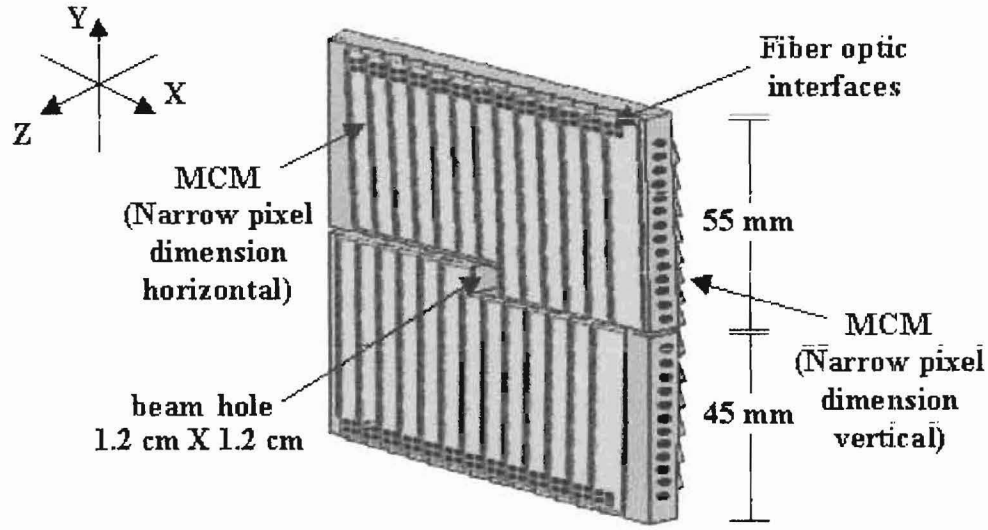


Figure 5: Station composed by two 5 cm X 10 cm half stations. The station will contain two planes, one plane with the narrow pixel dimension vertical, and the other with the narrow pixel dimension horizontal.

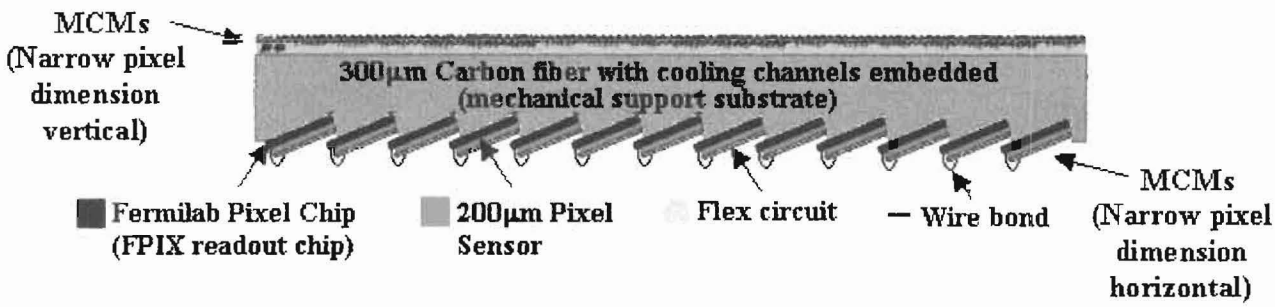


Figure 6: Top view of the future station.

The elementary charged particles generated by the proton-antiproton collision will be bent by the magnetic field generated by means of the SM3 magnet. They will produce tracks in the pixel vertex detector. The curvature of a track will allow its momentum to be measured. Track will be used to form vertices. The RICH detector is made to use the *Čerenkov* effect to know the mass of these elementary particles. With this information many of the B particle decays will be able to be fully reconstructed.

Table 1 summarizes the properties of the future pixel vertex detector.

Property	Value
Pixel size	rectangular: 50 μm × 400 μm
Plane Dimensions	10 cm × 10 cm
Central Square Hole Dimensions (adjustable)	nominal setting: 12 mm × 12 mm
Total Planes	62
Total Stations	31
Pixel Orientations (per station)	one with narrow pixel dimension vertical & the other with narrow dimension horizontal
Separation of Stations	4.25 cm
x-Plane to y-Plane Separation (within station)	5.0 mm
Total Station Depth (incl cooling, supports)	6.5 mm
Sensor Thickness	250 μm
Readout Chip Thickness	200 μm
Total Station Radiation Length (incl RF shielding)	2%
Total Pixels	3×10^7
Total Silicon Area	$\approx$0.6 m^2
Readout	analog readout (3 bits)
Trigger	signals are used in Level 1 trigger
Rate Requirements	time between beam crossings is 132 ns.
Noise Requirement	desired: $< 10^{-6}$ per channel/crossing required: $< 10^{-5}$ per channel/crossing
Resolution	better than 9 μm
Radiation Tolerance	$> 6 \times 10^{14}$ particles/cm^2
Power per Pixel	$<$60 μWatt
Operating Temperature	$\sim$-5 °C

Table 1: Properties of the future Pixel Vertex Detector.

1.1 BTeV Requirements for the Future Pixel Vertex detector

The BTeV experiment has very stringent requirements for the future Pixel Vertex detector. The first constraint is that all the 31 stations must tolerate a high radiation dose. This dose has been calculated by people in the experiment. It depends on the radial distance from the beam, see Fig. 7.

We can see from Fig. 7 that the FPIX chips near from the beam will receive about 3-5 Mrad during one year of running and the electronics sitting on the perimeter of the pixels planes will receive about 100kRad.

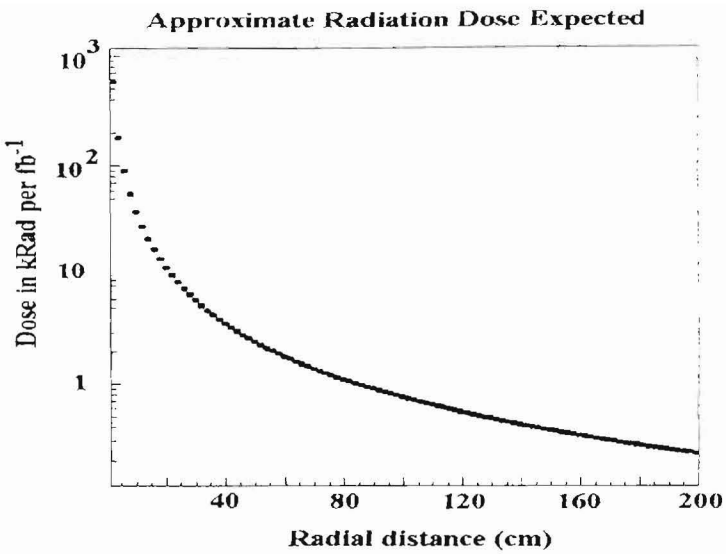


Figure 7: Expected radiation dose at the Tevatron for one year running [4].

Another constraint associated with the pixel planes is their mass, they should be as light as possible to decrease particle interactions with the material. Strong interactions are the source of unwanted secondary particles. Electromagnetic interactions and strong interactions cause scatterings, which increases the error in the track's reconstruction [5]. The mean scattering angle (in milliradians) is approximately given by Eq. 1.

$$\Theta = \frac{13.6}{P}\sqrt{\frac{X}{X_0}}, \tag{1}$$

where P is the momentum of the particle in GeV/c, X_0 is the radiation length and X is the thickness of the material in question.

Table 2 gives the radiation length of different materials.

Material	X_0 (mm)
Water	360
Beryllium	350
Carbon fiber	250
Beryllium oxide	143
Diamond CVD	123
Silicon	100
Aluminum	89
Nickel	15.7
Copper	14
Silver	8.7
Gold	3.4

Table 2: Radiation length of materials [5].

From Table 2 we can see that a particle traversing an aluminum sheet will have an approximately 2.5 times smaller mean scattering angle than in a copper sheet of same thickness.

The experiment requires that the FPIX chips read out all detected hits. Since the pixel vertex detector will be used for the main first level of trigger. Since the number of hits is quite large, it is necessary to provide significant readout bandwidth to transfer all data from the pixel chips to the trigger electronics. Simulations performed mapped the number of group hits per chip in a half plane [4], considering a pixel chip with active area of 8 mm X 8 mm ($64mm^2$), each chip with 3200 pixels cells of 50×400 μm. The pixel chip uses 17 bits to deliver all the information about the position of a hit (row and column), time stamp, ADC and chip ID. The results of these simulations are depicted in Fig. 8, where the numbers correspond to megabits per second (Mbits/sec). So, some of the innermost chips will have as many as 200 Mbits/sec to readout. These simulations provide enough information to allow an assessment of the number of busses necessary to readout the chips.

					13	**13**	13	12					
				13	15	**16**	16	15	15				
			19	23	23	**27**	24	26	20	17			
		15	24	29	36	**43**	41	36	26	23	16		
	18	19	35	46	66	**79**	79	60	43	30	19	16	
13	17	23	36	56	112	**196**	192	109	61	34	22	15	12
13	17	23	36	56	112	**196**							

Figure 8: Chip location on a half plane and its data rate (in Mega bits per second).

To achieve the high bandwidth required for the readout, ultra-high-speed digital optical links of 1-2 Gbps will be employed on each detector half-plane. A second type of digital optical link, which will send the command and control signals to the FPIX chips from the counting room to each detector half-plane, can operate at lower speed (~100 Mbps).

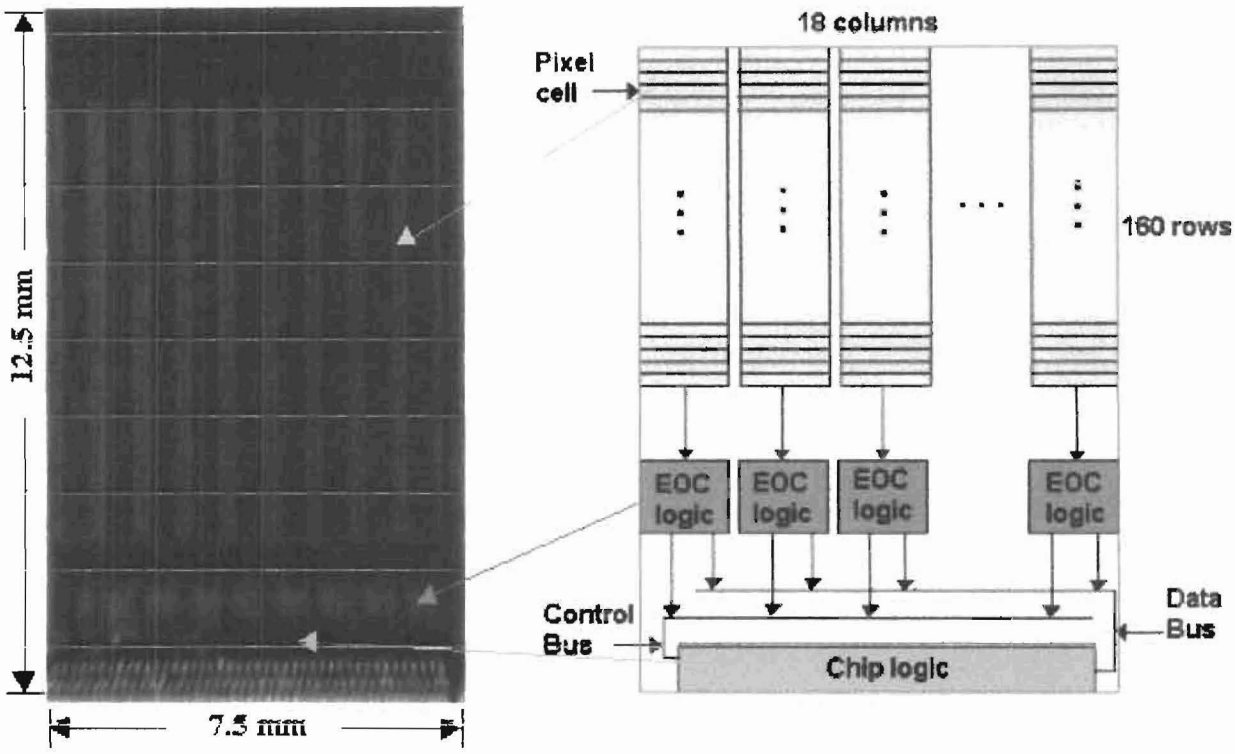
Both the emitters of the ultra-high-speed optical links and the receivers of the lower speed optical links will be about 7 cm from the beam if they are mounted on the detector planes as proposed in the baseline design. In this case, these devices will receive about 100 Krad of radiation per year of running and will suffer some radiation damage. A further, rather stringent requirement is that they must operate inside the beam pipe in vacuum at $\approx -5^0C$ [3]. Other solutions, which place the optical circuits outside of the vacuum vessel about 25 cm from the detector, are also being studied.

1.2 Fermilab Pixel Chip (FPIX chip)

FPIX1 is the second in the sequence of submissions aimed at developing a chip that meets the BTeV requirements. The FPIX1 is a column-based pixel chip; i. e., the readout and control circuitry is organized by column, with $50\mu m \times 400\mu m$ pixel cells arranged in an array of 160 rows by 18 columns for a total of 2880 pixel cells. The block diagram of the FPIX1 is shown in Fig. 9b

[6]. The FPIX1 chip can be divided into three mutually dependent parts, the pixel cell, the End of Column (EOC) Logic and the Chip Control Logic.

The Pixel cells hold the front-end electronics and the digital interface to the EOC logic. The front-end contains a charge-sensitive amplifier and a second amplification stage; the output of the second stage connects to a flash ADC and a discriminator. The discriminator output is asserted when the signal at the input of the discriminator is higher than the threshold (Th0). The pixel cell contains a digital interface with two major components, the command interpreter and the pixel token and bus controller.



a) b)

Figure 9: FPIX1, a) Chip die and b) Block Diagram.

The command interpreter has four inputs corresponding to the four EOC command sets. Four are provided for derandomization. Thus a hit or hits in a column can be recorded from the current beam crossing while hits from up to three previous beam crossing are still being read out. These commands are presented by the EOC logic simultaneously to all pixel cell interpreters in a column. When an interpreter is executing the input command and the hit output from the discriminator is asserted, the interpreter associates itself with the particular EOC set and simultaneously it alerts the EOC logic to the presence of a hit via the wire-or'ed HfastOR signal. After that, the information is stored in the cell until the same EOC set issues an output or reset command. When this command is an output command, the interpreter issues a bus request and asserts the wire-or'ed RfastOR signal. Then the balance of the readout proceeds synchronously with the ReadClk. The EOC logic provides a column token, the token quickly passes pixel cells with no information until it reaches a cell that is requesting the bus.

The data output is multiplexed and the data are delivered in two sets of 17 bits, the first set contains the Chip Identification (ChipID; 4 bits), the time stamp (BCO; 6 bits), the control/data indicator (D15; 1 bit), data valid (D16; 1 bit) and 5 logical 0 bits. The second set contains the analog-to-digital converter output (ADC; 2 bits), the row address (row; 8 bits), the column address (col; 5 bits), the control/data indicator (D15; 1 bit) and data valid (D16; 1 bit). When the hit pixel is read out, it then automatically resets itself and withdraws its assertion of the RfastOR. This signal returns to its inactivated state while the rest of the hit pixels are being read out [6].

1.2.1 FPIX1 Pad description

The FPIX1 chip contains 87 pads.

- Twelve pads provide ground:

Function	Pad number	Pad name	Description
Ground (0V)	1,87	**Vssa**	Pixel analog circuitry
	9,79	**Vssd**	Pixel commands interpreters and drivers
	13,19,25	**Vsub**	Substrate voltage
	15,21	**Vssd-eoc**	End of column Logic
	51	**Vss-pad**	Pad circuitry
	5,81	**Vss-comp**	Pixel A to D conversion

- Nine pads supply power:

Function	Pad number	Pad name	Description
Power (3.3V)	3,85	**Vdda**	Pixel analog circuitry
	11,77	**Vddd**	Pixel commands interpreters and drivers
	17,23	**Vddd-eoc**	End of column Logic
	53	**Vddd-pad**	Pad circuitry
	7,83	**Vddd-comp**	Pixel A to D conversion

- One pad is the input for the charge injection:

Function	Pad number	Pad name	Description
Inject Charge	2	**InjectIn**	Analog input for test charge

- Six pads give the current bias:

Function	Pad number	Pad name	Description
Current bias	4,10	**Ivbbnl**	Decoupling point and override for internal bias
	6	**Ivfb**	Feedback current (5nA)
	8	**Ivbbp**	Master bias current (7 μ A)
	12	**Ivbbpl**	Decoupling point and override for internal bias
	14	**Ivbb-comp**	Decoupling point and override for internal bias

- Three pads are the voltages threshold for the ADC and one pad represents the voltage threshold of the discriminator:

Function	Pad number	Pad name	Description
Thresholds	16	**Vth3**	Most significant threshold for ADC
	18	**Vth2**	Threshold for ADC
	20	**Vth1**	Threshold for ADC
	22	**Vth0**	Threshold for hit comparator

- Two pads are the voltage bias for the two different sensors i.e., p-stop and n-guard.

Function	Pad number	Path name	Description
Bias voltage	24	**Vpstop**	Bias voltage for the detector p-stop
	26	**Vnguard**	Bias voltage for the detector n-guard

- Fifteen control signals, with them we can program, control and readout the FPIX1 chip:

Function	Pad number	Pad name	Description
Control signals	27/28	**TokenIn/TokenIn***	Input for the chip token
	29	**TrigAcc**	Trigger mode: Trigger signal; Continous mode: Accept (3.3V) or reject (0V) hits.
	30	**ShiftIn**	Input for the scan paths
	31	**DataRes**	Reset signal
	32	**ProgramRes**	Reset signal
	33	**ShiftClk**	Shift clock signal
	34/35	**ReadClk*/ReadClk**	The read out clock
	36/37	**BCOClk*/BCOClk**	The beam cross over clock
	50	**LoadKill**	Load kill pattern into pixels on falling edge
	76,78,80	**Reg2, Reg1, Reg0**	Scan path selection bits (Reg2 is MSB)

Most of these control signals are CMOS i.e., a logical 1 represents 3.3V and a logical 0 represents 0V. Only the ReadClk, BCOClk and TokenIn signals are differential.

All the information to program the FPIX1 chip is received serially by the ShiftIn signal, this input receives the information and the **Reg [2:0]** signals indicate the scan path selection. They are CMOS inputs. At the rising edge of the clock signal (**ShiftClk**), the value at the **ShiftIn** will be scanned into the path chosen by the **Reg0**, **Reg1**, and **Reg2** signals. To choose a particular scan path we select one of the eight different codes shown in Table 3.

	Reg2, Reg1, Reg0	Path
0	0 0 0	Idle – No path
1	0 0 1	Trigger path
2	0 1 0	Not used
3	0 1 1	Programmable reset delay
4	1 0 0	Not used
5	1 0 1	Configure (Mode, ChipID and Lag)
6	1 1 0	Kill or Inject
7	1 1 1	Kill or Inject

Table 3. Scan paths to program the FPIX1 chip.

For example to configure the chip, one must select the code 101. To program the chip, **ShiftIn** correctly must be delayed more than 5ns from **ShiftClk**.

DataRes is a reset level signal. When this signal is high, the BCO counters are reset to zero; the End of column registers are reset and the chip stops outputting data. **ProgramRes** is a reset level signal. When this signal is high, the mask registers are set to zero; the chip is reset to continuous mode; the BCO lag is set to 2 and the ChipID is set to zero.

LoadKill latches the kill pattern scanned into the pixel array on the falling edge of the Shiftclck. It is a CMOS level signal and it is kept at logical 1 during the kill scan, and dropped to a logical 0 to latch the kill pattern. **TrigAcc** is a dual-mode signal. If the chip is operating in triggered mode, it is the trigger signal. If the chip is operating in continuous mode, this signal is used to Accept or Reject hits. In this conditions when this signal is logical 0 the chip rejects (ignores) incoming hits; and when it is logical 1 accepts incoming hits. This is a single ended CMOS signal.

To get the information acquired by the chip, we need to send a set of signals that controls the readout of the FPIX1 chip. Most of these signals are LVDS (Vhi≅ 1.75V; Vlow≅ 1.55V). **ReadClk*/ReadClk** is a free-running LVDS differential clock. The maximum readout frequency simulated was 26MHz, but the real frequency will be whatever the chip can handle. **BCOClk*/BCOClk** is a LVDS differential signal and is used to represent the beam crossing (time stamp). **TokenIn/TokenIn*** is a LVDS differential signal and is used to request the readout of the chip. When TokenIn is high (Pad 27=1.75V; Pad 28=1.55V), the chip can take control of the data bus. When this signal is low (Pad 27=1.55V; Pad 28=1.75V), the chip can not take control of the data bus and its data outputs are tri-stated.

- Four output signals:

Function	Pad number	Pad name	Description
Output signals	52	**ChipHasData**	Diagnostic path, it uses CMOS levels
	82	**ShiftOut**	Output from the scan path
	84/86	**TokenOut*/TokenOut**	Chip token output

These signals help us to verify the information we are programming into the FPIX1 chip, because **ShiftOut** will output the same serial pattern that we are putting into **ShiftIn**. The serial output pattern will be delayed a certain number of clock cycles (**ShiftClk** is its clock signal). This will depend on how many FPIX1 chips are connected in daisy chain and which path we are programming. The **ShiftOut** is single ended signal with CMOS level. This signal will be driven to the **ShiftIn** of the next chip when you connect several chips in daisy chain. **TokenOut*/TokenOut** represents the output of the chip token signal.

- Thirty-four differential signals that represent the 17 bits of the multiplexed data output:

Pad name	Pads number	Data Available Control Word	Data Available Data Word
Data 16/Data 16*	74/75	Logical1	Logical1
Data 15/Data15*	73/72	Logical 0	Logical 1
Data 14/Data 14*	71/70	Logical 0	ADC [1]
Data 13/Data 13*	69/68	Logical 0	ADC [0]
Data 12/Data 12*	67/66	Logical 0	Col Addr [4]
Data 11/Data 11*	65/64	ChipID [0]	Col Addr [3]
Data 10/Data 10*	63/62	ChipID [0]	Col Addr [2]
Data 9/Data 9*	61/60	ChipID [0]	Col Addr [1]
Data 8/Data 8*	59/58	ChipID [0]	Col Addr [0]
Data 7/Data 7*	57/56	Logical 0	Row Addr [7]
Data 6/Data 6*	55/54	Logical 0	Row Addr [6]
Data 5/Data 5*	49/48	BCO [5]	Row Addr [5]
Data 4/Data 4*	47/46	BCO [4]	Row Addr [4]
Data 3/Data 3*	45/44	BCO [3]	Row Addr [3]
Data 2/Data 2*	43/42	BCO [2]	Row Addr [2]
Data 1/Data 1*	41/40	BCO [1]	Row Addr [1]
Data 0/Data 0*	39/38	BCO [0]	Row Addr [0]

The data outputs are tri- statable LVDS outputs until the **TokenIn** signal is asserted. This indicates the readout request. **Data16** is the data valid signal; with this signal you can verify that the data available are valid or not. When the chip is releasing data **Data16** will be a logical 1 (3.3V); if the data are not valid this signal will be a logical 0 (0V). The information from the FPIX1 chip will be provided in a multiplexed way. First we will receive the control words and later the data words. Data words are indicated by **Data15**. If **Data15** is a logical 0, then we are receiving a control word, and if **Data15** is a logical 1, then we are receiving a data word. The control word contains the ChipID and the BCO number (time stamp). The data word contains the row address, column address and the ADC output. The data word contains information from only one pixel cell. If many pixel cells in a FPIX1 chip are hit at the same time then we will read out only one control word indicating the same ChipID and the same time stamp for all the pixel cells. Later the chip will release as many data words as pixel cells were hit.

1.3 Multi-Chip Module (MCM)

The innermost detector for the BTeV experiment will be the pixel vertex detector. As we have seen, this detector is composed by 62 pixel half planes. Each plane contains many pixel chips bump bonded to the sensors. A very important constraint associated with these planes is their mass. They should be as light as possible to decrease particle interactions with the material. This includes the material used to support the planes as well as the material in the planes themselves. Other important constraints related to the pixel detector are that they must survive significant radiation and operate in vacuum. The detector will suffer substantial radiation dose and must be built with radiation hard material. Also these materials can not outgas or evaporate in vacuum. Since the detector is inside vacuum, most of the heat has to be conducted from the chips to the cooling channels. In this case carbon fiber support structures are good candidates because they provide lower mass associated with good thermal conductivity characteristics. For all these reasons the BTeV experiment has decided to glue high density interconnect (HDI) circuits on the top of a

module placed on a carbon fiber plate containing liquid cooling channels which supports the detector and associated electronics as shown in Fig. 10. The FPIX readout chips will be wire-bonded to the HDI.

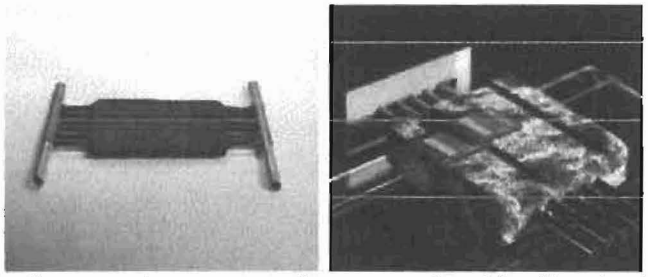


Figure 10: Sample fuzzy carbon composites; note the shingling in the picture on the right.

In the new electronics world the HDI or flex circuit has gained a very high importance. This is driven by the necessity for miniaturization and for high speed devices. This increases the demand for smaller semiconductor components with a high density of input-output signals and also the demand for a higher number of connection points on the printed circuit board (PCB). Multi-layer HDI will provide the interconnection densities needed to meet the demands for the BTeV experiment.

The test of the prototype Multi Chip Module (MCM) is the first attempt to characterize the performance of more than one chip bump bonded to a pixel detector. The prototype MCM contains five FPIX1 chips connected in daisy chain. The MCMs assembled for the actual detector will contain a somewhat smaller or larger number of FPIX chips. The prototype MCM was made using a mounting board wire bonded to a HDI manufactured by Fujitsu Computer Packaging Technologies Inc. The HDI is used to carry the configuration, control and data signals to and from the FPIX1 chips connected in daisy chain to the mounting board. Figure 11a shows a sketch of the MCM board and Fig. 11b shows a photograph of a complete MCM board assembled.

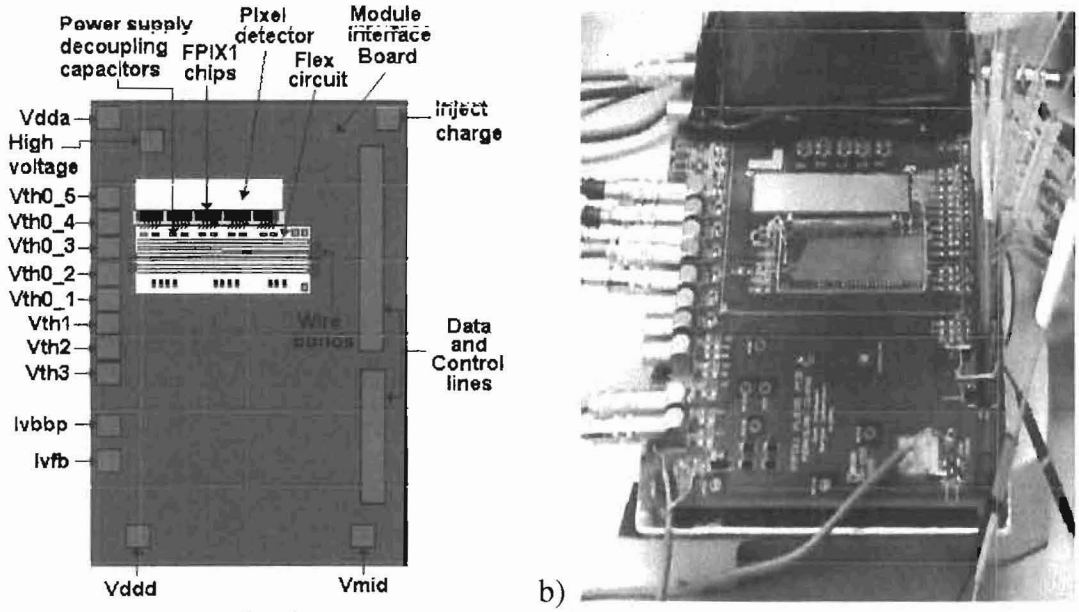
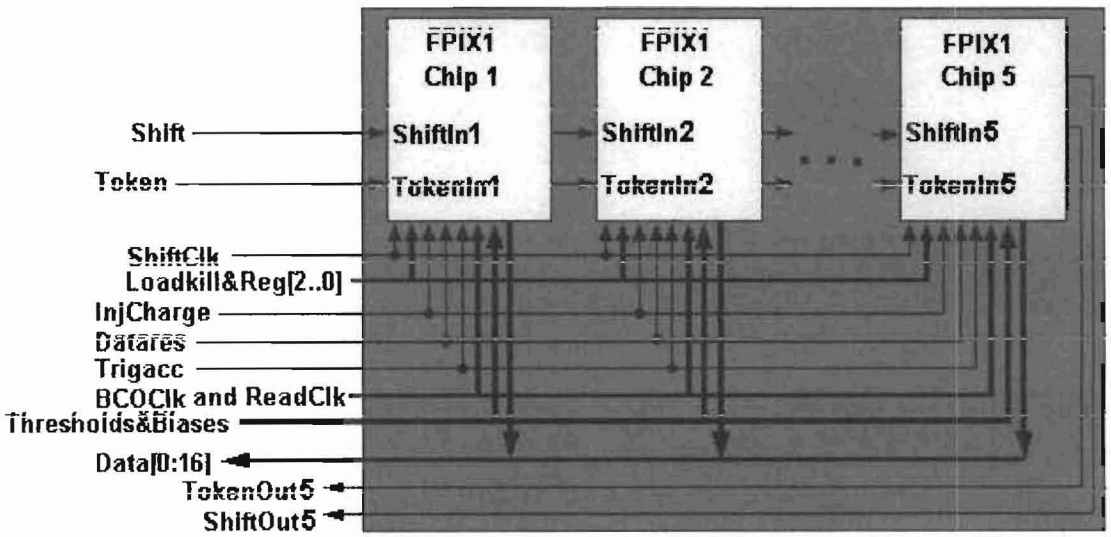
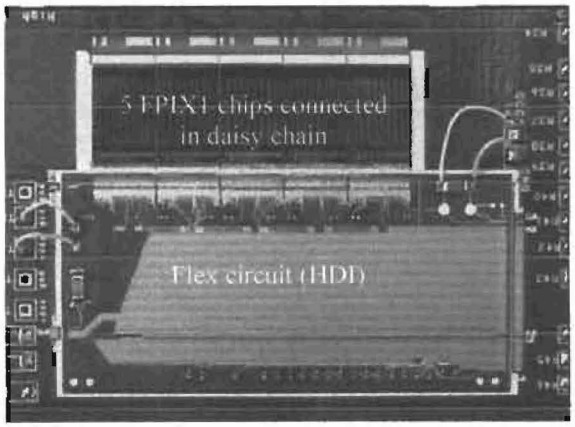


Figure 11: MCM board. a) Sketch and b) Picture.

The MCM has a flex circuit or HDI attached to the top of a rigid printed circuit board (PCB). The chips are wire-bonded to the flex circuit, which interconnects all pixel chips. There are also wire bonds to connect the flex circuit to the PCB. Several decoupling capacitors are mounted on the flex circuit. The power supply decoupling capacitors need to be located close to the pixel chips. Most of the signals are bussed in parallel to all chips with the exception of **ShiftIn**, **ShiftOut**, **TokenIn** and **TokenOut**, which are daisy chained. Two bias currents bias need to be provided to the FPIX1 chips, **Ivbbp** and **Ivfb**. All the bias currents of the same type are tied together (one trace feeding all FPIX1 chips for each bias current), and they are fed to the rigid board through the wire bonds. The rigid board of the MCM should contain resistors which can be used to vary the setting of all bias currents. Each of the four threshold voltages threshold, **Vth0**, **Vth1**, **Vth2**, and **Vth3**, are also tied together and are provided to the rigid board through connectors. The inputs for the threshold voltages also need to be decoupled by capacitors mounted on the top of the flex circuit. There is a distance of 324 microns between the centers of the outside pads of two adjoining FPIX1 chips. Figure 12a shows a block diagram of the flex circuit with 5 FPIX1 readout chips on it. Fig. 12b shows a photograph of the flex circuit with the 5 FPIX1 chips assembled.



a)



b)

Figure 12: Flex circuit with 5 FPIX1 readout chips connected in daisy chain. A) Block diagram and b) Photograph.

The MCM operates essentially like a single FPIX1. The only difference is that in the single FPIX1 we have 2880 pixel cells, and with the MCM we have 14400 pixel cells. To connect the FPIX1 chips in daisy chain we need to connect the **Shift** signal to **ShiftIn1**, the **ShiftOut1** to **ShiftIn2, ShiftOut2** to **Shiftin3,** and so on. We need to do the same with the **Token** signal. The readout operates more or less like a single FPIX1. The only difference is the Token signal, which needs to pass trough each FPIX1 chip in the chain. One needs to be careful setting this signal because if you don't keep this signal at high level for the full readout time then you can lose information.

1.4 Conclusions

We have seen that we need to provide a very high bit rate transmission to read out all the hit data coming from the MCM. Because of this the BTeV experiment has decided to use two optical links. One optical link is to program and control all the FPIX readout chips on the MCM. The other optical link will be to read out all the data hit generated in the MCM. The first will be a 106 Mbps optical link and the second will be 1.06 Gbps optical link. The main goal is to design and build the first prototype of these optical links. The first steps are to investigate how a simple digital optical link works and to look for radiation hard devices such as the new laser diode called VCSEL.

Chapter Two

Performance of VCSELS and PIN photodiodes

VCSELs are becoming a very important device for use as transmitters in optical links operating at 850 nm. In this chapter we show the results of the tests performed on VCSELs manufactured by Mitel and Honeywell. Based on these results we should be able to choose the VCSEL with the best performance. We also performed tests on PIN photodiodes.

2.1 Single VCSELs and single PIN photodiodes

To design an optical link we need to know very well the electrical and optical characteristics of the light source [7, 8, 9, 10] and the photodetector [11, 12]. In our case we will use VCSELs as light sources, PIN photodiodes as photodetectors and multimode optical fibers [13] will carry the optical signal between them. In order to study the properties of these devices, we carried out performance tests on 6 Mitel 1A444 single VCSELs [14], 6 Honeywell HFE4080 single VCSELs [15], and 3 Mitel 1A354 PIN photodiodes [16] and also on 1 Mitel 4D469 VCSEL array [17] and 1 Mitel 4D470 PIN photodiode array [18].

2.1.1 DC tests on single VCSELs and PIN photodiodes

To perform the DC test on PIN photodiodes and single VCSELs we use the following instruments and materials: Tektronix PS2521G programmable power supply, PHOTODYNE 2275XQ Fiber Optic Test Set used as an optical power meter, FLUKE 76 multimeter in current mode, 1m multimode optical fiber cable (62.5 μm/125 μm, core/cladding) assembled with ST connectors. A sketch of the setup is shown as Fig. 13.

The DC test on the single VCSEL consisted of measuring the variations in its optical power as a function of its forward current and its forward voltage. Since the VCSEL is a laser diode the relationship between its forward current and its forward voltage is not linear. To characterize the VCSELs we measured the forward current and the light intensity for three different voltage levels, 1.39, 1.47 and 1.54 Volts. Afterwards we increased the forward current from 2 mA up to 28 mA in steps of 2 mA. In this case we measured the forward voltage and the light intensity for each current level. With this test we measured the optical power delivered by the single VCSELs as a function of forward current (Fig. 14), the forward current as a function of the forward voltage (Fig. 15), and the VCSELs' resistance as a function of forward current (Fig. 16 and 17).

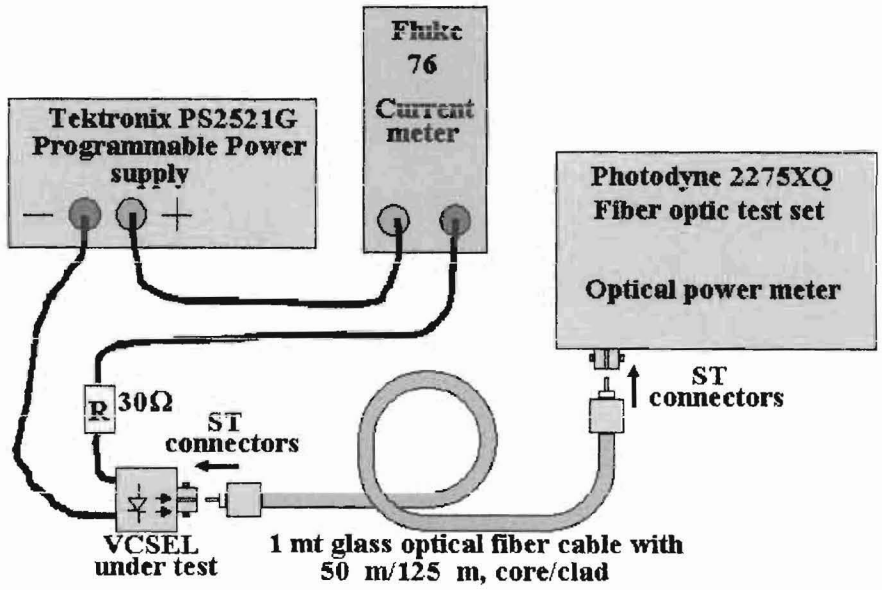


Figure 13: Setup used to perform the DC tests on VCSELs.

We tested 6 Mitel 1A444 single VCSELs and 6 Honeywell HFE4080-322 single VCSELs. To make it easy to understand these test results we focus only on the two Mitel or Honeywell VCSELs with the highest and lowest optical power. The test results are shown in Table 4 and Table 5.

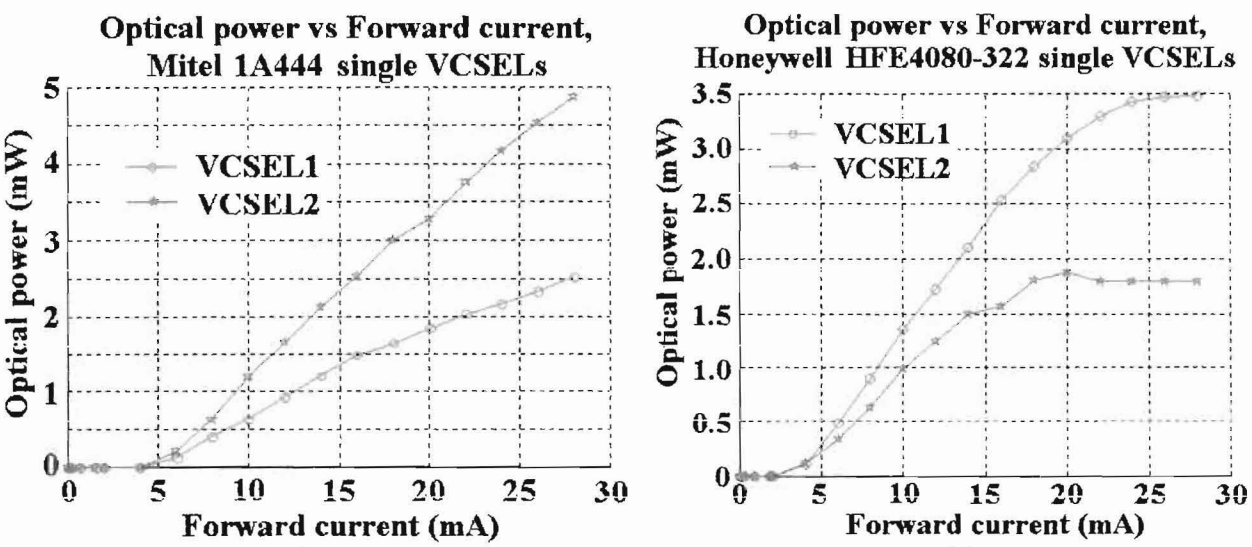
VCSEL Current (i) mA	VCSEL-1		VCSEL-2	
	Voltage (V) Volt	Intensity (I) µW	Voltage (V) Volt	Intensity (I) µW
0.167	1.39	0.018	1.39	0.017
0.672	1.48	0.165	1.48	0.153
1.5	1.55	0.495	1.55	0.456
2	1.59	0.728	1.60	0.714
4	1.70	2.196	1.72	2.265
6	1.80	132.000	1.83	205.000
8	1.88	397.000	1.91	611.000
10	1.96	629.000	2.00	1,190.000
12	2.04	917.000	2.09	1,650.000
14	2.10	1,202.000	2.16	2,119.000
16	2.17	1,475.000	2.24	2,519.000
18	2.23	1,635.000	2.30	3,000.000
20	2.30	1,846.000	2.37	3,288.000
22	2.36	2,044.000	2.44	3,759.000
24	2.42	2,164.000	2.50	4,170.000
26	2.48	2,334.000	2.57	4,528.000
28	2.52	2,517.000	2.62	4,870.000

Table 4: Intensity, voltage and current for the two Mitel VCSELs 1A444 with the lowest and highest optical power.

VCSEL Current (i) (mA)	VCSEL-1 Voltage (V) Volts	VCSEL-1 Intensity (I) µW	VCSEL-3 Voltage (V) Volts	VCSEL-3 Intensity (I) µW
0.273	1.39	0.014	1.39	0.010
0.9	1.47	0.092	1.47	0.072
1.795	1.54	0.303	1.54	0.245
2	1.56	0.365	1.56	0.277
4	1.67	112.000	1.67	151.000
6	1.77	487.000	1.76	446.000
8	1.85	897.000	1.85	864.000
10	1.94	1,352.000	1.94	1,275.000
12	2.03	1,723.000	2.03	1,555.000
14	2.10	2,099.000	2.11	1,808.000
16	2.19	2,532.000	2.19	1,988.000
18	2.26	2,845.000	2.27	2,126.000
20	2.34	3,103.000	2.35	2,234.000
22	2.42	3,290.000	2.43	2,479.000
24	2.49	3,430.000	2.50	2,522.000
26	2.56	3,474.000	2.58	2,407.000
28	2.63	3,484.000	2.65	2,557.000

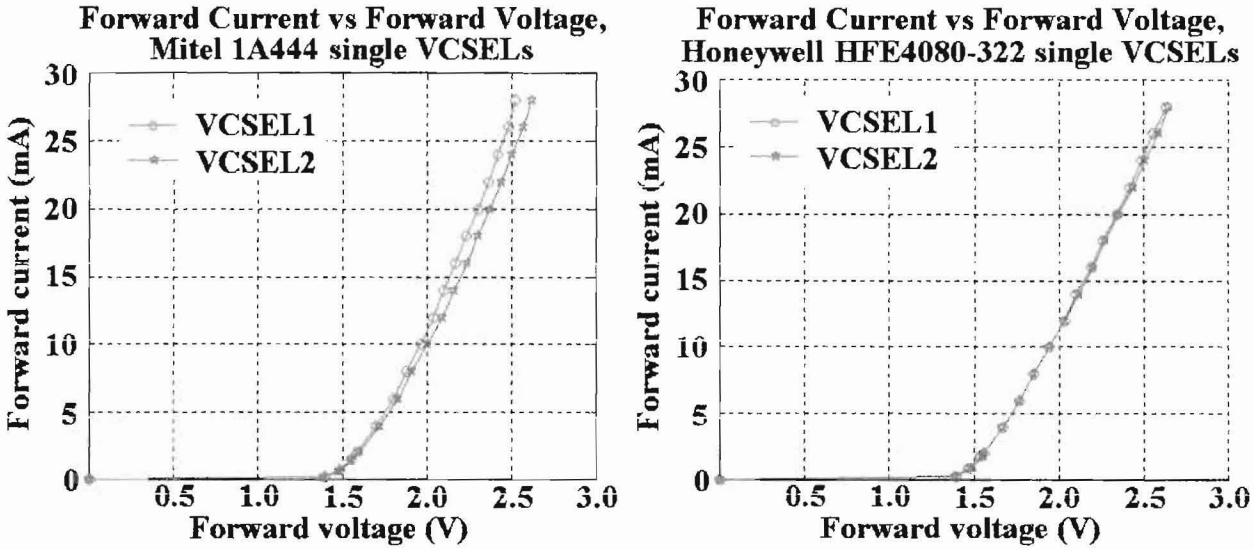
Table 5: Intensity, voltage and current for the two Honeywell HFE4080-322/XBA VCSELs with the lowest and highest optical power.

Figure 14 shows the Optical power as a function of forward current for both Honeywell and Mitel VCSELs and Fig. 15 shows the forward current as a function of forward voltage.



a) b)

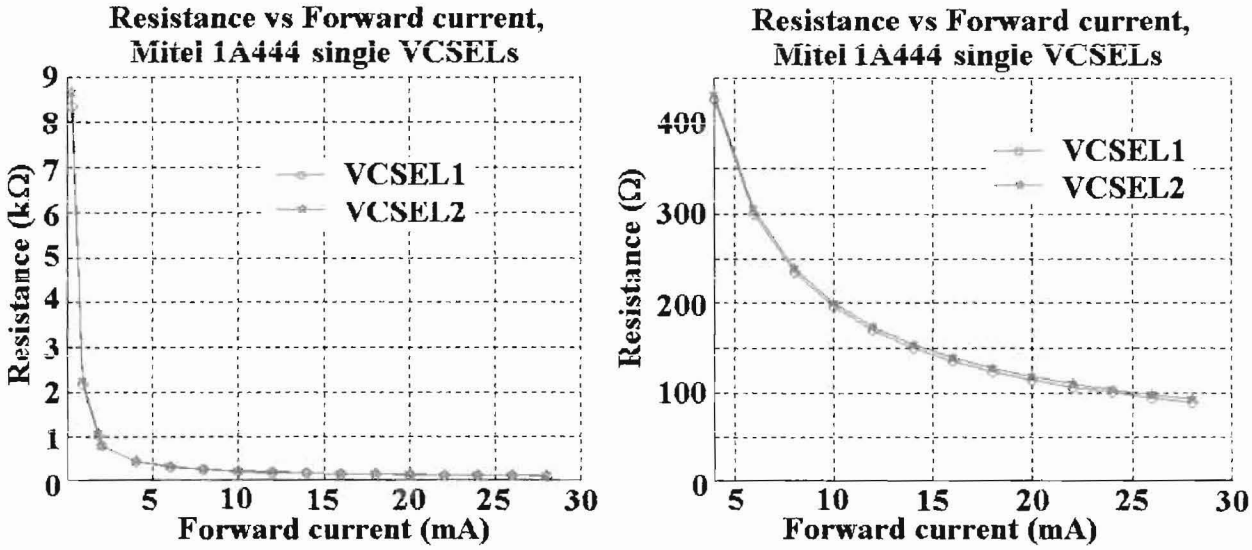
Figure 14: Optical power as a function of forward current for single VCSELs. a)Mitel 1A444 and b) Honeywell HFE4080-322.



a) b)

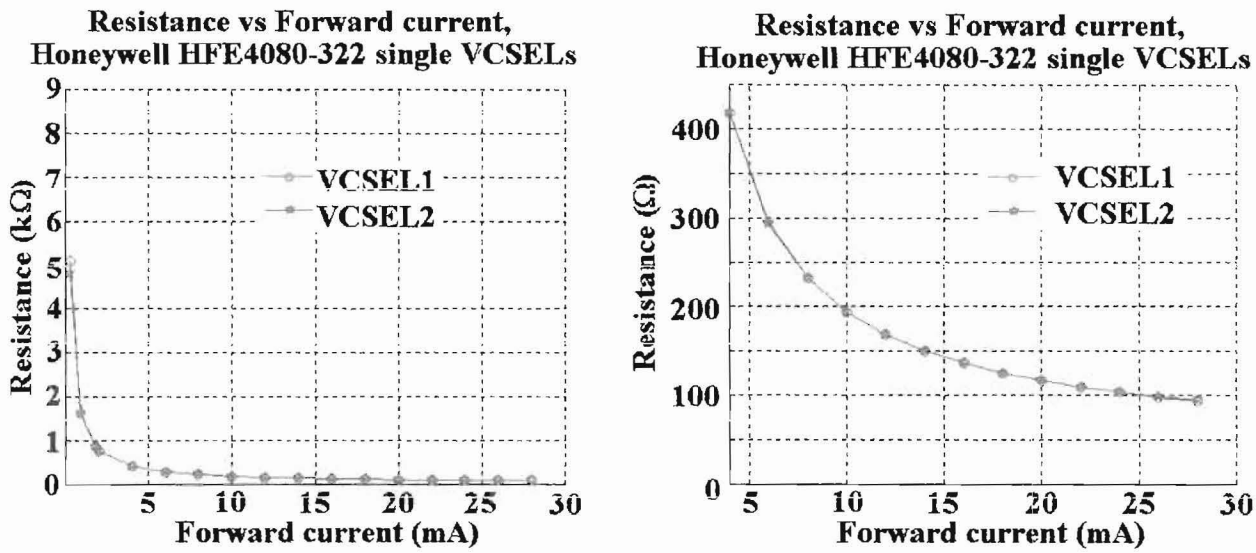
Figure 15: Forward current as a function of forward voltage for single VCSELs. a) Mitel 1A444 and b) Honeywell HFE4080-322.

Another important characteristic is the relationship between the resistance of the VCSEL and its forward current. We present plots showing this relationship as Fig. 16 for Mitel 1A444 single VCSELs and 17 for Honeywell HFE4080-322 single VCSELs.



a) b)

Figure 16: Resistance as a function of forward current. Mitel 1A444 single VCSELs. a) Forward current from 0-30 mA and b) Forward current from 4-30 mA.



a) b)

Figure 17: Resistance as a function of forward current. Honeywell HFE4080-322 single VCSELs. a) Forward current from 0-30 mA and b) Forward current from 4-30 mA.

A comparison between the characteristics of the Mitel single VCSELs and the Honeywell single VCSELs, shows that the Mitel single VCSEL offers better linearity in its optical power-forward current relationship. The results indicate that in all our designs we should use the Mitel 1A444 single VCSELs for best performance.

The PIN photodiodes used in photovoltaic mode are expected to have a linear relationship between the optical power impinging on them and the photocurrent generated. To verify this we have done a simple DC test. We took ten measurements of photocurrent for different values of optical power. The results are shown in Table 6.

Optical power (mW)	PIN photocurrent (μA)
0	0
0.470	208.2
0.861	387.1
1.270	607.1
1.655	766.7
2.056	973.8
2.474	1169.1
2.772	1301.8
3.025	1360.2
3.202	1486.0

Table 6: Test result on the Mitel 1A354 PIN photodiode.

These data are plotted in Fig. 18. The figure includes the result of a straight line fit to the data. We measured a PIN photodiode responsivity (R) equal to 0.46A/W in good agreement with the data sheet [16] value of 0.45A/W.

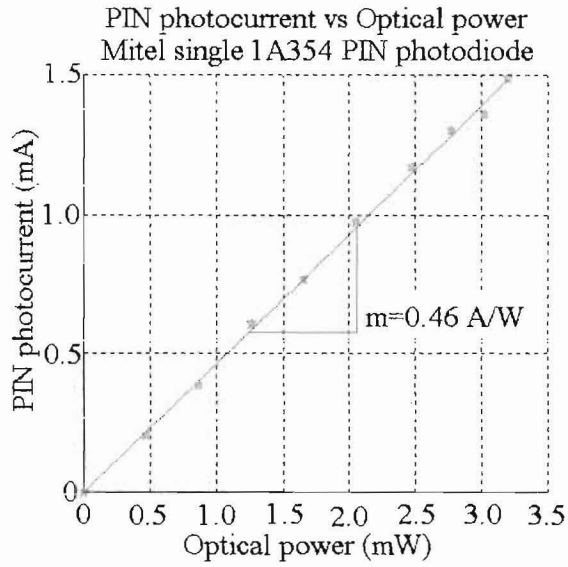


Figure 18: PIN photocurrent as function of Optical power.

We can see from Fig. 18 that the Mitel 1A354 PIN photodiode operated in photovoltaic shows a linear response, i. e. the PIN photocurrent is directly proportional to the optical power impinging on the detector.

2.1.2 Radiation harness Mitel and Honeywell single VCSELs

In the BTeV experiment, since the pixel vertex detector including the readout will be very close to the interacting beams, it is very important to know the radiation damage produced on VCSELs and PIN photodiodes. Radiation test results have shown that Mitel 1A444 VCSELs and the Honeywell HFE4080 VCSELs are radiation hard. Figure 19 and Fig. 20 show the radiation test result.

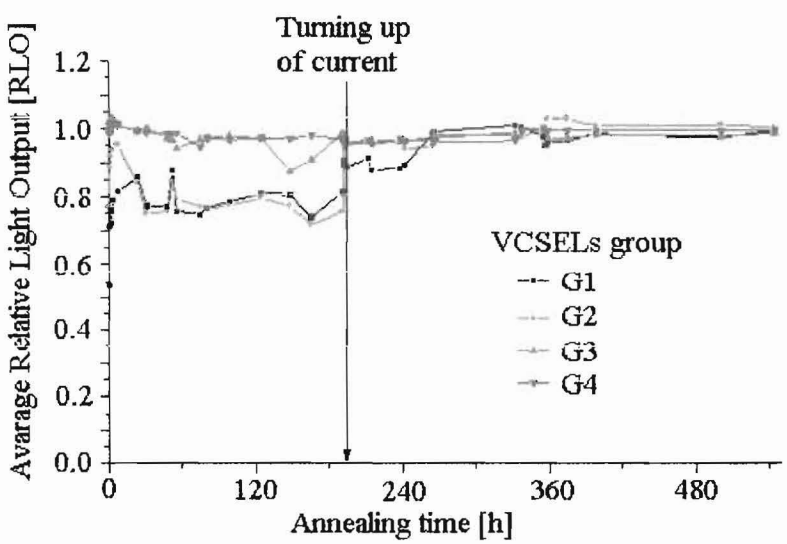


Figure 19: Radiation test on Mitel 1A444 single VCSELs [19].

Radiation tests on twenty MITEL 1A444 single VCSELs were done in order to test the annealing time required to bring them back to the original performance. The fluence was (4.1 +/- 1.39)* 10^14 n/cm^2. Figure 54 shows the relative light output (RLO) of these 20 VCSELs vs. Annealing time. These 20 VCSELs were divided into 4 groups called G1, G2, G3 and G4. Each group was driven with a different forward current: 10, 15, 20 and 25 mA respectively to study the annealing time vs forward current. The 4 curves always show the RLO group average. VCSELs which were irradiated with a fluence of 4.1x10^14 n/cm^2 annealed within seconds when they were driven with 20mA. Also, the VCSELs irradiated with 2.9x10^15 n/cm^2 annealed to an acceptable level in a reasonable time when driven with 20mA (order of 24 hours). The VCSEL irradiated with 4.1x10^14 n/cm^2 driven with 10 and 15 mA annealed rapidly. But they only annealed up to a level of 80%. There is no evidence of further annealing after the first minutes. On the other hand, when they are driven with 20 mA they anneal within seconds up to 100%. To determine whether these VCSELs annealed slowly just because the drive current was less than 20 mA, the current was turned up to 20 mA. They then annealed to a level of 100% (marked with an arrow in Fig. 19). The VCSELs driven with 10 mA appear to reach the 100% level very slowly. This is due to one slowly annealing VCSEL. The light outputs of the rest of this group rose directly up to 100% [19]. These test shown that the Mitel single VCSELs 1A444 are radiation hard.

Figure 20 shows the results of the radiation test performed on a Honeywell single VCSEL HFE4080. We can see from the figure that the PIN photodiode current in the receiver decreases because of the VCSEL radiation damage. The VCSEL's optical power decreased by up to 25 % after an irradiation of 10^13 p/cm^2. The result of this test shows that the Honeywell HFE4080 single VCSELs are somewhat radiation hard [20].

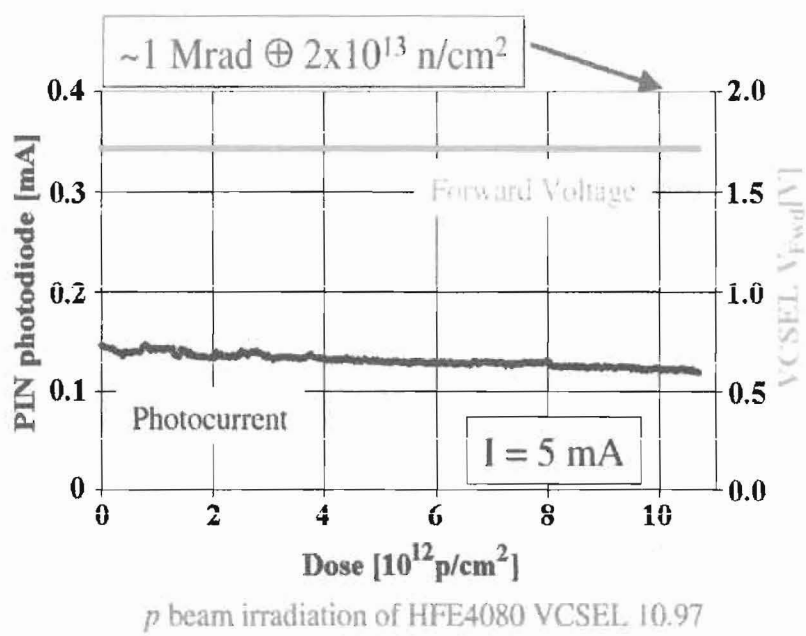


Figure 20: Radiation test on Honeywell HFE4080 single VCSEL [20].

2.1.3 AC test on single VCSELs and PIN photodiodes

To perform the AC tests on the Mitel 1A444 single VCSEL, we used a VCSEL driver and a voltage controlled crystal oscillator (VCXO) with the frequency fixed at 52 MHz. A multimode optical fiber carried the optical signal, which was measured using a Tektronix P6701A optical probe. Figure 21 shows a picture of the VCSEL driver used in the test.

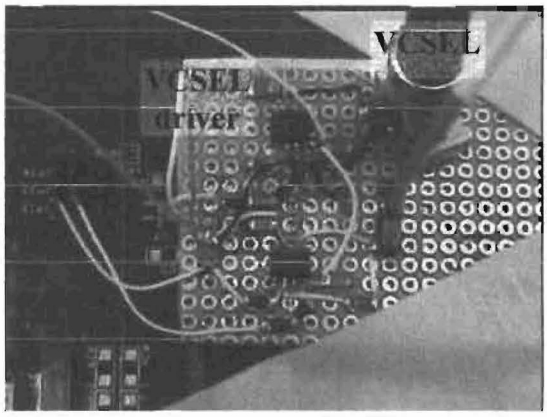


Figure 21: VCSEL driver used to make the high frequency tests on the Mitel 1A444 single VCSEL.

Figure 22 shows the rise time, fall time and jitter measured on the optical signal coming from the Mitel 1A444 single VCSEL. The measurement was made at the output of the optical fiber.

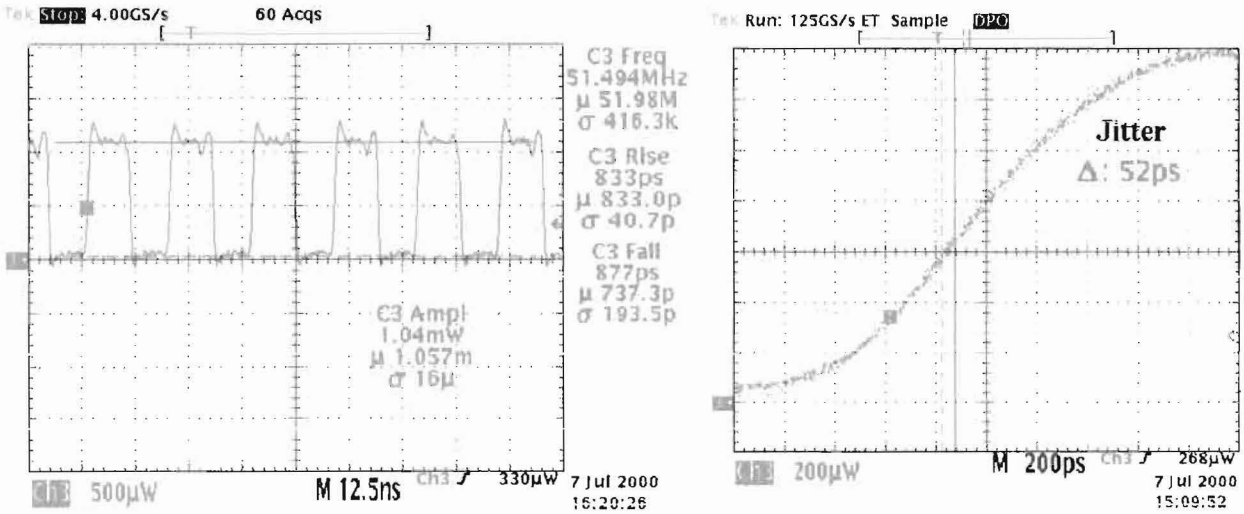


Figure 22: Rise time, fall time and jitter of the optical signal coming from the Mitel 1A444 single VCSEL at 52 MHz.

To perform the AC tests on the Mitel 1A354 single PIN photodiode, we used the setup shown in Fig. 23.

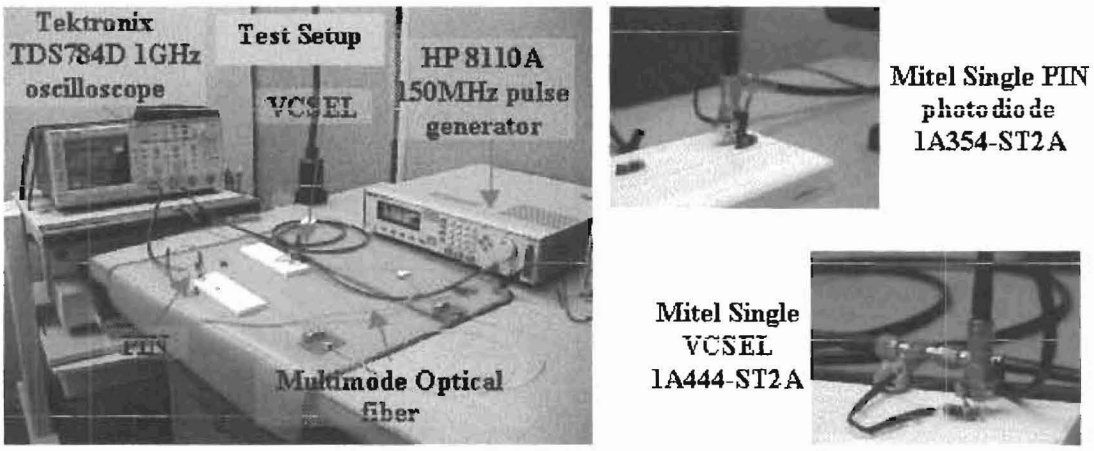


Figure 23: Test setup used to make the high frequency tests on the Mitel 1A354 single PIN photodiode.

Figure 24 shows the rise time, fall time and jitter measured on the PIN photodiode signal. The frequency used in the test was 20 MHz. The PIN photodiode was operated in photovoltaic mode. The waveforms are input to channel 1 (black trace) in the figure. As we can see the rise and fall times are only 600 ps and 980 ps respectively, and the jitter is 200 ps. The signal coming from the pulse generator had about 1.4 ns rise and fall times and a jitter of 110 ps. With these results we can see that the PIN photodiode response is very fast. This means that its cutoff frequency should be a lot higher than 20 MHz.

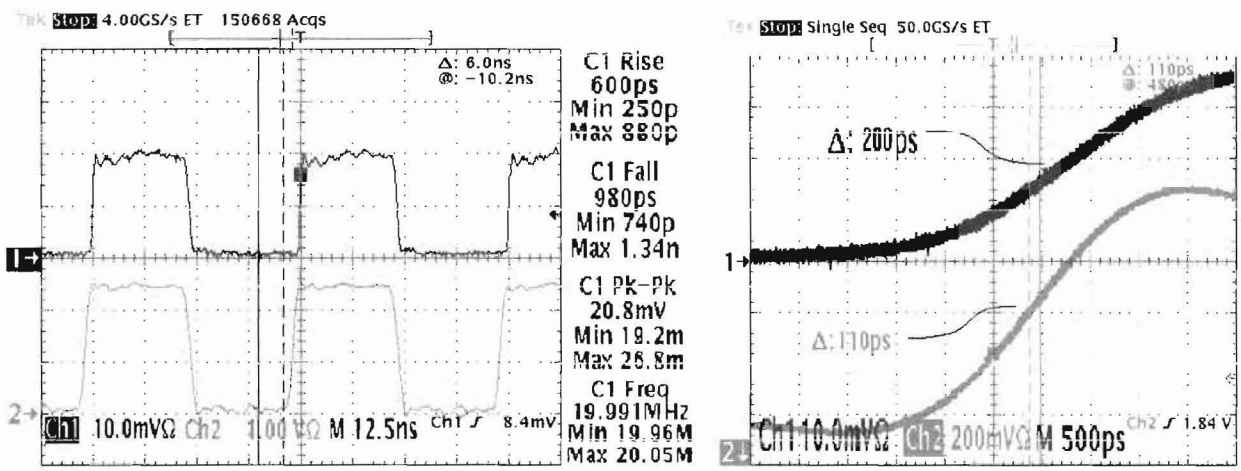
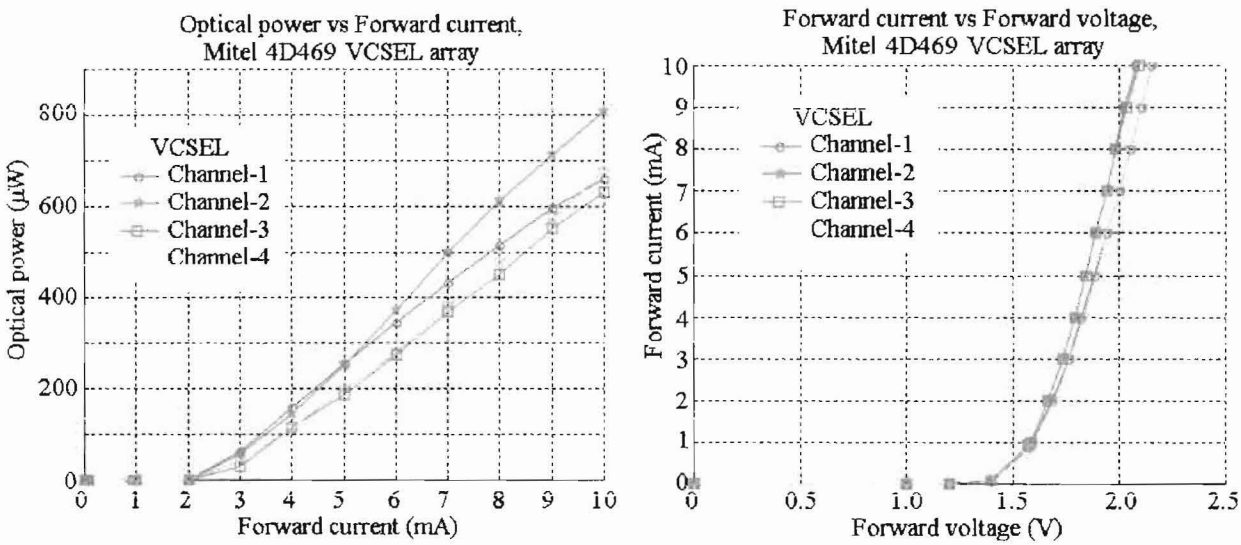


Figure 24: Rise time, fall time and jitter measured on the PIN photodiode's signal, the frequency used in the test was 20 MHz.

2.2 Performance of VCSEL and PIN photodiode arrays

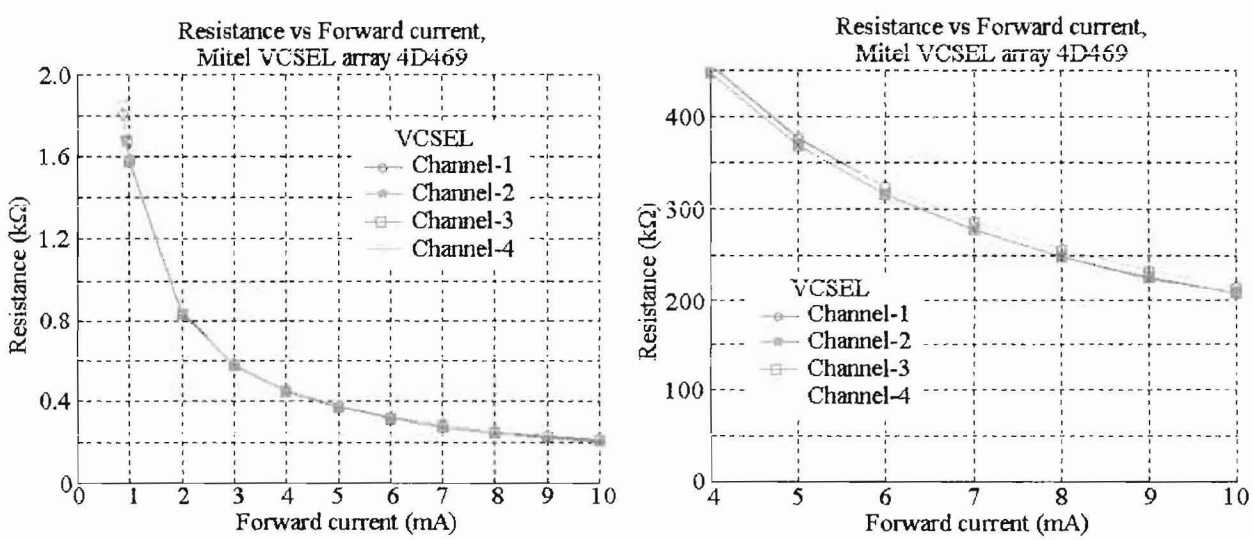
In this section we will show the results of tests performed on VCSEL and PIN photodiode arrays. To develop the DC test of all the VCSELs in the array we used the following instruments

and materials: Tektronix PS2521G programmable power supply, FLUKE 76 multimeter in current mode, Tektronix TDS 754C oscilloscope, 1m 4-channel fiber ribbon (62.5 μm/125 μm, core/cladding) assembled with MT-4 connectors. As an optical power meter we used the PIN photodiodes in the Mitel PIN array 4D470. The DC test on the VCSELs in the array consisted of measuring variations of optical power for changes in the forward current ranging from 1mA to 10mA in steps of 1mA, because the VCSELs in the array are DC current limited to 10mA [17]. Figure 25a shows the relationship between the optical power and the forward current of the 4 VCSELs contained in the Mitel VCSEL array 4D469. Figure 25b shows the relationship between the forward current and their corresponding forward voltage. Figure 26 shows the resistance as function of the forward current.



a) b)

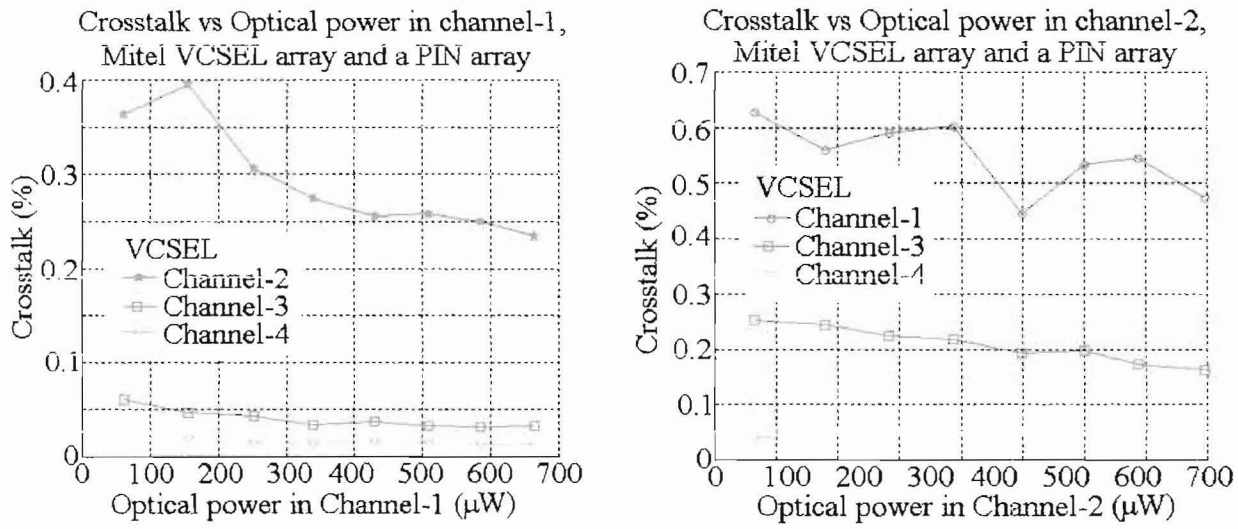
Figure 25: Characteristic curves for each VCSEL in the 4D469 VCSEL array. a) Optical power as a function of forward current and b) Forward current as a function of forward voltage.



a) b)

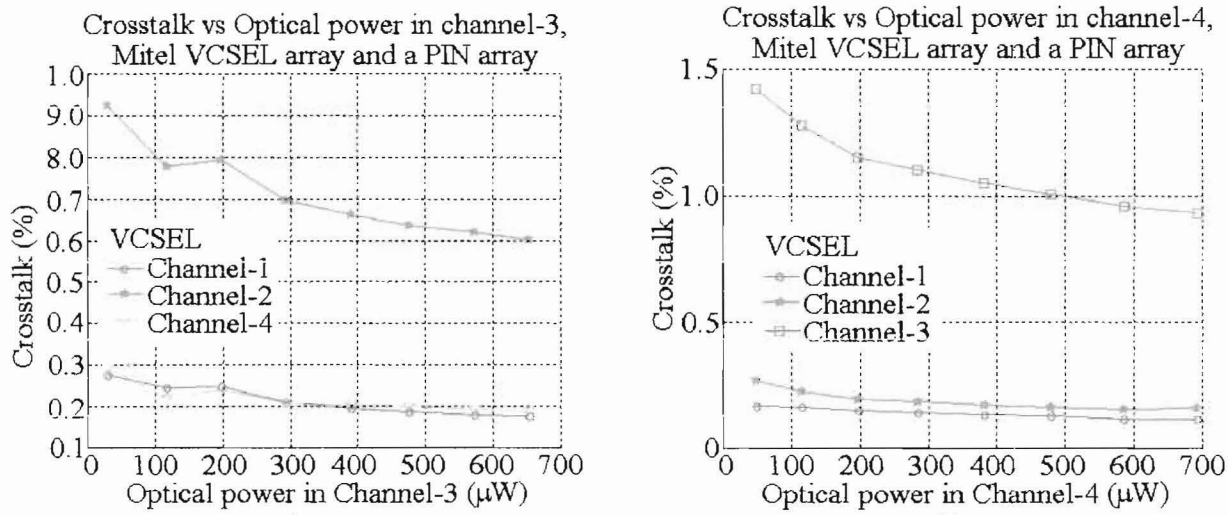
Figure 26: Resistance as a function of forward current. Mitel 4D469 VCSEL array. a) Forward current from 0-10 mA and b) Forward current from 4-10 mA.

In an optical link array the VCSELs and the PIN photodiodes are very closely packed. They are separated by only a few tens of microns in the array. Then it is very important to know how much crosstalk there is between the channels in the optical link array. Figure 27 and 28 shown the crosstalk measured. The optical link array is based on the Mitel 4D469 VCSEL array and the Mitel 4D470 PIN photodiode array.



a) b)

Figure 27: Crosstalk of the optical link array. a) Crosstalk produced by the optical power in channel-1 and b) Crosstalk produced by the optical power in channel-2.



a) b)

Figure 28: Crosstalk of the optical link array. a) Crosstalk produced by the optical power in channel-3 and b) Crosstalk produced by the optical power in channel-4.

From Fig. 27 and 28, we can see that the maximum crosstalk measured is 1.5 %.

2.2.1 AC tests on an optical link array

The AC test on the single VCSELs and PIN photodiodes was done at frequencies ranging from 0Hz to 50MHz, while the AC test on the link array was done over a wider range from 0Hz to 2GHz. The single VCSEL and the single PIN test range was limited to 50MHz because we did not have available a test board capable of operating at ultra-high frequencies. To perform the AC test on the single links and the link array between 0 Hz and 50 MHz, we used the following instruments and materials: Hewlett Packard 8110A 150 MHz Pulse Generator, Tektronix TDS 754C 500 MHz Oscilloscope, and three RG58C/U cables assembled with SMA connectors. To carry out the AC test between 50 MHz and 2 GHz on the 4-channel optical link array based on the Mitel 4D469 VCSEL array and the Mitel 4D470 PIN array we used the following instruments: HP 8133A 3 GHz pulse generator and Tektronix TDS794D 2 GHz oscilloscope. A picture of this setup is shown as Fig. 29.

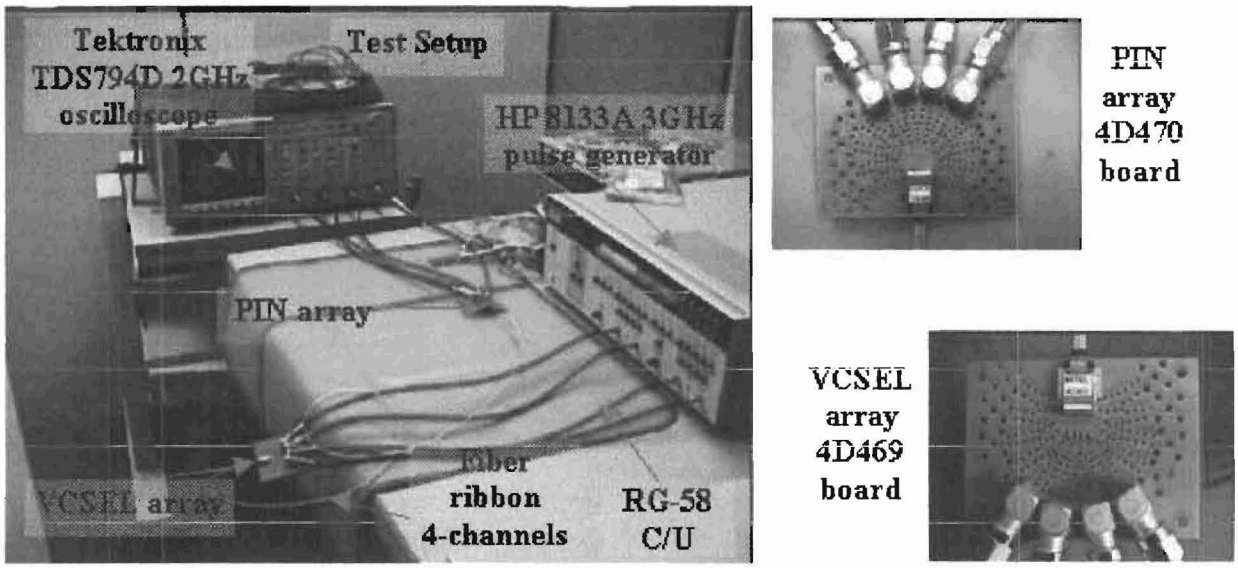


Figure 29: Test setup used to make the ultrahigh frequency tests on the Mitel VCSEL array and PIN array.

The AC test on the 4-channel array consisted of measuring the jitter, rise time, fall time, cutoff frequency and the optical power response without previous applied bias. The test was done using the following test setup: one output channel from the pulse generator was connected in series with a 30 ohm resistor. This resistor was connected in series with the VCSEL's anode and the VCSEL's cathode was connected to ground. Also, the VCSELs were connected to the fiber ribbon by means of the MT-4 connector. The fiber ribbon was connected to the PIN photodiodes in the array using a MT-4 connector too. Each PIN's cathode was connected to ground and the PIN's anode was connected in series with a 30 ohm resistor, the other leg of which was connected directly to a channel of the oscilloscope. The oscilloscope was set to 50 ohms input. The pulse generator drove the VCSEL directly while we took all the measurements with the oscilloscope. Note that all the PIN photodiodes were used in photovoltaic mode as with the single PIN photodiodes. To obtain the cutoff frequency we measured the voltage peak-peak

at low frequencies and then looked for the frequency at which the voltage peak-peak was three dB lower than this.

The rise and fall times of each VCSEL connected to its corresponding PIN photodiode in the array are shown in Fig. 30.

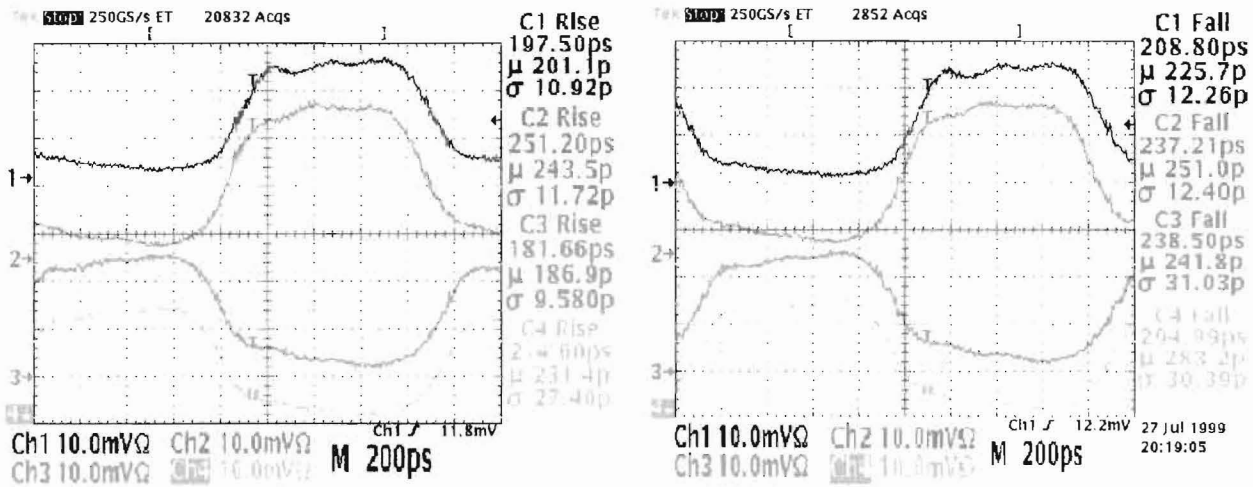


Figure 30: Rise and fall times on each channel contained in the link array. The PIN photodiodes are receiving the optical signal from the VCSEL by means of the fiber ribbon. The frequency used in this test was 550 MHz.

The jitter present in each channel of the optical link array is shown in Fig. 31.

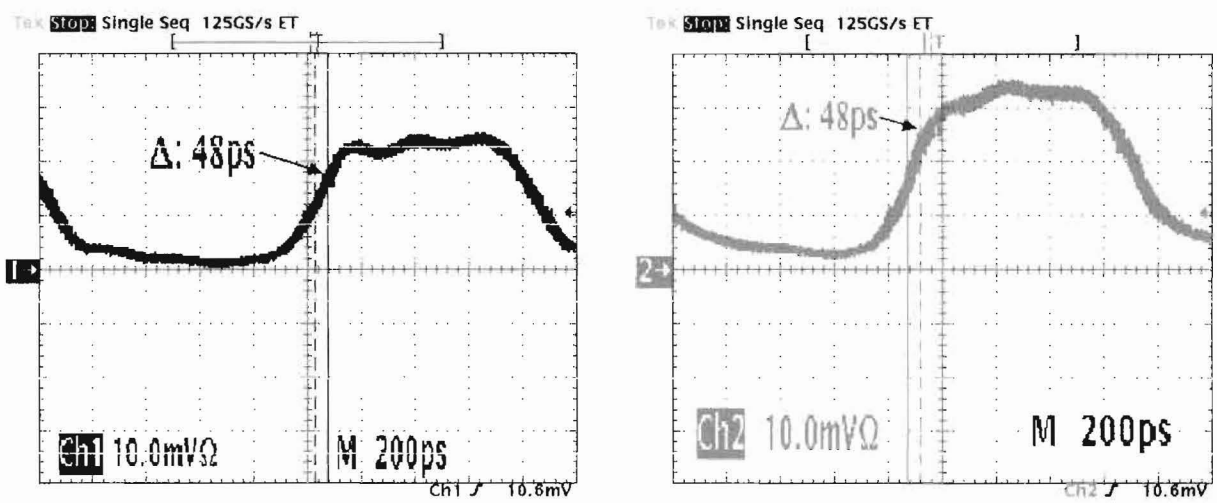
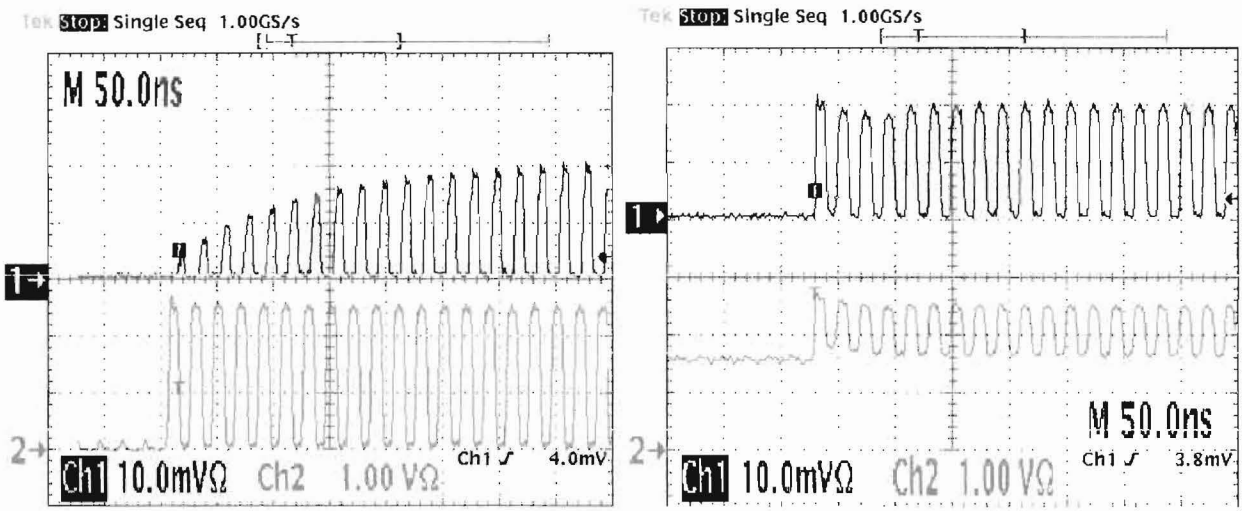


Figure 31: Jitter in channel-1 and channel-2 contained in the link array. The frequency used in this test was 550 MHz.

As we can see from Fig. 31 the jitter produced by all the channels in the link array is very low, only 48ps. This is approximately the same jitter measured for the Mitel single VCSEL, and is less than the jitter seen in the single link based on the Mitel single VCSEL and the Mitel single

PIN photodiode, which was about 200ps. However, we should take into consideration that the pulse generator and the VCSEL driver used to perform the tests are different sources and have different jitter, which has a big impact in the results. The conclusion is: single VCSELs, single PINs, VCSELs in arrays and PINs in arrays do not increment the jitter substantially. Thus jitter in the optical readout circuit will be a function of the jitter generated by the device driving the VCSEL.

The measurement of transient is very important because we need for the VCSEL to reach full optical power when we start to transmit data. The result of the test is shown as Fig. 32. The transient was seen to depend on the bias applied prior to pulsing the VCSEL driver.



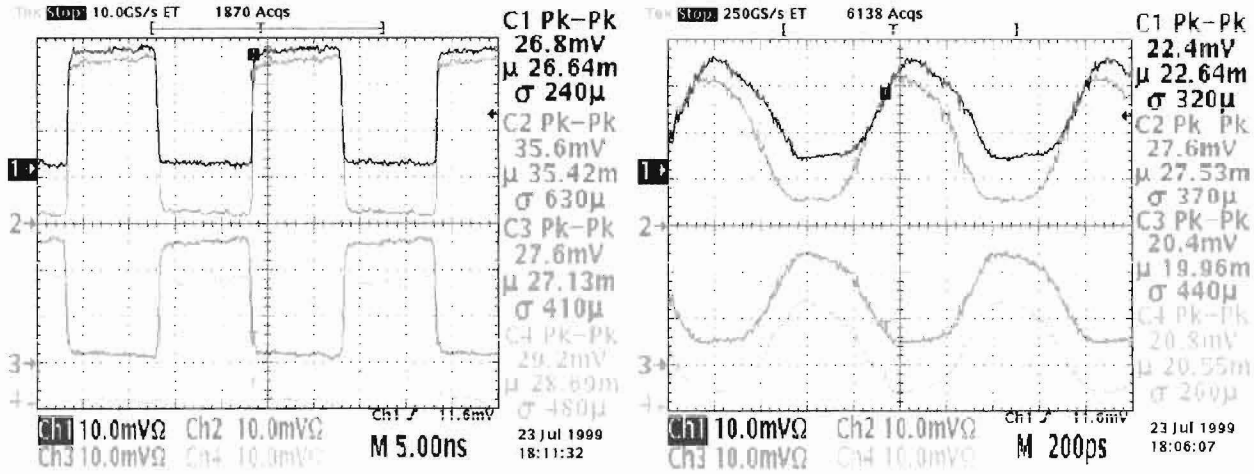
a) b)

Figure 32: Transient channel-1 in the link array. a) Transient when we do not drive the VCSEL with a previous applied bias and b) Transient when one applies a previous bias to the VCSEL.

As we can see from Fig. 32, there is a big difference in the transient when we drive the VCSEL with a previous applied bias and without. This effect can be explained as follows: The VCSELs without previous applied bias do not have enough carriers to generate photons when the VCSEL is turned on. This effect is present in all the VCSELs, including the single VCSELs and the VCSELs in the arrays. The previous biasing produces enough carriers before the VCSEL is turned on. Then, when the VCSEL is turned on, it is able to emit its normal optical power. In conclusion the best way to drive the VCSELs is to apply a current bias in addition to the current modulation.

The bandwidth of the VCSELs and PIN photodiodes determines the maximum frequency at which the readout of the pixel hits can proceed. We have therefore performed tests to measure the cutoff frequency of the channels in the optical link array. As we indicate previously, we were not able to measure the cutoff frequency for the links based on single VCSELs and single PIN photodiode because we did not have a fast enough board to run ultra-high frequency tests. However, the Mitel VCSEL array and the Mitel PIN array have a board provided by the manufacter that operates at frequencies up to a few GHz. The test results show that all the channels in the optical link array are able to transmit up to 1.18 GHz, which implies that we can

transmit up to 2.36 Gbps in each channel in the array. This gives us the possibility to transmit in total about 8 Gbps by one 4-channel optical link array. The test results are shown as Fig. 33.



a) b)

Figure 33: Cutoff frequency for each channel in the link array. a) Test at 50 MHz and b) test at 1.18 GHz.

We can see from Fig. 33 that channel-1 has the lower cut frequency. Then we will take 1.18 GHz as cutoff frequency for all channels in the array to guarantee good transmission in all of them. With this cutoff frequency we can transmit up to 2.36 Gbps per channel. Another important result is that all the PIN photodiodes in the array were operated successfully in photovoltaic mode at ultra-high frequency.

Table 7 summarizes the performance test results in AC on the single optical link and the optical link array.

	Rise time (ps)	Fall time (ps)	Jitter (ps)	Cutoff frequency (GHz)	Crosstalk (%)
Single optical link (based on the Mitel 1A444 single VCSEL and the Mitel 1A354 PIN photodiode)	833	877	200	No Available	It don't apply to single links
Optical link array 4-Channel (based on the Mitel 4D469 VCSEL array and the Mitel 4D470 PIN photodiode array)	250	250	48	1.18	1.5 maximum

Table 7: Performance test results on the single optical link and the optical link array.

2.3 Conclusions

The Mitel single VCSELs show better performance than the Honeywell single VCSELs, e. g. the Mitel VCSELs have a linear optical power-forward current relationship. The optical power variation between the Mitel single VCSELs is very large, up to 80%. We need to find a means by which we can reduce the optical power variation between the Mitel VCSELs. All the Mitel PIN photodiodes used in photovoltaic mode have demonstrated excellent performance at ultra-high frequency (~GHz). The Mitel and Honeywell single VCSELs are radiation hard (10^13 n/cm^2), The Mitel single VCSELs have shown rise and fall times about 800 ps and might be even faster but the cutoff frequency test could not be performed. This Mitel single VCSEL also had only 50ps of jitter and a threshold of only 4mA. All these characteristics make the Mitel single VCSEL 1A444 an excellent choice to be used in optical links of high and ultra-high frequencies. The VCSEL and PIN arrays showed very good performance with rise and fall times of only 250 ps, a jitter of 48 ps, a cutoff frequency of 1.18 GHz, current threshold of only 2 mA, and a maximum crosstalk of only 1.5 %, which is negligible. The PIN photodiodes in the array used in photovoltaic mode as for the single PIN photodiodes are able to work at ultra-high frequencies. The best way to drive the VCSEL is with previously applied current bias plus a modulated current.

Now that we have established that the Mitel single VCSEL and PIN are an excellent choice for our optical readout system. Then in the next chapter we will work on designing a VCSEL driver and a PIN receiver to be able to make the 106 Mbps optical link.

Chapter Three

Designing a 106Mbps digital optical link

In this chapter we will design the VCSEL driver and the PIN receiver circuits. The VCSEL driver should be designed to minimize the optical power variation between different Mitel single VCSELs and produce as low jitter and as fast rise and fall times as possible. The PIN receiver should be able to recover the digital signal with low jitter and fast rise and fall times.

3.1 VCSEL driver

Traditionally laser diodes have been driven with current. However, if we drive the Mitel single VCSELs 1A444 with current we will get up to 80% of optical power variation between them. We need to look for a means by which to drive the VCSELs to get a smaller optical power variation. The performance tests showed that the VCSELs with the highest optical power have also the highest forward voltage, and the VCSELs with the lowest optical power have the lowest forward voltage. This result was seen for both the Mitel and Honeywell VCSELs. This is very interesting, because if we apply the same forward voltage, then the VCSELs with the highest optical power emission will have a smaller forward current than the VCSELs with the lowest optical power emission. This should produce a smaller optical power variation between them. This can be verified observing the relationship between the optical power and the forward voltage for Mitel single VCSELs 1A444 shown as Fig. 34.

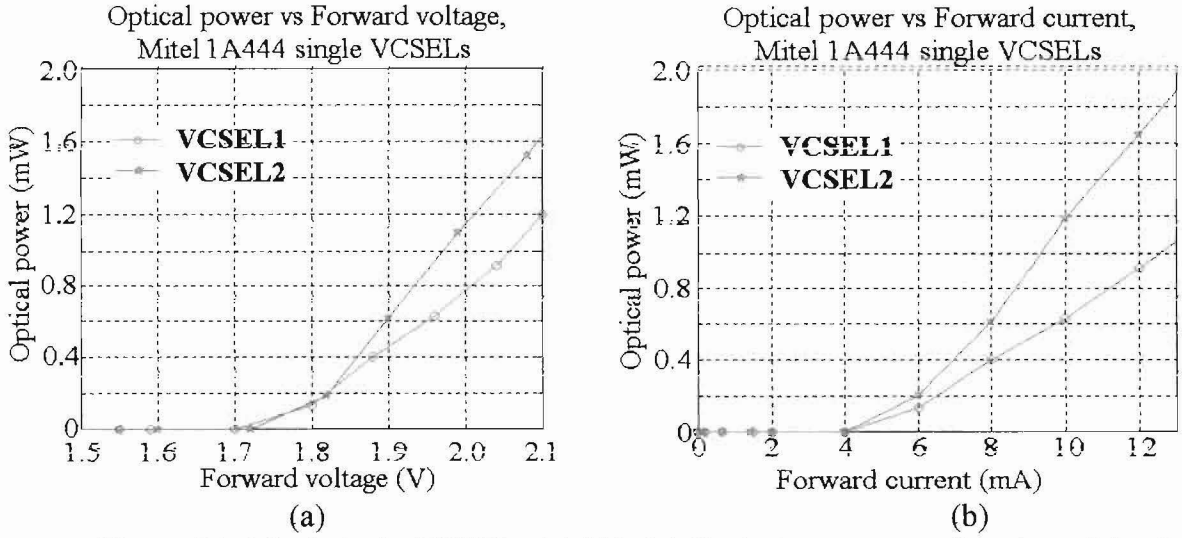


Figure 34: Mitel single VCSELs 1A444. (a) Optical power as a function of the forward voltage, and (b) Optical power as function of the froward current.

We can see from Fig. 34b that with forward current of 12.5 mA we produce 1 mW of optical power from VCSEL1 and 1.8 mW from VCSEL2. This is an 80% optical power variation between them with respect to the lower optical power. When we drive the VCSELs with voltage, we get a maximum variation of only 40 % at 2.05 V, see Fig. 34a.

The VCSEL BTeV prototype driver based on the National CLC449 monolithic Op. Amp. [22] is shown as Fig. 35.

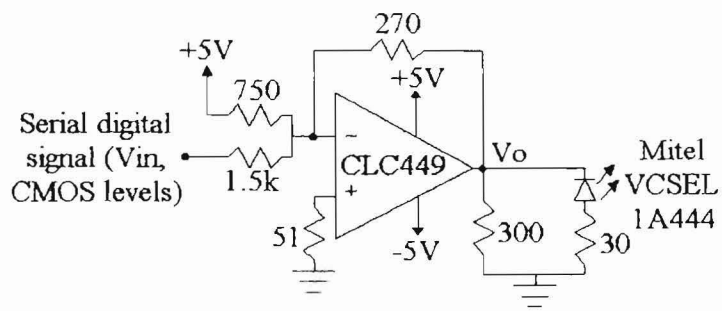


Figure 35: VCSEL driver connected with the Mitel single VCSEL 1A444.

The equation that describes the VCSEL driver is:

$$-\frac{Vin}{1.5k}-\frac{5V}{750}-\frac{Vo}{270}=0, \tag{2}$$

where Vin is the CMOS digital signal, and Vo is the voltage output.

Using Eqn. 2 we write the voltage output (Vo) as

$$Vo=-1.8V-0.18Vin, \tag{3}$$

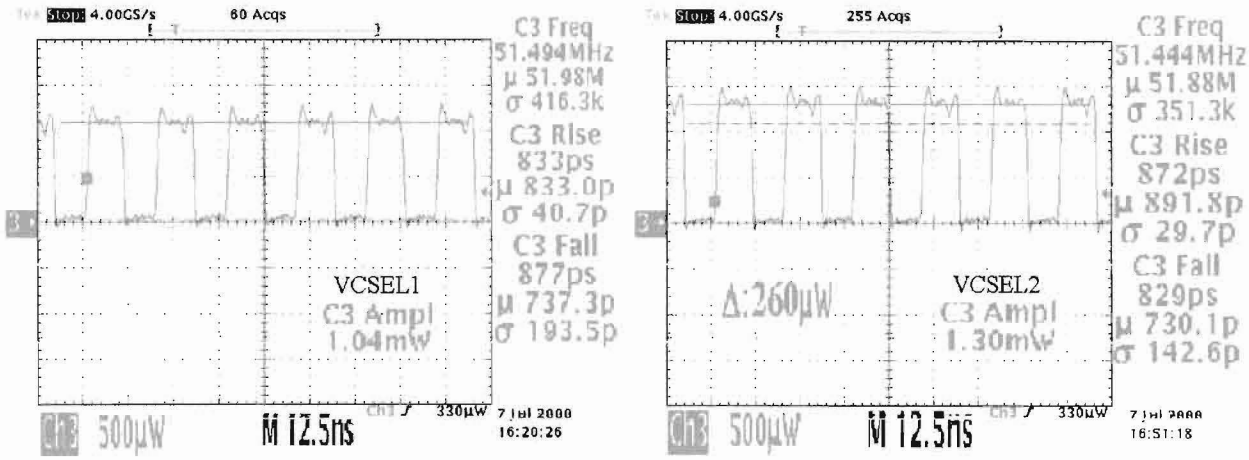
From Eqn. 3 we can obtain that

$$V_{OL}=-1.8V \text{ and } V_{OH}=-2.4V, \tag{4}$$

where V_{OL} represents the voltage corresponding to the optical power, low level. A V_{OH} represents the voltage for the high level of optical power. These voltage levels were chosen to get 1mW of optical power (high level) from the Mitel 1A444 single VCSEL that emits the lowest optical power of the six we tested.

Tests performed using the BTeV prototype VCSEL driver have shown that there is actually only a maximum of 25 % optical power variation between different Mitel VCSELs instead of the 80 % of optical power variation that we got driving these VCSELs with current and even somewhat lower variation than the 40 % we saw in our preliminary DC tests. Figure 36 show the optical signals emitted by the Mitel single VCSELs 1A444 with the lowest and highest optical power. The optical signals in Fig. 36 are shown as they are seen on a Tektronix TDS

784D digital oscilloscope. The optical signals are input to the oscilloscope by means of the Tektronix P6701A optical probe.



(a) (b)

Figure 36: Optical signals emitted by the Mitel single VCSELs 1A444 using the VCSEL driver. (a) VCSEL1 and (b) VCSEL2.

3.2 PIN receiver

The PIN receiver utilizes a Mitel 1A354 PIN photodiode or a Lasermate RST-M85A306 PIN photodiode operated in photovoltaic mode. This is connected to an amplifier based on the CLC449; the output of the amplifier is connected to a discriminator MAX999 [23] that recovers the digital signal as shown in Fig. 72. The discriminator has a threshold of 33mV, which is well above the noise level but still low enough to ensure that all data bits are received.

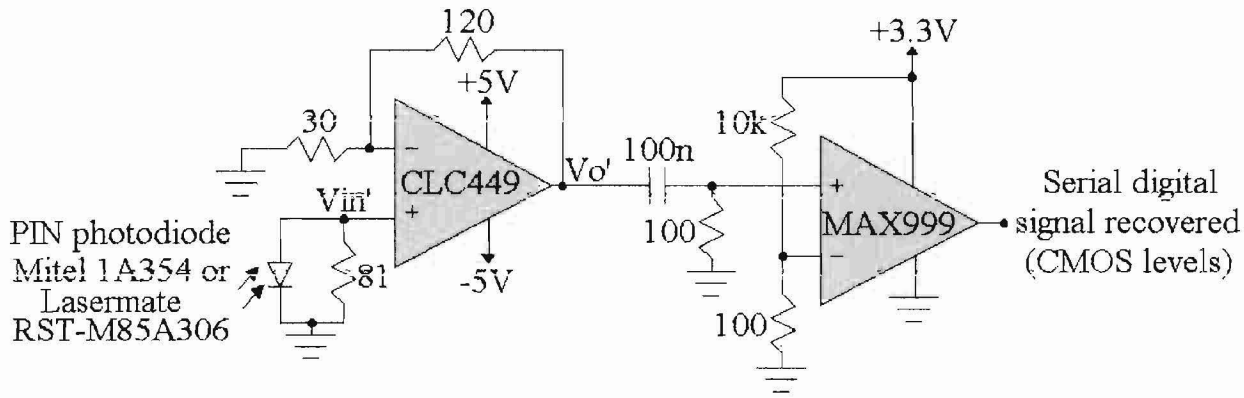


Figure 37: PIN receiver connected with the Mitel PIN photodiode 1A354 or the Lasermate PIN photodiode RST-M85A306.

Equation 5 describes the amplifier based on the CI CLC449 shown on Fig. 37.

$$Vin'\left(\frac{1}{120}+\frac{1}{30}\right)-\frac{Vo'}{120}=0 \tag{5}$$

where Vin' = SP_iR_L, S is the sensitivity of the PIN photodiode, R_L is equal to 81Ω, P_i is the optical power impinging on the PIN photodiode, and Vo' is the amplifier voltage output.

Using Eqn. 5 we can get Vo' as

$$Vo'=182.25\frac{mV}{mW}P_i \tag{6}$$

where P_i is the optical power impinging on the PIN photodiode

From the equation we can see that if P_i is equal to 1 mW then the amplifier output would be 182.25 mV. As the 100 nF capacitor holds the DC component then the signal at the input of the discriminator MAX999 would have a Vpp equal to 182.25 mV. This voltage is very small and we need to be very careful about the noise generated by the other devices in the vicinity of the PIN receiver. When the PIN receiver is located near a source of noise we can increase the load resistance (R_L) value. But this increment is inversely proportional to the bandwidth, i. e. if you increase the load resistance value then the bandwidth will be narrower.

The PIN receiver is an inherently low noise circuit, because the PIN photodiode is being used in photovoltaic mode [4]. Since modern PIN photodiodes are fast enough to operate without a bias voltage being applied, both the dark current and the noise produced by a power supply used to do the biasing can be avoided. In the absence of an applied electric field, charge motion is caused only by the small electric field produced by the electron-hole pairs generated in the depletion region of the PIN photodiode [5]. Also, the depletion region is limited in size by the properties of the device, since there is no reverse bias voltage applied which would increase its size. We believe that this will reduce the impact of Single Event Upset (SEU) due to strong interactions in the PIN photodiodes and plan to carry out tests to demonstrate this in the near future.

3.3 Schematic of the 106 Mbps

The 106 Mbps digital optical link transmitter consists of the VCSEL driver and the Mitel single VCSEL 1A444. The 106 Mbps digital optical link receiver contains of the PIN receiver and the Mitel single PIN photodiode 1A354 or the Lasermate PIN photodiode RST-M85A306. The schematic of the complete 106 Mbps digital optical link is shown as Fig. 38.

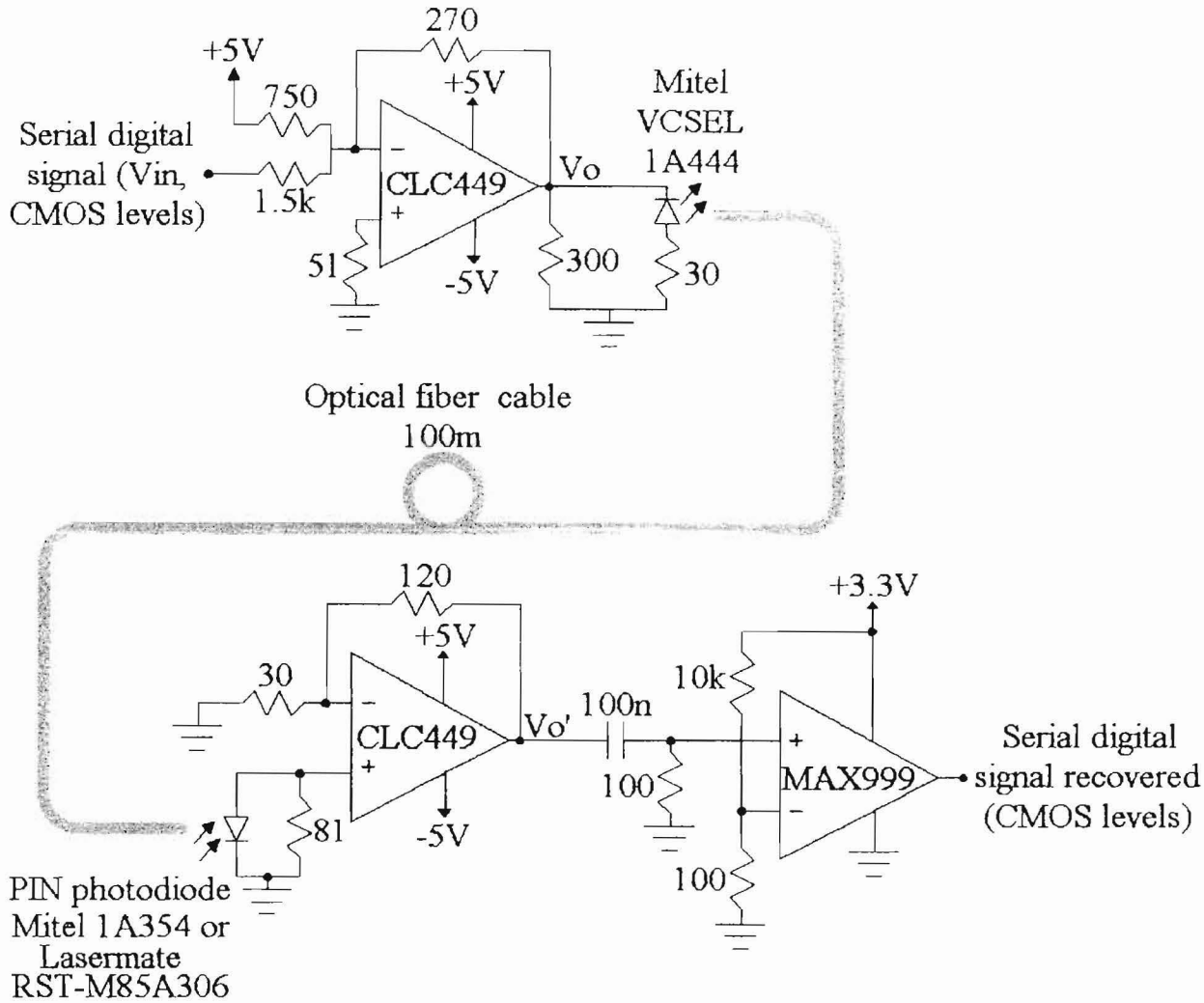


Figure 38: Schematic of the 106 Mbps digital optical link.

3.4 Conclusions

The 106 Mbps optical link transmitter was designed to produce a minimum variation in optical power between different Mitel 1A444 VCSELs. Measurements have shown that if we drive the VCSEL with current we get up to 80% optical power variation among the VCSELs under test. When we drive the VCSELs with voltage with the BTeV prototype driver, we get a maximum variation of only 25%. This difference provides an important safety margin, especially when designing a driver for use in a high radiation environment where performance may be degraded progressively by radiation damage.

The 106 Mbps optical link receiver is an inherently low noise circuit, because the PIN photodiode is being operated in photovoltaic mode [11]. Since modern PIN photodiodes are fast enough to operate without a bias voltage being applied, both the dark current and the noise produced by a power supply used to do the biasing can be avoided. In the absence of an applied

electric field, charge motion is caused only by the small electric field produced by the electron-hole pairs generated in the depletion region of the PIN photodiode [21]. Also, the depletion region is limited in size by the properties of the device, since there is no reverse bias voltage applied which would increase its size. We believe that this will reduce the impact of Single Event Upset (SEU) due to strong interactions in the PIN photodiodes and plan to carry out tests to demonstrate this in the near future.

The 106 Mbps link receiver has a capacitor to hold the dc component of the incoming signal, which obligates us to keep the DC balance in the channel. This helps to make the receiver less sensitive to the optical power variation between different VCSELs. There are special codes to keep the dc balance. One of them is the Biphase Mark code. In the next chapter we will work on designing a Biphase Mark encoder and decoder.

Chapter Four

Designing a Biphase Mark Encoder and Decoder

As we have seen, to get the best performance from our 106 Mbps optical link, we need to keep the DC balance in the channel. To do this we use the Biphase Mark code: this code combines the clock signal and the command signal to generate one signal with a constant DC level. The encoding scheme is shown as Fig. 39.

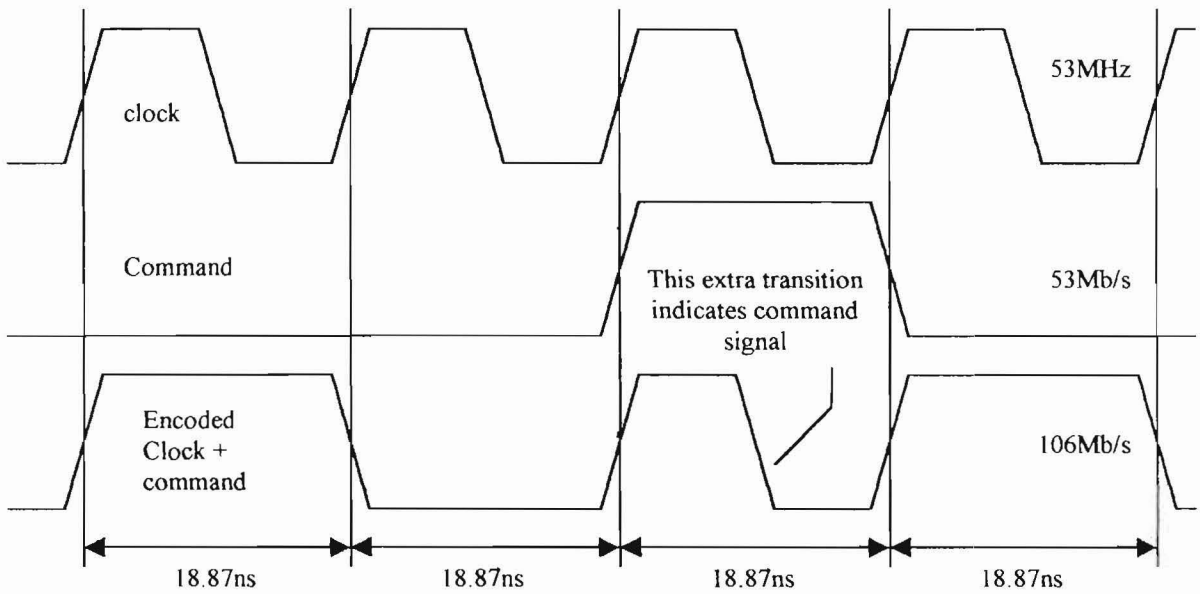


Figure 39: Biphase-Mark encoded clock and command signals.

Biphase-Mark code sends transitions corresponding to the clock signal leading edges only. Extra transitions at the clock trailing edges indicate command signals. The clock signal has to be regenerated from leading edge transitions and the command signals from the extra trailing edge transitions.

When one want to use Bipahse-Mark code, one needs to keep in mind that to recover this code we need to synchronize the incoming signal with the reference clock signal in the receiver in some way. Also, to decode the incoming Biphase-Mark signal, we need to use a square signal with a frequency two times the clock frequency. Then we need to be careful that the jitter and the pulse length distortion of the decoded output signal be as low as possible so that these effects do not cause loss of synchronization.

To implement the Biphase-Mark encoder and decoder we will use Field Programmable

Gate Array (FPGA).

4.1 Altera FPGAs

Altera [24] has many families of FPGAs, which are shown in Table 8

Device Family	User I/O pins	Usable Gates	Core Voltages
APEX 20K	252 to 808	65,024 to 1,520,640	2.5 V and 1.8 V
ACEX	130 to 333	10,000 to 150,000	2.5 V and 1.8 V
FLEX 10K	59 to 470	10,000 to 250,000	2.5 V, 3.3 V and 5.0 V
FLEX 6000	71 to 218	10,000 to 24,000	3.3 V and 5.0 V
FLEX 8000	68 to 208	2,500 to 16,000	3.3 V and 5.0 V
MAX 9000	59 to 216	6,000 to 12,000	5.0 V
MAX 7000	36 to 212	600 to 10,000	2.5 V, 3.3 V and 5.0 V
MAX 3000	34 to 158	600 to 5,000	2.5 V and 3.3 V
Classic	22 to 64	300 to 900	5.0 V

Table 8: Altera devices families: User I/O pins, usable gates and core voltages.

To select a device family for our design, we use the following scheme provided by Altera:

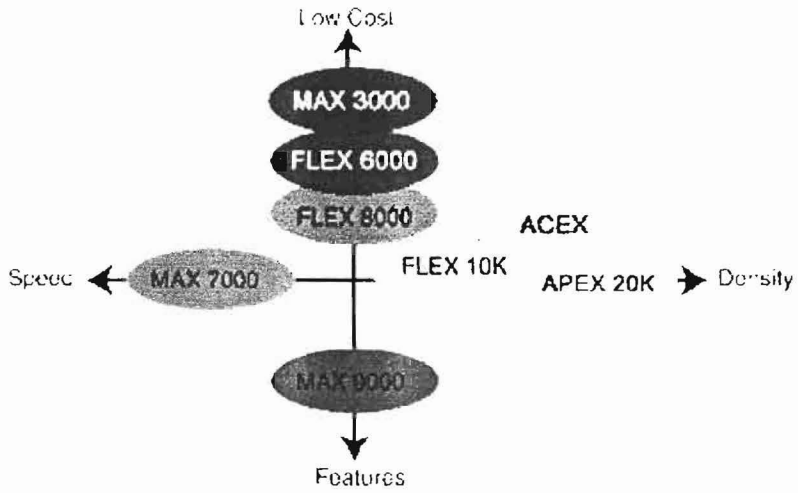


Figure 40: Altera device selection [24].

In our case we need speed. Thus we will focus on the MAX7000 device family. Table 9 shows the features of these devices [25].

Feature	EPM7032AE	EPM7064AE	EPM7128AE EPM7128A	EPM7256AE EPM7256A	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212

Table 9: MAX7000A device features [25].

We need an FPGA with at least 85 user I/O pins and a time response of 5ns. As we can see from the table above the EMP7128AE and the EMP7128A have 100 user I/O pins. Table 10 shows the speed grade for the MAX7000A devices.

Device	Speed Grade					
	-4	-5	-6	-7	-10	-12
EPM7032AE	✓			✓	✓	
EPM7064AE	✓			✓	✓	
EPM7128A			✓	✓	✓	✓
EPM7128AE		✓		✓	✓	
EPM7256A				✓	✓	✓
EPM7256AE		✓		✓	✓	
EPM7512AE				✓	✓	✓

Table 10: MAX7000A speed grades [25].

From the table we can see that the EMP7128AE is faster than the EPM7128A, then we will use the Altera EMP7128AE-5 FPGA.

4.1.1 Programming the Altera FPGAs

Today the FPGAs can be so complex that we need to use software to make it easier to program them. Altera offers MAX PLUS II [26] and Quartus [27] software to program their FPGAs. Quartus is a software package able to program the most sophisticate FPGAs, up to 1,500,000 usable gates. For us the MAX+PLUS II software is sufficient to use to program the Altera EMP7128AE-5 FPGA.

The Altera Multiple Array MatriX Programmable Logic User System (MAX+PLUS II) provides a multi-platform, architecture-independent design environment that easily adapts to our specific design needs.

MAX+PLUS II applications software, shown in Fig. 41, is a fully integrated package for creating logic designs for Altera FPGAs (including the Classic, MAX 5000, MAX 7000, MAX 9000, FLEX 6000, FLEX 8000, and FLEX 10K families of devices).

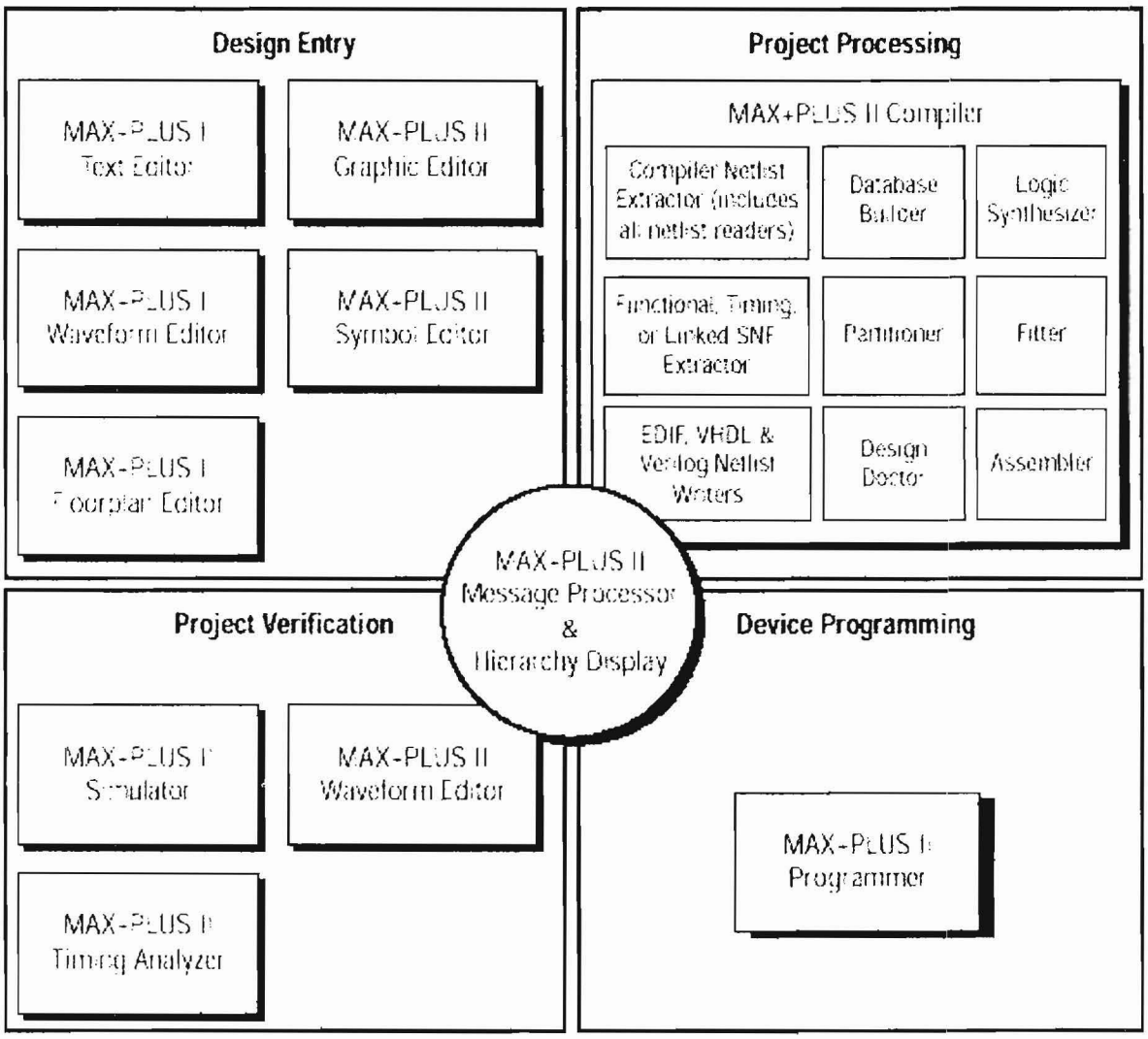


Figure 41: MAX+PLUS-II design environment [27].

MAX+PLUS II offers a full spectrum of logic design capabilities: a variety of design entry methods for hierarchical designs, powerful logic synthesis, timing-driven compilation, partitioning, functional and timing simulation, linked multi-device simulation, timing analysis, automatic error location, device programming and verification.

The design entry can be done through the editors as one can see from Fig. 41; the graphic editor generates a graphic design file (.gdf), the text editor generates a text design file (.tdf) and the waveform editor generates a waveform design file (.wdf). With the graphic editor you can enter symbols from a large database of logic devices and interconnect them as shown in Fig. 42.

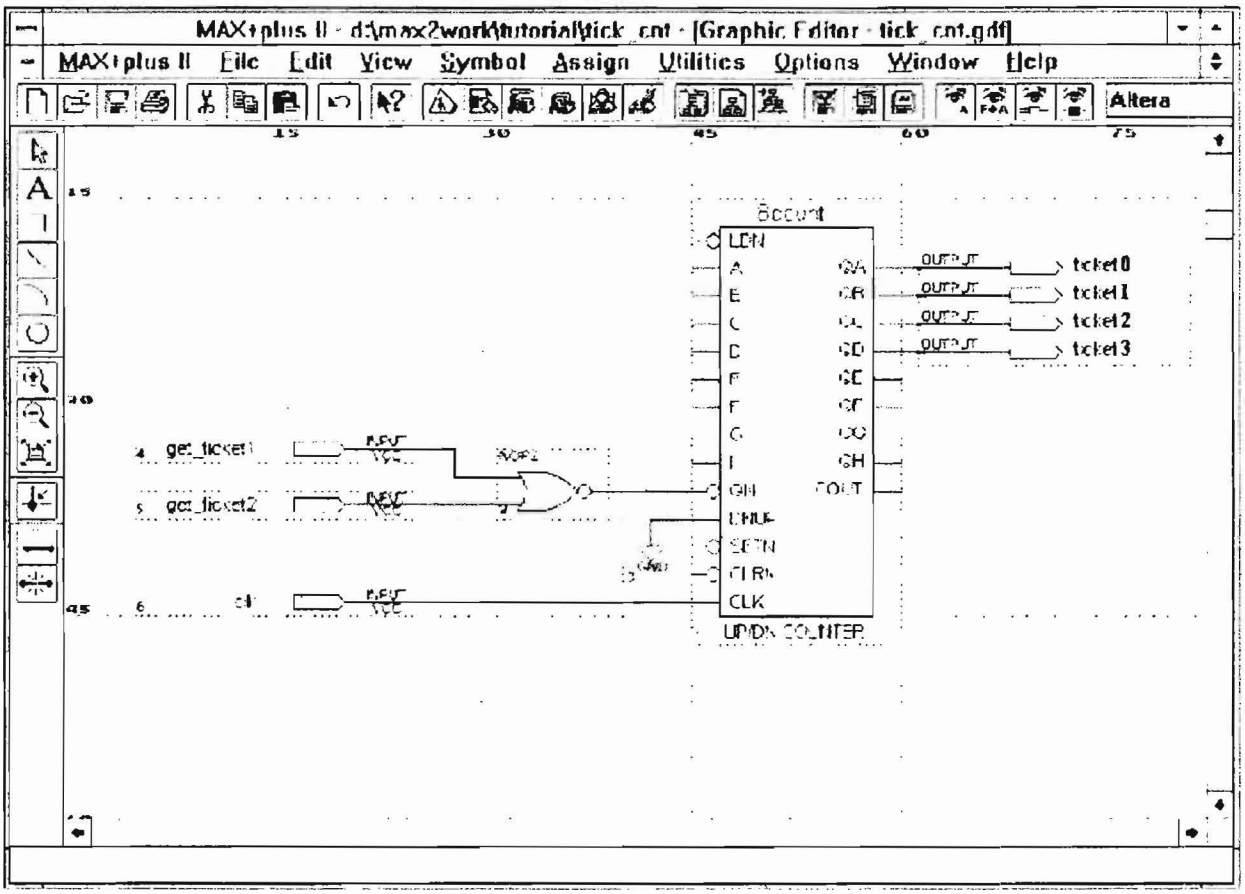


Figure 42: MAX+PLUS-II graphic editor [27].

With the text editor MAX+PLUS II one can read and write Altera Hardware Description Language (AHDL) files and standard EDIF netlist files, Verilog Hardware Description Language (VHDL) files. And, with the waveform editor one can set the inputs and outputs and see the results of the simulation based on these chioces.

4.2 Biphase-Mark Encoder

The Biphase-Mark Encoder was designed using the Altera EMP7128AE-5 FPGA. The Biphase-Mark Encoder has to use a 106 MHz square signal to generate the code for the 106Mbps optical link. The Biphase-Mark Encoder was written in Altera Hardware Description Language (AHDL), the text file was called bifm_gen.tdf and is listed as follows:

```
SUBDESIGN bifm_gen
%Declaring the inputs and outputs%
(
        NRZdata, clock106                       : INPUT = GND;
        RESETN                                  : INPUT = VCC;
        fm_out                                  : OUTPUT;
        clock53                                 : OUTPUT;
)

VARIABLE
%Declaring the variables, in this case they can be Flip-Flops or State Machines, and so on%
        clock53                                         : TFF;
        % State machine to generate the bi-phase mark signal %
        OUT_GEN     :MACHINE WITH STATES ( STATE0,
                                                        STATE1,

                                                        STATE2,
                                                        STATE3,
                                                        STATE4);


BEGIN

DEFAULTS
        fm_out = GND;
END DEFAULTS;

 %Declaring the clk input and the reset for the state machine %
OUT_GEN.(clk,reset) = (clock106,!RESETN);
clock53.(clk,clrn) = (clock106,RESETN);

clock53.t = VCC;

CASE ( OUT_GEN ) IS

  WHEN STATE0 =>
        IF (NRZdata==GND) THEN
                fm_out = VCC;
                OUT_GEN = STATE1;
        ELSIF (NRZdata==VCC) THEN
                fm_out = VCC;
                OUT_GEN = STATE4;
        END IF;

  WHEN STATE1 =>
        fm_out = VCC;
```

```
        OUT_GEN = STATE2;

  WHEN STATE2=>
        IF (NRZdata==VCC) THEN
                fm_out = GND;
                OUT_GEN = STATE3;
        ELSIF (NRZdata==GND) THEN
                fm_out = GND;
                OUT_GEN = STATE4;
        END IF;

  WHEN STATE3 =>
        fm_out = VCC;
        OUT_GEN = STATE2;

  WHEN STATE4 =>
        fm_out = GND;
        OUT_GEN = STATE0;

END CASE;

END;
```

The Biphase-Mark Encoder uses a state machine with a 106 MHz clock signal to generate the code for the 106Mbps optical link.

4.3 Biphase-Mark Decoder

The Biphase-Mark Decoder was also designed using an Altera EMP7128AE FPGA. The Biphase-Mark Decoder has to use a 106 MHz square signal to separate the command and clock signals. The Biphase-Mark Decoder was written in Altera Hardware Description Language (AHDL), the text file was called recover.tdf and is listed as follows:

```
SUBDESIGN recover
(
        bi_phase_in,clock106                : INPUT;
        resetN                              : INPUT;
        NRZ_data,clock53,dclock53           : OUTPUT;
)

VARIABLE
clock53                                     :DFF;
buffer[1..0]                                :DFF;
NRZ_datal,NRZ_datah                         :DFF;
divider                                     :TFF;
```

```
BEGIN
buffer[].(clk,clrn)=(clock106,resetN);
divider.(clk,clrn)=(clock106,resetN);
NRZ_datal.(clk,clrn)=(clock106,resetN);
NRZ_datah.(clk,clrn)=(clock106,resetN);
clock53.(clk,clrn)=(clock106,resetN);

%Comparison between the previous and current values of the incoming signal using as reference
the low level of the 53 MHz square signal %
buffer[0]=bi_phase_in;
buffer[1]=buffer[0];
IF (buffer[1] == buffer[0] & dclock53 == GND) THEN
        NRZ_datal.d=GND;
ELSIF (buffer[1] != buffer[0] & dclock53 == GND) THEN
        NRZ_datal.d=VCC;
ELSIF(dclock53==VCC) THEN
        NRZ_datal.d=NRZ_datal.q;
END IF;

%Comparison between the previous and current values of the incoming signal using as reference
the high level of the 53 MHz square signal %
buffer[0]=bi_phase_in;
buffer[1]=buffer[0];
IF (buffer[1] == buffer[0] & dclock53 == VCC) THEN
        NRZ_datah.d=GND;
ELSIF (buffer[1] != buffer[0] & dclock53 == VCC) THEN
        NRZ_datah.d=VCC;
ELSIF(dclock53==GND) THEN
        NRZ_datah.d=NRZ_datah.q;
END IF;

NRZ_data=!NRZ_datal.q # !NRZ_datah.q;
divider.t=VCC;
dclock53=divider.q;
clock53.d=dclock53;

END;
```

The Biphase-Mark decoder uses shift registers with a 106 MHz clock signal to recover the command signal. The shift registers store the previous and current values (high or low) of the incoming Biphase-Mark (BM) signal. Afterwards, we make the comparison of these values. This comparison is done using as reference one level (high or low) of the 53 MHz square signal, which is generated from the 106 MHz square signal.

Because of the way in which we are using the 53 MHz square signal as reference to make the comparison, we need to design in a means to avoid an undesirable feature. If the incoming signal changes its phase unexpectedly, then the decoder can remain hung at one value. This can

be avoided by including two comparison blocks in the program. One block will make the comparison using as reference the low level of the 53 MHz square signal, and the other will make the comparison using as reference the high level of the 53 MHz square signal.

The 106 MHz and the 53 MHz square signals need to be synchronized with the incoming Biphase-Mark signal. It is not easy to synchronize these signals, because the Biphase-Mark signal does not have periodic phase, periodic rising edge or periodic falling edge. We need look for something to generate a periodic signal from the Biphase-Mark signal. Then we will be able to use a Phase Locked Loop (PLL) to synchronize this periodic signal with the 53 MHz clock signal in the 106 Mbps optical receiver.

4.3.1 PLL used to synchronize the incoming Biphase-Mark signal with the 53 MHz and the 106 MHz square signals used to recover the command signal.

As we said above the PLL can not synchronize the incoming Biphase-Mark signal with the local 53 MHz clock directly. In this section we describe how we generated a periodic signal from the incoming Biphase-Mark signal. First we use an edge detector, which generates pulses for each edge in the Biphase-Mark signal. Afterwards we use an AND gate to eliminate the undesirable pulses as is shown in Fig. 43.

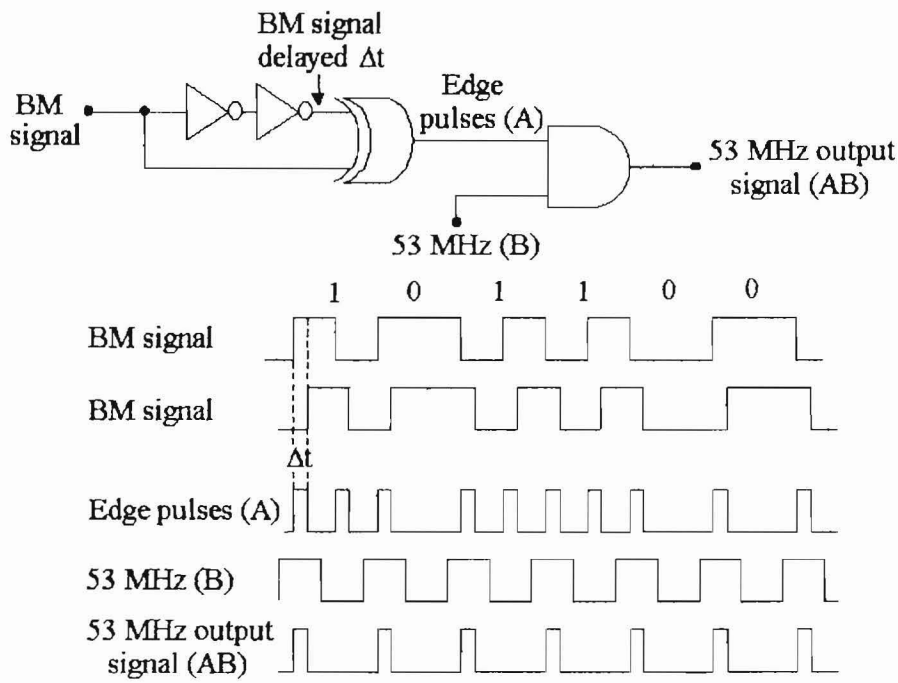


Figure 43: Circuit to get a periodic signal from the incoming Biphase-Mark (BM) signal.

Now we can synchronize this periodic signal with the 53 MHz clock signal using a digital PLL (DPLL).

The DPLL is a control system, which causes a particular system to track with another one. The PLL is able to synchronize an output signal (generated by a crystal oscillator) with a reference or input signal in frequency and phase. In the synchronized –often called locked- state

the phase error between crystal oscillator's output signal and the reference signal is zero, or remains constant.

If a phase error builds up, a control mechanism acts on the crystal oscillator in such a way that the phase error is again reduced to a minimum. In such a control system the phase of the output is actually locked to the phase of the reference signal. This is why it is referred to as a phase-locked loop [28]. Figure 44 shows the block diagram of a DPLL and Fig. 45 shows its mathematical model in the locked state.

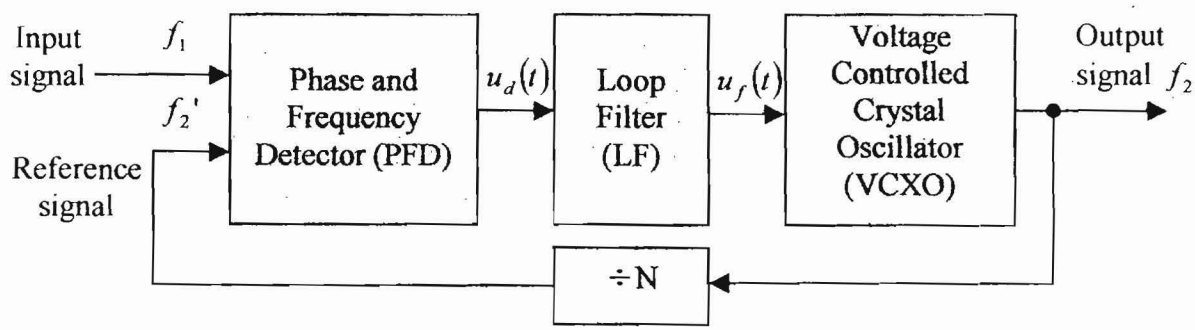


Figure 44: Block diagram of a DPLL.

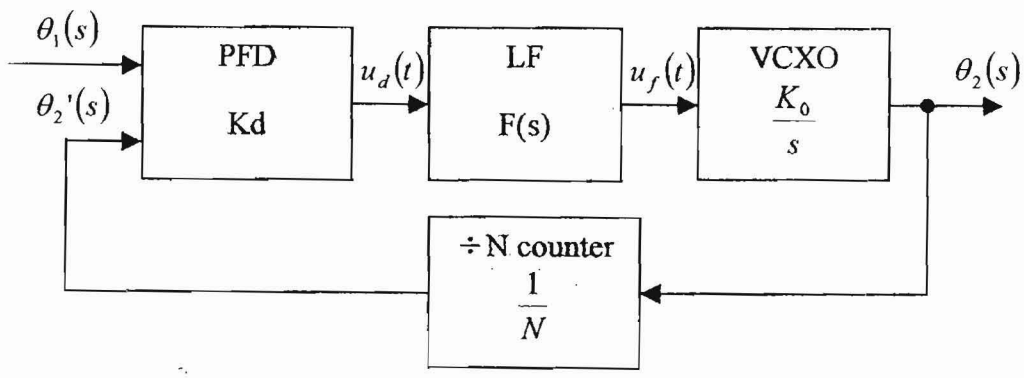


Figure 45: Mathematical model of the DPLL in the locked state.

The DPLL circuit shown in the figure can be described as follow

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{KdF(s)\frac{Ko}{s}}{\left[1 + \frac{KdF(s)Ko}{Ns}\right]} \tag{7}$$

where Kd represents the gain of the PFD, F(s) is the transfer function of the low-pass filter, Ko represents the gain of the VCXO and 1/N is the gain of the frequency divisor.

The phase and frequency detector of the PLL used in the 106 Mbps optical link receiver is shown as Fig. 46. The low-pass filter is shown in Fig. 47.

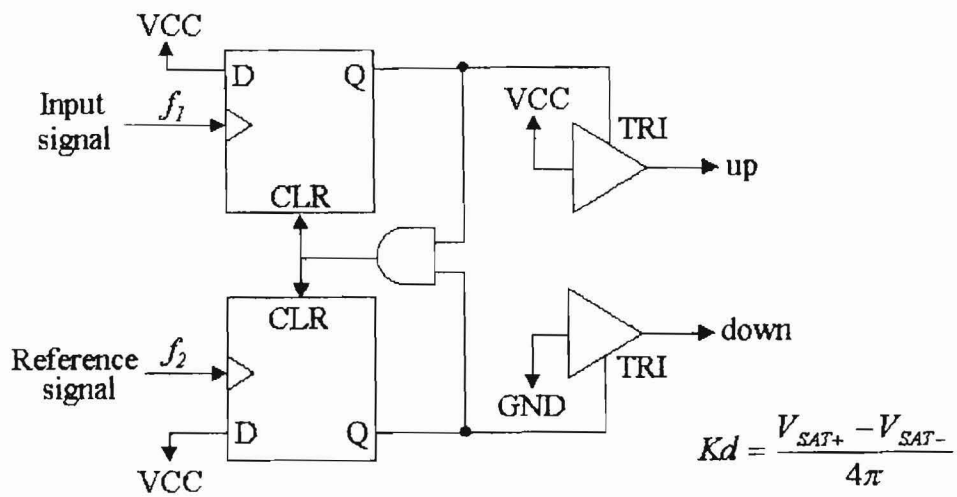


Figure 46: PFD of the DPLL used in 106 Mbps digital optical link receiver. Kd is the gain of the PFD.

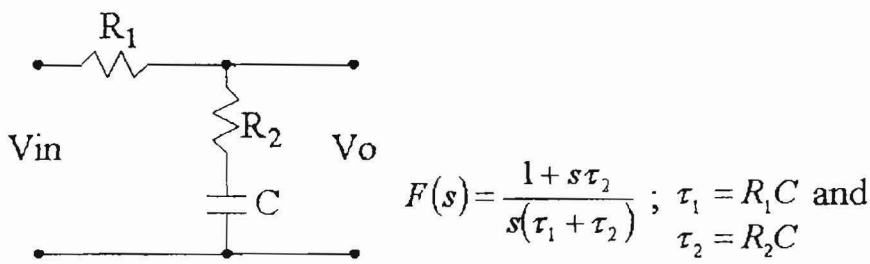


Figure 47: Low-pass filter of the DPLL used in the 106 Mbps optical link.

When a PFD is used to drive the filter showed above; no current flows in the resistors R_1 and R_2, however, when the output of the PFD is in high-impedance state. Under this condition, the voltage across the capacitor remains unchanged. Neglecting leakage currents the output signal Vo of the passive lag filter can have any voltage level while the input signal is 0 (i. e. while the PFD outputs are in tri-state). Hence the passive lag filter behaves like an ideal integrator then its transfer function is like the shown in Fig. 47 [28, page 103].

Using the PFD shown in Fig. 46 and the low-pass filter shown in Fig. 47, we can analyze the phase transfer function inserting the loop filter transfer function in Eqn. 35. The result is

$$H(s) = \frac{\frac{\tau_2 KdKo}{(\tau_1 + \tau_2)}\left(s + \frac{1}{\tau_2}\right)}{s^2 + \left(\frac{KdKo\tau_2}{N(\tau_1 + \tau_2)}\right)s + \frac{KdKo}{N(\tau_1 + \tau_2)}} \tag{8}$$

In circuit and control theory it is common practice to write the denominator of the transfer function in the so-called *normalized form* [28, page 17],

$$\text{Denominator} = s^2 + 2\xi w_n s + w_n^2$$

where w_n is the natural frequency of the DPLL system and ξ is the damping factor.

Solving Eqn. 8 to get the natural frequency and the damping factor, we get

$$w_n = \sqrt{\frac{KdKo}{N(\tau_1 + \tau_2)}} \quad \text{and} \quad \xi = w_n \frac{\tau_2}{2} \tag{9}$$

We need to calculate the values of the resistors and the capacitor of the low-pass filter, but first we need the values of Ko and Kd. Which we can get them from their definition [28, pages 63 and 99]. Using the data sheet of the VECTRON VCXO VDUGLD 52 [29] we can calculate Ko as follow

$$Ko = \frac{2\pi(f_{2MAX} - f_{2MIN})}{Vcmax - Vcmin} = \frac{2\pi 10kHz}{2.7V} = \frac{20\pi kHz}{2.7V} \tag{10}$$

where f_{2MAX} and f_{2MIN} are the maximum and minimum frequencies respectively of the VCXO. $Vcmax$ and $Vcmin$ are the maximum and minimum control voltages respectively of the VCXO.

To calculate Kd one only needs the saturation voltages of a TLL/CMOS devices, then kd can be calculated as follow

$$Kd = \frac{V_{SAT+} - V_{SAT-}}{4\pi} = \frac{3V - 0.3V}{4\pi} = \frac{2.7V}{4\pi} \tag{11}$$

where V_{SAT+} is the maximum output voltage of the loop filter and V_{SAT-} is the minimum output voltage of the loop filter.

When N is constant, the damping factor (ξ) remains constant, too, and can be chosen arbitrarily [28, page 129]. For constant N, it is optimum to select

$$\xi = 0.7 \tag{12}$$

When one is using a PFD, the lock range of the DPLL [28, page 111] becomes approximately

$$\Delta w_L = \pi \xi w_n \tag{13}$$

where Δw_L is equal to the lock range around the reference frequency.

Combining Eqns. 9, 10, 11, 12 and 13 we can get

$$\tau_1 = R_1 C = \frac{1.96}{(\Delta f_L)^2}\left[\frac{5kHz}{N} - \Delta f_L\right] \quad \text{and} \quad \tau_2 = R_2 C = \frac{1.96}{\Delta f_L} \tag{14}$$

where τ_1 and τ_2 are the time constants of the low-pass filter shown in Fig. 47 and Δf_L is the lock range around the reference frequency.

When one is using the low-pass filter shown in Fig. 47, normally τ_1 should be considerably greater than τ_2, typically 5 to 10 times [28, page 64]. If τ_1 is smaller than τ_2 then try another type of loop filter.

Figure 48 shows τ_2, $\tau_1(N=1)$ and $\tau_1(N=2)$ as a function of the lock range frequency Δf_L.

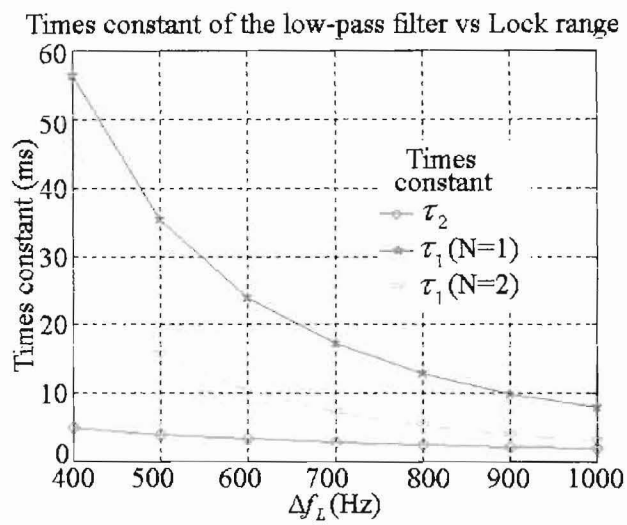


Figure 48: Time constants as a function of the lock range.

As we can see from the figure the best values of the time constants are at 400 Hz for N=2 and at 1 kHz for N=1. Preliminary tests shown that to always have synchronization of the incoming Biphase-Mark signal and the local VCXO we need to use a DPLL with N=2. Then the best time constants values are at $\Delta f_L = 400Hz$, with $\tau_1 = 56.35ms$ and $\tau_2 = 4.9ms$. The capacitor value C can be chosen arbitrarily, so chose C=0.2 μF, with $R_1 = 221k\Omega$ and $R_2 = 22.1k\Omega$. To test our designs we found a commercial VCXO, the VECTRON VCXO VDUGLD 52 with a central frequency of 52 MHz instead of the 53 MHz frequency needed in the 106 MHz optical link. This crystal will be used only for testing because its frequency is close enough to the 53 MHz. A schematic of the 106 Mbps optical link receiver including the DPLL circuit is shown as Fig. 49. The DPLL synchronized the incoming signal and the crystal oscillator at 26 MHz, this was done to get the best DPLL performance.

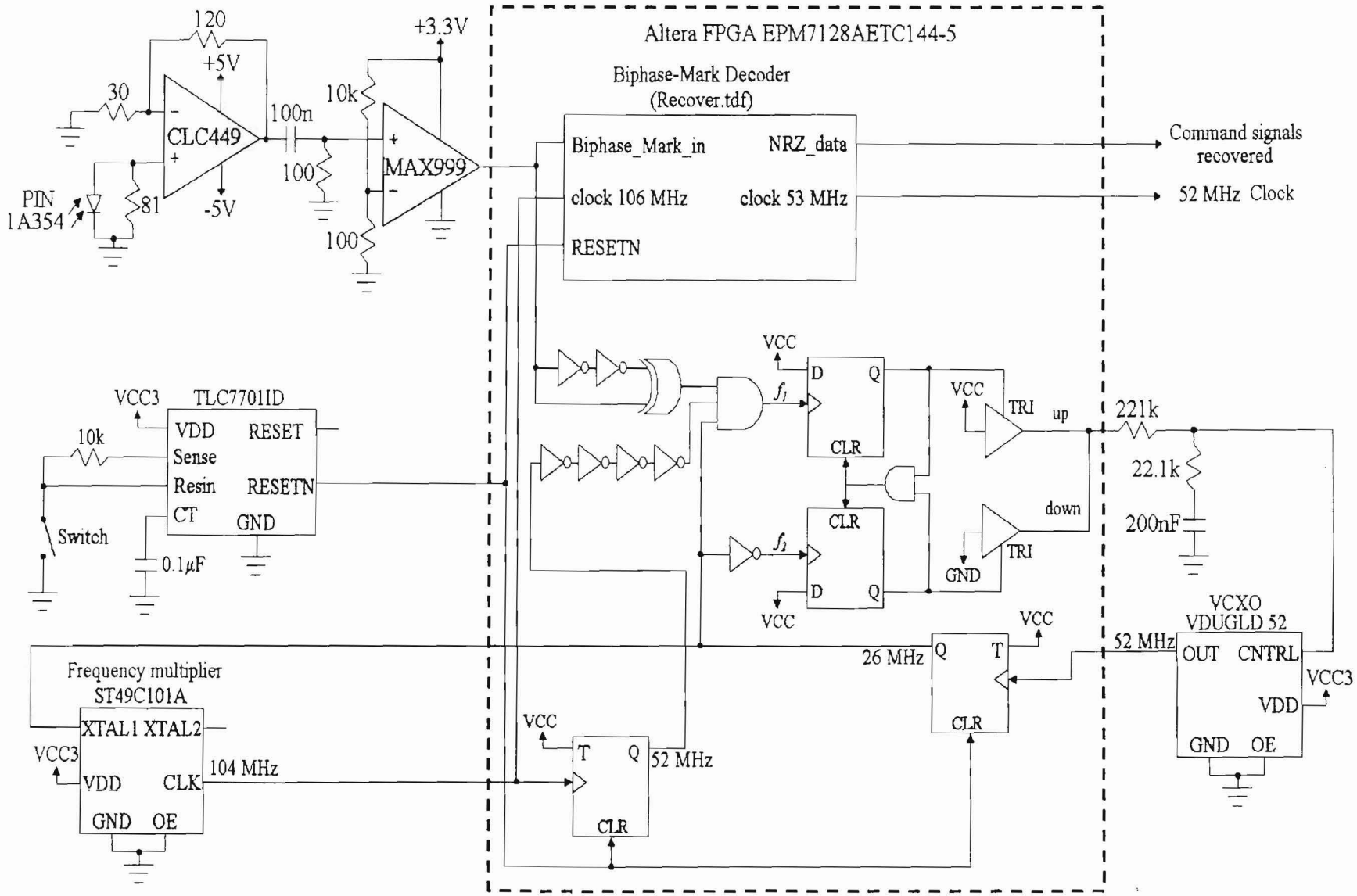


Figure 49: Schematic of the 106 Mbps optical link, including the DPLL.

The frequency multiplier ST49C101A-06 [30] used in the schematic multiplies the frequency of the input signal by a factor of 4. The IC TLC7701ID [31] is a micropower supply voltage supervisor.

4.4 Conclusions

We have designed completely the 106 Mbps optical link, now we will work on the 1.06 Gbps optical link. Afterwards we will try to put everything together to design the first prototype of the Readout and Control Optical Interface for the BTeV Pixel Vertex Detector.

Chapter Five

1.06 Gbps Digital Optical Link

In this chapter we will implement the 1.06 Gbps digital optical link. People at Fermilab and CERN have been using the Gigabit Rate Transmit/Receive Chip Set HDMP-10XX [32, 33 and 34] as the baseline for their G-Link designs. This Chip set has shown a very good performance and a very low Bit Error Rate (BER). Then the first step will be to study this G-Link Chip Set. Another very interesting option is a new radiation hard G-Link transmitter, which is a custom VLSI serializer fabricated in the CHFET process [35]. This is 100% compatible with the G-Link receiver HD10X4 from Agilent. In the next section we describe the Gigabit Rate Transmit/Receive Chip Set HDMP-10XX.

5.1 Gigabit Rate Transmit/Receive Chip Set HDMP-10XX

The Gigabit Transmit/Receive Chip Set consists of two ICs. One is a serializer, which translates a parallel frame of 16 or 20 bits into a (16+4) or (20+4) bit serial frame using the Conditional Invert Master Transition (CIMT) protocol [32, 33 and 34]. A 16/20 bit simplex transmission using this Transmit/Receive chip set is shown as Fig. 50.

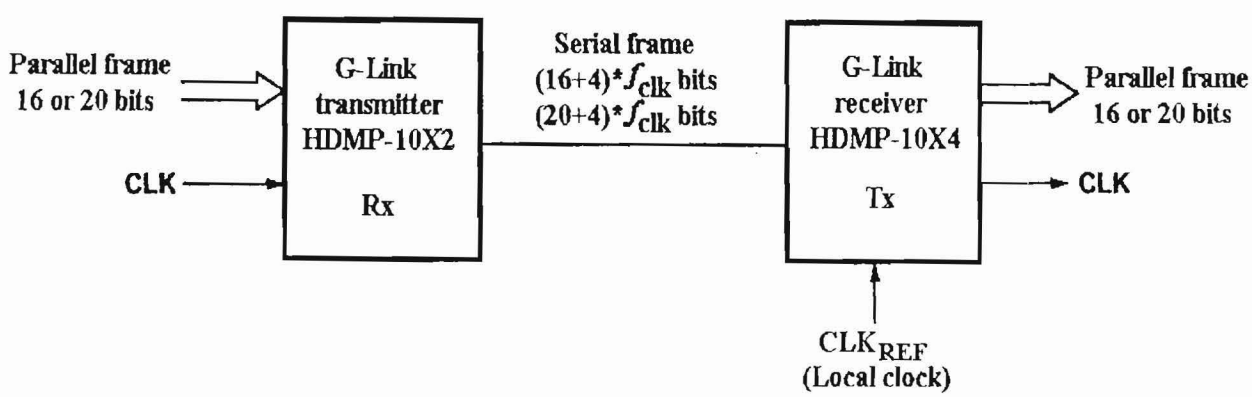


Figure 50: 16/20 bits simplex transmission.

There are three versions of these Transmit/Receive sets, and they are shown in Table 11.

G-Link chip set		Parallel frame		Version	Receiver is capable being synchronized with the local clock	Parallel Word Rate (Mword/sec)
Transmitter	Receiver	16 bits	20 bits			
HDMP-1012	HDMP-1014	Yes	Yes	ECL	No	7.5-75
HDMP-1022	HDMP-1024	Yes	Yes	TTL	No	7.5-75
HDMP-1032	HDMP-1034	Yes	No	CMOS	Yes	13-70

Table 11: G-Link chip set features.

The ECL version was the first version in the market and is able to receive and release the data bits and clock signal in ECL levels. The next version was the TTL version. This version is able to handle TTL levels. The last version is the CMOS low power version, which is able to receive the data bits in TLL or CMOS levels and releases the data bits in CMOS levels. Also the G-link low power version is able to release the data synchronized to the local clock. Since in our case we need to synchronize the received data to the local clock, and low power consumption is an issue, our best option is the G-Link low power version.

All the G-Link Chip Set versions use the CIMT to translate the 16 or 20 bits parallel frame into (16+4) or (20+4) bit serial frames. The CIMT protocol has two distinct features:

1. At a fixed point in each data frame, there is a guaranteed transition (from 0 to 1 or 1 to 0), which is suited to a clock recovery system that is based on a frame-rate clock. This is the case with the G-Link, in which a PLL-based frequency multiplier is used to provide a shift clock at Nf.

2. In order to maintain DC line balance, data frames are flipped as required to keep the average number of 1s equal to the average number of 0s.

The serial stream has a master transition (MT) occurring once per frame. In the G-Link implementation of the CIMT protocol, the data are transmitted first (starting with the LSB) followed by the coding bits. The MTs occur between the 2nd and 3rd coding bits as shown in Fig. 51.

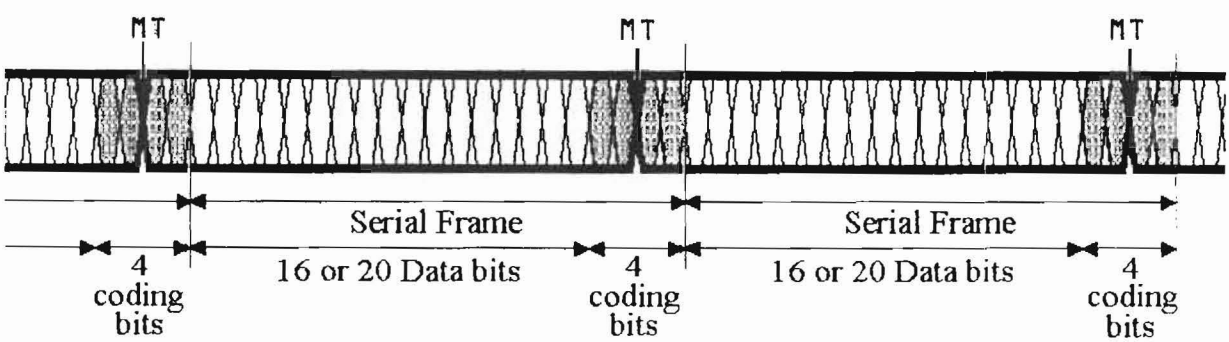


Figure 51: Serial frame containing the 16 or 20 Data bits plus 4 coding bits generated by the CIMT protocol.

In the G-Link versions both the ECL and the TTL, both 16 and 20 bits of data were possible, whereas in the low power version only 16 bits are possible.

The G-Link transmitter HD1032 is a 64 pin IC and has 8 control inputs to select the parallel frequency range and the transmission mode. Figure 52 represents the HDMP1032 G-link transmitter with its most important input/output signals.

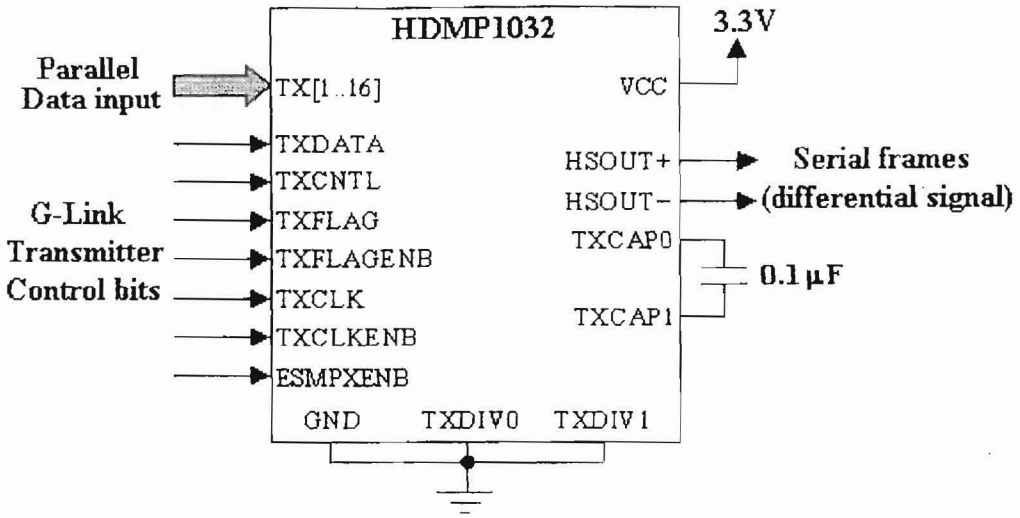


Figure 52: HDMP1032 G-Link transmitter with its most important input/output signals.

The G-Link receiver HD1034 is a 64 pin IC and has 4 input bits to select the parallel frequency range and the clock reference. Also the G-Link receiver has 9 outputs to indicate if the G-link is ready, to flag errors, and tell us whether it is receiving Fill Frames (FF), Control words, data words or data word plus flag bit. Figure 53 represents the HDMP1034 G-link receiver with its most important input/output signals.

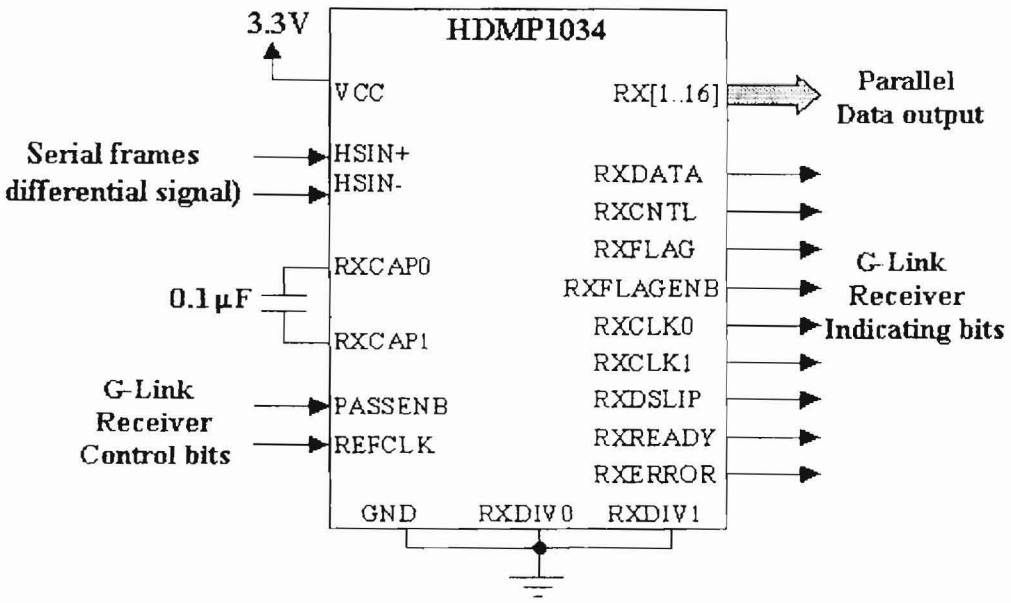


Figure 53: HDMP1034 G-Link receiver with its most important input/output signals.

All the G-Link versions have four operation modes, these modes are the Fill Frame mode, Data mode, Control mode and Flag mode. The operation modes of the low power version are summarized in Tables 12, 13, 14 and 15, with ESMPXENB=0 (Compatible with previous G-Link chips, HDMP-1012/14, HDMP-1022/24).

Fill Frame (FF) mode [TXDATA=GND, TXCNTL=GND, TXFLAG=X, TXFLGENB=GND, TXCLK=CLK and TXCLKENB=GND]:

	Data Field																Flag	Coding-Field			
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	bit	C1	C2	C3	C4
Sent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	--	--	--	--
FFa	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	X	0	0	1	1
FFb	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	X	0	0	1	1

Table 12: In this table we show the levels applied to each input signal in the G-link transmitter (Sent) and what we should receive in the G-Link receiver (FFa and FFb). The G-Link transmitter alternates frames between FFa and FFb when is in FF mode.

Data mode [TXDATA=VCC, TXCNTL=GND, TXFLAG=X, TXFLGENB=GND, TXCLK=CLK and TXCLKENB=GND]:

	Data Field																Flag	Coding-Field			
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	bit	C1	C2	C3	C4
Sent	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	X	--	--	--	--
True	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	0	1	1	0	1
Inverted	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{D8}$	$\overline{D9}$	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$	$\overline{D14}$	$\overline{D15}$	$\overline{D16}$	0	0	0	1	0
True	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	1	1	0	1	1
Inverted	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{D8}$	$\overline{D9}$	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$	$\overline{D14}$	$\overline{D15}$	$\overline{D16}$	1	0	1	0	0

Table 13: In this table we show the levels applied to each input signal in the G-link transmitter (Sent) and what we should receive in the G-Link receiver. The CMIT inverts the data bits in order to maintain the DC balance.

Control mode [TXDATA=GND, TXCNTL=VCC, TXFLAG=X, TXFLGENB=GND, TXCLK=CLK and TXCLKENB=GND]:

	Data Field																Flag	Coding-Field			
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	bit	C1	C2	C3	C4
Sent	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	X	--	--	--	--
True	D1	D2	D3	D4	D5	D6	D7	0	1	D8	D9	D10	D11	D12	D13	D14	X	0	0	1	1
Inverted	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	1	0	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$	$\overline{D14}$	$\overline{D15}$	$\overline{D16}$	X	1	1	0	0

Table 14: In this table we show the levels applied to each input signal in the G-link transmitter (Sent) and what we should receive in the G-Link receiver. The CMIT inverts the data bits in order to maintain the DC balance.

Flag mode [TXDATA=GND, TXCNTL=GND, TXFLAG=F, TXFLGENB=VCC, TXCLK=CLK and TXCLKENB=GND]:

	Data Field																Flag	Coding-Field			
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	bit	C1	C2	C3	C4
Sent	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	F	--	--	--	--
True	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	0	1	1	0	1
Inverted	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{D8}$	$\overline{D9}$	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$	$\overline{D14}$	$\overline{D15}$	$\overline{D16}$	0	0	0	1	0
True	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	1	1	0	1	1
Inverted	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{D8}$	$\overline{D9}$	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$	$\overline{D14}$	$\overline{D15}$	$\overline{D16}$	1	0	1	0	0

Table 15: In this table we show the levels applied to each input signal in the G-link transmitter (Sent) and what we should receive in the G-Link receiver. The CMIT inverts the data bits in order to maintain the DC balance.

The HD1032 and the HD1034 G-Link Chip Set uses two bits to indicate the parallel word rate. Table 16 shows the possible combinations of these control bits called DIV0 and DIV1 [34].

DIV0	DIV1	Parallel Word Rate (MWord/sec) Range		Serial Baud Rate (Mbit/s) Range	
0	0	40	72 (max)	800	1400 (max)
0	1	20	45	400	900
1	0	13 (min)	26	260 (min)	520

Table 16: Typical data rates showing ranges of operation.

Since our clock frequency is 53 MHz, the serial baud rate will be 1.06 Gbit/s. Then DIV0=0 and DIV1=0. The serial link is synchronous, and both frame synchronization and bit synchronization are maintained. When data is not available to send, the link maintains synchronization by transmitting FF. Two (training) FF are reserved for handshaking during link startup. Data frames are not able to synchronize the G-Link chip set during the startup.

When the user is not using the Flag mode then the Flag bit is not user controllable and is alternately sent as 0 and 1 by the Tx during data frames to provide enhanced error detection. The detection reduces the probability that the loop could lock onto random data at a point away from the true master transition.

The G-Link chip set is only able to detect all single-bit errors in the C-field (non-data bit fields) of the frame. When we transmit in Flag mode the probability of undetected false lock is higher. To get the best performance of the G-link chip set we should not transmit in Flag mode, and during the startup, we should transmit only FF. It is also important to keep transmitting FF when we are not sending data.

5.2 Finisar optoelectronic modules

The serial output of the G-Link transmitter is a differential electrical signal and we need an optoelectronic device to translate the electrical signal into an optical signal.

To translate the electrical signal into an outgoing optical signal we will use the Finisar transmitter module FTM8510 [36]. Table 17 shows the parameters of the Finisar transmitter module FTM8510 and Table 18 shows its Pin-out and specifications. This optoelectronic device has its optical center at 850 nm.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icc	70	90	120	mA	Positive temperature coefficient
Input Impedance	Zin		50		ohms	Rin > 100 kohm @ DC
Baud Rate	BR	100		1500	Mbit/s	
Fiber Length		0.1		500	meters	
Fiber Core Diameter			50		um	
Avg. Opt. Power	Popt	-5.0	-2.5	0.0	dBm	
Extinction Ratio	ExtR	5	5.5		dB	
Optical Center		770	850	870	nm	
Spectral Width				4	nm	RMS
Output Rise/Fall	tr/tf		350	400	psec	Optical Rise/Fall Time
Operating Temperature		0		70	deg. C	-40 to +85 C available

Table 17: Parameters of the Finisar transmitter module FTM8510.

FTM8510 Optical Transmitter

PIN #	DESCRIPTION	SIGNAL TYPE	MIN	TYP	MAX	UNITS	CONNECTION
1	Rx Opt. Power	Analog Input	0.0		Vcc	V	Rx pin 16 or no connect
2	Rx Sys 1	CMOS I/O	CMOS values				Rx pin 14 or no connect
3	5 VDC ± 5%	Power Supply	4.75	5.00	5.25	V	
4	CS	CMOS Input	All CMOS Inputs/Outputs				Active low
5	OFC Status	CMOS Output		MIN	MAX		
6	Tx Off	CMOS Input	VinL		1.5	V	Active High
7	Ready	CMOS I/O	VinH	3.5		V	
8	Reset	CMOS Input	VoL		0.5	V	Active low
9	Ground		VoH	4.5		V	
10	Tx +	ECL (+) Input AC	350		1000	mVpp	AC coupled, 50 ohm Zin
11	Tx -	ECL (-) Input AC	350		1000	mVpp	AC coupled, 50 ohm Zin
12	Ground	System Ground					
13	SO	CMOS Output	CMOS values				
14	SI	CMOS Input					
15	SClk	CMOS Input					
16	Rx Signal Detect	CMOS Input					Rx pin 17, or ground
17	Rx Sys 2	CMOS I/O					Rx pin 13, or no connect

Table 18: Pin-out and description of the Finisar transmitter module FTM8510.

A basic diagram of the Finisar FTM8510 is shown as Fig. 54.

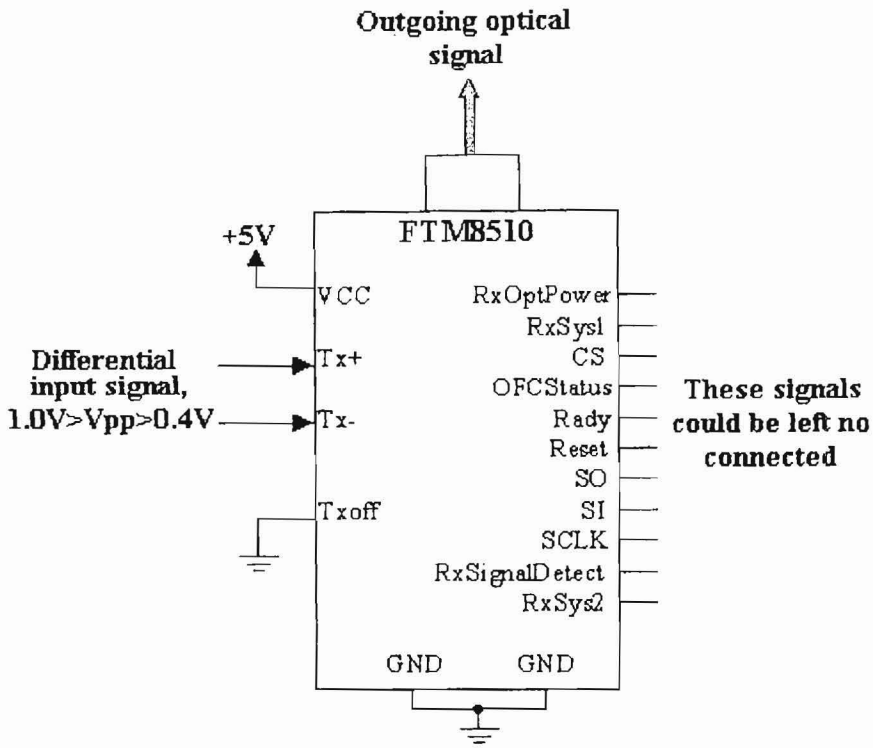


Figure 54: Basic diagram of the Finisar FTM8510.

The serial input signal of the G-Link receiver is a differential electrical signal. and we need another optoelectronic device to translate the optical signal back into an electrical signal.

To translate the incoming optical signal into an electrical signal we will use the Finisar receiver module FRM8510 [36]. Table 19 shows the parameters of the Finisar receiver module FRM8510, and Table 20 shows its Pin-out and specifications. This optoelectronic device has its optical center at 850 nm as well.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icc	70	80	90	mA	Positive temperature coefficient
Standby Current	Iccs		0.5	2	mA	Standby Mode
Output Impedance	Zout		50		ohms	Rin > 100 kohm @ DC
Baud Rate	BR	100		1500	Mbit/s	
Fiber Core Diameter			50		um	
Rec. Sensitivity	Ptan	-16		2	dBm	BER<1.0E-12, PRBS 27-1
OFC Start	OFCs	-16			dBm	
Optical Input WL		770	850	870	nm	
Optical Return Loss	ORL	12			dB	
Output Rise/Fall	tr/tf		350	400	psec	
Operating Temperature		0		70	deg. C	-40 to +85 C available

Table 19: Parameters of the Finisar receiver module FRM8510.

FRM8510 Optical Receiver

PIN #	DESCRIPTION	SIGNAL TYPE	MIN	TYP	MAX	UNITS	CONNECTION
3	5 VDC Standby	Power Supply	4.75	5.00	5.25	V	
6, 7	Ground						
8	Rx +	ECL (+) Input AC	400		1000	mVpp	50 ohms to DC level
9	Rx -	ECL (-) Input AC	400		1000	mVpp	50 ohms to DC level
10, 11	Ground						
12	5 VDC ± 5%	Power Supply	4.75	5.0	5.25	V	
13	Rx Sys 2	CMOS I/O	CMOS values				Tx pin 17, or no connect
14	Rx Sys 1	CMOS I/O					Tx pin 2, or no connect
16	Rx Optical Power	Analog Output	0.0		Vcc	V	Tx pin 1, or no connect
17	Rx Signal Detect	CMOS Output	CMOS values				Tx pin 16, or no connect
Note: Pins 1, 2, 4, 5 and 15 are reserved and require no connection							

Table 20: Pin-out and description of the Finisar receiver module FRM8510.

A basic diagram of the Finisar FRM8510 is shown as Fig. 55.

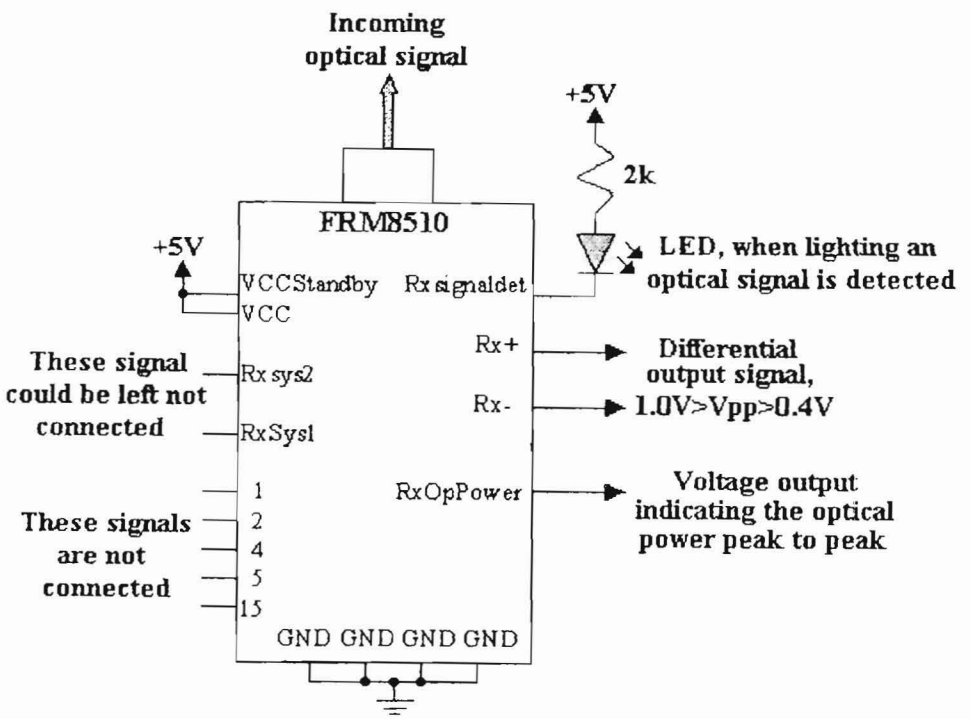


Figure 55: Basic diagram of the Finisar FRM8510.

Two signals provided by this Finisar receiver module FRM8510 are very interesting. One is the optical signal detected (Rxsignaldet), which indicates when the module is receiving an optical signal. In the diagram above we can see that the LED is activated by Rxsignaldet signal, and then when this LED is lit there is an incoming optical signal. The other signal is the optical power (RxOpPower), which indicates the optical power peak to peak by means of a voltage level. We have measured the voltage output on pin 16 of the FRM8510 as function of the optical power peak to peak. The results are shown in Table 21.

Voltage pin 16 FRM8510 (V)	Optical power peak to peak (mW)
0.76	0.587
0.92	0.640
1.04	0.693
1.14	0.764
1.28	0.871
1.66	1.013
1.76	1.120
1.92	1.173
2.08	1.262
2.16	1.298
2.72	1.582
3.08	1.724
3.44	1.867
3.76	2.080
4.20	2.187

Table 21: Voltage output on pin 16 of the FRM8510 as function of the optical power.

These data are plotted in Fig. 56. The graphic includes the result of a straight line fit to the data.

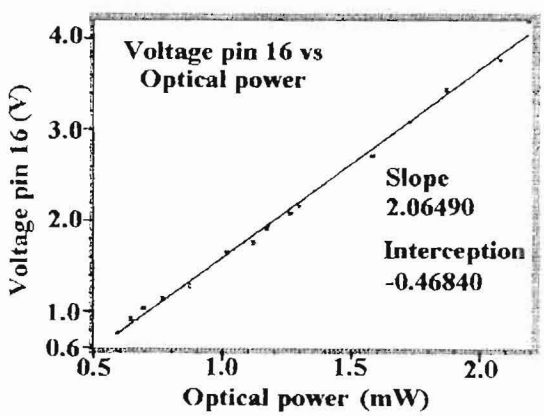


Figure 56: Voltage pin 16 (Vo16) of the FRM8510 as a function of the optical power peak to peak (LIpp) impinging on the Finisar receiver.

We can conclude that

$$Vo16 \approx ILpp \times \frac{2.0649V}{mW} - 0.4684V \tag{15}$$

5.3 1.06 Gbps optical link

The schematics of the G-Link transmitter and receiver daughter cards are shown as Fig. 57 and Fig. 58. The receiver is based on the G-link receiver HDMP1034 and the Finisar module FRM8510.

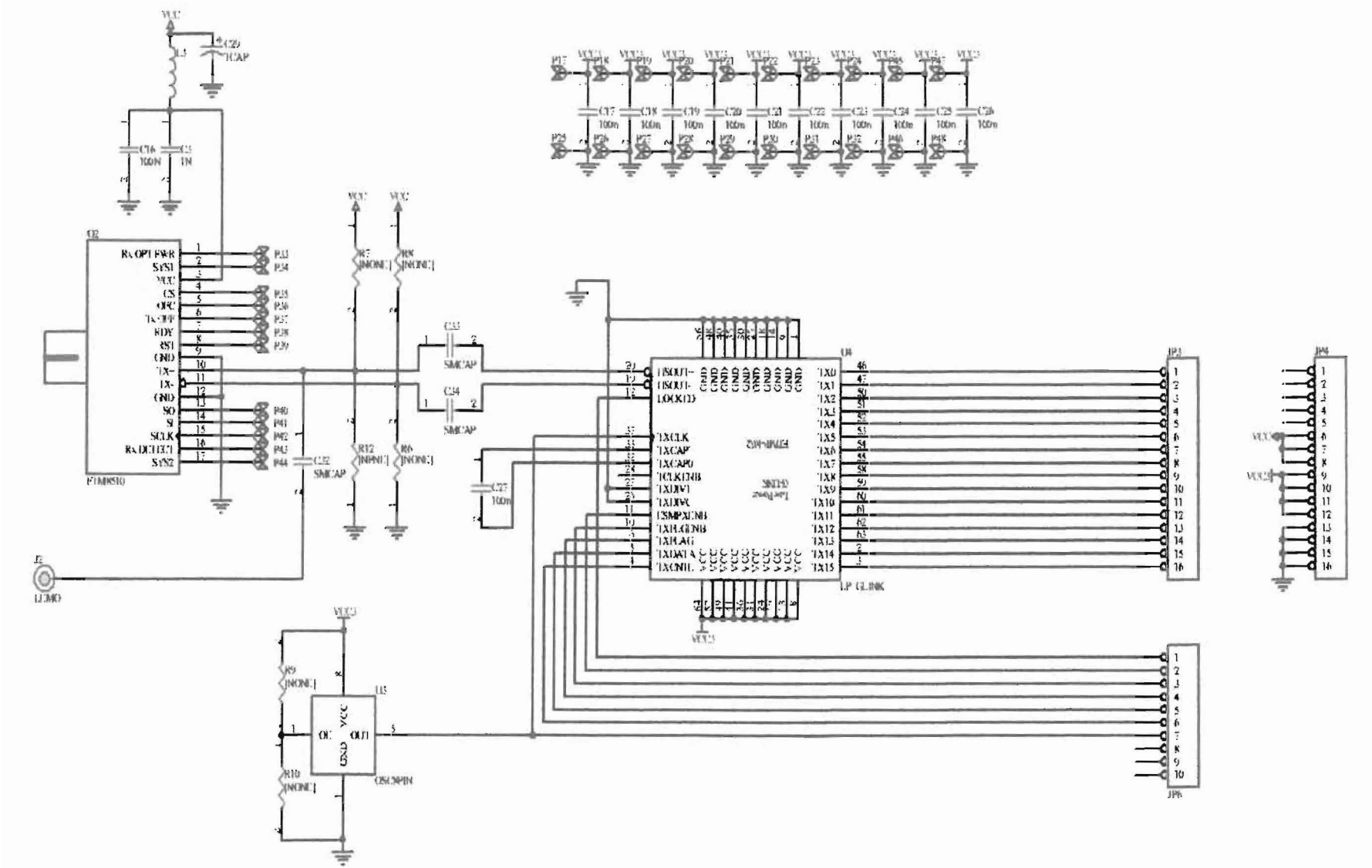


Figure 57: Schematic of the G-Link transmitter daughter card based on the G-Link transmitter HDMP1032 and the Finisar module FTM8510.

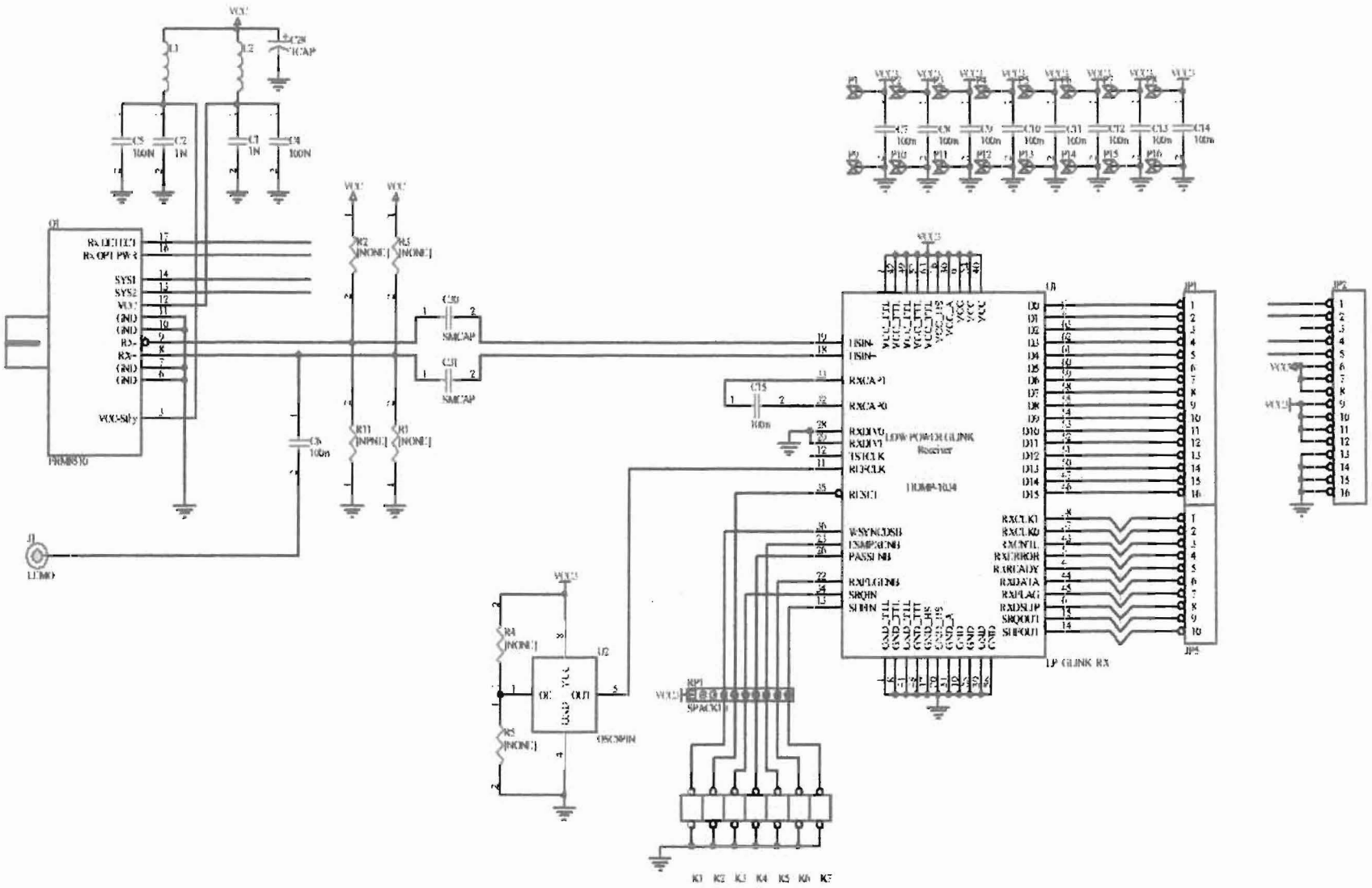


Figure 58: Schematic of the G-Link receiver daughter card based on the G-Link receiver HDMP1034 and the Finisar module FRM8510

5.4 Radiation hard CHFET Serializer

The v.2 CHFET serializer is Agilent G-Link compatible. The circuit consists of three logical sections:

1. Serializer – the serializer converts a 20-bit parallel stream, clocked in at the word clock rate, to a single serial output stream.
2. Protocol – the protocol is used to convert a 16-bit input Data word into a 20-bit DC-free code. The HP G-Link CIMT protocol is used.
3. Driver – the VCSEL Driver converts the high-speed serial stream into a modulation current for a VCSEL (external to the chip).

The CIMT protocol incorporated in the chip is designed to be compatible with the Low Power G-Link receiver (HDMP-1034).

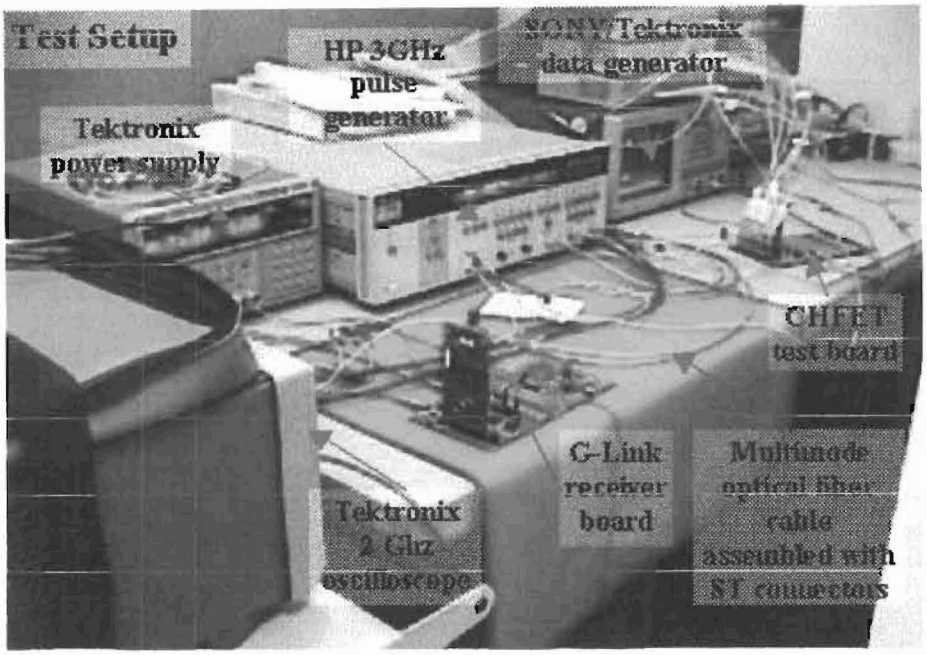
As for the G-Link transmitters, the CHFET serializer has control bits to select the operation mode. In this case the CHFET serializer can be operated as a serializer or as a G-Link transmitter. Using it as G-Link transmitter we can send FFs, Data words, Control words and Data word+Flag bit. But as we noted for the G-Link chip set from Agilent, it is better not to use the Flag mode because we will increase the errors.

The CHFET serializer is an IC of 52 pin. This IC has 6 control bits to select the operation mode as is shown in Table 22.

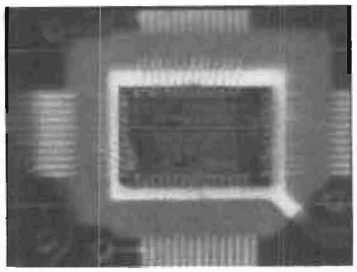
Operation mode	MODE	ED	D17	D18	D19	D20
Fill Frame (FF)	H	L	X	X	X	X
Data	H	H	X	H	H	X
Control	H	H	X	L	H	X
Flag	H	H	X	H	L	F

Table 22: Control bits of the CHFET serializer to select its operation mode.

Since the CHFET serializer is a custom chip, we need to characterize it. Performance tests were carried out on this chip. A photograph of the setup used is shown as Fig. 59. The instruments used in the setup are 2 Tektronix PS2521G programmable power supplies, Tektronix TDS794D 2 GHz oscilloscope, HP 8133A 3 GHz pulse generator, SONY/Tektronix DG2020A data generator with 2 Sony/Tektronix P3420 programmable outputs and a Tektronix P6701A optical probe.



- CHFET serializer



- CHFET test board

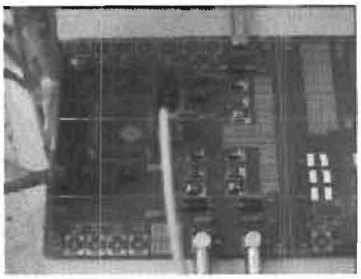


Figure 59: Setup used to characterize the CHFET serializer.

The test results were as follow

a) Power up test:

The chip powers up OK. Three voltages are supplied:

- V5 powers the input interface circuit and can be set to 3.3 or 5 volts, depending on the technology circuit driving the CHFET inputs.
- V13 powers the CHFET logic.
- V2 powers the optical interface and bias the VCSSEL.

Table 23 shows the average current and power consumption of each power supply for the chip operating at 53 MHz. Table 24 shows the same when the chip operates at 40 MHz.

f = 53MHz	Voltage	Clock signal ON		Clock signal OFF	
Power supply	V (V)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
V5	5	3	15	3	15
V2	2.2	60	132	45	99
V13	1.8	40-42	75.6	26-28	50.4
		Total power consumption	222.6	Total power consumption	164.4

Table 23: Power consumption at 53MHz, serializer and VCSEL.

f = 40MHz	Voltage	Clock signal ON		Clock signal OFF	
Power supply	V (V)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
V5	5	3	15	3	15
V2	2.2	56	123.2	45	99
V13	1.4	16	22.4	8-10	14
		Total power consumption	160.6	Total power consumption	128

Table 24: Power consumption at 40MHz, serializer and VCSEL.

The CHFET chip has an internal regulator, which can also supply the voltage needed by V13. Due to some fabrication problems the CHFET chip needs V13 to be a little higher than the nominal value 1.3 V. Furthermore, since V13 controls the voltage of the DLL circuit, it has an impact on the range of frequencies in which the device can be used. The power supply V13 needs a higher voltage when the device is operated at 53 MHz (see Table 23 and 24). As a consequence, the CHFET has been tested mostly using an external V13.

b) DLL output voltage (VDLY):

The CHFET serializer latches the data bits to be sampled, but instead of using an ultra-high speed clock signal, the chip uses a DLL (Delay-Locked Loop) to delay copies of the clock signal. Each copy is delayed by a time equal to the clock frequency over 20. These copies are used to sample the data inputs during the serialization as shown in Fig. 60.

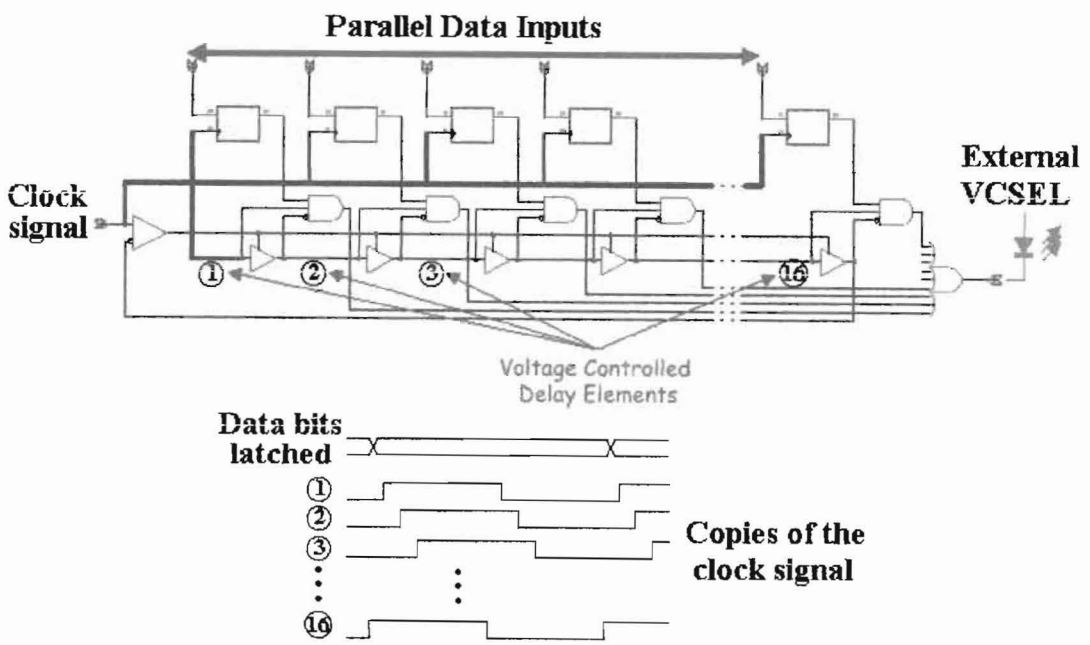


Figure 60: CHFET serializer principle of operation.

The DLL outputs a voltage VDLY, which defines the bit time for the serializer circuit. The higher VDLY, the longer is the time assigned to a data bit in the serial output. VDLY is a function of the input clock frequency. Nominally, VDLY must be such that the internal delays adjust every one of the 20 bits in the serial output to $1/(20*f)$, where f is the frequency of the clock signal. Another important feature is that the transference function VDLY(f) must be linear. Hence, the power supply of the circuit generating VDLY, i.e. V13 must have sufficient power available to place the operatiing point of VDLY around the center of the linear region. Table 25 and Figure 61 show the measured values and a plot of the VDLY(f) transference function.

The principle of operation makes the CHFET chip very sensitive to any jitter in the clock signal. And, the ultra-high speed needed to serialize the parallel stream makes the rise and fall times of the clock signal of crucial importance, because if the rise and fall times are large then the CHFET chip can sample the wrong data.

V13=1.3V, V2=2.2V		V13=1.4V, V2=2.2V		V13=1.6V, V2=2.2V		V13=1.8V, V2=2.2V		V13=2V, V2=2.2V		V13=2.2V, V2=2.2V	
f (MHz)	VDLY (V)	f (MHz)	VDLY (V)	f (MHz)	VDLY (V)	f (MHz)	VDLY (V)	f (MHz)	VDLY (V)	f (MHz)	VDLY (V)
34	0.992	32	0.961	36	1.025	38	1.063	38	1.064	40	1.105
36	1.031	34	0.991	38	1.064	40	1.101	40	1.102	42	1.144
38	1.069	36	1.029	40	1.101	42	1.136	42	1.139	44	1.182
40	1.106	38	1.068	42	1.137	44	1.174	44	1.177	46	1.222
42	1.141	40	1.105	44	1.175	46	1.214	46	1.217	48	1.266
44	1.18	42	1.14	46	1.214	48	1.256	48	1.26	50	1.311
46	1.22	44	1.178	48	1.256	50	1.301	50	1.304	52	1.359
48	1.263	46	1.219	50	1.302	52	1.349	52	1.353	53	1.385
50	1.309	48	1.262	52	1.351	53	1.375	53	1.378	54	1.412
-----	-----	50	1.308	53	1.377	54	1.401	54	1.405	56	1.469
-----	-----	52	1.357	54	1.403	56	1.458	56	1.461	58	1.532
-----	-----	53	1.383	56	1.461	58	1.522	58	1.525	60	1.605
-----	-----	54	1.408	58	1.525	60	1.595	60	1.597	62	1.609
-----	-----	56	1.468	60	1.599	62	1.613	62	1.612	64	1.605
-----	-----	-----	-----	62	1.616	64	1.61	64	1.608	-----	-----
-----	-----	-----	-----	64	1.613	-----	-----	-----	-----	-----	-----

Table 25: VDLY as a function of the frequency and V13.

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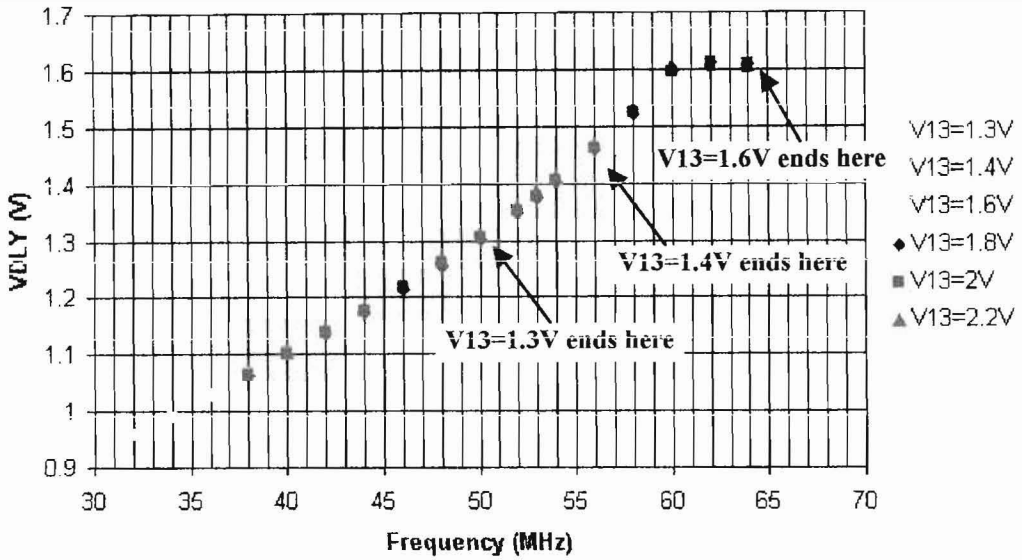


Figure 61: VDLY as a function of the frequency and V13.

Note: All these measurements was done verifying that the signals from the G-link were sync with the serializer CLK (RR) and in Fill frame mode.

c) CHFET operative modes (FF mode, Data mode (16 bits), Control mode and Flag mode):

Fill frame mode (PWRUP=H, MODE=H, ED=L, D17=X, D18=H, D19=H and D20=X):

	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
Sent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
R	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Table 26: In this table we show the levels applied to each input signal on the serializer (Sent) and what we received from the G-Link (R).

Test result: This mode works very well. The G-Link receiver chip has no problem to synchronize to FF patterns set by the CHFET. The FF patterns alternate as expected.

Data mode (PWRUP=H, MODE=H, ED=H, D17=X, D18=H, D19=H, D20=X):

	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
S	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
R	?	?	?	?	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
	?	?	?	?	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16

Table 27: In this table we show the levels applied to each Data bit from serializer (S) and what we received from the G-Link (R).

Test result: The first four data bits are not received right. Bits D15-D16 are received correctly.

Control mode (PWRUP=H, MODE=H, ED=H, D17=X, D18=L, D19=H and D20=X):

	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
S	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
R	?	?	?	?	D5	D6	D7	D10	D11	D12	D13	D14	D15	D16	0	0

Table 28: In this table we show the levels applied to each input signal on the serializer (S) and what we received from the G-Link (R).

Test result: The first four data bits are not received right. Bits D15-D16 are received correctly.

Flag mode (PWRUP=H, MODE=H, ED=H, D17=X, D18=H, D19=L and D20=f):

	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
S	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
R	?	?	?	?	D5	D6	D7	D10	D11	D12	D13	D14	D15	D16	0	0

Table 29: In this table we show the levels applied to each Data bit from serializer (S) and what we received from the G-Link (R).

Test result: The first data bits are not received right. Bits D5-D20 are received correctly. The flag bit *f* (D20 on the serializer), is inverted with respect to the standard G-Link protocol. This particular problem can be corrected by software.

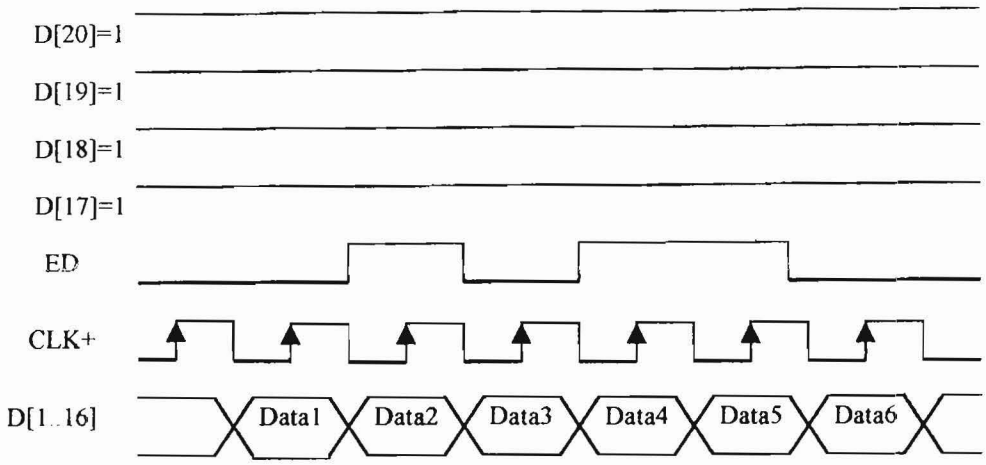
Other conclusions:

1. Only Fill frames synchronize the serializer with the G-link. Control, Data or Flag frames do not synchronize the serializer with the G-link.

2. The CHFET registers the control signals (ED, D[17..20]) and data bits (D[1.. 16]) at the rising edge of CLK+. The data out (1st bit sent out to the VCSEL) is aligned to the falling edge of CLK+. The delay between the rising edge which latches the parallel data to the 1st bit out is 1½ clock cycles.

3. The CHFET seems to register the ED signal one clock cycle later than the data present at the inputs. In principle when ED is active (low) the CHFET must generate a Fill Frame word. Hence, the data lines D1-D15 are all don't-care. However, as shown in Fig. 62, the data word concurrent with the 1st active ED cycle is taken by the CHFET and transmitted out. Instead, the serializer does not transmit the data word following the last ED active clock.

Serializer settings



We expect

FF Data2 FF Data4 Data5 FF

But the G-Link receives:

FF FF Data3 FF Data5 Data6

Figure 62: An example to show the problem with ED signal.

This problem could be solved by software.

4. Clock Issues: The serializer generates an error when going from Fill Frame or Control mode to Data mode if the 53Mhz clock signal rise or fall time is larger than 1.5 ns. The errors were almost totally removed using a better clock signal (less than 5OOps of rise and fall times). However, the error still exists when the CHFET is set to send one Fill frame and then one Data frame alternately. This error is not present if the transmitted pattern is n Fill Frames followed by m Data frames, with n>1 and m>1.

5. The frames sent by the means of the VCSEL can be seen by reviewing the optical power signal and the RR clock signal. You can see the frame starting in the rising edge of the RR clock signal.

6. Optical power measurements of the Honeywell HFE4080 VCSEL connected to the CHFET serializer were performed using a Tektronix TEK P6701A optical probe.

The optical signal shown as Fig. 63 explains why we are having problems with Dl, D2, D3 and D4. Because Dl has 2 values in one frame, D2, D3 and D4 have a large variation in their width. If this problem is solved in future versions then the CHFET serializer will be a very good option for the Readout and Control Optical Interface of the BTeV Pixel Vertex Detector.

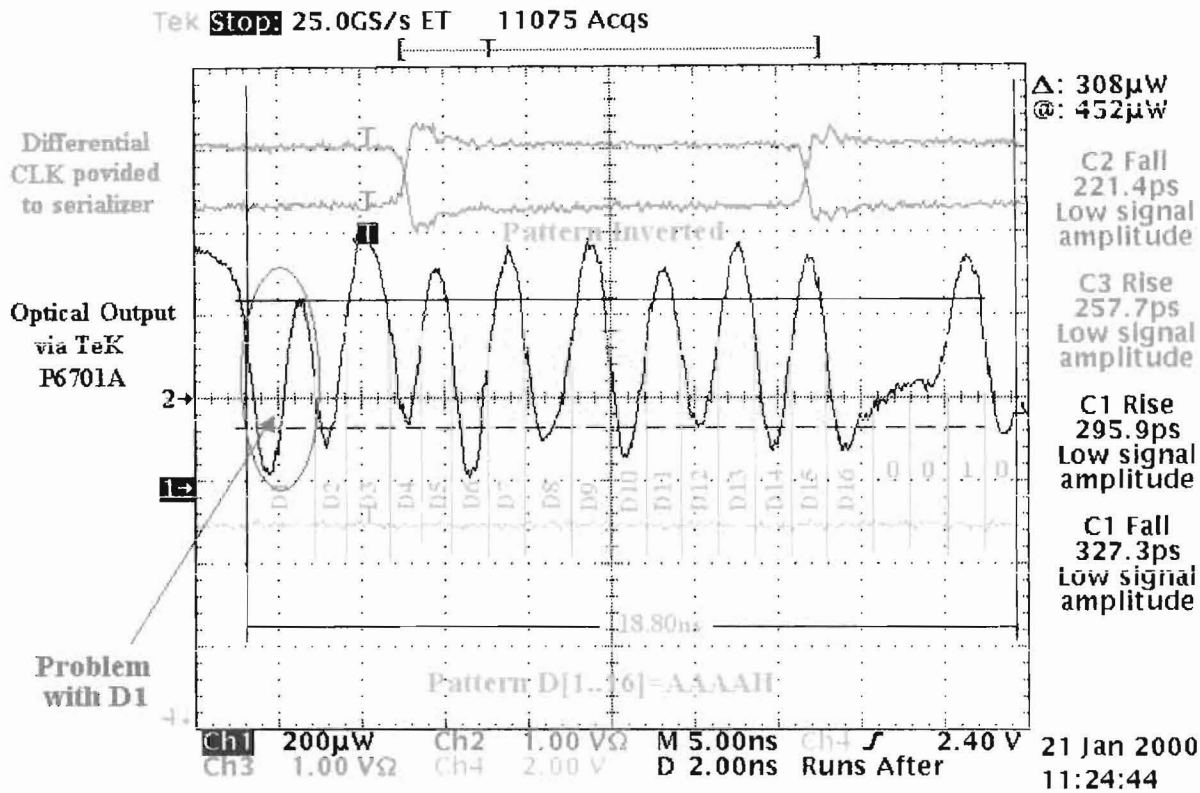


Figure 63: Optical signal emitted from the Honeywell HFE4080 VCSEL. The pattern set was D[1..16]=AAAAH, as we can see from the figure the optical pattern is inverted.

d) Signal Voltage Ratings:

The data (D[1.. 16]) and control (ED, D1117..20]) bits needs a maximum of 0.9 V to be recognized as a Boolean 0. The data (D[1..16]) and control (ED, D[17..20]) bits needs a minimum voltage of 1.1 V to be recognized as a Boolean 1. The signals were tested up to 3.3V.

5.4.1 Optical G-Link transmitter based on the CHFET serializer and the Honeywell HFE4080 VCSEL.

Figure 64 shows the schematic of the daughter card containing the optical G-Link transmitter based on the CHFET serializer and the Honeywell VCSEL HFE4080. This daughter was designed to be 100 % compatible with the optical G-Link transmitter daughter card based on the G-Link transmitter HDMP1032 and the Finisar module FTM8510. If future version of the CHFET serializer works correctly its optical G-Link transmitter daughter card will be a very good option.

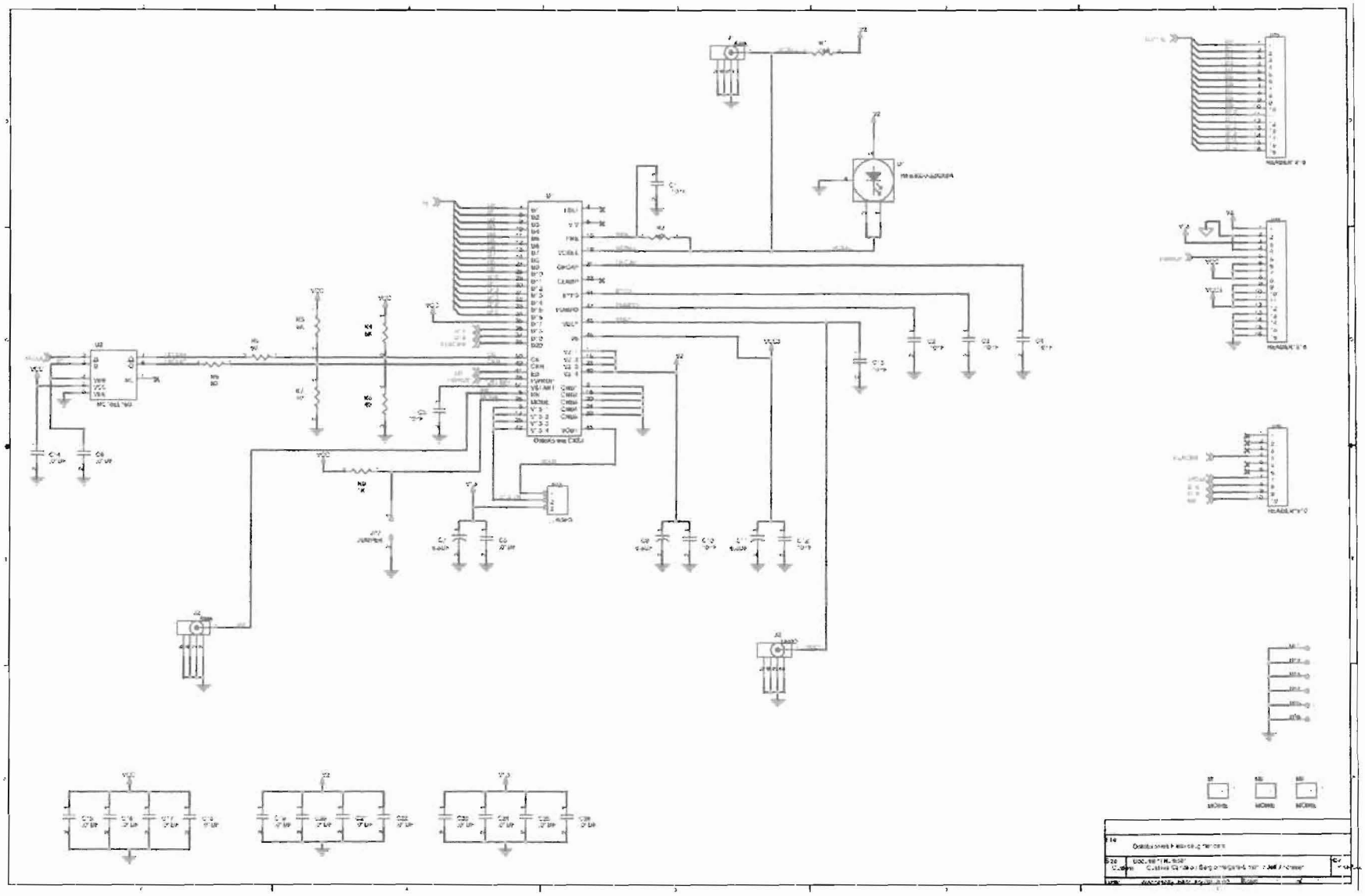


Figure 64: Schematic of the G-Link transmitter daughter card based on the CHFET serializer and the Honeywell HFE4080 VCSEL.

5.5 Conclusions

In this chapter we have implemented the 1.06 Gbps optical link with two options, the first is based on the Agilent G-Link chip set HDMP1032/34 with the Finisar modules FTM8510 and FRM8510. The other option is based on the CHFET serializer with a Honeywell HFE4080 VCSEL and the Agilent G-Link receiver HDMP1034 with the Finisar module FRM8510. The second option requires that the CHFET serializer performs correctly.

We have designed the 106 Mbps optical link and implemented the 1.06 Gbps optical link. We are finally ready to build the first prototype of the Readout and Control Optical Interface Board for the BTeV Pixel Vertex Detector.

Chapter Six

Optical Readout and Control Interface for the BTeV Pixel Vertex Detector

The design and performance of the first prototype of the Optical Readout and Control Interface (ORCI) designed and built at Fermilab is detailed in this article. Features of note are the decision to operate PIN photodiodes in photovoltaic mode and the decision to drive VCSELs with voltage rather than current. The reasons for these choices are given in Chapter 3. While not all components included in the present design are radiation hard, a completely radiation hard version is envisioned for the future.

6.1 First prototype of the Optical Readout and Control Interface (ORCI) for the BTeV Pixel Vertex detector

The first prototype of the ORCI for the BTeV pixel vertex detector contains two optical links. The first one operates at 104 Mbps and transmits commands to program and control the FPIX readout chips [6] contained on one multi-chip module (MCM) from the counting room to the detector. The second one operates at 1.04 Gbps and reads out all the detector hit data from the MCM and sends it to the counting room. A block diagram of the system is shown in Fig. 65.

The MCM is an array of pixel readout chips (FPIX) mounted on a single sensor and connected in daisy chain using a flexible interconnect circuit [37]. The FPIX chips contain the front-end electronic cells and column-based readout circuitry for the pixel sensors. In order to achieve the needed resolution for tracking and vertexing, the pixel unit cell is very small, 50 microns by 400 microns in size. The FPIX chips contain cells of the same size, which will be bump-bonded to the sensors. The control and readout protocol of the current version of the FPIX chips, called FPIX1, requires that there be 13 control inputs to the MCM, 7 command lines to program the chips and 6 command lines to control the readout. It also contains 17 data output lines for readout of the hit information provided by the detector. We expect that the control and readout protocols of more advanced versions of the FPIX readout chips will be different.

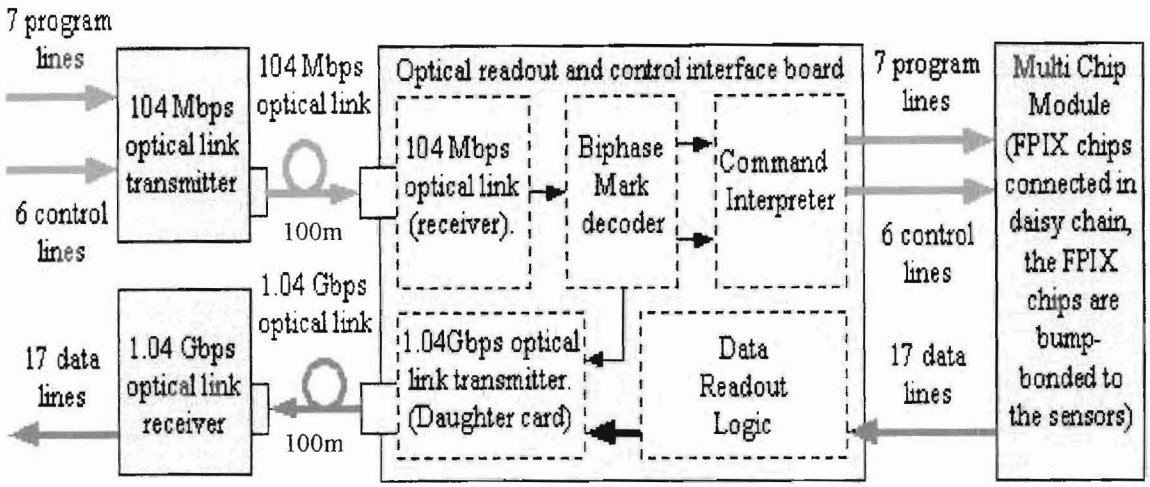


Figure 65: Block diagram of the first prototype of the ORCI for the BTeV pixel detector.

6. 2 The command and control link transmitter

Figure 66 contains a block diagram showing the components of the 104 Mbps optical link transmitter, which receives the program and control lines from the data acquisition system and encodes the information into a 7-bit protocol, see Fig. 67. The first bit is always one to indicate the beginning of the data frame. The next five bits provide the unique identifier for the command and control line being sent. The seventh bit is the data (high or low) to be sent to the corresponding command and control line. The signal produced by the 7-bit protocol generator is non-return to zero (NRZ). In order to send both the NRZ signal and the clock in a single data stream they are converted to bi-phase mark code. The protocol generator and the bi-phase mark encoder are implemented in a Field Programmable Gate Array (FPGA). The 104 Mbps transmitter uses a VCSEL driver to modulate the signal supplied to a Mitel 1A444 VCSEL. The VCSEL translates the bi-phase signal into an optical signal.

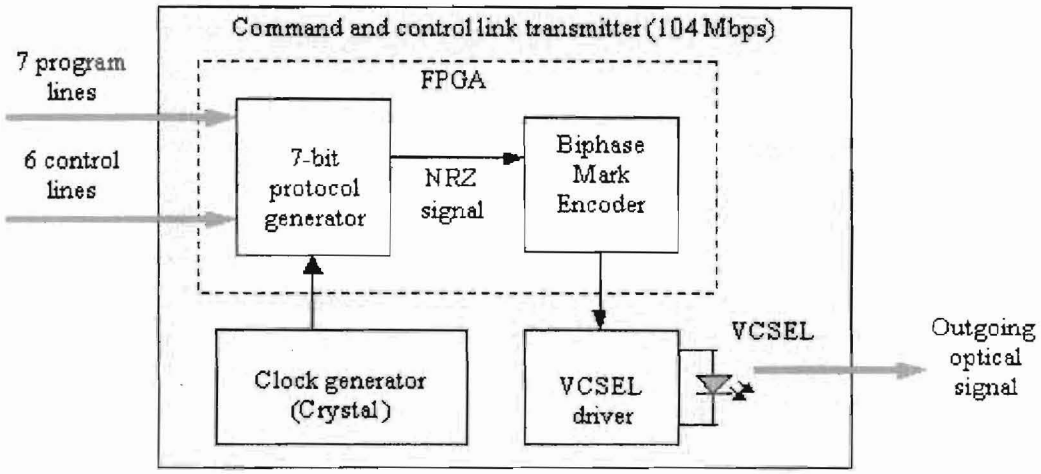
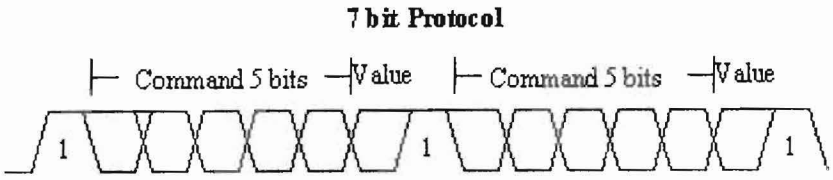


Figure 66: Block diagram of the 104 Mbps optical link transmitter.



Signal	Command	Signal	Command
Programres	00001	Token_in1	01001
Reg0	00010	TReadClk	01010
Reg1	00011	TBCOClk	01011
Reg2	00100	Datares	01100
Load_Kill	00101	Reserved from	01101
Shiftin1	00110	to	11101
ShifClk	00111	Software Preset	11110
Trigacc	01000	Software Reset	11111

Figure 67: 7 bit protocol.

6.3 The command and control link receiver

Figure 68 contains a block diagram of the command and control link receiver. The recovered signal must pass through a bi-phase mark decoder to separate the command signal and the clock signal. Following this, the command signal passes through an interpreter that identifies the data received and the corresponding command line. These functions have been implemented in an FPGA. Finally, the data are sent on the correct command line to the MCM.

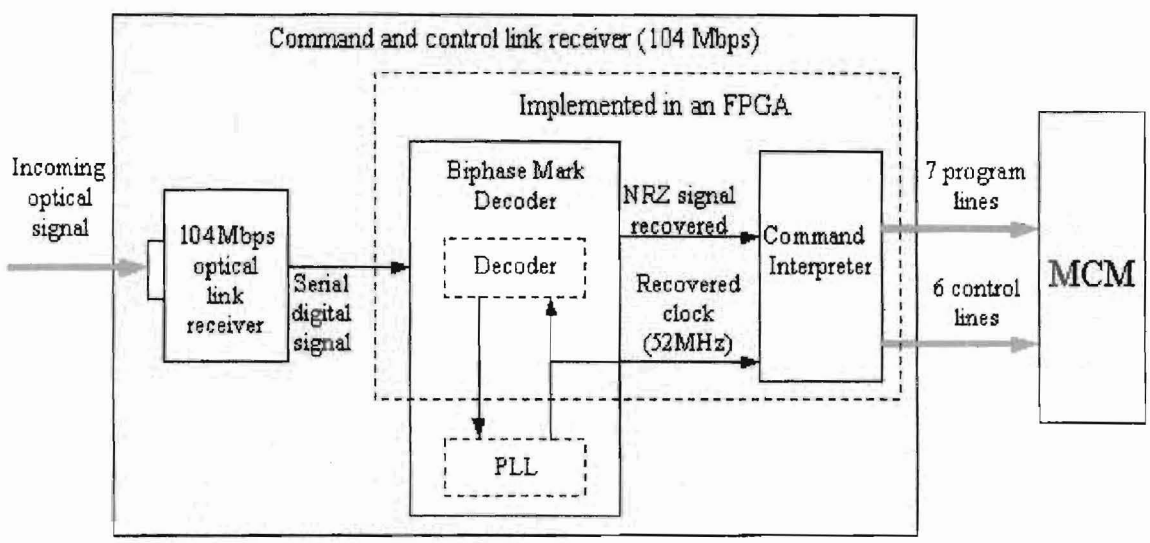


Figure 68: Block diagram of the command and control receiver section of the Optical Readout and Control Interface Board.

The bi-phase mark decoder uses a 104 MHz square signal to separate the clock signal from the command signal. A phase-locked loop (PLL) is used to keep the receiver circuit synchronized with the incoming optical signal. The PLL uses a voltage controlled crystal oscillator (VCXO) to generate a 52 MHz clock signal and a phase and frequency detector that it is implemented in the FPGA. We synchronize the signal recovered with a 26 MHz square signal to get the best performance from the PLL. The original design the VCXO should be at 53 MHz, however, the VCXO available with the closest frequency was the VECTRON VCXO VDUGLD at 52 MHz. Then all the performance tests of the 106 Mbps and the 1.06 Gbps optical links will be at 104 Mbps and 1.04 Gbps respectively.

6.4 The readout optical link transmitter

The data acquisition system sends the request to the MCM to read out the hit data using the 6 readout control lines. These are sent and received by means of the 104 Mbps optical link described above. The 17 data lines which output the hit data from the MCM are input to the FPGA, which delivers 16 of these data bits in parallel to the 1.04 Gbps optical link transmitter along with the corresponding 52 MHz clock, as shown in Fig. 69. The 17th bit, data valid, is transmitted and received as one of the four G-link control bits.

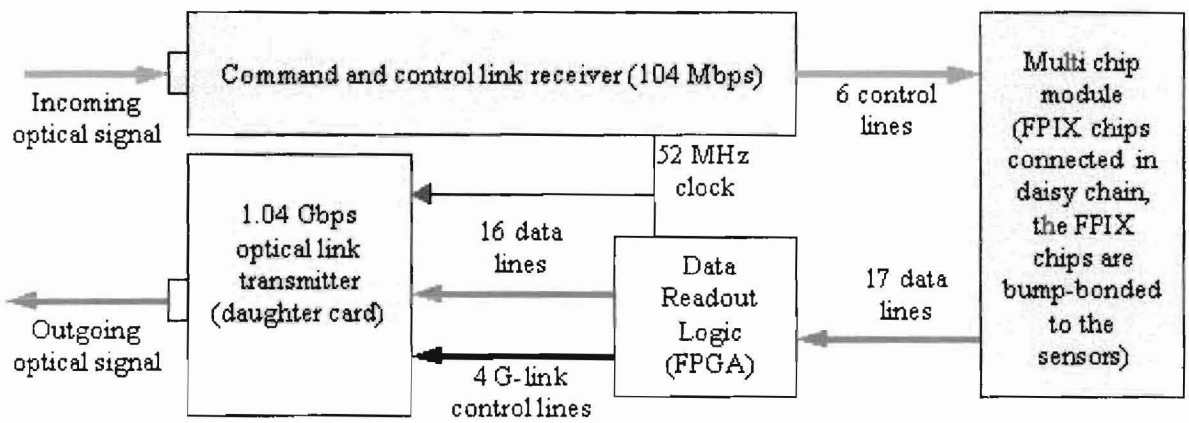


Figure 69: Block diagram of the circuit used to read out all the data generated by the detectors on the MCM.

The use of the data readout logic to input the data to the optical transmitter provides the possibility of checking out all the commands that are sent to the MCM. When we are transmitting commands to program the FPIX chips on the MCM, we need only to reroute the information in the control words to the FPGA and input them to the 1.04 Gbps optical link transmitter instead of the hit data generated in the MCM.

The 1.04 Gbps transmitter has been placed on a daughter card to allow the use of two versions of the 1.04 Gbps optical link transmitter. The first version, which is not radiation hard, is based on the HDMP-1032 G-Link transmitter [34], low power version, and the optoelectronic Finisar module FTM-8510 (See Fig. 70). The second option will be radiation hard. It will be

built using a custom VLSI serializer in CHFET process [14]. Since this serializer includes a VCSEL driver, the serializer can be connected directly to the VCSEL as shown in Fig. 71. Both the G-link transmitter and the CHFET serializer encode the information using the Conditional Invert Master Transition (CIMT) protocol [34]. Because the serializer is compatible with the HDMP-10X2 G-Link transmitter series, the daughter boards are interchangeable and both are fully compatible with the rest of the system. Thus, either daughter card can be used on the Optical Readout and Control Interface Board (ORCIB) without having to make any other changes. The function of the daughter card is to translate the parallel frame at 52MHz into a serial frame at 1.04 Gbps to send the MCM information to the counting room.

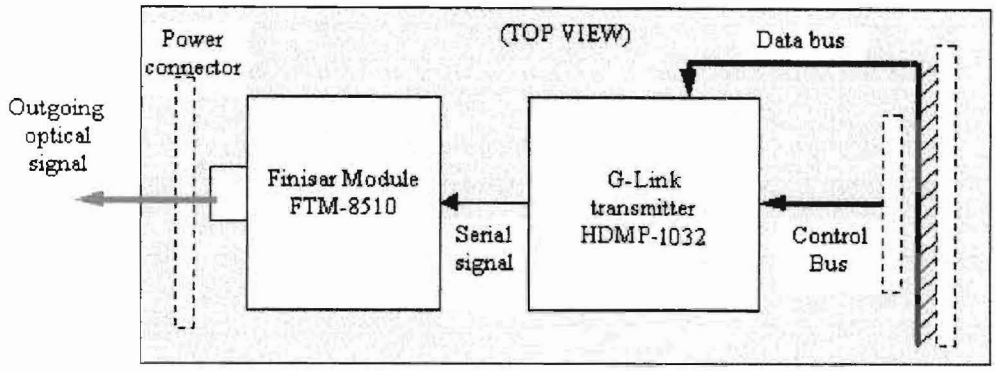


Figure 70: Block diagram of the Daughter board based on the G-link transmitter HDMP-1032.

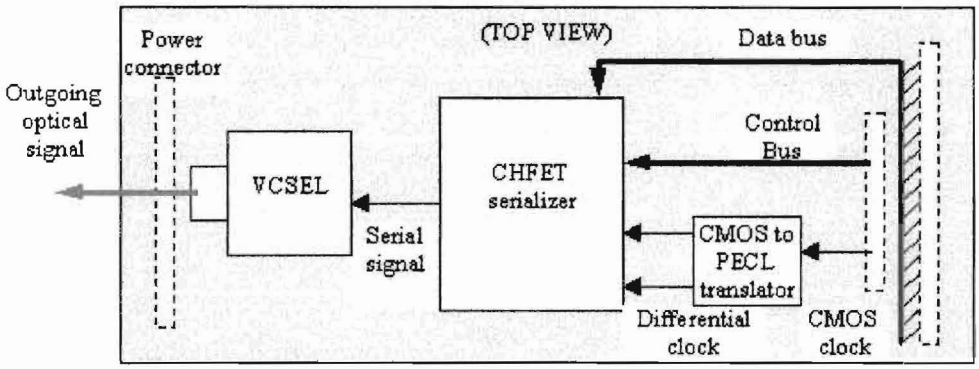


Figure 71: Block diagram of the Daughter board based on the CHFET serializer and a Honeywell HFE4080 VCSEL.

Tests of a preliminary version of the CHFET serializer show that it needs a differential clock signal with rise and fall times no more than 500ps and a jitter peak to peak of 100ps. This places rather stringent timing requirements on the bi-phase mark decoder, which supplies the clock signal to the daughter cards. On the CHFET serializer daughter card, we translate the CMOS clock signal coming from the mother board into a differential PECL signal and provide it to the CHFET serializer. The translator delivers a PECL clock signal with 350 ps rise and fall times. The daughter card with the HDMP-1032 G-link transmitter needs a clock signal with less than 250 ps jitter peak to peak and less than 1.5 ns rise and fall time. Thus, the clock signal

supplied by the mother board to the daughter cards must have less than 100 ps jitter peak to peak and less than 1.5 ns rise and fall times to work with either of the daughter cards.

6.5 The readout optical link receiver

The 1.04 Gbps optical link receiver uses a Finisar module FRM 8510, which translates the optical signal at 1.04 Gbps into an electrical signal. This electrical signal is supplied to an HDMP-1034 G-Link receiver, low power version. The chip translates the serial frames into parallel frames, recovers the 52 MHz clock, and synchronizes the recovered clock with the 52 MHz local clock as shown in Fig. 72.

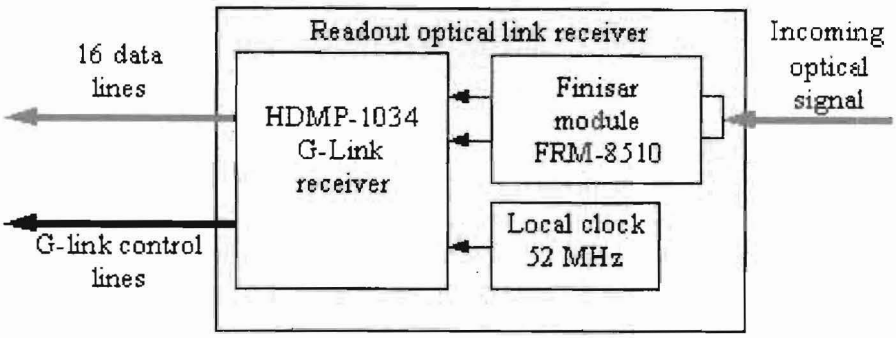
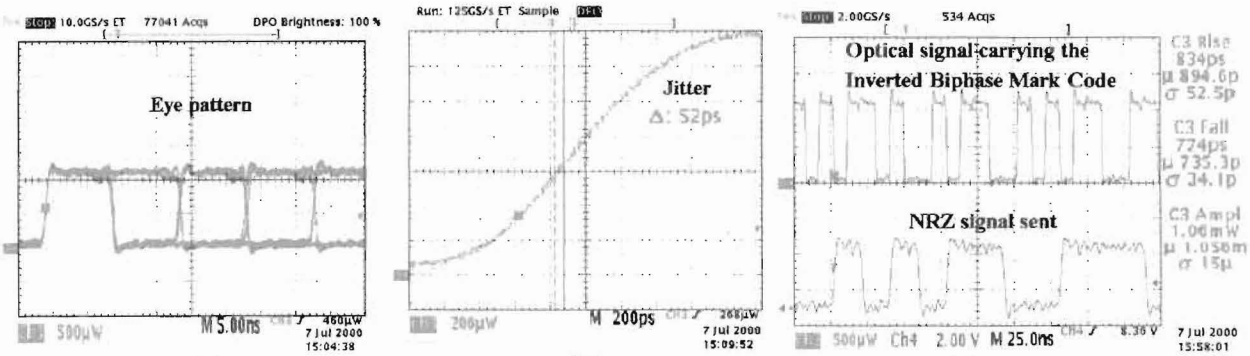


Figure 72: Block diagram of the readout optical link receiver.

6.6 Performance of the first prototype of the ORCI

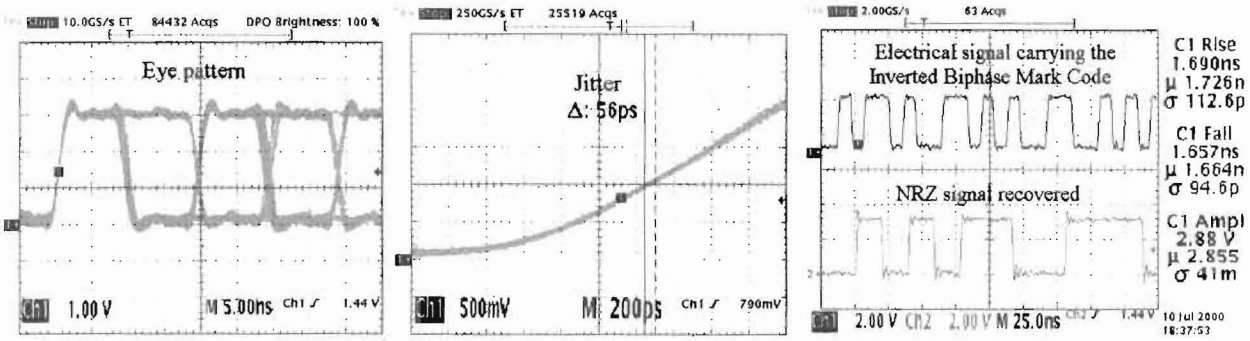
The VCSEL driver in the 104 Mbps optical link transmitter was designed to produce a minimum variation in optical power between different Mitel 1A444 VCSELs. The characteristics of the optical signal output by the 104 Mbps optical link transmitter are very open-eye pattern, 52 ps of jitter peak to peak, and rise and fall times of about 800 ps. These are shown in Fig. 73 along with the NRZ signal and the corresponding optical signal carrying the inverted bi-phase mark code.



(a) (b) (c)

Figure 73: Optical signal carrying the inverted bi-phase mark code. (a) Eye pattern, (b) Jitter and (c) Rise and fall times of the optical signal transmitted. Figure 73c also shows the NRZ signal sent.

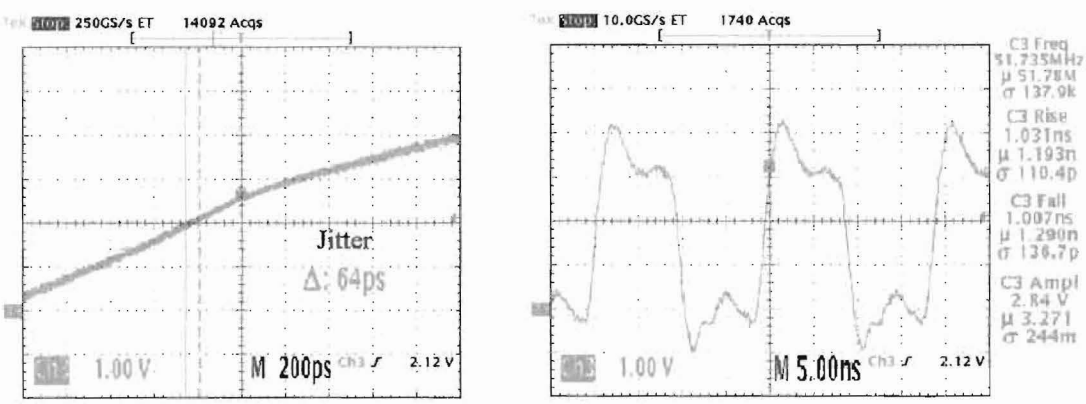
The 104 Mbps optical link receiver recovers the signal with very open-eye pattern, 56 ps of jitter peak to peak, and rise and fall times of 1.7 ns (See Fig. 74).



(a) (b) (c)

Figure 74: Electrical signal carrying the bi-phase mark code recovered. (a) Eye pattern, (b) Jitter and (c) Rise and fall times of the 104 Mbps optical link receiver. Figure 74c also shows the NRZ signal recovered.

The PLL designed and built for the ORCIB provides a clock signal with a jitter of only 64 ps peak to peak and rise and fall times of 1.2 ns to the G-Link daughter cards. The characteristics of this clock signal are shown in Fig. 75.



(a) (b)

Figure 75: Clock signal supplied to the CHFET serializer or HDMP-1032 Glink receiver. (a) Jitter and (b) Rise and fall times.

The performance of the first prototype of the ORCI for the BTeV Pixel Vertex Detector is very good. The 104 Mbps optical link receiver recovers the signal with only a slight increase in jitter (about 4 ps) relative to the optical signal transmitted. The rise and fall times increase to 1.7 ns because of the performance limitations of the discriminator. The Bit Error Rate (BER) is another very good indicator of the performance of an optical link and can be calculated [38] as follows:

$$BER \approx \frac{e^{-(SNR^2/2)}}{SNR \times \sqrt{2\pi}} \tag{16}$$

with SNR = Signal to Noise ratio.

We have measured a peak to peak noise of 5mV on the PIN photodiode's output terminal without any optical signal impinging on it. The responsivity of the PIN photodiode is 0.45A/W and is operated in photovoltaic mode with a load resistance of 190 ohms. Using these inputs we can calculate the SNR ratio as a function of the optical power impinging on the PIN photodiode as follows:

$$SNR = \frac{0.45\frac{mA}{mW}R_L P_0}{5mV} = \frac{0.45\frac{mA}{mW}\times 190\Omega}{5mV}P_0 = {}^{17.1P_0}\!/_{mW} \tag{17}$$

where R_L is the load resistance of the PIN photodiode operated in photovoltaic mode and P_0 is the peak to peak optical power impinging on the photodetector.

With Eqn. 16 and 17 we can obtain BER. The experimental BER was measured using the 7-bit protocol generator as our pattern generator; this generates a long serial stream of bits. This signal is encoded by the bi-phase mark encoder. The bi-phase mark signal is input to the 104 Mbps optical link transmitter. The 104 Mbps optical link receiver recovers the signal. Afterwards, there is a comparison between the recovered signal and the original signal. If they are not equal, the error counter is incremented by one. A block diagram is shown as Fig. 76.

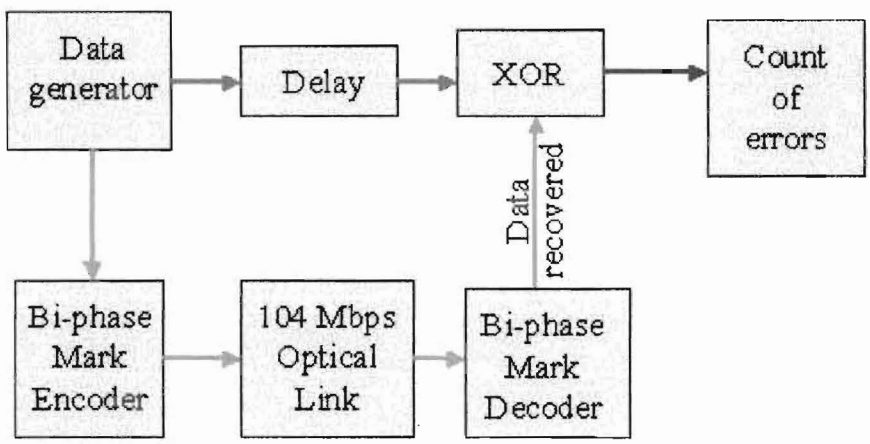


Figure 76: Block diagram of the BER test of the 104 Mbps optical link.

In Fig. 77 we show the theoretical and experimental BER of the 104 Mbps optical link as a function of the optical power impinging on the PIN photodiode.

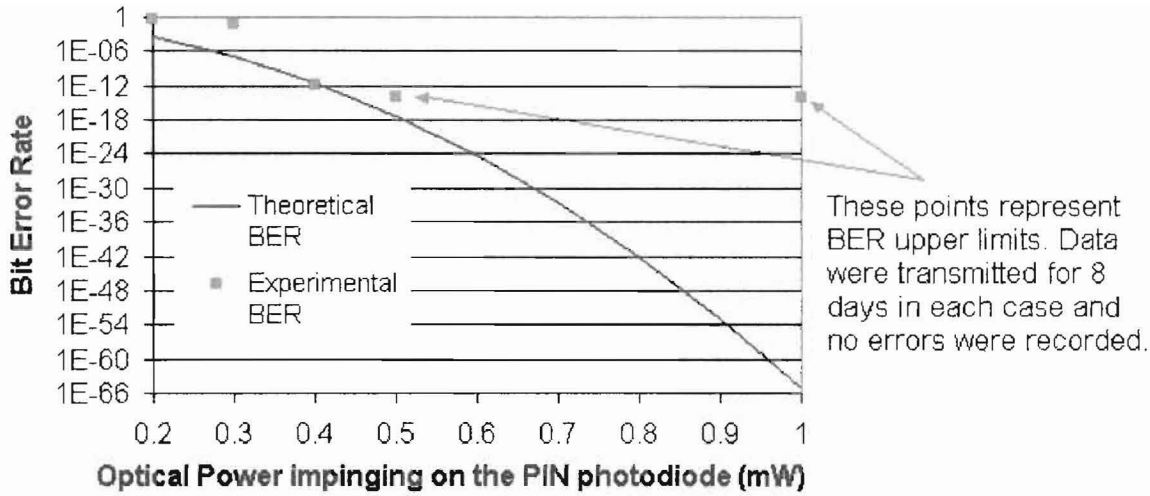


Figure 77: Theoretical and experimental BER of the 104 Mbps optical link.

The measured BER is very small, as expected, which indicates that the bi-phase mark decoder accurately reproduces the information sent from the counting room.

The 1.04 Gbps optical link, which transmits the data generated in the MCM, presents a very open-eye pattern, 56 ps of jitter peak to peak, and rise and fall times about 700 ps (See Fig. 78).

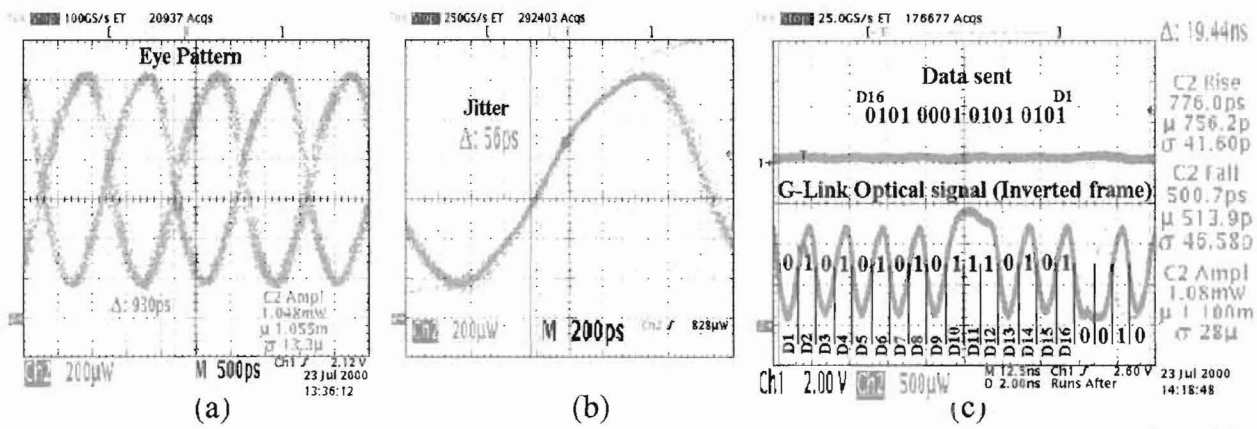


Figure 78: G-Link, Optical signal carrying the 16 data bits plus the 4 coding bits generated by the CIMT. (a) Eye pattern, (b) Jitter and (c) Rise and fall times of the 1.04 Gbps optical link transmitter.

To test the 1.04 Gbps optical link it was generated an walking one pattern. In Fig. 79 is shown the pattern recovered by the 1.04Gbps receiver.

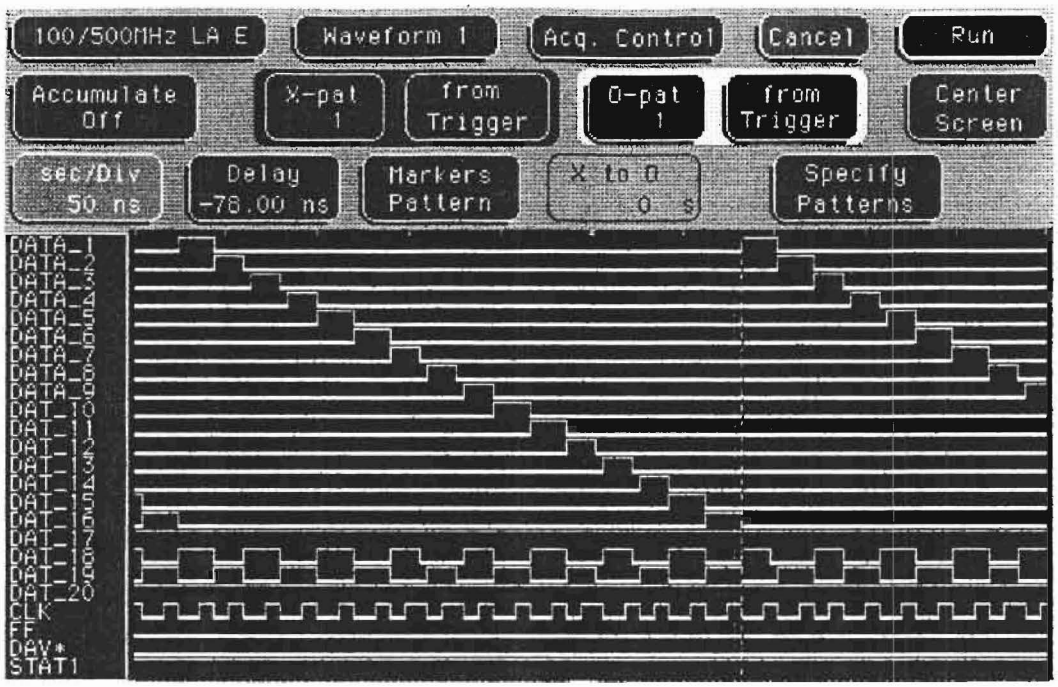


Figure 79: Walking one pattern recovered.

The 1.04 Gbps optical link has been shown by others to have a very low BER [39]. The FPGA is not radiation hard, but radiation hard FPGAs are available up to 300kRad [40]. As we have seen in Chapter 3, both the HFE-4080 VCSELs from Honeywell and the 1A444 VCSELs from Mitel have been shown to be radiation hard.

6.7 Tests of the ORCI with the MCM

To verify that the ORCI provides the correct command and control signals to the MCM and performs the readout without introducing errors, we took advantage of an existing test stand at Fermilab, including software. We repeated the noise and threshold uniformity tests that had been carried out using the test stand without the ORCI, and thus were able to make a direct comparison between the two performances. The software developed runs under the LABVIEW framework and was designed to execute the threshold dispersion and noise measurements to characterize the FPIX1 chips on the MCM. Two computers running two different programs are used. One computer controls the test stand instruments and the data acquisition (DAQ); the second performs the data analysis. The DAQ program uses one data generator to send all the commands to configure the MCM and another data generator to send the commands to control the readout. The data acquired are input to a logic analyzer, which transfers them via a local area network (LAN) to the second computer for analysis. The analysis program first fits the threshold curve for each pixel to get the threshold and noise for the individual cells. It then fits a Gaussian to the threshold and noise distributions for the pixels on each chip to determine the mean threshold, threshold dispersion, mean noise, and noise dispersion for each of the five FPIX1 chips on the MCM. Full details are contained in reference 42.

We made the following modifications to the test stand to include the ORCI in the system. For the control path, instead of connecting the two data generators directly to the inputs of the MCM, we connected them to the inputs of the 104 Mbps optical link transmitter and connected the outputs of the 104 Mbps optical link receiver to the command and control lines of the MCM. For the readout path, instead of connecting the 17 data output lines of the MCM directly to the logic analyzer, we connected them to the inputs of the 1.04 Gbps optical link transmitter and the outputs of the 1.04 optical link receiver to the logic analyzer. No changes were needed to the software used to characterize the FPIX1 readout chips on the MCM. A picture of the setup is shown as Figure 80.

Table 30 shows the results of the threshold and noise uniformity tests of the MCM, obtained with and without the ORCI in the setup. Figure 81 shows the threshold and noise distribution of the first of the five FPIX1 chips on the MCM without using the ORCI. Figure 82 shows the threshold and noise distribution of the same FPIX1 chip using the ORCI. The results are seen to be the same within errors. The noise is slightly higher for the case with the ORCI, most likely because of the unshielded flat cables used to interface it to the MCM.

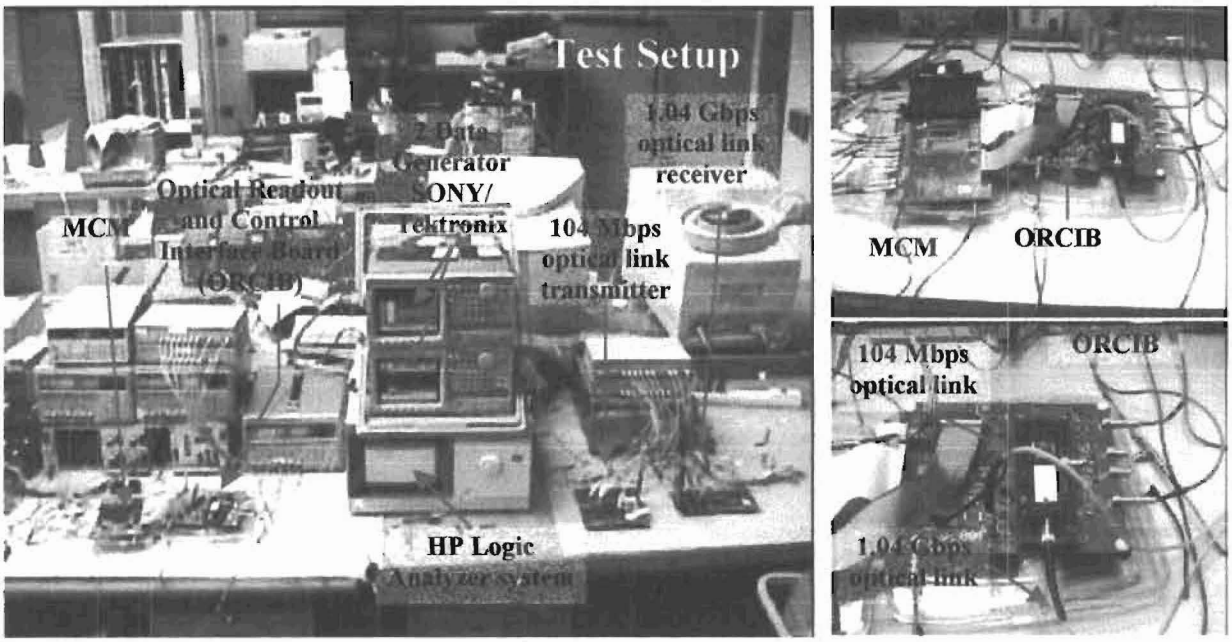
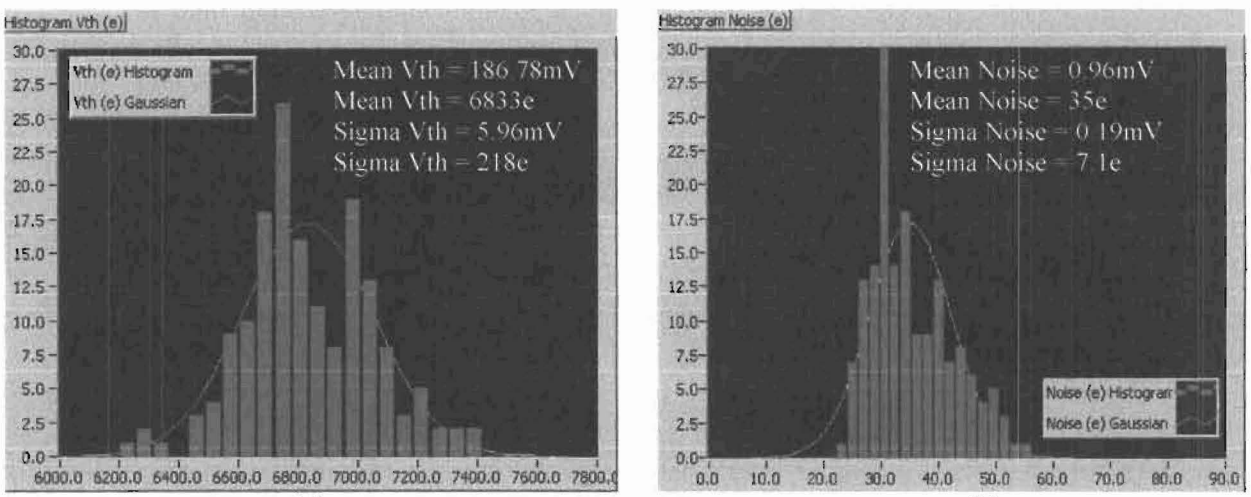


Figure 80: Setup used to characterize the MCM using the optical links to program, control and read out the MCM.

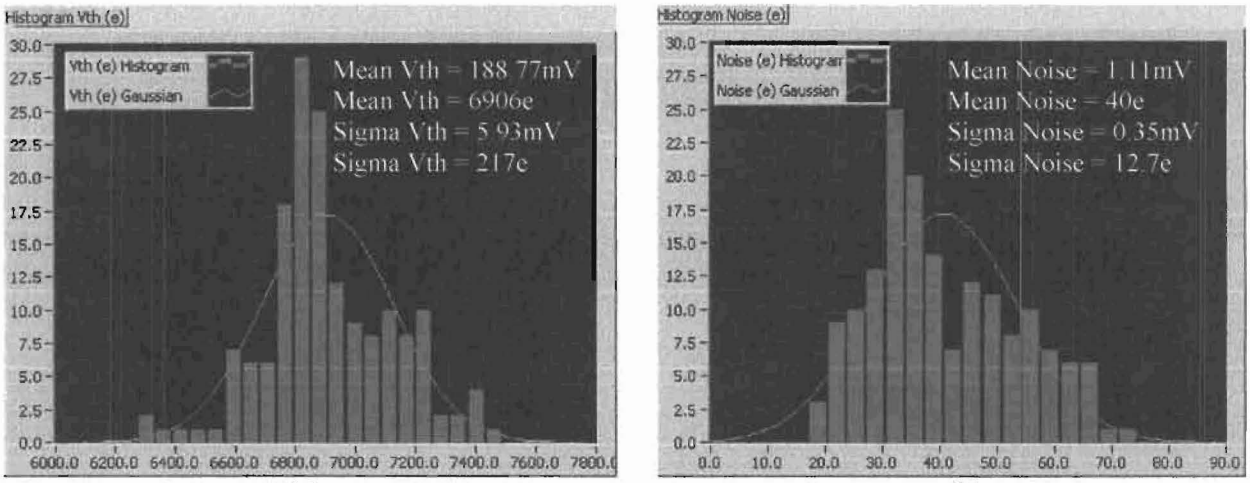
Vth0 = 1.95V	Results of the characterization of the MCM when tested without the ORCI				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6833	6657	6581	6792	6956
Threshold dispersion (e-)	218	239	217	168	146
Mean noise (e-)	35	37	37	31	31
Noise dispersion (e-)	7.1	8.1	9.0	5.9	6.2
Vth0 = 1.95V	**Results of the characterization of the MCM when tested with the ORCI**				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6906	6886	6820	6910	7051
Threshold dispersion (e-)	217	184	179	142	161
Mean noise (e-)	40	37	38	32	30
Noise dispersion (e-)	12.7	13.5	12.9	9.6	9.6

Table 30: Results of the threshold and noise uniformity of the MCM when tested with and without the ORCI.



(a) (b)

Figure 81: Distribution of the first of the five FPIX1 chips on the MCM when tested without the ORCI. a) Threshold distribution and b) Noise distribution.



(a) (b)

Figure 82: Distribution of the first of the five FPIX1 chips on the MCM when tested with the ORCI. a) Threshold distribution and b) Noise distribution.

6.8 Conclusions

The first prototype of the ORCI for the BTeV pixel vertex detector has been designed, built, and tested at Fermilab. The 104 Mbps optical link provides high accuracy transmission of information in a very wide range of optical power as is evident from the low BERs measured. By driving the VCSELs with voltage we achieve better system uniformity. The decision to use the PIN photodiode in photovoltaic mode results in an improved SNR and is expected to make it less susceptible to SEU. Both of these design choices are expected to provide a larger margin of safety relative to potential radiation damage. And, the 1.04 Gbps optical link has shown a very good performance. We have not performed BER test on this optical G-link because previous studies have shown that this optical G-link has very low BER.

GENERAL CONCLUSIONS

- We have seen that we need to provide a very high bit rate transmission to read out all the hit data coming from the MCM. Because of this the BTeV experiment has decided to use two optical links. One optical link is to program and control all the FPIX readout chips on the MCM. The other optical link will be to read out all the data hit generated in the MCM. The first will be a 106 Mbps optical link and the second will be 1.06 Gbps optical link.

- The Mitel single VCSELs show better performance than the Honeywell single VCSELs, e. g. the Mitel VCSELs have a linear optical power-forward current relationship. The optical power variation between the Mitel single VCSELs is very large, up to 80%. All the Mitel PIN photodiodes used in photovoltaic mode have demonstrated excellent performance at ultra-high frequency (~GHz). The Mitel (up to 10^14 n/cm^2) and Honeywell (up to 10^13 n/cm^2) single VCSELs are radiation hard, The Mitel single VCSELs have shown very fast rise and fall times about 800 ps and might be even faster but the cutoff frequency test could not be performed. This Mitel single VCSEL also had only 50ps of jitter and a threshold of only 4mA. The VCSEL and PIN arrays showed very good performance with a very fast rise and fall times of only 250 ps, a jitter of 48 ps, a cutoff frequency of 1.18 GHz, current threshold of only 2 mA, and a maximum crosstalk of only 1.5 %, which is negligible. The PIN photodiodes in the array used in photovoltaic mode as for the single PIN photodiodes are able to work at ultra-high frequencies. The best way to drive the VCSEL is with previously applied current bias plus a modulated current.

- The 106 Mbps optical link transmitter was designed to produce a minimum variation in optical power between different Mitel 1A444 VCSELs. Measurements have shown that if we drive the VCSEL with current we get up to 80% optical power variation among the VCSELs under test. When we drive the VCSELs with voltage with the BTeV prototype driver, we get a maximum variation of only 25%. The 106 Mbps optical link receiver is an inherently low noise circuit, because the PIN photodiode is being operated in photovoltaic mode [11]. In the absence of an applied electric field, charge motion is caused only by the small electric field produced by the electron-hole pairs generated in the depletion region of the PIN photodiode [21]. Also, the depletion region is limited in size by the properties of the device, since there is no reverse bias voltage applied which would increase its size. We believe that this will reduce the impact of Single Event Upset (SEU) due to strong interactions in the PIN photodiodes and plan to carry out tests to demonstrate this in the near future. We use the Biphase-Mark code to hold the DC balance in the 106 Mbps optical link.

- To recover the command and clock signals from the Biphase-Mark code we need to use two square signals one of 106 MHz and the other of 53 MHz. These square signals need to be synchronized with the incoming Biphase-Mark signal. It is not easy to synchronize these signals, because the Biphase-Mark signal does not have periodic phase, periodic rising edge or periodic falling edge. We designed a circuit to generate a periodic signal from the incoming Biphase-Mark signal. Using this circuit we were able to use a Phase Locked Loop (PLL) to synchronize the periodic signal with the 53 MHz clock signal in the 106 Mbps optical receiver.

- We implemented the 1.06 Gbps optical link with two options, the first is based on the Agilent G-Link chip set HDMP1032/34 with the Finisar modules FTM8510 and FRM8510. The other option is based on the CHFET serializer with a Honeywell HFE4080 VCSEL and the Agilent G-Link receiver HDMP1034 with the Finisar module FRM8510. The second option requires that the CHFET serializer performs correctly.

- The first prototype of the ORCI for the BTeV pixel vertex detector has been designed, built, and tested at Fermilab. The 104 Mbps optical link provides high accuracy transmission of information in a very wide range of optical power as is evident from the low BERs measured. By driving the VCSELs with voltage we achieve better system uniformity. The decision to use the PIN photodiode in photovoltaic mode results in an improved SNR and is expected to make it less susceptible to SEU. Both of these design choices are expected to provide a larger margin of safety relative to potential radiation damage. And, the implemented 1.04 Gbps optical link has shown a very good performance. We have not performed BER test on this optical G-link because previous studies have shown that this optical G-link has very low BER.

- With the first prototype of the Optical Readout and Control Interface for the BTeV pixel vertex detector we are doing a contribution to help that the BTeV experiment comes true.

REFERENCES

[1] Fermilab's webpage, http://www.fnal.gov/pub/tour.html.

[2] Butler J., Stone S., "*Proposal for an Experiment to Measure Mixing, CP Violation and Rare Decays in Charm and Beauty Decays at the Fermilab Collider, BTeV*", Fermilab Internal document, May 1999.

[3] J. Butler, S. Stone, et. al., "*Proposal for an experiment to measure mixing, CP violation, and rare decays in Charm and Beauty particle decays at the Fermilab collider- BTeV*", submitted to the Fermilab Program Advisory Commite, May 2000. Stage I approval given June 27, 2000.

[4] Santoro, A., et al., *"BTeV: An Expression of Interest for a Heavy Quark Program at C0"*, Fermilab Internal document, May 18, 1997.

[5] Ed Barsotti, et. al., *"Flex Circuit for the Detector Plane Interconnect"*, Internal Document # ESE-PIX-9981014, October 14, 1998.

[6] G. Cancelo, et. al., "*High readout speed pixel chip development at Fermilab*, Fourth Workshop on Electronics for LHC Experiments", 528-532, 1998.

[7] Scott W. Cortize, *"Semiconductor light source essentials"*, IEEE Spectrum, c1998.

[8] Orazio Svelto, *"Principles of Lasers"*, Plenum Press New York and London, c1982.

[9] http://w3.osa.org/ABOUTOSA/LOCALSEC/speakers/chouquette.html

[10] http://www.cco.caltech.edu/~nanofab/AScherer/VCSELArr.html

[11] Jasprit Singh, *"Semiconductor Optoelectronics"*, McGraw-Hill, c1995.

[12] Watson, *"Optoelectrónica"*, Limusa, c1993.

[13] Fiber options, *"Learning about options in fiber"*, Fiber options, New York, c1994. You can download this document from: http://www.fiberoptions.com/home/index.html selecting Literature and later Introduction to fiber.

[14] Mitel Semiconductor , "*Mitel VCSEL Laser Diode 1A444 Data Sheet*", c1998.

[15] Honeywell, "*Honeywell High Speed Fiber Optic VCSEL HFE4080 Data Sheet*", c1998.

[16] Mitel Semiconductor, "*Mitel High-Performance PIN 1A354 Data Sheet*", c1998.

[17] Mitel Semiconductor, "*Mitel VCSEL array 4D469 Data Sheet*", c1999.

[18] Mitel Semiconductor, "*Mitel PIN array 4D470 Data Sheet*", c1999.

[19] P. Denes, "*Digitalization and Data Transmission for the CMS Electromagnetic Calorimeter*", Proccedings of the 4th workshop on electronics for the LHC experiments. Rome, Italy September 1998.

[20] http://www.atlas.uni-wuppertal.de/optolink/wuppertal/annealing.html.

[21] G. F. Knoll, "*Radiation Detection and Measurement*", Wiley, New York, 2nd edition, c1989, p. 350.

[22] National Semiconductor, *"National 1.1 GHz Ultra-Wideband Monolithic Op Amp Data Sheet"*, c1998.

[23] Maxim, "*Maxim Single/Dual/Quad, Ultra-High-Speed, +3V/+5V, Beyond-the_Rails Comparators Data Sheet*", c1998.

[24] http://www.altera.com

[25] Altera corporation, "*Altera Programmable Logic Device Family MAX7000A Data Sheet*", c2000.

[26] Altera corporation, "*Altera MAX+PLUS II getting started*", c1997.

[27] Altera corporation, "*Altera Quartus Programmable Logic Development System and Software*", c1999.

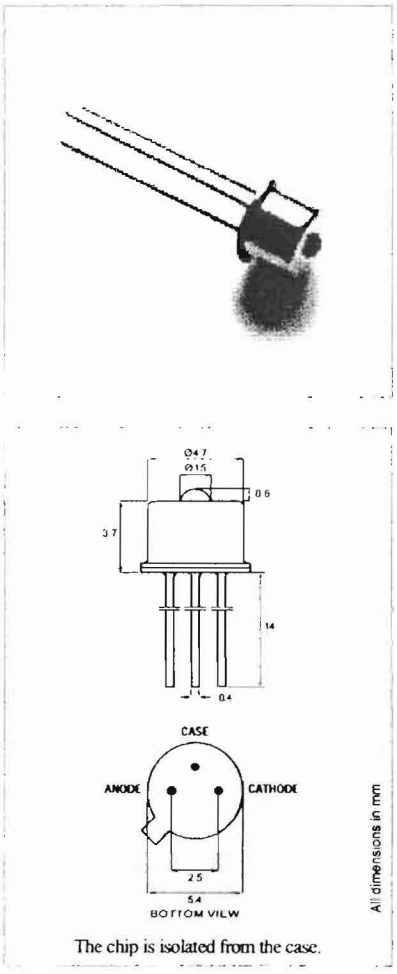
[28] Roland E. Best, "*Phase-Locked Loops, McGraw-Hill, New York*", 4th edition, c1999.

[29] VECTRON International, *"VECTRON Voltage Controlled Crystal Oscillator (VCXO) Data Sheet"*, c1999.
[30] EXAR corporation, *"EXAR High Frequency Clock Multiplier STA49C101A-XX Data Sheet"*, c1999.
[31] Texas Instruments, *"Texas Instruments Micropower Supply Voltage Supervisor TLC7701 Data Sheet"*, c1999.
[32] Hewlett-Packard Co., *"HP Low Cost Gigabit Rate Transmit/Receive Chip Set HDMP-1012/1014 Data Sheet"*, c1994.
[33] Hewlett-Packard Co., *"HP Low Cost Gigabit Rate Transmit/Receive Chip Set with TTL I/Os HDMP-1022/1024 Data Sheet"*, c1997.
[34] Agilent Technologies, Inc., *"Agilent HDMP-1032/1034 Transmitter/Receiver Chip Set Data Sheet"*, c2000.
[35] P. Denes, *"CHFET Fiber Optic Transmitter"*, CMS experiment at CERN, Internal Document, January 2000.
[36] Finisar Corporation, *"Finisar FTM/FRM-8510 Low Cost Gigabit Optical Transmitter/Receiver"*, c2000.
[37] S. Zimmermann, *"Development of High Data Readout Rate Pixel Module and Detector Hybridization at Fermilab"*, Presented at Pixel 2000, Genoa, Italy, June 2000.
[38] V. Arbert-Engels, et. al., *"Characterization of Optical Data Links for CMS experiment"*. Proceedings of the 3rd Workshop on Electronics for the LHC experiments. London, UK September 1997.
[39] K. Anderson, et. al., *"Neutron Irradiation Tests of an S-Link-over-G-Link System"*, ATLAS Tile Calorimeter internal document, November 1999.
[40] Actel Corporation, *"Data Sheet of Radiation-Hardened FPGAs"*, c2000.
[41] I. M. Gregor, *"Optical Links for the ATLAS SCT and Pixel Detector"*, Presented at PIXEL 2000. Genoa, Italy, June 2000.
[42] M. A. Vargas, et. al., *"The Development of Software to Characterize the Fermilab Pixel Readout Chip, FPIX1, for the BTeV experiment"*, Fermilab Preprint No. EFNAL-E-0897 accepted by NIMA, November 2000.
[43] K. Gill, et. all., *"Comparative Study of Radiation Hardness of Optoelectronic Components for the CMS Tracker Optical Links"*, Presented at the RADECS conference, Oxford, Sept. 1998 and the 4th LEB Workshop, Rome, Sept. 1998.
[44] F. Vasey et al, *"Development of radiation-hard optical links for the CMS tracker at CERN"*, IEEE Trans. Nucl. Sci., Vol 45, No. 3, pp. 331-337, 1998. Also visit the www page at: http://www.cern.ch/CERN/Divisions/ECP/CME/OpticalLinks/.
[45] J. Beringer, et. al., *"Final Results of Radiation Hardness and Life Time Studies of LEDs and VCSELs for Optical Links of the ATLAS Inner Detector"*, Proceedings of the Third Workshop on lectronics for the LHC Experiments, London, UK, 1997.
[46] Altera corporation, *"Byte Blaster Pararllel Port Download Cable Data Sheet*, pp. 299-312, February c1998". Also visit the www page at: http://www.altera.com .
[47] Penn Well, *"The importance of wide-bandwidth photodiodes/photoreceivers"*, Reprinted from the February 1999 edition of LIGHTWAVE, c1999.

PRODUCT INFORMATION

840nm	1A444 VCSEL Laser Diode	Datacom, General Purpose

This Vertical Cavity Surface-Emitting Laser is designed for Fibre Channel, Gigabit Ethernet, ATM and general applications. It operates in multiple transverse and single longitudinal mode, ensuring stable coupling of power and low noise. And it matches the 1A354 PIN Photodiode.



The chip is isolated from the case.

TO-46 Package With Lens

WARNING: Laser Radiation, avoid exposure to beam. Class 3B laser product, potential eye hazard. Warning labels in each box.

Optical and Electrical Characteristics (25°C Case Temperature)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Fiber-Coupled Power	P_{fiber}		1.3		mW	I_F=12mA (Note 1)
Optical Power	P_o	0.9	1.7	3.0	mW	I_F=12mA
Slope Efficiency (dP_o/dI_F)	η		200		mW/A	I_F=12mA
Bandwidth ($3dB_{el}$)	f_c		2		GHz	I_F=12mA
Peak Wavelength	λ_p	830	840	860	nm	I_F=12mA
Spectral Width (FWHM)	$\Delta\lambda$		0.5	1	nm	I_F=12mA
Forward Voltage	V_F		1.9	2.2	V	I_F=12mA
Threshold Current	I_{th}		3.5	6	mA	
Relative Intensity Noise	RIN		-130		dB/Hz	I_F=12mA, f=1 GHz

Note 1: Fiber: 50/125 Graded Index, NA=0.2 or 62.5/125 Graded Index, NA=0.275.

Absolute Maximum Ratings

PARAMETER	SYMBOL	LIMIT
Storage Temperature	T_{stg}	-55 to +125°C
Operating Temperature	T_{op}	0 to +70°C
Electrical Power Dissipation	P_{tot}	35 mW
Continuous Forward Current (f≤10 kHz)	I_F	15 mA
Peak Forward Current (duty cycle≤50%, f≥1 MHz)	I_{FRM}	25 mA
Reverse Voltage	V_R	1.5 V
Soldering Temperature (2mm from the case for 10 sec)	T_{sld}	260°C

Thermal Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Thermal Resistance - Infinite Heat Sink	R_{thjc}		400		°C/W
Thermal Resistance - No Heat Sink	R_{thja}		700		°C/W
Temp. Coefficient - Wavelength	$d\lambda/dT_j$		0.06		nm/°C
Optical Power - Variation 0 to 70°C	ΔP		±0.7		dB
Threshold Current - Variation 0 to 70°C	ΔI_{th}		±0.6		mA

13457 11 1998-02-04

MITEL SEMICONDUCTOR

Europe: Tel (46) 8 58 02 45 00 Fax (46) 8 58 02 01 10
Tel (44) 1291 436180 Fax (44) 1291 436771

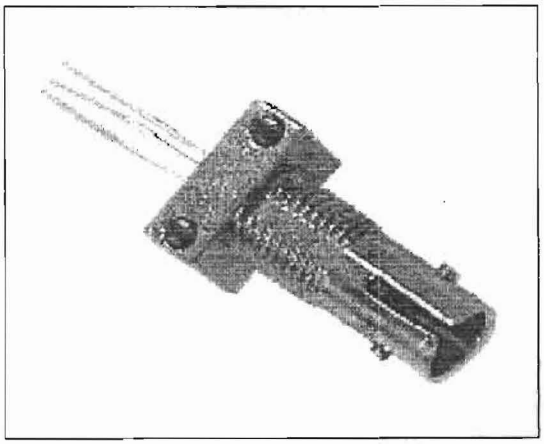
America: Tel 1-800-96MITEL Fax (613) 592-6909
Asia: Tel (65) 293 5312 Fax (65) 293 8527

HFE4080-32X/XBA

High Speed Fiber Optic VCSEL

FEATURES

- Industry standard ST®-LP fiber connector
- Designed for drive currents between 5 and 15 mA
- Optimized for low dependence of electrical properties over temperature
- High speed > 1 Ghz



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DESCRIPTION

The HFE4080-32X/XBA is a high-performance 850 nm VCSEL (Vertical Cavity Surface-Emitting Laser) intended for high-speed data communications. It combines many of the desirable features of an LED with the desirable features of a laser diode operating in a single longitudinal mode, but with multiple transverse modes reducing coherence and consequent modal noise in multimode fiber applications.

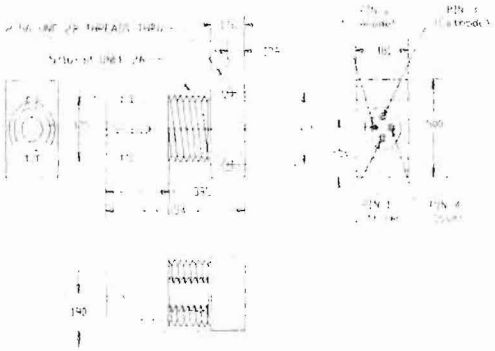
APPLICATION

The HFE4080-32X/XBA is a high radiance VCSEL packaged on a TO-46 header with a metal can assembled in a standard ST®-LP fiber connector. Data rates can vary from DC to above 2 GB/s depending upon component application. The VCSEL is designed to convert electrical current into optical power that can be used in fiber optic communications and other applications. As the current varies above threshold, the light intensity increases proportionally.

The component produces a circularly symmetric, narrow divergence beam. The stability of operating characteristics with temperature potentially allows operation without continuous photodiode feedback control, simplifying drive circuits considerably. The HFE4080-32X/XBA is designed to be used with inexpensive silicon or gallium arsenide detectors, but excellent performance can also be achieved with some indium gallium arsenide detectors.

The low drive current requirement of the HFE4080-32X/XBA makes direct drive from PECL or ECL logic gates feasible and eases driver design.

OUTLINE DIMENSIONS in inches (mm)



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Pin 1 identified by red sleeve

ST is a registered trademark of AT & T.

Honeywell

Honeywell reserves the right to make changes in order to improve design and supply the best products possible.

HFE4080-32X/XBA

High Speed Fiber Optic VCSEL

APPLICATION (continued)

The VCSEL is a class IIIb laser and should be treated as a potential eye Hazard. Due to the size of the component, the applicable warning logo type, aperture label, and certification/identification label cannot be placed on the component itself. The labels can be found inserted into the individual envelope in which the VCSEL unit is packaged, or attached to the envelope.

This product has been manufactured under a process license from Rockwell for U.S. PATENT # 4,368,098.

HFE4080-32X/XBA

High Speed Fiber Optic VCSEL

ELECTRO-OPTICAL CHARACTERISTICS (0°C<T<70°C unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Output power						
HFE4080-321/XBA	P_O	200	400	1000	µW	I_F = 10 mA (1)
		-7.0	-4.0	0.0	dBm	(1)
HFE4080-322/XBA	P_O	400	800	1500	µW	I_F = 10 mA (1)
		-4.0	-1.0	+1.8	dBm	(1)
Threshold current	I_{TH}		3.5	6	mA	(1)
Slope Efficiency	η		0.3		mW/mA	I_F = 10 mA
Forward Voltage	V_F		1.75	2.10	V	I_F = 10 mA
Reverse Breakdown Voltage	BVR	5.0	10.0		V	I_R = 10 µA
Peak Wavelength	λ_P	820	850	860	nm	I_F = 10 mA DC
Spectral Bandwidth	$\Delta\lambda$		0.5		nm	I_F = 10 mA DC
Rise and fall time	t_R, t_F		100	400	ps	Prebias above threshold, T = 25°C, 10-90% I_F = 10 mA DC
Analog bandwidth (2)						
Analog bandwidth[1]	BW		6		GHz	Small signal sinusoidal modulation
Relative Intensity Noise	RIN		-125	-116	dB/Hz	Measured into 1 GHz noise bandwidth
I_{TH} Temperature Coefficient	$\Delta I_{TH}/\Delta T$	-.042	0	.042	mA/°C	I_F = 10 mA
η Temperature Coefficient	$\Delta\eta/\Delta T$		-0.001		mW/mA/°C	I_F = 10 mA
P_O Temperature Coefficient	$\Delta P_O/\Delta T$		0		dB/°C	I_F = 10 mA
λ_P Temperature Coefficient	$\Delta\lambda_P/\Delta T$		0.06		nm/°C	I_F = 10 mA
V_F Temperature Coefficient	$\Delta V_F/\Delta T$		-0.2		mV/°C	I_F = 10 mA
Series Resistance	r_S		30.0		Ω	DC
Thermal Resistance	θ_{JA}		900		°C/W	

Notes

1. This product is tested with a 50/125 micron fiber.
2. Packaged components are limited by the electrical parasitics of the package.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-40 to +100°C
Case operating temperature	0 to +70°C
Lead solder temperature	260°C, 10 sec.
Continuous forward current (heat sinked)	15 mA
Reverse voltage	5 V @ 10 µA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Honeywell

Honeywell reserves the right to make changes in order to improve design and supply the best products possible.

HFE4080-32X/XBA

High Speed Fiber Optic VCSEL

ORDER GUIDE

Description	Catalog Listing
High speed VCSEL, 400µw typ. Po	HFE4080-321/XBA
High speed VCSEL, 800µw typ. Po	HFE4080-322/XBA

CAUTION

The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation to equipment, take normal ESD precautions when handling this product.

FIBER INTERFACE

Honeywell VCSELs are specifically designed to interface with 50/125 and 62.5/125 multimode fiber. While larger fiber sizes are possible, essentially all of the VCSEL power can be coupled into even the 50/125 fiber.

Fig. 1 Typical Power Output vs Forward Current

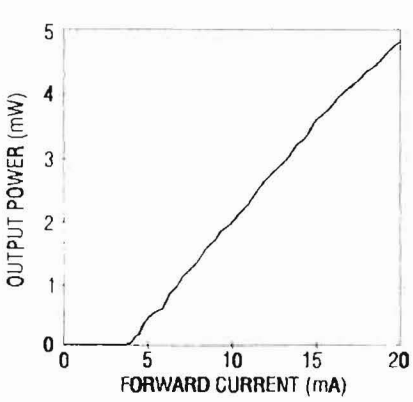


Fig. 2 Typical Threshold Current vs Temperature

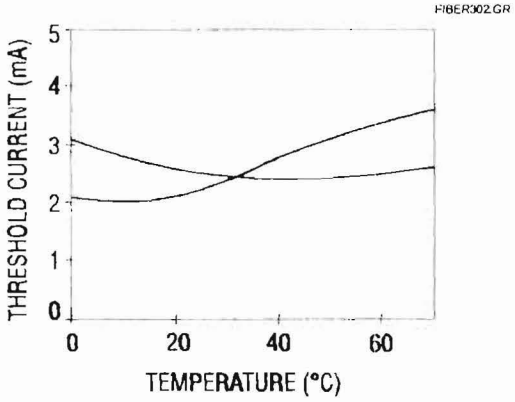


Fig. 3 Typical Spectral Output vs Wavelength

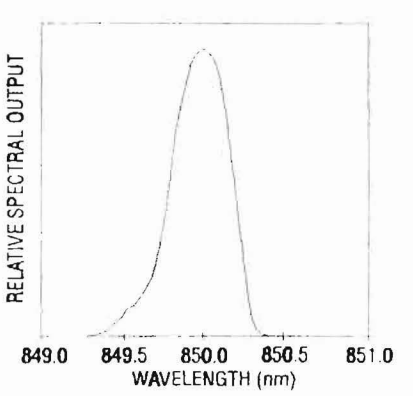
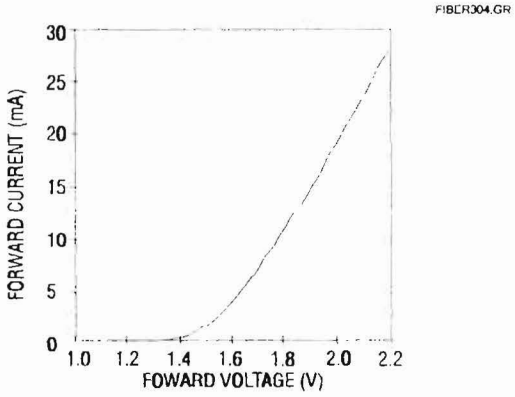


Fig. 4 Typical Current vs Forward Voltage



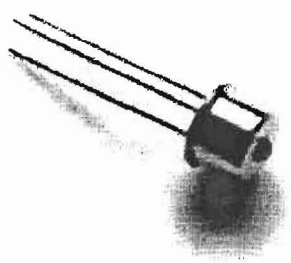
Honeywell reserves the right to make changes in order to improve design and supply the best products possible.

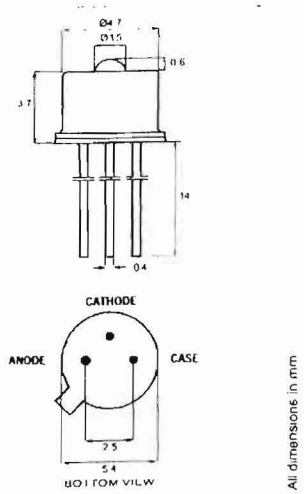
Honeywell

PRODUCT INFORMATION

750nm 850nm	1A354 High-Performance PIN	Datacom, General Purpose

The very high speed and low capacitance of this GaAs PIN Photodiode makes it ideal for datacom and general purpose applications. Its double-lens optical system is designed for single-mode fiber as well as for multimode fiber with core diameter up to 62.5µm. And a reverse voltage of only 5 Volts makes interfacing to a preamplifier easy.





The diode chip is isolated from the case.

TO-46 Package With Lens

Optical and Electrical Characteristics (25°C Case Temperature)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Responsivity (Fig. 1 & 2) (Table 1)	R	0.35	0.45		A/W	λ=850nm
Bandwidth	f_c		1		GHz	R_L=50Ω
Capacitance (Fig. 4)	C		1	2	pF	f=1MHz
Dark Current	I_d		0.4	1	nA	

Operating Conditions: V_R=5V. Fiber: Single-mode to multimode 62.5/125µm.

Absolute Maximum Ratings

PARAMETER	SYMBOL	LIMIT
Storage Temperature	T_{stg}	-55 to +125°C
Operating Temperature	T_{op}	-55 to +125°C
Reverse Voltage	V_R	30V
Soldering Temperature (2mm from the case for 10 sec)	T_{sld}	260°C

Thermal Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Temperature Coefficient - Dark Current	dI_d/dT_j		5		%/°C

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Asia: Tel (65) 293 5312 Fax (65) 293 8527

Typical Responsivity		
Core Diameter/Cladding Diameter Numerical Aperture		
10/125 µm 0.11	50/125 µm 0.20	62.5/125 µm 0.275
0.45 A/W	0.45 A/W	0.45 A/W

Table 1

FIGURE 1

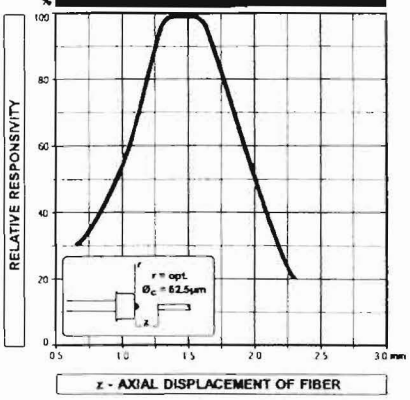


FIGURE 2

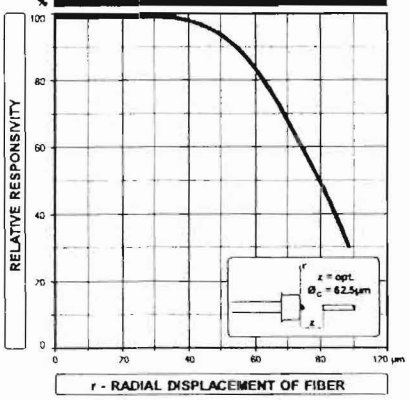


FIGURE 3

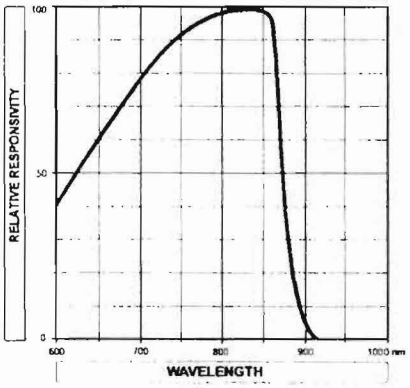
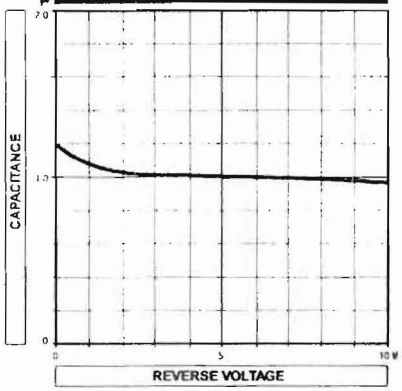


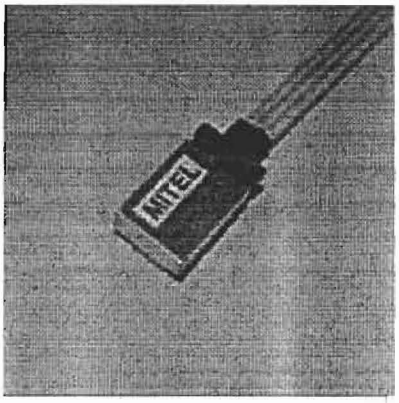
FIGURE 4

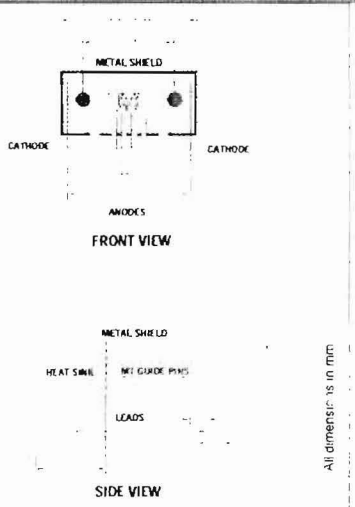


PRODUCT INFORMATION

840nm 4D469 VCSEL Array — **Parallel Datacom, Telecom** — PRELIMINARY/β

This device consists of a 4-channel VCSEL array in a miniature surface-mountable MT package. It is based on a unique combination of self-alignment technology and direct optical coupling to fiber, resulting in pure beam shapes and optimum coupling efficiency without need for active alignment. Applications include parallel Fibre Channel and optical interconnect inter/intra-board. And it matches the 4D470 PIN Photodiode Array.





The cathode is connected to the metal shield

VCSEL Array in MT Package

WARNING: Laser Radiation, avoid exposure to beam. Class 3B laser product, potential eye hazard. Warning labels in each box.

Optical and Electrical Characteristics (25°C Case Temperature)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Fiber-Coupled Power	P_{fiber}		1.0		mW	
Optical Power	P_O		1.1		mW	
Slope Efficiency (dP_O/dI_F)	η		250		mW/A	
Beam Divergence	Θ		15		deg	Full Width at $1/e^2$
Bandwidth ($3dB_{el}$)	f_c		2		GHz	
Peak Wavelength	λ_p	830	840	860	nm	
Spectral Width (FWHM)	$\Delta\lambda$		0.5	1	nm	
Forward Voltage	V_F		1.8		V	
Threshold Current	I_{th}		5.5		mA	
Relative Intensity Noise	RIN		-130		dB/Hz	f=1 GHz
Crosstalk	X		-25		dB_{el}	(Note 1)

Test Condition: I_f=10mA. Fiber Ribbon: 50/125 GI, NA=0.2 or 62.5/125 GI, NA=0.275.

Note 1: Crosstalk between adjacent channels operating at 2GHz.

Absolute Maximum Ratings

PARAMETER	SYMBOL	LIMIT
Storage Temperature	T_{stg}	-40 to +85°C
Operating Temperature	T_{op}	0 to +70°C
Electrical Power Dissipation	P_{tot}	20 mW/Channel
Continuous Forward Current ($f \leq 10$ kHz)	I_F	11 mA/Channel
Peak Forward Current (duty cycle ≤ 50%, f ≥ 1 MHz)	I_{FRM}	18 mA/Channel
Reverse Voltage	V_R	1.5 V
Soldering Temperature (2mm from the case for 10 sec)	T_{sld}	260°C

Thermal Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Thermal Resistance	R_{th}		TBD		°C/W
Temp. Coefficient -Wavelength	$d\lambda/dT_j$		0.06		nm/°C
Optical Power - Variation 0 to 70°C	ΔP		±0.7		dB
Threshold Current - Variation 0 to 70°C	ΔI_{th}		±0.6		mA

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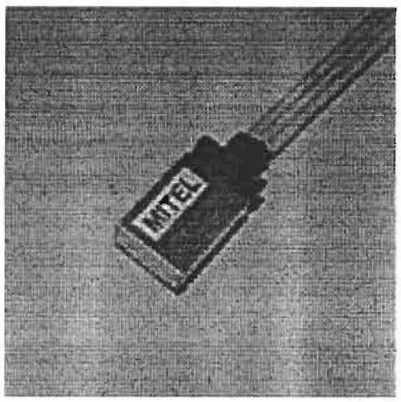
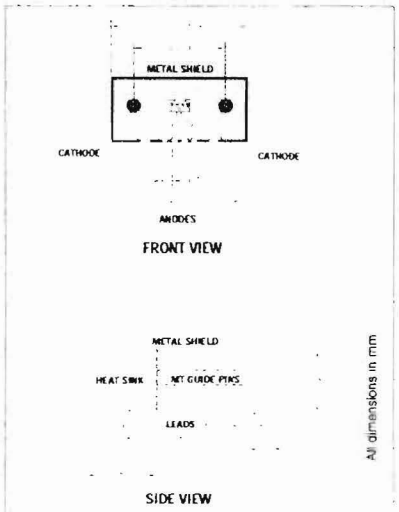
Asia: Tel (65) 293 5312 Fax (65) 293 8527

PRODUCT INFORMATION

840nm 4D470 PIN Array — **Parallel Datacom, Telecom** — PRELIMINARY/β

This device consists of a 4-channel PIN Photodiode array in a miniature surface-mountable MT package. It is based on a unique combination of self-alignment technology and direct optical coupling to fiber, resulting in optimum coupling efficiency without need for active alignment. Applications include parallel Fibre Channel and optical interconnect inter/intra-board. And it matches the 4D469 VCSEL Array.





The cathode is connected to the metal shield

PIN Array in MT Package

Optical and Electrical Characteristics (25°C Case Temperature)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Responsivity	R		0.45		A/W	λ=850nm
Bandwidth (3dB$_{el}$)	f_c		2		GHz	R_L=50Ω
Capacitance	C		1		pF	f=1MHz
Dark Current	I_d		0.4		nA	
Crosstalk	X		-30		dB$_{el}$	λ=850nm (Note 1)

Test Condition: V_R=3.3V or 5V. Fiber Ribbon: 50/125 GI, NA=0.2 or 62.5/125 GI, NA=0.275.

Note 1: Crosstalk between adjacent channels operating at 2GHz.

Absolute Maximum Ratings

PARAMETER	SYMBOL	LIMIT
Storage Temperature	T_{stg}	-40 to +85°C
Operating Temperature	T_{op}	0 to +70°C
Reverse Voltage	V_R	20V
Soldering Temperature (2mm from the case for 10 sec)	T_{sld}	260°C

Thermal Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Temperature Coefficient - Dark Current	dI_d/dT_j		5		%/°C

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PUBLICATIONS

1. S. Vergara, M. Sheaff, M. A. Vargas, "High Speed Radiation Hard Optical Links", Proceedings SOMI XIV CONGRESO DE INSTRUMENTACION, pp. 790-794, Tonanzintla, Puebla, MEXICO. 1999.

2. G. Cancelo, S. Vergara, A. Vargas, "Fiber Optic based readout for BTeV's Pixel Detector", Precedings, LEB 2000 Sixth Workshop on Electronics for the LHC experiments, pp. 502-506, Cracow, Poland, October, 2000.

3. S. Vergara, G. Cancelo, M. Sheaff, M. A. Vargas, "Optical Readout and Control Interface for the BTeV Pixel Vertex Detector", Fermilab Preprint FERMILAB-PUB-00-246E, November 2000, submitted to NIMA on September 2000.

HIGH SPEED RADIATION HARD OPTICAL LINKS

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RESUMEN
Los enlaces ópticos están llegando a ser una parte importante en los sistemas de lectura de datos generados en los experimentos de Física de alta energía, tales como el BTeV (Fermilab, USA), el ATLAS y el CMS del LHC (CERN, Suiza). En Fermilab, el BTeV ha decidió usar enlaces ópticos en el detector innermost, para este experimento el detector pixel estará compuesto de 93 planos pixel de 10x10cm cada uno, estos planos estarán colocados perpendicularmente y a solo unos milímetros del haz colimado. Los enlaces ópticos serán usados para enviar los comandos de la sala de control a los pixel chips para programarlos, para esto se usara un enlace óptico de 106Mbps. Por otro lado los datos generados por plano serán alrededor de 4Gbps, en este caso se podrían usar 4 u 8 enlaces ópticos de 1Gbps. Para ambos enlaces ópticos se ha decidido usar el Láser de Emisión Superficial con Cavidad Vertical (VCSEL).

Abstract
Optical links are becoming an important part in the readout systems of high energy physics experiments such as BTeV (Fermilab, USA) and both ATLAS and CMS at the LHC (CERN, Switzerland). At Fermilab, BTeV has decided to use optical links for control and readout of the innermost detector. This will be a pixel detector composed of 93 pixel planes of 10x10cm each. These planes will be perpendicular to the colliding beam and will be installed a few millimeters from the beam. Optical links will be used to send the commands from the control room to the pixel chips to program them. For this we will use an optical link of 106Mbps. On the other hand the data generated by each plane will be about 4Gbps. In this case we will use 4 to 8 optical links of 1Gbps each. For both the 1Gbps and 106Mbps optical links it has been decided to use Vertical Cavity Surface Emitting Laser (VCSEL) diodes as the light source.

1. INTRODUCTION

The BTeV experiment has been proposed for the C-Zero interaction region of the Tevatron at Fermilab. A sketch of the apparatus is shown in Fig. 1a. The magnet that we will use, called SM3, exists at Fermilab. The other important parts of the experiment include the vertex detector, the RICH detectors, the EM calorimeters and the muon system [1]. The vertex detector is a multi-plane pixel device that sits inside the beam pipe. The pixel detector is composed of 93 pixel planes of 10x10cm each, divided in 31 triple-stations perpendicular to the colliding beam and installed a few millimeters from the beam (Fig. 1b). A single pixel plane including attached readout electronics is shown as Fig. 2. This detector will be employed for on-line track finding for the lowest level trigger system, and, therefore, the pixel readout chip bump-bonded to the sensors will have to read out all detected hits. . Each pixel readout chip has 2880 channels and there will be about 13000 chips. This means a total of 3.8×10^7 channels receiving data from proton-antiproton collisions every 132ns. To send the commands to program each of these chips we will use an optical link of 106Mbps per half plane. To read out all the data generated by the pixel detectors we will use 4-8 optical links of 1Gbps per plane. Both the emitters of the 1Gbps optical links and the receivers of the 106 Mbps optical links will be about 10cm from the beam since they will be mounted on the detector planes. These devices will thus receive about 100Krad of radiation and will suffer some radiation damage. A further rather stringent requirement is that they must operate inside the beam pipe in vacuum at -10^0C.

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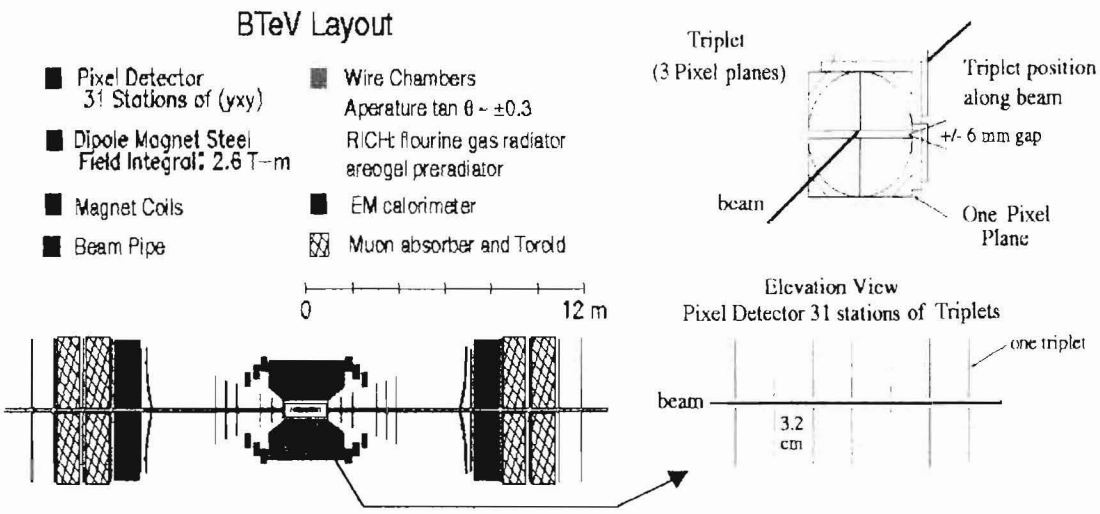
[1] *Scholarship holder of CONACyT, MEXICO/Work developed in a stay at Fermilab, PO Box 500, Batavia, ILL, 60510, USA*
[2] *University of Wisconsin, Madison WI 53706, USA/CINVESTAV, Mexico D.F., MEXICO*



a) b)

Figure 1. a) Sketch of the BTeV spectrometer and b) Single Pixel plane

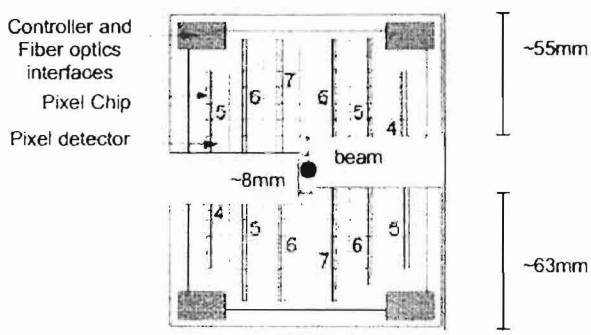


Figure 2. Two halves of the pixel plane

Thinking about these requirements BTeV has decided to use a relatively new kind of laser diode called a VCSEL (Vertical Cavity Surface Emitting Laser) as the light source in the optical links, since VCSELs have been shown to be radiation hard devices. A test developed by the CMS Electromagnetic Calorimeter at CERN [2] has shown that the Honeywell VCSEL HFE4080 has a decrease in its optical power of about 30% after an irradiation of 1Mrad. Another test developed by the D0 experiment at Fermilab [3] has shown that a Vixel VCSEL LA-M-850 has an increase in its current threshold of about 6% and a decrease in its optical power output of about 50% after an irradiation of $4.1\times10^{13}\ protons/cm^2$. The radiation was provided by a pulsed beam of 8GeV protons. A digital optical link has three main components (See Fig. 3), each with a specific function. The transmitter contains a light source, e. g., light-emitting diode (LED), edge-emitting laser diode (LD), or VCSEL that converts an electrical current into an optical signal. The receiver contains a photodiode that converts the light back into an electrical signal and an amplifier that makes the signal easier to detect. The fiber-optic cable carries the optical signal between them.

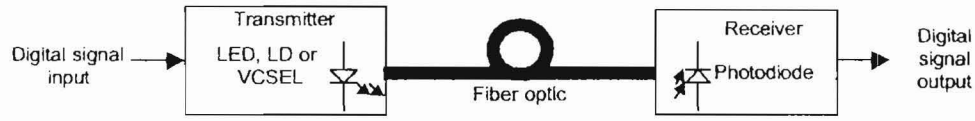


Figure 3: Basic digital optical link.

2. PERFORMANCE TESTS OF VCSELs AND PIN PHOTODIODE

To design an optical link we need to know very well the electrical and optical characteristics of the light source and the photodiode that we want to use to build it. In our case a VCSEL will be used as the light source. In order to study the properties of the device, we carried out performance tests on 2 Mitel single VCSELs 1A444, 3 Honeywell single VCSELs HFE4080, 1 Mitel VCSEL array 4D469, 3 Mitel PIN photodiodes 1A354 and 1 Mitel PIN photodiode array 4D470.

To perform the dc test on the PIN photodiodes and on single VCSELs we use the following instruments and materials: Tektronix PS2521D programmable power supply, PHOTODYNE 2275XQ Fiber Optic Test Set used as an optical power meter, FLUKE 76 multimeter, 1m fiber optic multimode cable ($50\ m/125\ m$, core/cladding) assembled with ST connectors or, in the case of the array, 1m 4-channel fiber ribbon assembled with MT-4 connectors. To develop the dc test of all the VCSELs in the array we used the following instruments and materials: Tektronix PS2521G programmable power supply, FLUKE 76 multimeter, Tektronix TDS 754C oscilloscope, 1m 4-channel fiber ribbon ($62.5\ m/125\ m$, core/cladding) assembled with MT-4 connectors. As an optical power meter we used the PIN photodiodes in the Mitel PIN array 4D470. The ac test on the single links was done at frequencies ranging from 0Hz to 50MHz, while the ac test on the link array was done over a wider range from 0Hz to 2GHz. The single link test range was limited to 50MHz because we didn't have available a test board capable of operating at ultra-high frequencies. To do the ac test on the single links and the link array between 0Hz and 50MHz, we used the following instruments and materials: Hewlett Packard 8110A 150MHz Pulse Generator, Oscilloscope Tektronix TDS 754C 500MHz and three RG58C/U cables assembled with SMA connectors. To develop the ac test between 50MHz and 2Hz on the 4-channel optical link based on the Mitel VASEL array 4D469 and the Mitel PIN array 4D470 we used the following instruments, HP 8133A 3GHzpulse generator and Tektronix TDS794D 2GHz oscilloscope.

The dc test on the PIN photodiode is based on characterizing each single PIN or each PIN in the array to get their responsivity (R, units A/W). This consists of generating ten different levels of optical power by means of one VCSEL, then measuring it with the optical power meter (PHOTODYNE 2275XQ) as a reference. We then measure the current generated at each value by the PIN photodiode. With this procedure we got the responsivity for all the PIN photodiodes. The dc test on the single VCSEL consisted of measuring the variations in its optical power as a function of its forward current and its forward voltage. We changed the forward current from 2mA to 28mA in steps of 2mA. Also, we tested using two different fiber optic cables to check the variation that results. With this test we measured the optical power delivered by the single VCSELs as a function of forward current (Fig. 6), and the VCSELs' resistance as a function of forward current (Fig. 7a). The dc test on the VCSELs in the array consisted of taking variations of optical power for changes in the forward current ranging from 1mA to 10mA in steps of 1mA, because the VCSELs in the array are dc current limited to 10mA.

The ac test on the single links consisted of measuring the jitter, rise time, fall time and the optical response without previous biasing. The test was done using the following test setup: One output channel from the pulse generator was connected in series with a 30 ohm resistor. This resistor was connected in series with the VCSEL's anode and the VCSEL's cathode was connected to ground. Also, the single VCSEL was connected with the fiber optic and the fiber optic was connected to the single PIN photodiode. The PIN's cathode was connected to ground and the PIN's anode was connected in series with a 30 ohm resistor, the other leg of which was connected directly to the oscilloscope. The oscilloscope was set to 50 ohms input. The pulse generator drove the VCSEL directly while we took all the measurements with the oscilloscope. Note that we found that we did not need to bias any of the single PIN photodiodes to do the tests. The ac test on the 4-channel array consisted of measuring the jitter, rise time, fall time, cut frequency and the optical power response without previous biasing. The test was done connecting each VCSEL in the array exactly as we did for the single VCSELs (same resistor in series, etc.). Also, each PIN photodiode in the

array was connected exactly like the single PIN photodiode. The pulse generator drove the VCSEL directly while we took all the measurements with the oscilloscope. As with the single PIN photodiodes, we found that we did not need to bias any of the PIN photodiodes in the array to do the tests. To get the cut frequency we measured the voltage peak-peak at low frequencies and then looked for the frequency at which the voltage peak-peak was three dB lower than this. The test setup used to do the measurements on the link array between 0Hz and 50MHz is shown as Fig. 4.

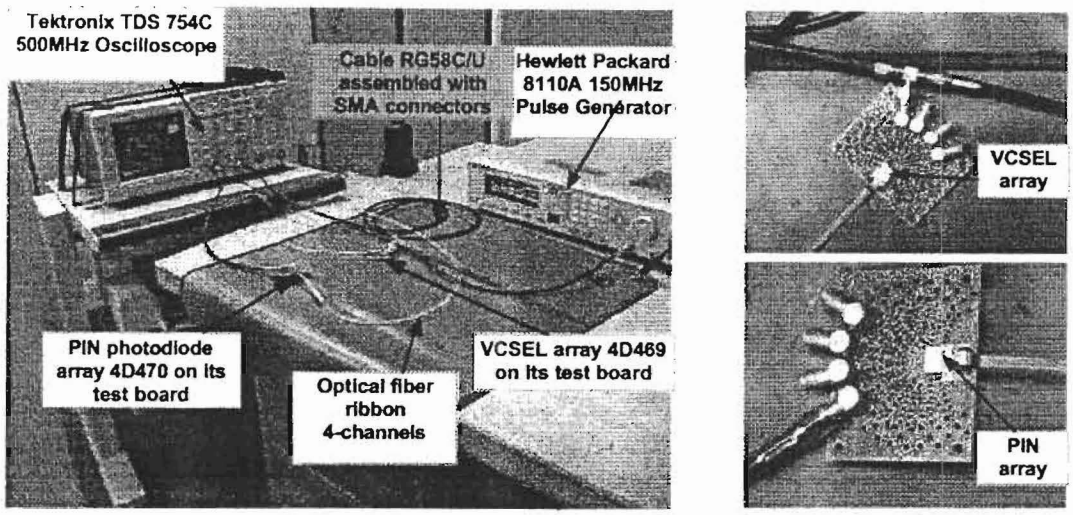
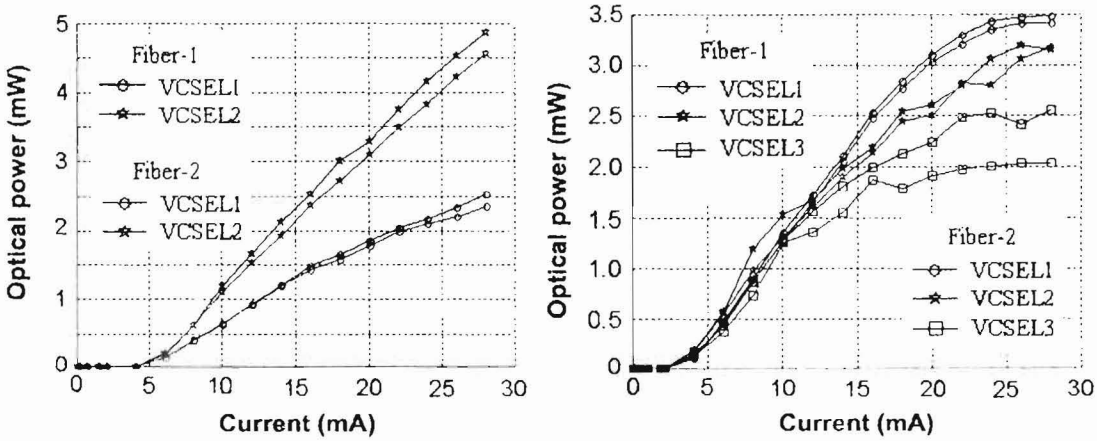


Figure 4: AC Test setup to get the VCSEL array performance to middle frequencies.

3. RESULTS

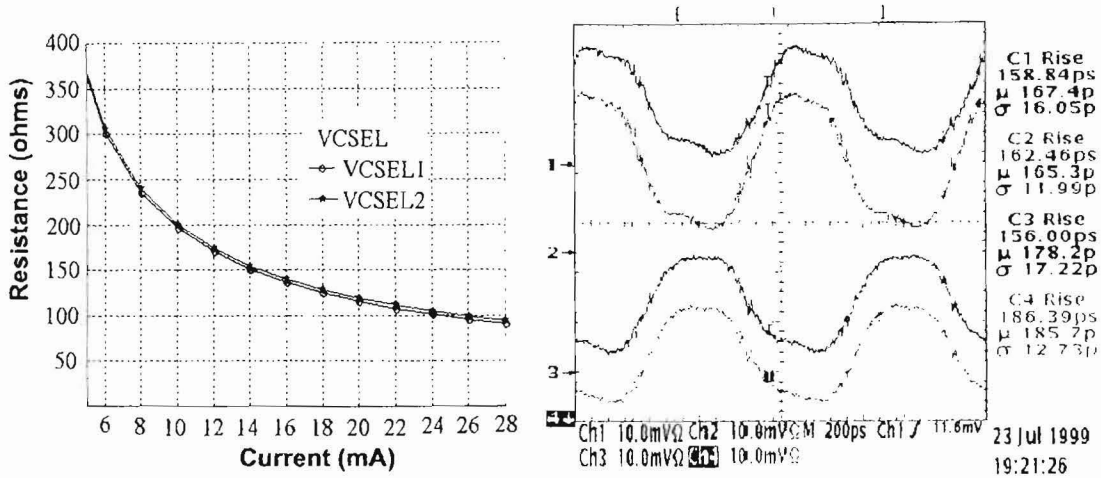
The results for the dc test on the Mitel single VCSEL are shown as Fig. 5a and the results for the Honeywell single VCSEL are shown as Fig. 5b. The VCSELs in the array demonstrate the same characteristic curve of optical power versus forward current as the Mitel single VCSEL2 shown in Fig. 5a. However, the VCSELs in the array support a maximum forward current of 10mA (dc) and 18mA (ac).



a) b)

Figure 5. Optical power as function of forward current, a)Mitel VCSELs and b)Honeywell VCSELs

The resistance for the single VCSELs as a function of forward current is shown as Fig. 6a for Mitel VCSELs. The resistance for the Honeywell VCSELs is also a hyperbolic curve that decreases from 355 ohms at 5mA to 195 ohms at 10mA. Similarly, the resistance for the VCSELs in the array is a hyperbolic curve that decreases from 380 ohms at 5mA to 210 ohms at 10mA.



a) b)

Figure 7. a) Resistance Mitel single VCSELs and b) Signals delivered from the link array at 1GHz.

The jitter peak-peak for the single links between Mitel single VCSEL and Mitel single PIN photodiode was about 180ps. This includes a jitter peak-peak of 115ps measured at the output of the pulse generator. The jitter peak-peak for the single links between Honeywell single VCSEL and the single PIN photodiode was of about 185ps. This was measured having a jitter of 116ps at the output of the pulse generator. The rise time measured for the links between the Mitel single VCSELs and the Mitel single PIN photodiodes was approximately 1.5ns and the fall time was 1.6ns. The link between the Honeywell single VCSEL and the single PIN photodiode has the same rise time, 1.5ns. Its fall time was 1.7ns. In these cases the rise and fall times were limited by the test setup. The optical response for all the single links is as follows. The bits arrive at turn on with only 60% of the maximum amplitude. The amplitude grows with time and takes about $1.5\ s$ to stabilize at maximum amplitude. This problem can be alleviated by previously biasing the VCSEL at or near its current threshold.

The jitter peak-peak for the all the channels in the link array between Mitel VCSEL array and Mitel PIN photodiode array was about 50ps including a jitter peak-peak of 40ps at the output of the pulse generator. The rise time measured for all the channels in the link array was about 160ps (See Fig. 7b), and the fall time was about 250ps. The cut frequency was 1.18GHz; this means a maximum bit rate of 2Gbps. The optical response for all the channels in the link array was as follows: The bits arrive at turn on with 20% of the maximum amplitude. The amplitude grows with time and takes about 200ns to become stable at maximum amplitude. Again, this problem can be removed by previously biasing the VCSEL at or near its current threshold.

4. REFERENCES

1. S. Stone, *The BTeV programm at Fermilab*, BTeV pub. note, Fermilab, July 1998.
2. P. Denes, personal communication, (1998).
3. M. Johnson, personal communication, (1998).

Fiber Optic based readout for BTeV's Pixel Detector

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Guilherme Cardoso*, Aurora Vargas**, Jeff Andresen*
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Abstract

The current paper describes the design of Fiber Optics Links for BTeV's Pixel Detector readout. BTeV pixel detectors chips will be located as close as 6mm from the accelerator's beam into the vacuum pipe. The readout electronics will be located at about 6cm from the beam, imposing strong constrains regarding radiation, mass, power dissipation, and size. The current development is the first prototype designed to initialize, control and readout pixel detector chips using optical links. Results of link performance are shown. The current development is designed in two boards, which will become the major parts of a test stand for pixel detector bench and beam tests.

I. INTRODUCTION

BTeV's pixel detector consists of 31 double-plane stations of about 100 cm² of active detection area. These planes are perpendicular to the direction of the beam. The beam passes through the center of each plane formed by two halves. One of the half planes is shown in Figure 1. Since BTeV will use the pixel detector as part of the lowest level trigger system, one of the most important requirements is hit readout speed [1]. The primary goal is to achieve a data transfer rate capable of handling the hit rate generated by Fermilab's Tevatron beam with a luminosity of $2 * 10^{32}$ p/cm² and a bunch crossing (BCO) time of 132 ns. Furthermore, the required readout bandwidth must be achieved while keeping a small power and mass budget. In particular, mass is very critical for the Pixel Detector, the most inner part of BTeV's detector where multiple scattering must be minimized.

A fiber optic based design, as proposed in this paper, is the technology that best adapts to BTeV's requirements. Every pixel plane will generate up to 16 Gb/s of data. The pixel amplifier and discriminator chips, located underneath the pixel detectors will store that information. However, since the pixel detector is the primary component of BTeV's trigger, the data must be readout as soon as possible. A multi chip module (MCM) design is being proposed for the pixel detector electronics as shown in Figure 1. Every module is autonomous. It groups a certain number of Pixel amplifier/discriminator chips and the readout electronics to transfer the data from the pixel planes to the trigger processor and DAQ. Furthermore, every module must allow for an incoming link to receive commands to initialize and control the pixel devices and provide them with timing information (i.e. clocks). A second approach under consideration moves the Pixel Detector Fiber Optic components 25 cm away of the MCMs. The advantage here is that the optoelectronics, and specially, the serializers and decoder chips receive much less radiation. Furthermore, it decreases the amount of mass in the active region.

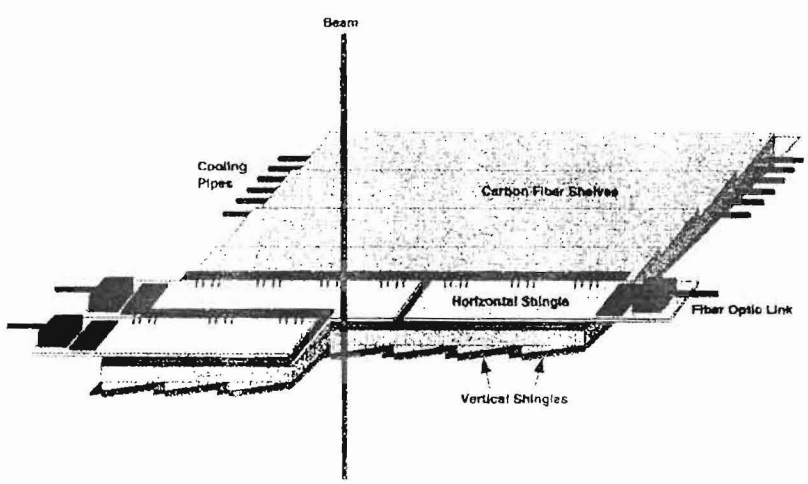


Figure 1: BTeV's Pixel Detector Plane

II. THE CONTROL AND READOUT OPTICAL LINK PROTOTYPE

A Control and Readout Optical Link prototype has been designed with the following purpose:

- Test optical transmission and reception issues such as dynamic range, noise, biasing, bandwidth, optical power, etc.
- Test the bi-phase mark encoded signal concept for the FPIX pixel chip [2] initialization and control link.
- To provide a good step toward the system integration of BteV Pixel Detector's.

The Optical Link Control and Readout prototype is organized in such a way that builds up a test stand for Pixel Detector Modules. Figure 2 shows a block diagram of the system.

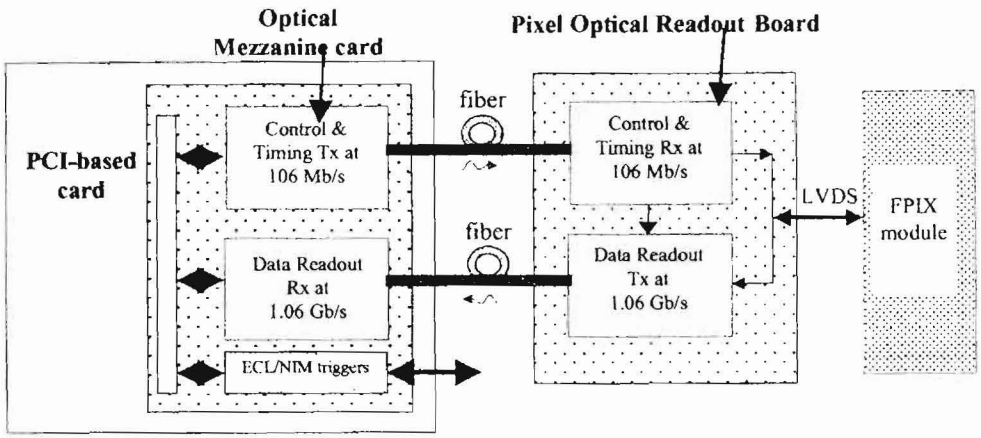


Figure 2: Two board Control and Readout Optical Link prototype

III. THE CONTROL OPTICAL LINK

The Control Optical Link carries initialization, control and timing information for the Pixel chips. The encoding used for this link is of bi-phase mark type. A 53 MHz clock modulates the initialization and control data in order to reduce the total number of fibers and provide an electrically balanced transmission. The bi-phase mark encoding guarantees at least one transition per bit reducing synchronization problems at the receiving end. As shown in Figure 3, the receiver uses a Phase Lock Loop (PLL) to recover the clock and data. The PLL must serve the double function of recovering the clock and reducing the jitter. The Command interpreter decodes the serial information. Commands are of two different types, the ones used to initialize pixel cell and chip parameters and others to control or reset the FPIX chip in running mode. The commands are decode by the Command Interpreter and sent to the MCM as LVDS signals.

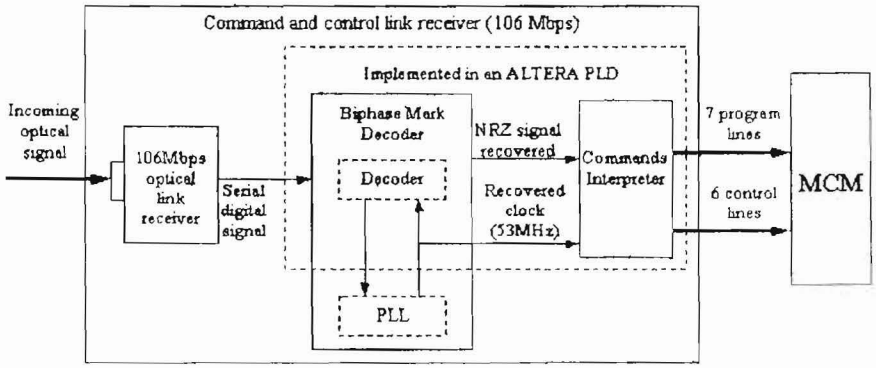


Figure 3: Control & Timing Receiver block diagram

The Control link receiver utilizes a Mitel 1A354 PIN photodiode operated in photovoltaic mode, connected to a high speed amplifier and discriminator as shown in Figure 4. The peek optical power in the fiber is 1mW. The PIN output signal is about 90mV and the output of the amplifier is 370 mV. Figure 5 shows scope images of the optical eye pattern and the bi-phase mark signal decodification at the receiving end. The amplifier used is high bandwidth allowing for a rise and fall time of about 1.5 ns. The PIN's response is very linear up to at least 1.5 mW.

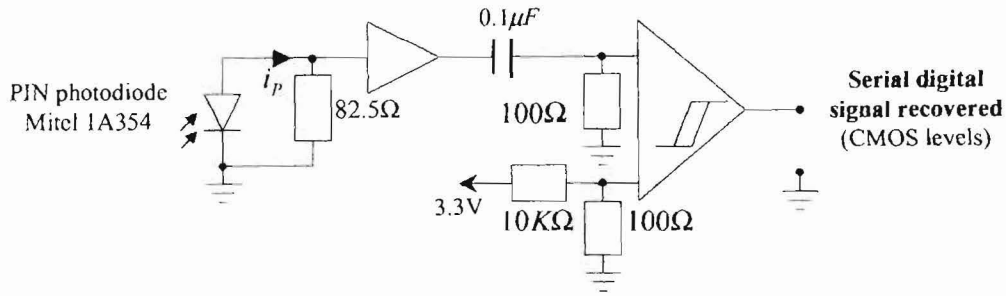


Figure 4: PIN, amplifier and discriminator

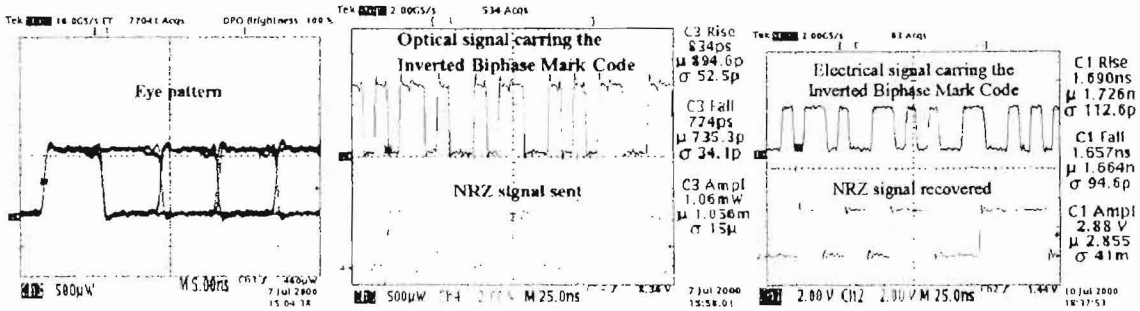


Figure 5: 53 MHz link signals: a) Eye pattern, b) NRZ-bi phase sent, c) NRZ-bi phase received

A strong constraint on the recovered clock is jitter, because the clock is used to readout pixels and to clock the Gigabit serializer. Gigabit serializers multiply the input clock frequency by 20 but they are unable to reject jitter. A small jitter may represent a big percentage of the output data's period, increasing the bit error rate in the channel. As it can be appreciated in Figure 6a, the jitter of the recovered clock in the present board is very low, about 64 ps peek-to-peek. The bit error rate of the channel has been measured to be better than 10^{-14}. Figure 6b shows the signal rise and fall time of the clock to be around 1.05ns.

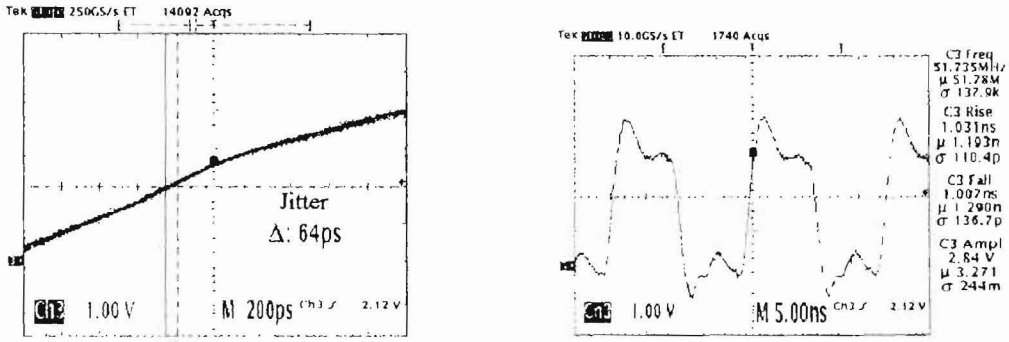


Figure 6: a) Clock's jitter, b) Clock's rise and fall time

IV. THE READOUT OPTICAL LINK

The readout electronic serializes the data from the 5-chip Pixel Module into a G-Link based serial link operating at 1.06 Gb/s. In the final design the G-Link will be replaced by a radiation hardened serializer [3]. Alternative approaches are also being analyzed to relocate the optoelectronics. Extending the LVDS signals from the FPIX module to about 25 cm will allow us to place the optoelectronics outside the high radiation area. Performance of the G-Link has already been reported in [4].

V. INTEGRATION OF THE OPTICAL LINKS TO THE READOUT OF A PIXEL MODULE

As shown in Figure 2 the optical links will be used to initialize and deliver commands and clocks to the Pixel chips as well as to readout the pixel data. BTeV Pixel Detector chip characterization has been extensively carried out at Fermilab and is reported elsewhere [5][6]. However, the optical links were integrated with the existing pixel assemblies. Several comparison tests were run using a single FPIX chip and a MCM with 5 pixel devices. Figure 7 shows the current setup.

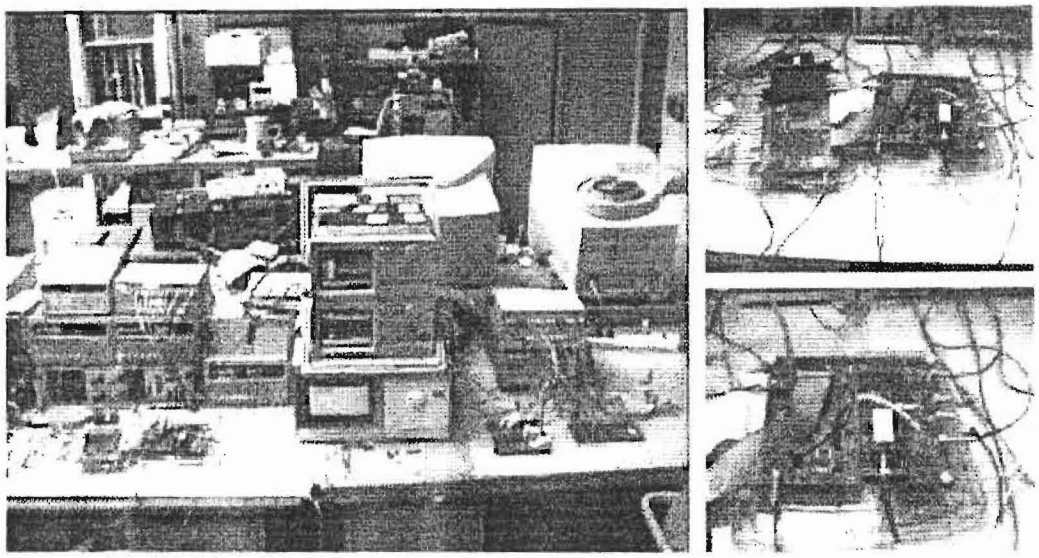
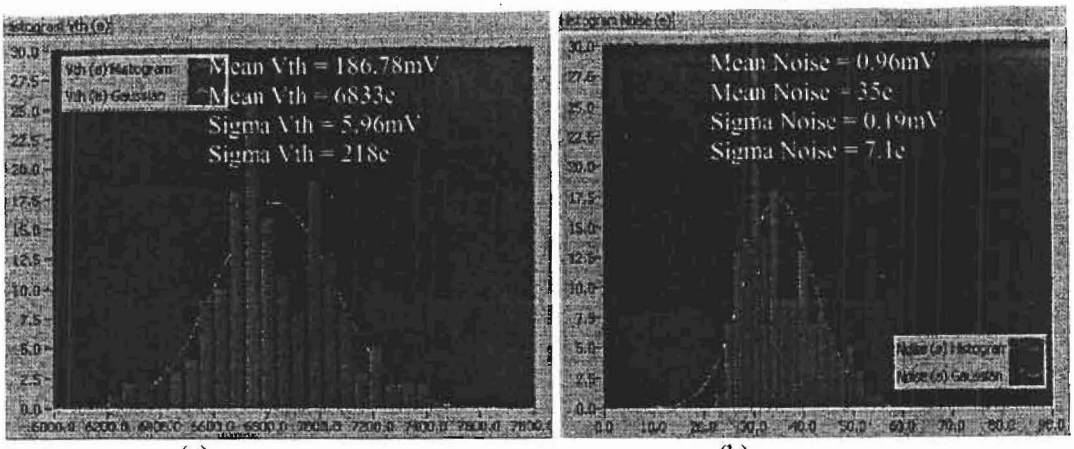


Figure 7 Control and Readout Optical Link prototype setup

Table 1 compares mean and sigma of noise and threshold of a five-chip FPIX module using two different setups. In the first experiment, the MCM was controlled by a probe station and the data was stored directly into a logic state analyzer. The FPIX initialization patterns were generated by a pattern generator, whose outputs were directly connected to the MCM inputs. In the second case, the initialization and control data is provided through the Control Optical Link at 52MHz and the data is readout through the 1.06 Gb/s optical link. Figures 8 and 9 show the comparative histograms of noise and threshold for both tests.

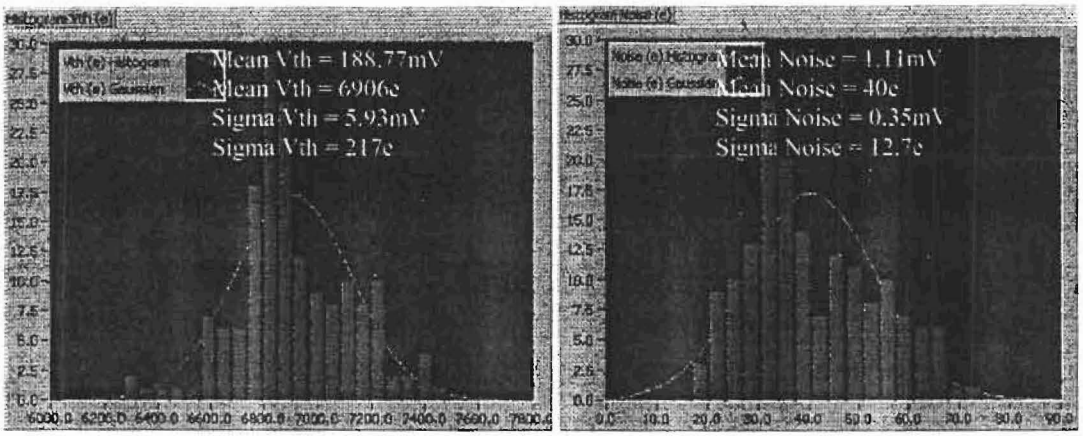
Vth0 = 1.95V	Results of the characterization of the MCM without Optical Link				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6833	6657	6581	6792	6956
Sigma threshold (e-)	218	239	217	168	146
Mean noise (e-)	35	37	37	31	31
Sigma noise (e-)	7.1	8.1	9.0	5.9	6.2
Vth0 = 1.95V	Results of the characterization of the MCM with Optical Link				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6906	6886	6820	6910	7051
Sigma threshold (e-)	217	184	179	142	161
Mean noise (e-)	40	37	38	32	30
Sigma noise (e-)	12.7	13.5	12.9	9.6	9.6

Table 1 MCM characterization comparison



(a) (b)

Figure 8: Five FPIX1 MCM without using the optical links. a) Threshold distribution and b) Noise Distribution.



(a) (b)

Figure 9: Five FPIX1 MCM using the optical links. a) Threshold distribution and b) Noise Distribution.

VI. CONCLUSIONS

A 5 chip FPIX1 Pixel Detector Multichip Module has been integrated to be controlled and readout through fiber optics. The first prototypes have proved to have an excellent performance. The readout clock has been recovered from the bi-phase signal with only 65 ps of jitter. This noise is acceptable for clocking a high-speed serializer at 1.06 Gb/s. The BER of the 106 MB/s link is better than 10^{-14}. EMI and radiation tests will define the location of BTeV's optoelectronics.

REFERENCES

[1] BTeV: An Expression of Interest for a Heavy Quark Program at C0, BTeV collaboration, Fermilab, May 18, 1997.

[2] ", G. Cancelo, D. Christian, S. Zimmermann, J. Hoff, A. Mekkaoui, R. Yarema, "Development of a pixel readout chip for BTeVNuclear Instruments & Methods in Physics Reasearch A 435 (1999) pp144-152.

[3] P. Denes, "Radiation hard gigabit systems", Proceedings of the 2nd Workshop on Optical Readout Technologies for ATLAS, Oxford, Jan. 1999.

[4] M.Pearce et al, Development of Radiation Tolerant Gb/s Optical Links for the Front-end Read-out of the ATLAS Liquid Argeon Calorimeter, Proceedings of Fourth Workshop on Electronics for LHC Experiments September 1998.

[5] G.Cancelo, G.Cardoso, S.Sihanguir, D.Christian, R.Downing, J.Hoff, A.Mekkaoui, A.Vargas, R.Yarema, S.Zimmermann. "Development of high data readout rate pixel module and detector hibriditization at Fermilab", Proceedings of PIXEL2000, Genoa, Italy, June 5-8 2000.

[6] M.A.Vargas, M.Sheaff, S.Vergara, The Development of Software to Characterize the Fermilab Pixel Readout chip FPIX1 for the BTeV experiment. Submitted to Niclear Instruments and Methodes, Aug. 2000.

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
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13 December 2000

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Re: TITLE: **Optical readout and control interface for the BTeV pixel vertex detector**
AUTHOR: S. Vergara, *et al.*
REG. No.: KNO-00-637

Dear Dr. Vergara:

A review of your manuscript has been carried out and some significant points have been raised in the process (enclosed). I would ask that you address them by making appropriate changes and/or additions to the manuscript and submitting your revised manuscript (with figures) in triplicate, together with one extra set of good quality figures, and (if possible) a revised electronic disk to this office.

Please again submit all copies in double-line-spaced format, per NIM/A's *Instructions to Authors*.

It would expedite the processing if you would also indicate the changes that have been made on the **enclosed** Copy 2 (the reviewer kept his copy) of your manuscript, and return it along with the revised versions.

Once these points have been resolved, we will proceed with the processing of your manuscript.

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Review: **Optical Readout and Control Interface for the BTeV Pixel Vertex Detector**
Author: S. Vergara, *et al.*
Reg. No. KNO-00-637

Suggested grammatical changes:

Where acronyms are used, I would define or cite defining references the first time they are used in the paper. Specifically, FPIX, PIN and VCSEL should all be defined/reference on page 2.

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The acronym for the ORCI is not consistently defined, the first definition is made on page 2, a second definition as ORCIB is made on page 6.

Page 4, 1st. paragraph, 4th. line: "corresponding command and control line" to "corresponding command or control line."

Page 5, 2nd. paragraph: "The PLL uses a voltage controlled crystal oscillator (VCXO) to generate a 52 MHz clock signal and a phase and frequency detector that it is implemented in the FPGA." to "The PLL uses a voltage controlled crystal oscillator (VCXO) to generate a 52 MHz clock signal and phase and frequency detectors, which are implemented in the FPGA."

Page 7, 1st. paragraph, 2nd. line: "no more than 500ps and a jitter peak to peak of 100ps." to "no more than 500ps and a maximum peak-to-peak jitter of 100ps."

Page 7, 1st. paragraph, 8th, 10th. lines and other instances: "peak to peak" to "peak-to-peak"

Page 11, last line: "distribution of the same FPIX1 chip using" to "distribution of the same FPIX1 chips using"

Page 12, 2nd. paragraph, 3rd. line: "renge" to "range"

Concept suggestions:

The estimate of 100 Krad/year radiation damage at a radius of ~7cm seems to be too low. Please double-check this value before publishing.

Those familiar with the operation of Fermilab's Tevatron will know the fundamental operating frequency is ~53.1MHz. It would be interesting to know why the system was not tested at integrals of this frequency.

The statement in the summary that the 104 Mbps optical link provides accurate transmission over a wide range of optical power is not supported by evidence presented in the paper. The paper presents evidence that the range of optical power was reduced by driving the VCSELs with voltage rather than current.

Technical suggestions

One aspect of optical data transmission that isn't included in the paper is the wavelength the two systems are being operated at. Others considering similar applications would appreciate this information.

The oscilloscope plots that shown for jitter measurements also show the oscilloscope trigger indication. Measuring jitter on the trace that the oscilloscope is triggering on, I is not truly measuring the jitter of the signal, but more so the jitter in the oscilloscope triggering system. For instance, in figure 12a, the jitter on subsequent edges seems to be greater than the jitter on the leading edge of the framing bit (presumably the oscilloscope trigger). Yet the paper publishes the jitter on the "best" edge. A jitter measurement should be made using an independent (non-

measured) trigger for the oscilloscope, then delaying (if necessary) to the edge of interest to measure the jitter. If this was done for the jitter measurements, a diagram indicating the test setup (including oscilloscope trigger)would help clarify this. If the jitter measurements were made on the oscilloscope trigger trace, references to these measurements shouldn't be included in paper

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Optical Readout and Control Interface for the BTeV Pixel Vertex Detector.*

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Abstract

Optical links will be used for sending data back and forth from the counting room to the detector in the data acquisition systems for future high energy physics experiments, including ATLAS and CMS in the LHC at CERN (Switzerland) and BTeV at Fermilab (USA). This is because they can be ultra-high speed and are relatively immune to electro-magnetic interference (EMI). The baseline design for the BTeV Pixel Vertex Detector includes two types of optical link, one to control and monitor and the other to read out the hit data from the multi-chip modules on each half-plane of the detector. The design and performance of the first prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector is described.

1. Introduction

The goals of the BTeV experiment are to measure mixing, CP violation, and rare decays in charm and beauty particle decays at the Fermilab collider. The pixel vertex detector is crucial for achieving these goals. This is a multi-plane pixel device that sits inside the beam pipe. It is composed of 124 pixel half-planes of approximately 5x10cm each, divided in 31 double-stations perpendicular to the colliding beam and installed a few millimeters from the beam. Each half-plane is comprised of several multi-chip modules (MCMs). The detector will be employed for on-line track finding for the lowest level trigger. This means that the pixel readout chips bump-bonded to the sensors will have to read out all detected hits and input them to the trigger processors. To achieve the high bandwidth required for the readout, ultra-high-speed digital optical links of 1-2 Gbps will be employed on each detector half-plane. A second type of digital optical link, which will send the command and control signals to the FPIX chips from the counting room to each detector half-plane, can operate at lower speed (~100 Mbps). Both the emitters of the ultra-high-speed optical links and the receivers of the lower speed optical links will be about 7 cm from the beam if they are mounted on the detector planes as proposed in the baseline design. In this case, these devices will receive about 100 Krad of radiation per year of running and will suffer some radiation damage. A further, rather stringent requirement is that they must operate inside the beam pipe in vacuum at $\approx -5^{o}C$ [1]. Other solutions, which place the optical circuits outside of the vacuum vessel about 25 cm from the detector, are also being studied.

The design and performance of the first prototype of the Optical Readout and Control Interface (ORCI) designed and built at Fermilab is detailed in this article. Features of note are the decision to operate PIN photodiodes in photovoltaic mode and the decision to drive VCSELs with voltage

* *Work supported by the U.S. Department of Energy under contract No. DE-AC02-76CH03000.*

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rather than current. The reasons for these choices are given in Sections 2.2 and 3, respectively. While not all components included in the present design are radiation hard, a completely radiation hard version is envisioned for the future.

2. First Prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector

The first prototype of the ORCI for the BTeV pixel vertex detector contains two optical links. The first one operates at 104 Mbps and transmits commands to program and control the FPIX readout chips [2] contained on one multi-chip module (MCM) from the counting room to the detector. The second one operates at 1.04 Gbps and reads out all the detector hit data from the MCM and sends it to the counting room. A block diagram of the system is shown in Figure 1.

The MCM is an array of pixel readout chips (FPIX) mounted on a single sensor and connected in daisy chain using a flexible interconnect circuit [3]. The FPIX chips contain the front-end electronic cells and column-based readout circuitry for the pixel sensors. In order to achieve the needed resolution for tracking and vertexing, the pixel unit cell is very small, 50 microns by 400 microns in size. The FPIX chips contain cells of the same size, which will be bump-bonded to the sensors. The control and readout protocol of the current version of the FPIX chips, called FPIX1, requires that there be 13 control inputs to the MCM, 7 command lines to program the chips and 6 command lines to control the readout. It also contains 17 data output lines for readout of the hit information provided by the detector. We expect that the control and readout protocols of more advanced versions of the FPIX readout chips will be different.

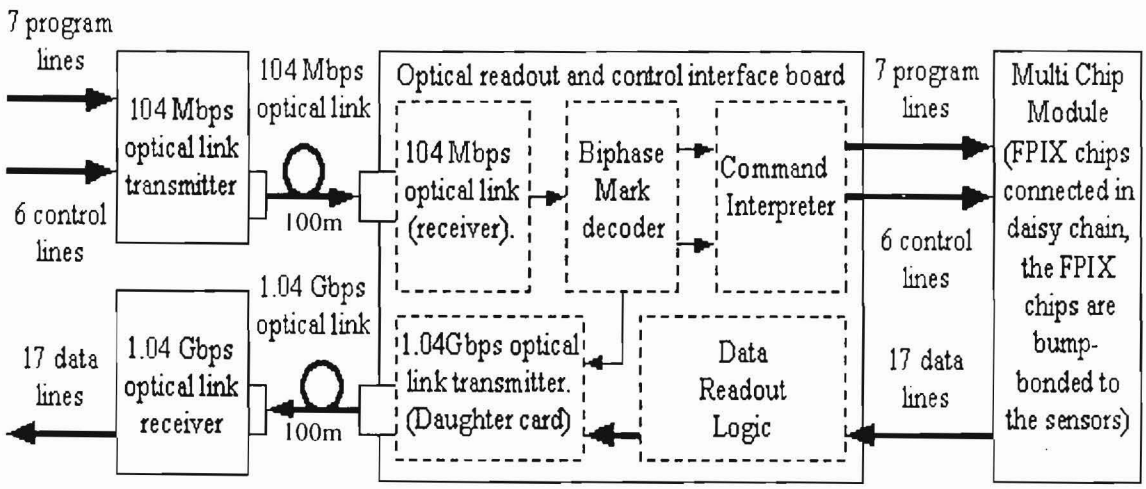


Figure 1: Block diagram of the first prototype of the ORCI for the BTeV pixel detector.

2.1 The command and control link transmitter

Figure 2 contains a block diagram showing the components of the 104 Mbps optical link transmitter, which receives the program and control lines from the data acquisition system and encodes the information into a 7-bit protocol. The first bit is always one to indicate the beginning of the data frame. The next five bits provide the unique identifier for the command and control line being sent. The seventh bit is the data (high or low) to be sent to the corresponding command and control line. The signal produced by the 7-bit protocol generator is non-return to zero (NRZ). In order to send both the NRZ signal and the clock in a single data stream they are converted to bi-phase mark code. The protocol generator and the bi-phase mark encoder are implemented in a Field Programmable Gate Array (FPGA). The 104 Mbps transmitter uses a VCSEL driver to

modulate the signal supplied to a Mitel 1A444 VCSEL. The VCSEL translates the bi-phase signal into an optical signal.

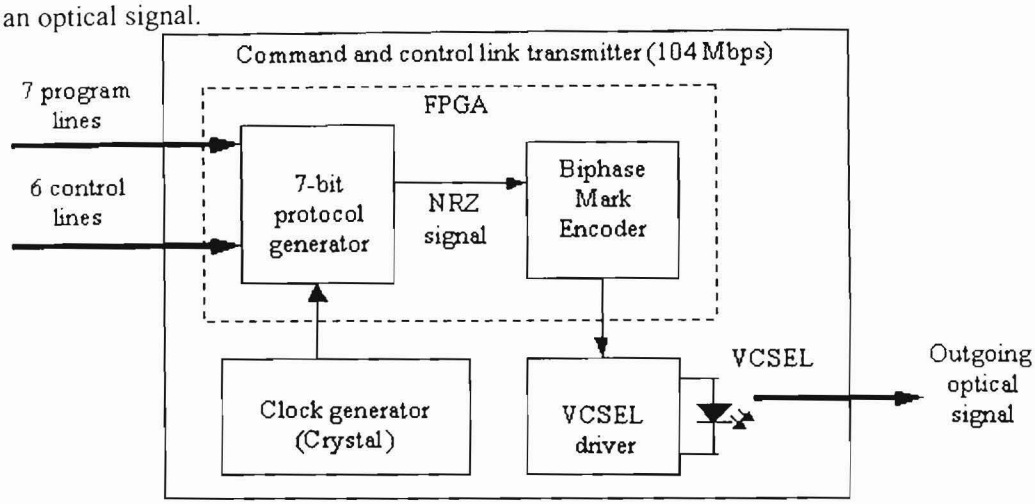


Figure 2: Block diagram of the 104 Mbps optical link transmitter.

2.2 The command and control link receiver

Figure 3 contains a block diagram of the command and control link receiver. The recovered signal must pass through a bi-phase mark decoder to separate the command signal and the clock signal. Following this, the command signal passes through an interpreter that identifies the data received and the corresponding command line. These functions have been implemented in an FPGA. Finally, the data are sent on the correct command line to the MCM.

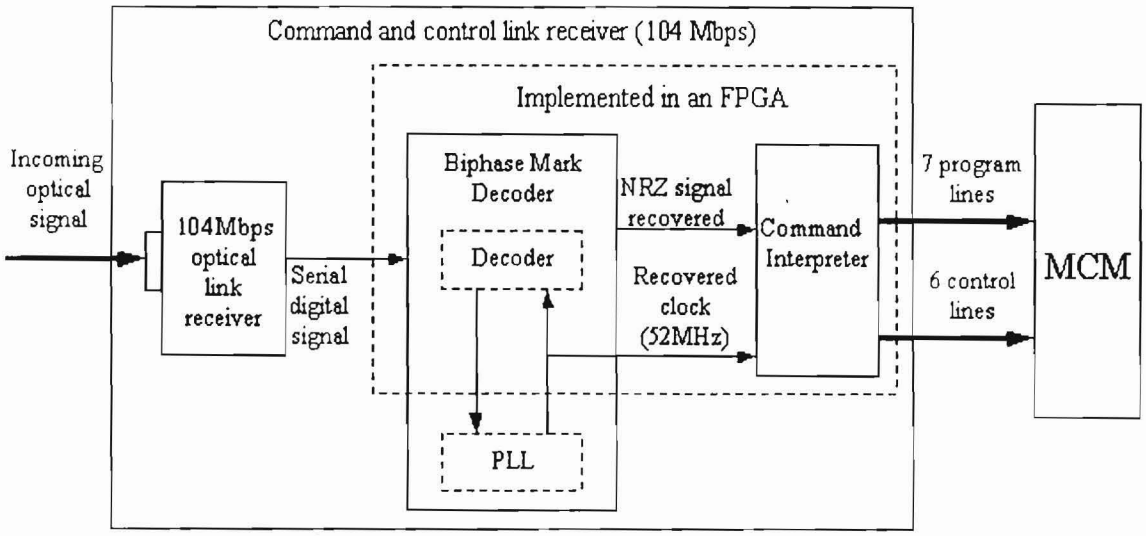


Figure 3: Block diagram of the command and control receiver section of the Optical Readout and Control Interface Board.

The 104 Mbps optical link receiver utilizes a Mitel 1A354 PIN photodiode or a Lasermate RST-M85A306 PIN photodiode operated in photovoltaic mode. This is connected to an amplifier; the output of the amplifier is connected to a discriminator that recovers the digital signal as shown in Figure 4. The discriminator has a threshold of 33mV, which is well above the noise level but still low enough to ensure that all data bits are received.

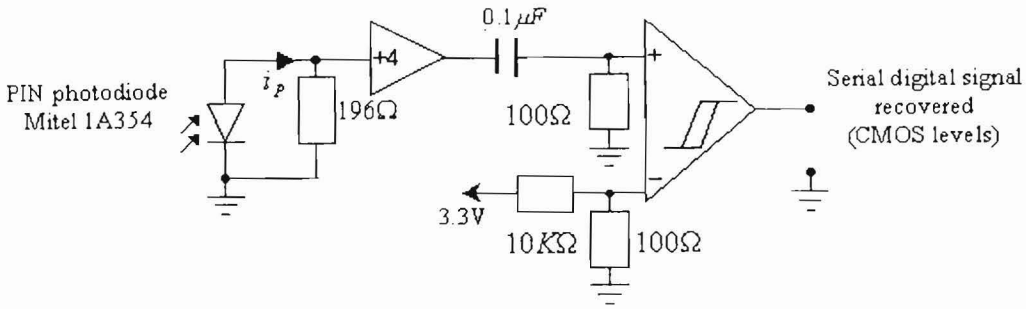


Figure 4: 104 Mbps optical link receiver.

The 104 Mbps optical link receiver is an inherently low noise circuit, because the PIN photodiode is being used in photovoltaic mode [4]. Since modern PIN photodiodes are fast enough to operate without a bias voltage being applied, both the dark current and the noise produced by a power supply used to do the biasing can be avoided. In the absence of an applied electric field, charge motion is caused only by the small electric field produced by the electron-hole pairs generated in the depletion region of the PIN photodiode [5]. Also, the depletion region is limited in size by the properties of the device, since there is no reverse bias voltage applied which would increase its size. We believe that this will reduce the impact of Single Event Upset (SEU) due to strong interactions in the PIN photodiodes and plan to carry out tests to demonstrate this in the near future.

The bi-phase mark decoder uses a 104 MHz square signal to separate the clock signal from the command signal. A phase-locked loop (PLL) is used to keep the receiver circuit synchronized with the incoming optical signal. The PLL uses a voltage controlled crystal oscillator (VCXO) to generate a 52 MHz clock signal and a phase and frequency detector that it is implemented in the FPGA. We synchronize the signal recovered with a 26 MHz square signal to get the best performance from the PLL.

2.3 The readout optical link transmitter

The data acquisition system sends the request to the MCM to read out the hit data using the 6 readout control lines. These are sent and received by means of the 104 Mbps optical link described above. The 17 data lines which output the hit data from the MCM are input to the FPGA, which delivers 16 of these data bits in parallel to the 1.04 Gbps optical link transmitter along with the corresponding 52 MHz clock, as shown in Figure 5. The 17th bit, data valid, is transmitted and received as one of the four G-link control bits.

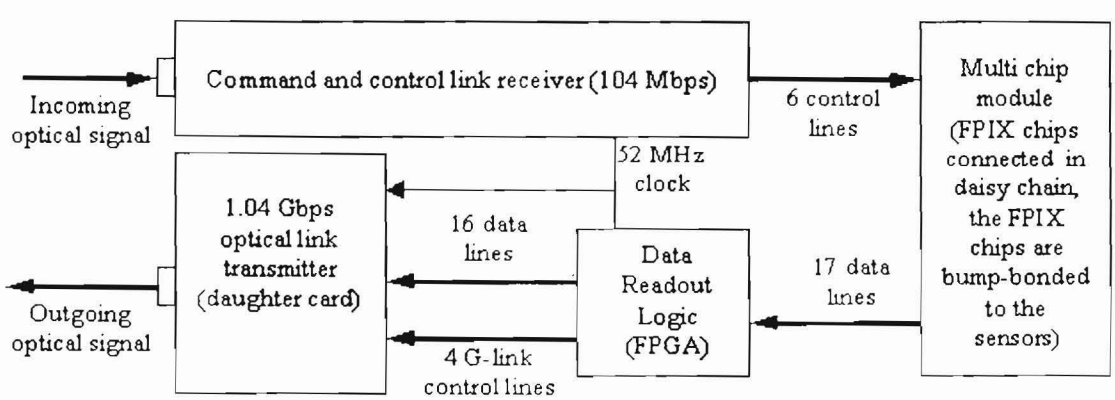


Figure 5: Block diagram of the circuit used to read out all the data generated by the detectors on the MCM.

The use of the data readout logic to input the data to the optical transmitter provides the possibility of checking out all the commands that are sent to the MCM. When we are transmitting commands to program the FPIX chips on the MCM, we need only to reroute the information in the control words to the FPGA and input them to the 1.04 Gbps optical link transmitter instead of the hit data generated in the MCM.

The 1.04 Gbps transmitter has been placed on a daughter card to allow the use of two versions of the 1.04 Gbps optical link transmitter. The first version, which is not radiation hard, is based on the HDMP-1032 G-Link transmitter [6], low power version, and the optoelectronic Finisar module FTM-8510 (See Figure 6.). The second option will be radiation hard. It will be built using a custom VLSI serializer in CHFET process [7]. Since this serializer includes a VCSEL driver, the serializer can be connected directly to the VCSEL as shown in Figure 7. Both the G-link transmitter and the CHFET serializer encode the information using the Conditional Invert Master Transition (CIMT) protocol [6]. Because the serializer is compatible with the HDMP-10X2 G-Link transmitter series, the daughter boards are interchangeable and both are fully compatible with the rest of the system. Thus, either daughter card can be used on the Optical Readout and Control Interface Board (ORCIB) without having to make any other changes. The function of the daughter card is to translate the parallel frame at 52MHz into a serial frame at 1.04 Gbps to send the MCM information to the counting room.

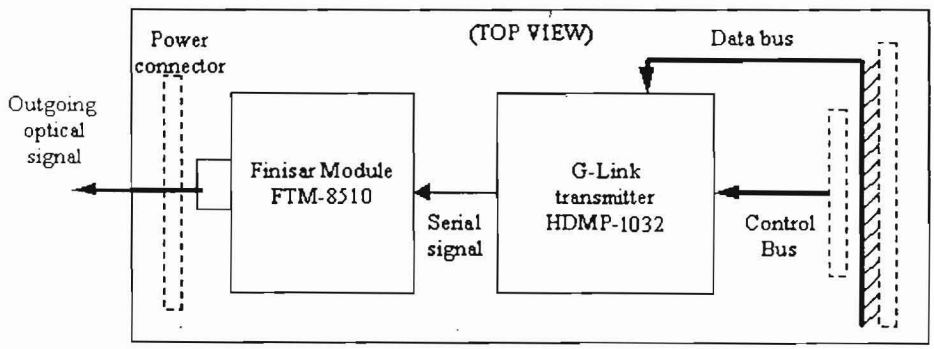


Figure 6: Block diagram of the Daughter board based on the G-link transmitter HDMP-1032.

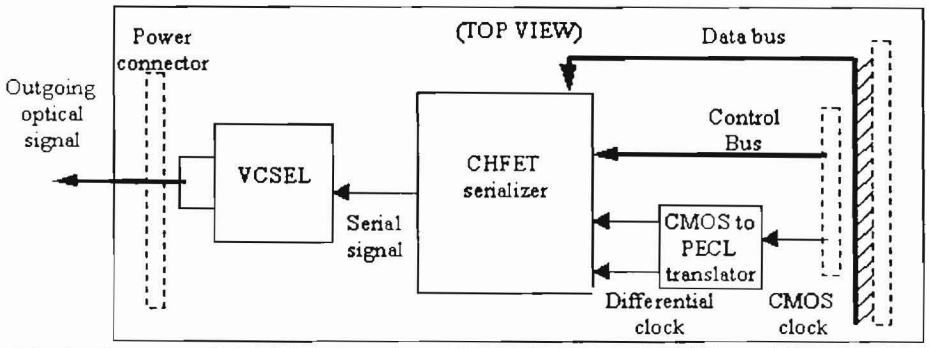


Figure 7: Block diagram of the Daughter board based on the CHFET serializer and a HFE4080 Honeywell VCSEL.

Tests of a preliminary version of the CHFET serializer show that it needs a differential clock signal with rise and fall times no more than 500ps and a jitter peak to peak of 100ps. This places rather stringent timing requirements on the bi-phase mark decoder, which supplies the clock signal to the daughter cards. On the CHFET serializer daughter card, we translate the CMOS

clock signal coming from the mother board into a differential PECL signal and provide it to the CHFET serializer. The translator delivers a PECL clock signal with 350 ps rise and fall times. The daughter card with the HDMP-1032 G-link transmitter needs a clock signal with less than 250 ps jitter peak to peak and less than 1.5 ns rise and fall time. Thus, the clock signal supplied by the mother board to the daughter cards must have less than 100 ps jitter peak to peak and less than 1.5 ns rise and fall time to work with either of the daughter cards.

2.4 The readout optical link receiver

The 1.04 Gbps optical link receiver uses a Finisar module FRM 8510, which translates the optical signal at 1.04 Gbps into an electrical signal. This electrical signal is supplied to an HDMP-1034 G-Link receiver, low power version. The chip translates the serial frames into parallel frames, recovers the 52 MHz clock, and synchronizes the recovered clock with the 52 MHz local clock as shown in Figure 8.

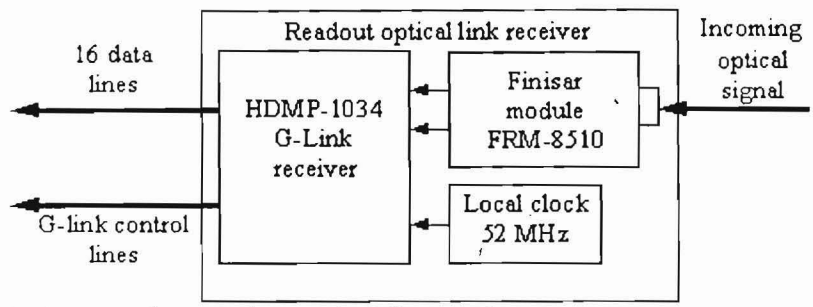


Figure 8: Block diagram of the readout optical link receiver.

3. Performance of the first prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector

The VCSEL driver in the 104 Mbps optical link transmitter was designed to produce a minimum variation in optical power between different Mitel 1A444 VCSELs. Our measurements have shown that if we drive the VCSEL with current we get up to 80% optical power variation among the VCSELs under test. When we drive the VCSELs with voltage, we get a maximum variation of only 25%. This difference provides an important safety margin, especially when designing a driver for use in a high radiation environment where performance may be degraded progressively by radiation damage. In Figure 9 we show the optical power as a function of the forward current for two VCSELs, one of which emits the lowest optical power and the other of which emits the highest optical power of the six VCSELs of this type that we tested.

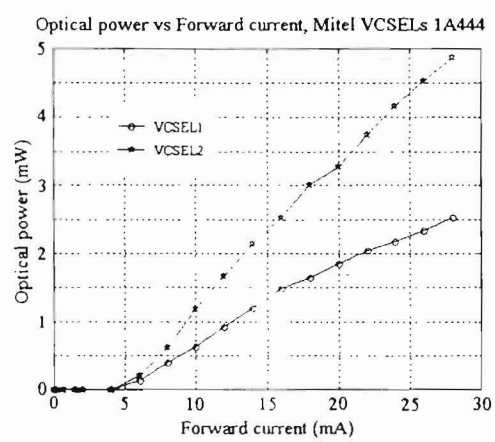
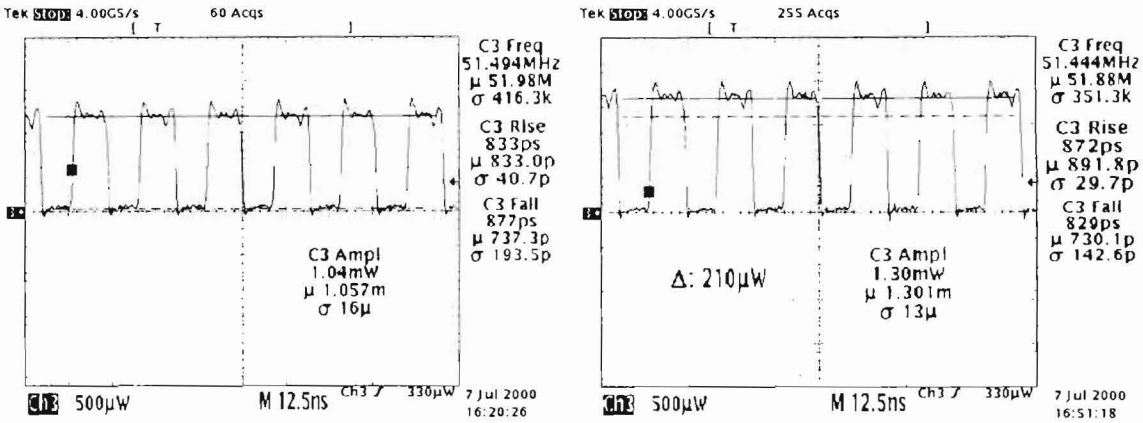


Figure 9: Optical power as a function of the forward current for two Mitel 1A444 VCSELs.

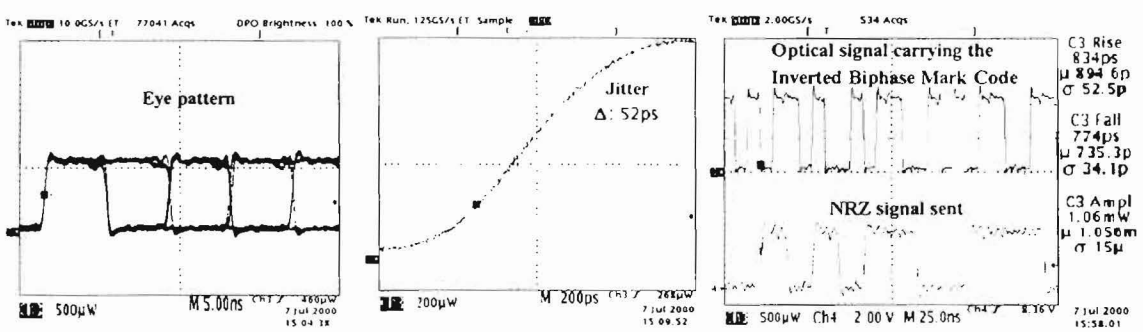
When we drive the VCSEL with a current bias of 5 mA and a modulation current of 7.5 mA, the maximum current driving the VCSEL is 12.5 mA. We can see from the figure that with this current we produce 1 mW of optical power from VCSEL1 and 1.8 mW from VCSEL2. This is an 80% optical power variation between them with respect to the lower optical power. But if we drive the VCSELs with voltage, for 1.99V maximum voltage applied, VCSEL1 emits 1.04 mW and VCSEL2 emits only 1.30 mW. This is a 25% optical power variation with respect to the lower optical power (See Figure 10.). This figure and the three that follow show the signals as seen on a Tektronix TDS 784D digital oscilloscope. The optical signals are input to the oscilloscope by means of the Tektronix P6701A optical probe.



(a) (b)

Figure 10: Optical signals when we drive the Mitel 1A444 VCSELs with voltage. (a) Optical signal from VCSEL1 at 103 Mbps and (b) Optical signal from VCSEL2 at 103Mbps.

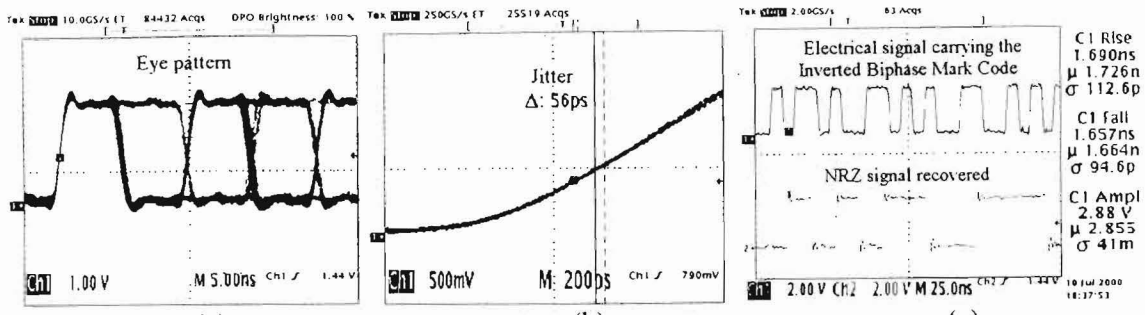
The characteristics of the optical signal output by the 104 Mbps optical link transmitter are very open-eye pattern, 52 ps of jitter peak to peak, and rise and fall times of about 800 ps. These are shown in Figure 11 along with the NRZ signal and the corresponding optical signal carrying the inverted bi-phase mark code.



(a) (b) (c)

Figure 11: Optical signal carrying the inverted bi-phase mark code. (a) Eye pattern, (b) Jitter and (c) Rise and fall times of the optical signal transmitted. Figure 11c also shows the NRZ signal sent.

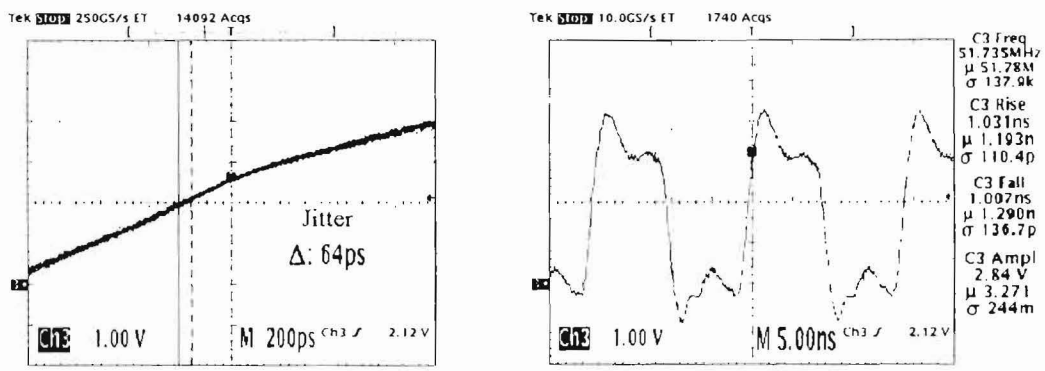
The 104 Mbps optical link receiver recovers the signal with very open-eye pattern, 56 ps of jitter peak to peak, and rise and fall times of 1.7 ns (See Figure 12.).



(a) (b) (c)

Figure 12: Electrical signal carrying the bi-phase mark code recovered. (a) Eye pattern, (b) Jitter and (c) Rise and fall times of the 104 Mbps optical link receiver. Figure 12c also shows the NRZ signal recovered.

The PLL designed and built for the ORCIB provides a clock signal with a jitter of only 64 ps peak to peak and rise and fall times of 1.2 ns to the G-Link daughter cards. The characteristics of this clock signal are shown in Figure 13.



(a) (b)

Figure 13: Clock signal supplied to the CHFET serializer or HDMP-1032 Glink receiver. (a) Jitter and (b) Rise and fall times.

The performance of the first prototype of the ORCI for the BTeV Pixel Vertex Detector is very good. The 104 Mbps optical link receiver recovers the signal with only a slight increase in jitter (about 4 ps) relative to the optical signal transmitted. The rise and fall times increase to 1.7 ns because of the performance limitations of the discriminator. The Bit Error Rate (BER) is another very good indicator of the performance of an optical link and can be calculated [8] as follows:

$$BER \approx \frac{e^{-(SNR^2/2)}}{SNR \times \sqrt{2\pi}} \tag{1}$$

with SNR = Signal to Noise ratio.

We have measured a peak to peak noise of 5mV on the PIN photodiode's output terminal without any optical signal impinging on it. The responsivity of the PIN photodiode is 0.45A/W. Using these inputs we can calculate the SNR ratio as a function of the optical power impinging on the PIN photodiode to get the theoretical BER by means of Equation 1.

The experimental BER was measured using the 7-bit protocol generator as our pattern generator; this generates a long serial stream of bits. This signal is encoded by the bi-phase mark encoder. The bi-phase mark signal is input to the 104 Mbps optical link transmitter. The 104 Mbps optical link receiver recovers the signal. Afterwards, there is a comparison between the recovered signal and the original signal. If they are not equal, the error counter is incremented by one. A block diagram is shown as Figure 14.

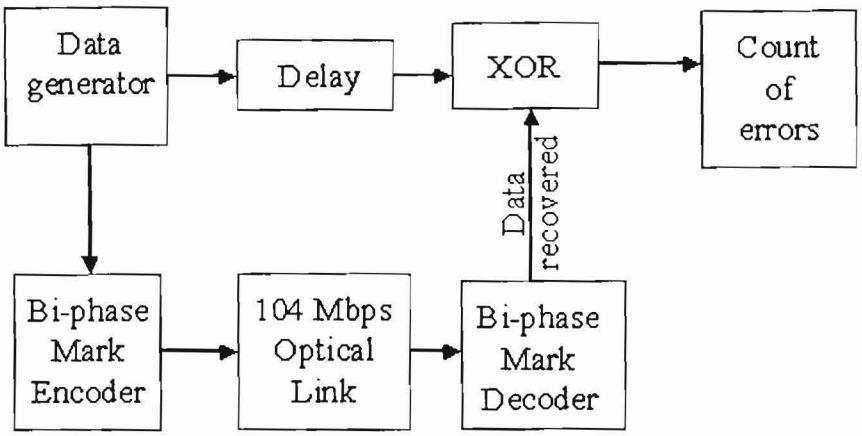


Figure 14: Block diagram of the BER test of the 104 Mbps optical link.

In Figure 15 we show the theoretical and experimental BER of the 104 Mbps optical link as a function of the optical power impinging on the PIN photodiode.

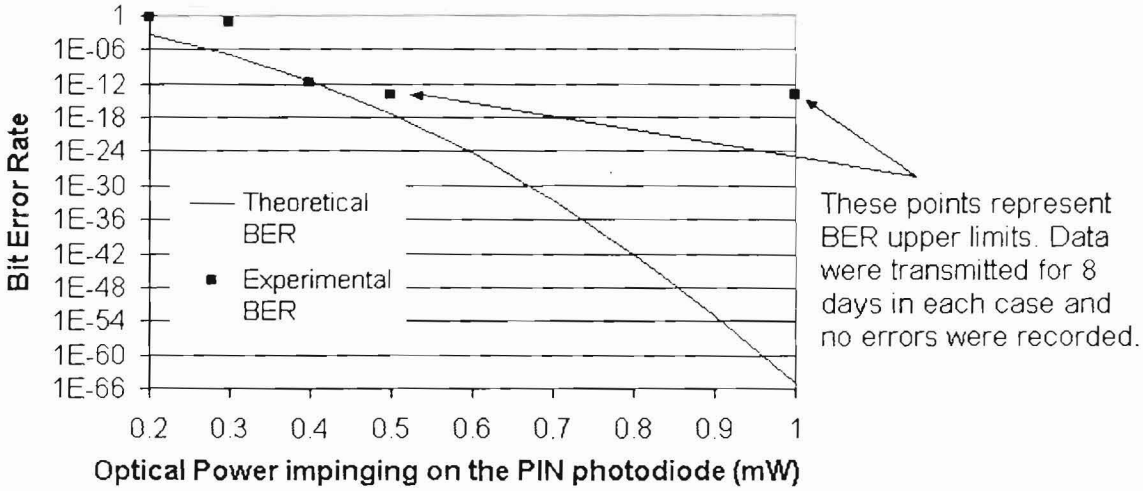


Figure 15: Theoretical and experimental BER of the 104 Mbps optical link.

The measured BER is very small, as expected, which indicates that the bi-phase mark decoder accurately reproduces the information sent from the counting room. The 1.04 Gbps optical link, which transmits the data generated in the MCM, has been shown by others to have a very low BER [9]. The FPGA is not radiation hard, but radiation hard FPGAs are available up to 300kRad [10]. Also, both the HFE-4080 VCSELs from Honeywell and the 1A444 VCSELs from Mitel have been shown to be radiation hard [7,11].

4. Tests of the Optical Readout and Control Interface

To verify that the ORCI provides the correct command and control signals to the MCM and performs the readout without introducing errors, we took advantage of an existing test stand at Fermilab, including software. We repeated the noise and threshold uniformity tests that had been carried out using the test stand without the ORCI, and thus were able to make a direct comparison between the two performances. The software developed runs under the LABVIEW framework and was designed to execute the threshold dispersion and noise measurements to characterize the FPIX1 chips on the MCM. Two computers running two different programs are used. One computer controls the test stand instruments and the data acquisition (DAQ); the second performs the data analysis. The DAQ program uses one data generator to send all the commands to configure the MCM and another data generator to send the commands to control the readout. The data acquired are input to a logic analyzer, which transfers them via a local area network (LAN) to the second computer for analysis. The analysis program first fits the threshold curve for each pixel to get the threshold and noise for the individual cells. It then fits a Gaussian to the threshold and noise distributions for the pixels on each chip to determine the mean threshold, threshold dispersion, mean noise, and noise dispersion for each of the five FPIX1 chips on the MCM. Full details are contained in reference 12.

We made the following modifications to the test stand to include the ORCI in the system. For the control path, instead of connecting the two data generators directly to the inputs of the MCM, we connected them to the inputs of the 104 Mbps optical link transmitter and connected the outputs of the 104 Mbps optical link receiver to the command and control lines of the MCM. For the readout path, instead of connecting the 17 data output lines of the MCM directly to the logic analyzer, we connected them to the inputs of the 1.04 Gbps optical link transmitter and the outputs of the 1.04 optical link receiver to the logic analyzer. No changes were needed to the software used to characterize the FPIX1 readout chips on the MCM. A picture of the setup is shown as Figure 16.

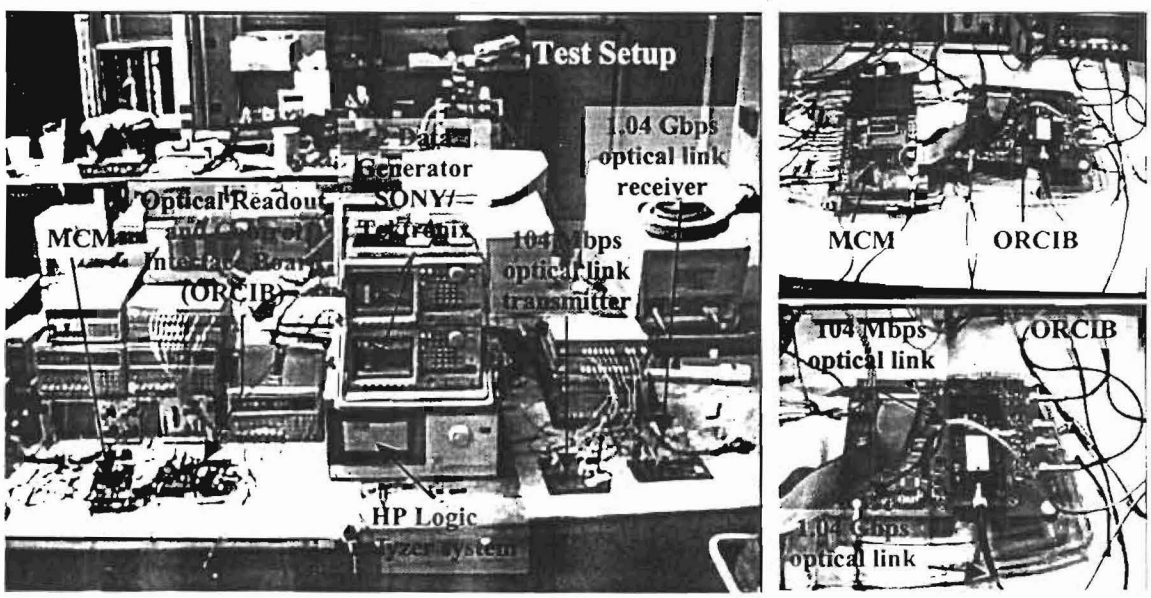
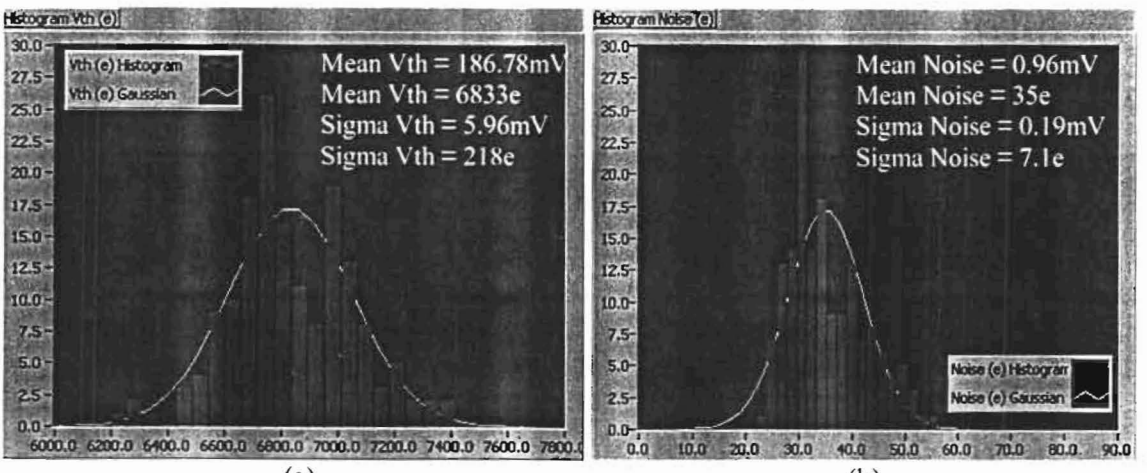


Figure 16: Setup used to characterize the MCM using the optical links to program, control and read out the MCM.

Table 1 shows the results of the threshold and noise uniformity tests of the MCM, obtained with and without the ORCI in the setup. Figure 17 shows the threshold and noise distribution of the first of the five FPIX1 chips on the MCM without using the ORCI. Figure 18 shows the threshold and noise distribution of the same FPIX1 chip using the ORCI. The results are seen to be the same within errors. The noise is slightly higher for the case with the ORCI, most likely because of the unshielded flat cables used to interface it to the MCM.

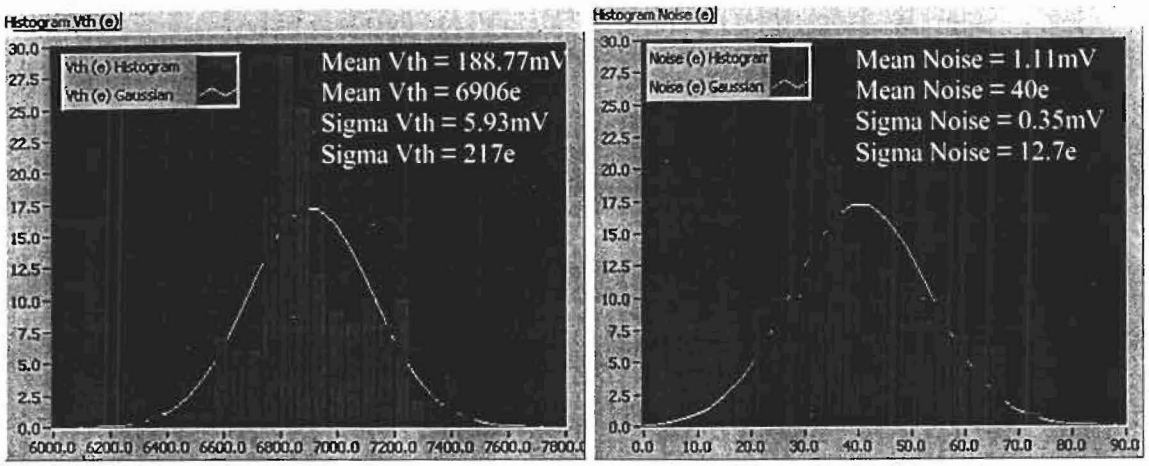
VthO = 1.95V	**Results of the characterization of the MCM when tested without the ORCI**				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6833	6657	6581	6792	6956
Threshold dispersion (e-)	218	239	217	168	146
Mean noise (e-)	35	37	37	31	31
Noise dispersion (e-)	7.1	8.1	9.0	5.9	6.2
VthO = 1.95V	**Results of the characterization of the MCM when tested with the ORCI**				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6906	6886	6820	6910	7051
Threshold dispersion (e-)	217	184	179	142	161
Mean noise (e-)	40	37	38	32	30
Noise dispersion (e-)	12.7	13.5	12.9	9.6	9.6

Table 1: Results of the threshold and noise uniformity of the MCM when tested with and without the ORCI.



(a) (b)

Figure 17: Distribution of the first of the five FPIX1 chips on the MCM when tested without the ORCI. a) Threshold distribution and b) Noise distribution.



(a) (b)

Figure 18: Distribution of the first of the five FPIX1 chips on the MCM when tested with the ORCI. a) Threshold distribution and b) Noise distribution.

5. Summary

The first prototype of the ORCI for the BTeV pixel vertex detector has been designed, built, and tested at Fermilab. The 104 Mbps optical link provides high accuracy transmission of information in a very wide renge of optical power as is evident from the low BERs measured. By driving the VCSELs with voltage we achieve better system uniformity. The decision to use the PIN photodiode in photovoltaic mode results in an improved SNR and is expected to make it less susceptible to SEU. Both of these design choices are expected to provide a larger margin of safety relative to potential radiation damage

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References

[1] J. Butler, S. Stone, et. al., *Proposal for an experiment to measure mixing, CP violation, and rare decays in Charm and Beauty particle decays at the Fermilab collider- BTeV*, submitted to the Fermilab Program Advisory Commite, May 2000. Stage I approval given June 27, 2000.

[2] G. Cancelo, D. Christian, J. Hoff, A. Mekkaoui, R. Yarema, S. Zimmermann, *High readout speed pixel chip development at Fermilab*, Fourth Workshop on Electronics for LHC Experiments, 528-532, 1998.

[3] S. Zimmermann, *Development of High Data Readout Rate Pixel Module and Detector Hybridization at Fermilab*, Presented at Pixel 2000, Genoa, Italy, June 2000.

[4] J. Singh, *Semiconductor Optoelectronics: Physics and Technology*, McGraw-Hill, New York, c1995, p. 351.

[5] G. F. Knoll, *Radiation Detection and Measurement*, Wiley, New York, 2nd edition, c1989, p. 350.

[6] Agilent Technologies, Inc., *Agilent HDMP-1032/1034 Transmitter/Receiver Chip Set Data Sheet*, c2000.

[7] P. Denes, *Digitization and Data Transmission for the CMS Electromagnetic Calorimeter*, Proceedings of the 4th workshop on electronics for the LHC experiments. Rome, Italy September 1998.
[8] V. Arbert-Engels, et. al., *Characterization of Optical Data Links for CMS experiment*. Proceedings of the 3rd Workshop on Electronics for the LHC experiments. London, UK September 1997.
[9] K. Anderson, et. al., *Neutron Irradiation Tests of an S-Link-over-G-Link System*, ATLAS Tile Calorimeter internal document, November 1999.
[10] Actel Corporation, *Data Sheet of Radiation-Hardened FPGAs*, January 2000.
[11] I. M. Gregor, *Optical Links for the ATLAS SCT and Pixel Detector*, Presented at PIXEL 2000. Genoa, Italy, June 2000.
[12] M. A. Vargas, et. al., *The Development of Software to Characterize the Fermilab Pixel Readout Chip, FPIX1, for the BTeV experiment*, submitted to NIMA, August 2000.