Test Results for the SVX4 Version A/B Chip

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Abstract: We present and summarize the test results for the SVX4 version A/B chip. After all tests, we are confident that the SVX4 version A/B chip satisfies all requirements for full production.

1 Introduction

There are two versions of the SVX4 chip: Version A that has minimal changes and Version B that has maximal changes. The details of these changes can be found in References [1] and [2]. We aggressively choose to test Version B of the chip due to the expected improvement in performance.

2 The Preamplifier

We did a variety of studies to confirm no performance characteristics changed in the preamplifier of the SVX4. The three main quantities to study are the bandwidth, gain, and noise. In order to study these three topics, it is necessary to inject charge through an external capacitor. We are able to bond six channels of the SVX4 onto the chip carrier and place external capacitors on these inputs. Then using an external pulser, we can inject charge through the external capacitor. For experimental details see Reference [3].

2.1 Bandwidth Studies

In order to maximize the integration time of the preamplifier, it is necessary to inject charge directly after the falling edge of the front-end clock signal. We show the injection timing used in this study from an external pulser in Figure 1.

Channel 127 of the chip has special pads that allow direct observation of the preamplifier output. In Figure 2, we show the output of the preamplifier of the SVX4 for channel 127. We used the oscilloscope with the 0-90% definition to measure the rise time for all bandwidth settings of the chip for four different values of the external capacitance. In Table 1, we show the measured rise time values from channel 127 for four different values of the external capacitance and all bandwidth settings internal to the chip.

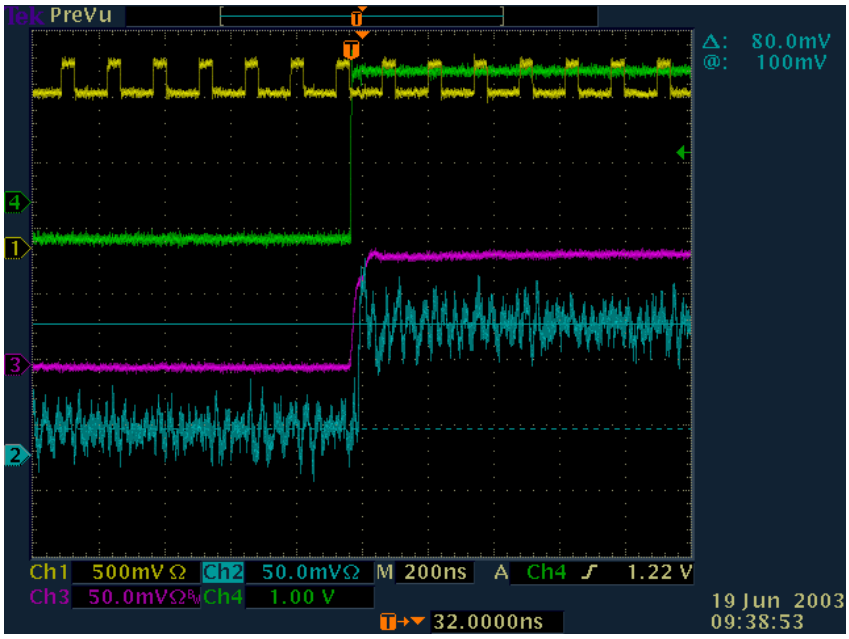

Figure 1 Oscilloscope picture showing the injection timing of the external pulse. The yellow trace is the front-end clock and the green trace is the external trigger generated from the Stimulus System when downloading the control pattern to the chip. The purple trace is the trigger signal of the external pulser. The blue trace is the actual voltage as seen by the external capacitor bonded to an input of a single channel of the SVX4. The front-end clock duty cycle is 28% and the period is 132 ns.

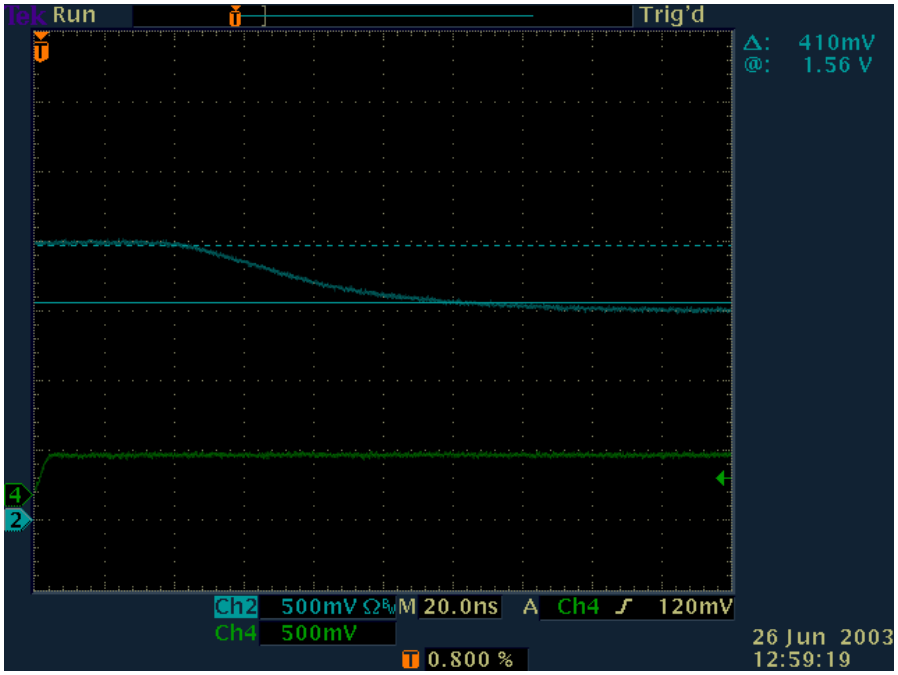

Figure 2 Oscilloscope picture showing the preamplifier output from channel 127 for an external capacitance of 10 pF. We used the 0-90% definition of rise time. The blue trace is the preamplifier output from channel 127. The dotted line and the solid line are the horizontal cursors used to measure the rise time. The green trace corresponds to the trigger.

BW\C	10 pF	20 pF	30 pF	40 pF
0	32	41	48	60
1	36	48	60	72
2	40	55	68	76
3	44	64	76	96
4	49	70	82	104
5	53	76	92	120
6	57	82	100	128
7	66	90	108	136
8	62	84	102	128
9	68	92	112	136
10	74	100	120	152
11	80	106	132	160
12	84	112	144	168
13	90	120	152	176
14	94	124	164	188
15	100	128	176	200

Table 1 Measured rise time values from channel 127 of the SVX4 for four different values of the external capacitance for all values of the bandwidth settings internal to the chip. All table values have units of ns.

In Figure 3, we show the graphical representation of the rise time data given in Table 1.

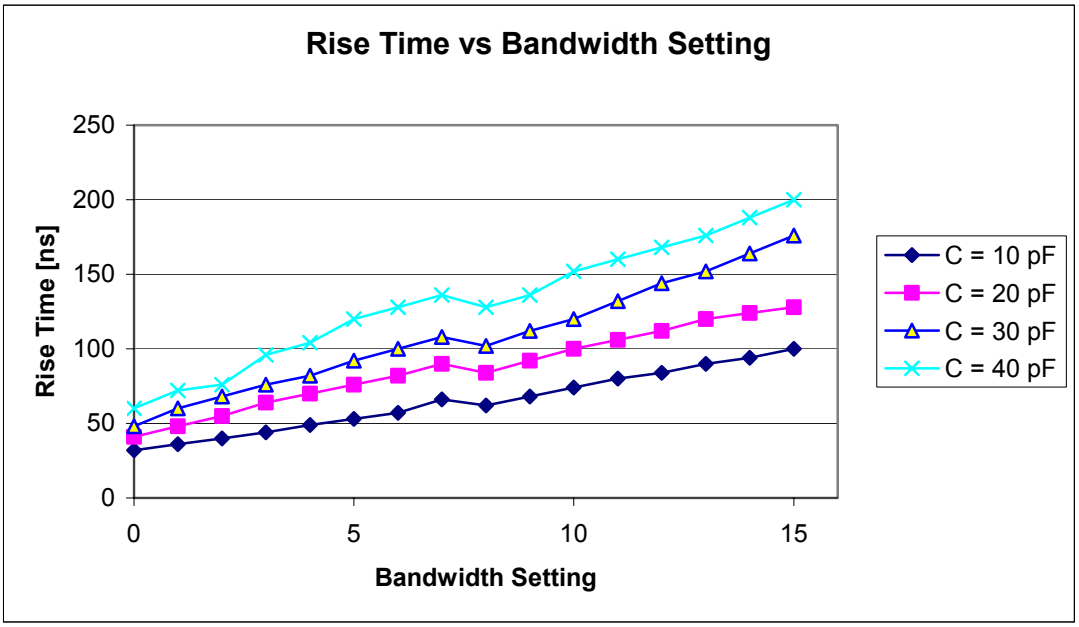

Figure 3 Graphical representation of the rise time for the four different values of the external capacitance and all internal bandwidth settings of the chip from channel 127.

2.2 Effective Gain

As stated above, we wirebonded six channels of the SVX4 in order to measure the gain for different values of external capacitance. It is important to note that the chip is optimized for 132 ns operation. First we measured the gain using a 132 ns front end

clock and then for a 396 ns front end clock which corresponds to the operating frequency when installed in the detector. We have also confirmed with the oscilloscope that the dynamic range of the preamplifier is greater than 200 fC.

2.2.1 Operation at 132 ns

In Figure 4 and Figure 5, we show the gain as a function of the external capacitance for four independent channels with different values of the external capacitance. The gain rises for the larger external capacitances because the preamplifier does not have enough time to integrate all the charge. The corresponding values are given in Table 2 and Table 3.

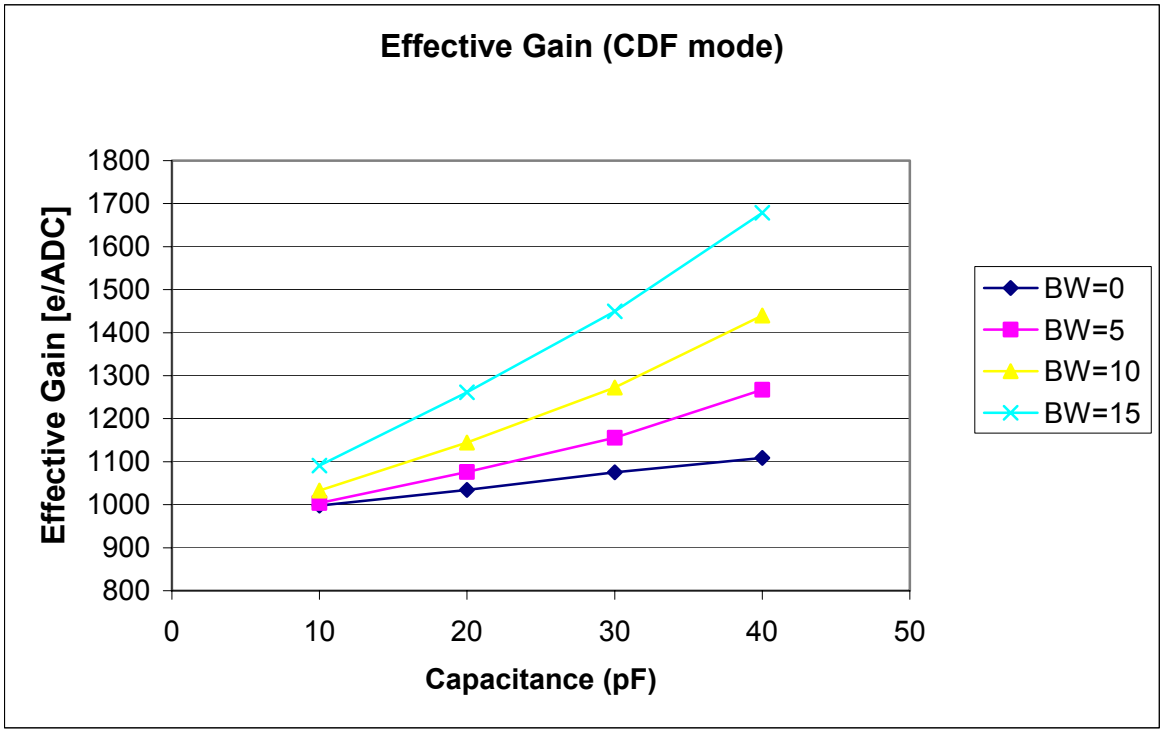

Figure 4 Effective gain as a function of external capacitance in CDF mode for a front end clock period of 132 ns. The curves begin to rise for higher capacitances because the amplifier does not have enough time to integrate the total charge injected. The ramp range was set to 1 and the digitization frequency is 50 MHz.

BW \ C	10 pF	20 pF	30 pF	40 pF
0	997.9	1034.6	1075.3	1108.9
5	1003.6	1075.8	1155.4	1266.9
10	1033.1	1144.1	1272.6	1439.5
15	1090.8	1261.2	1449.4	1678.6

Table 2 Effective gain as a function of the external capacitance in CDF mode for a front end clock period of 132 ns. All gain values are in electrons per ADC count.

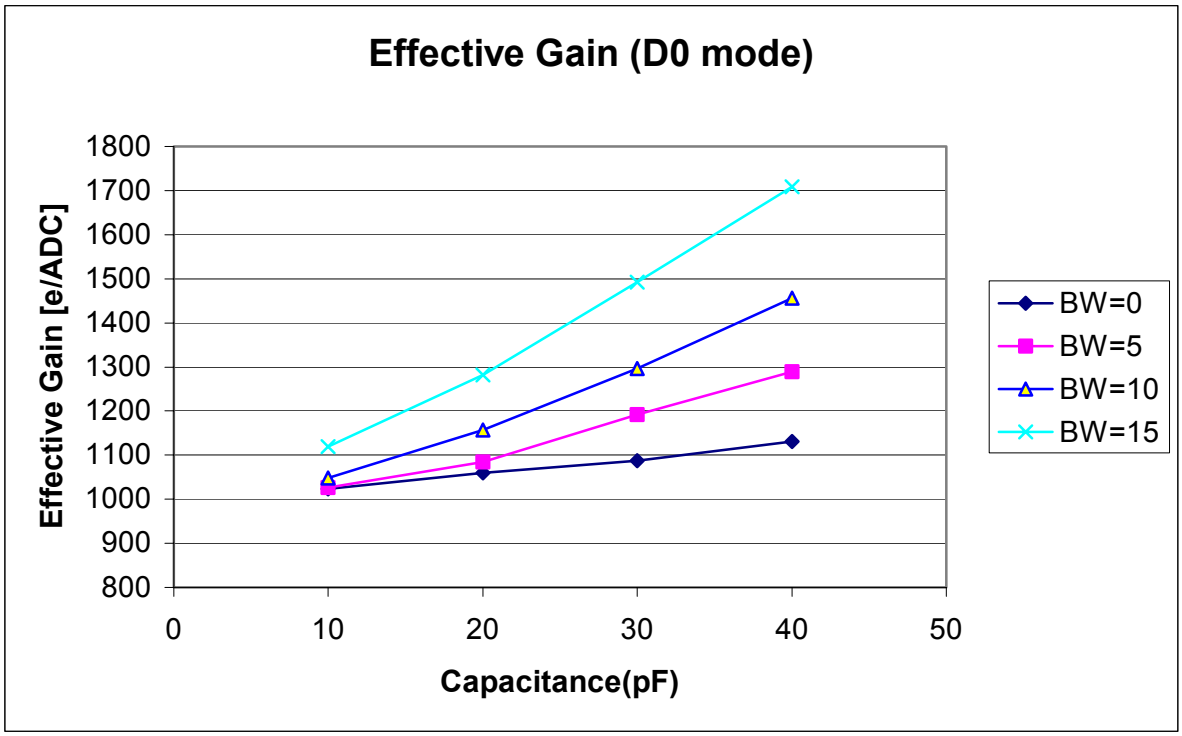

Figure 5 Effective gain as a function of external capacitance in DØ mode for a front end clock period of 132 ns. The curves begin to rise for larger capacitances because the amplifier does not have enough time to integrate the total charge injected. The ramp range was set to 1 and the digitization frequency is 50 MHz.

BW \ C	10 pF	20 pF	30 pF	40 pF
0	1024.1	1059.6	1087.5	1131.2
5	1027.0	1084.1	1192.0	1289.0
10	1048.5	1157.3	1296.1	1456.0
15	1118.6	1281.9	1492.6	1709.2

Table 3 Effective gain as a function of the external capacitance in DØ mode for a front end clock period of 132 ns. All gain values are given in electrons per ADC count.

2.2.2 Operation at 396 ns

In Figure 6 and Figure 7 we show the charge injection timing used in the gain and noise studies using a front end clock with a period of 396 ns. The clock used to generate the 396 ns interval is the original 132 ns clock with two clock pulses removed. We also adjusted the pipeline depth accordingly in order to see the external and internal charge injection.

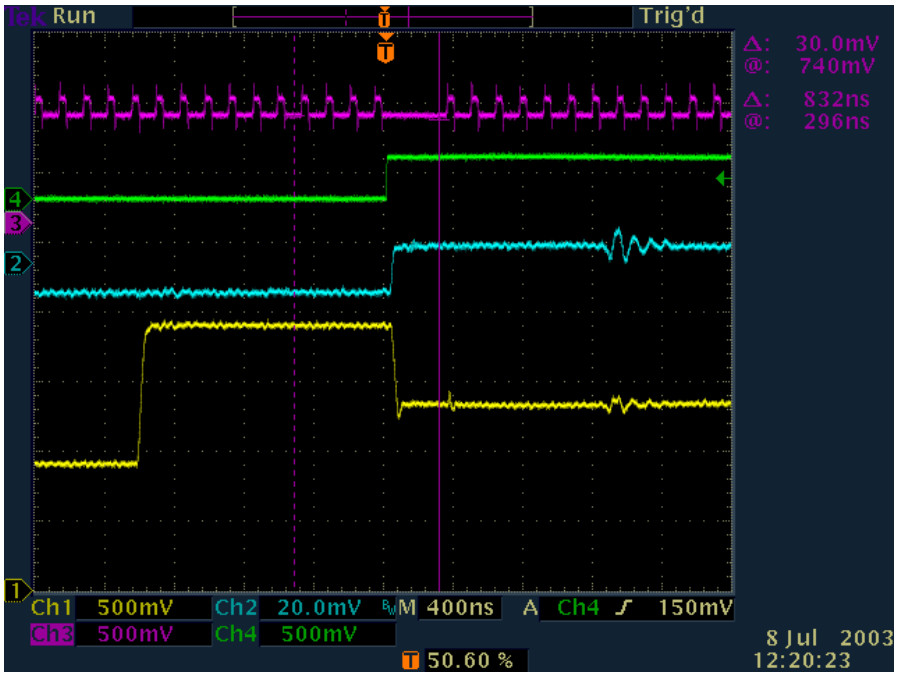

Figure 6 Charge injection timing for gain and noise studies at 396 ns. The pink trace is the front end clock and it is operating at 132 ns, but for the charge injected pipeline the clock is effectively at 396 ns. The green trace is the external pulser trigger. The blue trace is the change in voltage as seen by the external capacitor. The yellow trace is the preamplifier output from channel 127.

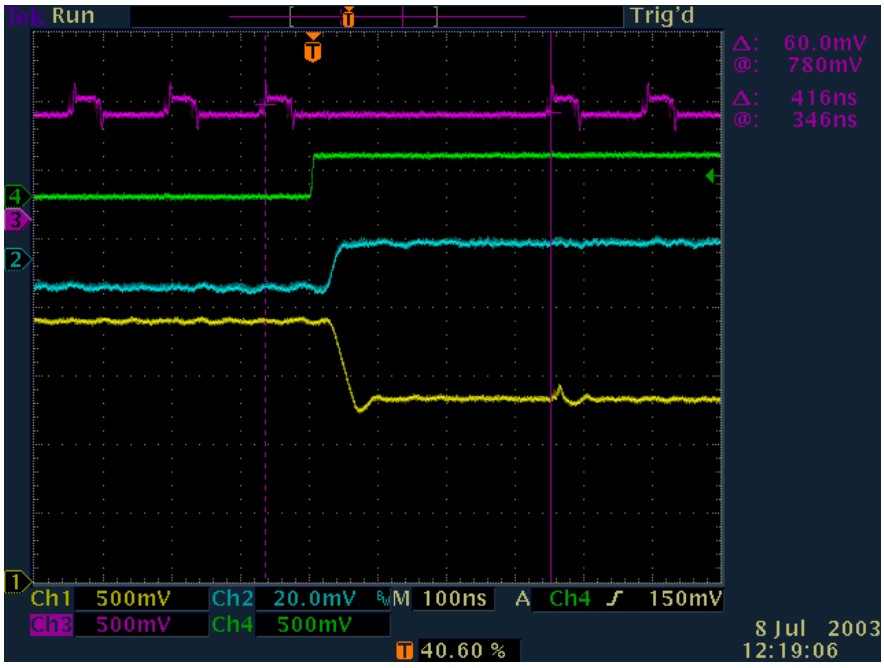

Figure 7 An enlarged view of the charge injection timing for gain and noise studies at 396 ns. The pink trace is the front end clock and it is operating at 132 ns, but for the charge injected pipeline the clock is effectively at 396 ns. The green trace is the external pulser trigger. The blue trace is the change in voltage as seen by the external capacitor. The yellow trace is the preamplifier output from channel 127.

In Figure 8 and Figure 9 we see the gain as a function of channel number. We can only bond six channels at a time on an individual chip carrier. We see a uniform gain across the chip.

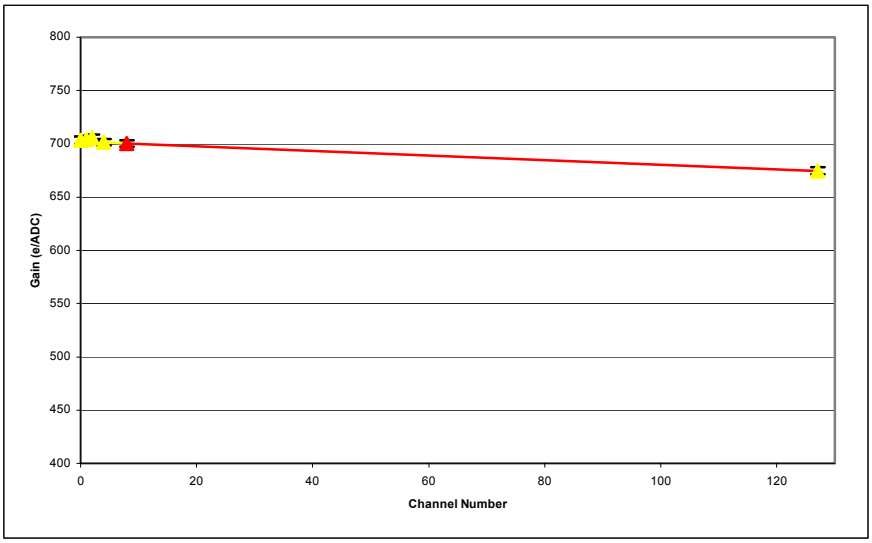

Figure 8 Gain as a function of channel number measured for six wire bonded channels. The digitization frequency is 50 MHz and the ramp range setting is 1.

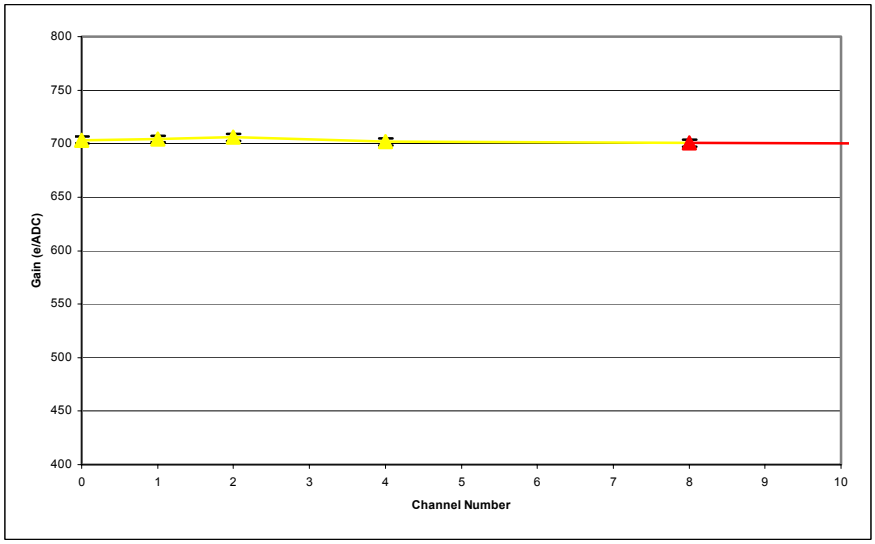

Figure 9 An enlarged view of the gain for bonded channels near the edge of the chip. The digitization frequency is 50 MHz and the ramp range setting is 1.

In Figure 10, we show a similar study from the PATT03 test stand. After conversion to 53 MHz (digitization frequency), a gain of 729 electrons/ADC count was calculated which is consistent with the previous versions of the SVX4 (~700 electrons/ADC count). Two different methods were used to connect the external capacitors to the input of the SVX4 to confirm that the preamplifier was insensitive (the gain remains the same) to the loading scheme.

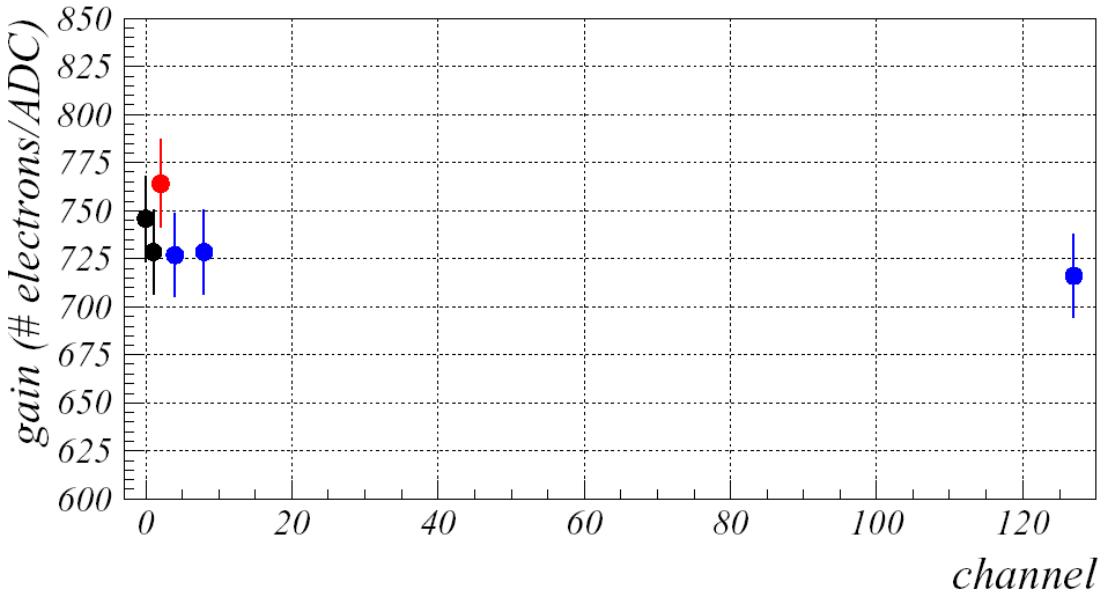

Figure 10 Effective gain (number of electrons per ADC count) for channels 0, 1, 2, 4, 8, and 127. The load capacitance is 10pF for channel 0 and channel 1, 30pF for channel 2, and 10pF (for charge injection) plus 20pF (for the load), 30pF in total, for channel 4, 8 and 12. A bandwidth setting of 4 was used.

In Figure 11 we show the measured gain for two different ramp slope values from the PATT03 test stand. These histograms show that there is no bandwidth dependence and that a 396 ns integration time is long enough to integrate all charge for a 30 pF load, but a huge charge injection may affect the gain.

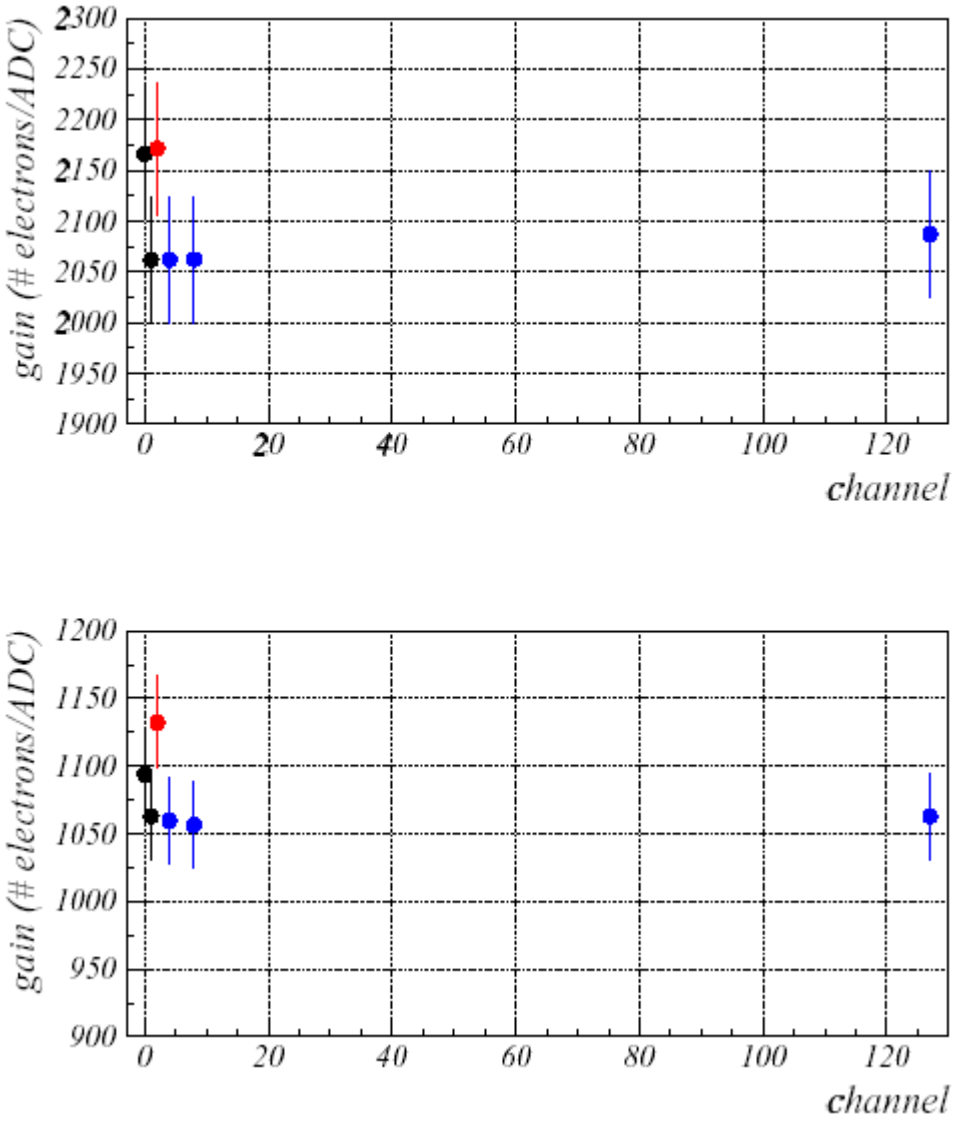

Figure 11 Gain (number of electrons per ADC count) for channel 0, 1, 2, 4, 8, and 127. The load capacitance is 10pF for channel 0 and 1, 30 pF for channel 2, and 10pF (for charge injection) plus 20pF (for the load), 30pF in total, for channel 4, 8, and 127. A bandwidth setting of 4 was used.

2.2.3 Making Proper Statements About Gain

It is important to clarify the meaning of gain used in this report. The true gain is independent of the input capacitance. The concept of gain used in this report is the effective gain. Second, changing the bandwidth settings of the SVX4 chip adjusts the rise time of the preamplifier. Third, in order to compare gain values, the channels in the comparison must have identical rise times.

The effective gain is exactly determined by the gain and the risetime as follows:

$$g_{eff} = g * \int (1 - \exp(-t/\tau))$$

where g is the gain (constant) and τ is the risetime (0 to 63%, or the 10-90% risetime divided by 2.2). To measure the gain simply use integration time >> τ. The gain we measure changes because the integration time is smaller than the true risetime of the preamplifier (as the bandwidth increases).

Strictly speaking, the gain is not constant vs. input capacitance. It will vary slightly because the injected charge will is shared between the feedback capacitor and the load capacitance. For zero load capacitance the gain will be highest (g_max). For non-zero load:

$$g = g_{max} * (G * C_f) / (C_L + G * C_f)$$

where C_f is the feedback capacitor, C_l is the load capacitance, and G is the open loop gain of the preamp op-amp, which is supposed to be in the thousands or tens of thousands. The open loop gain could actually be determined by measuring the gain vs. input capacitance for very long integration time. However, since G is so large, you would need to go to load capacitor values >100 pF to see and the effect. The open loop gain is interesting because it determines how much charge will be shared with the sensor back plane capacitance. When we say that 1 MIP is 24K electrons, this is actually shared with the sensor back plane capacitance and the chip will never see the full charge. However, the amplifier designs we use have a large open loop gain so that the fraction of charge lost and insignificant.

2.3 Noise Studies

Once the gain is measured, we can calculate the equivalent noise charge from the measured noise in ADC counts for the two clock periods of 132 ns and 396 ns. We discuss the results below.

2.3.1 Operation at 132 ns

Using the timing discussed in Section 2.2.1 and Section 2.2.2, we converted the measured noise values into the Equivalent Noise Charge. In Figure 12 and Figure 13, we show the ENC for 132 ns operation for CDF mode and DØ mode. Again, the curves rise because the gain is larger for larger values of the external capacitance.

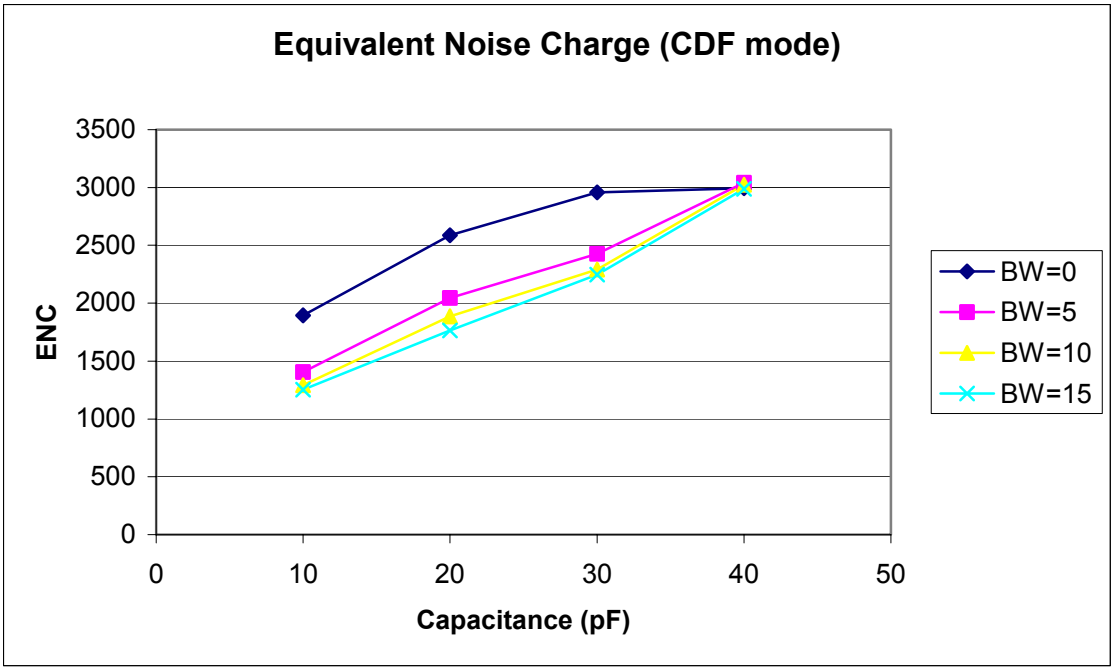

Figure 12 Equivalent Noise Charge (ENC) as a function of the external capacitance in CDF mode. The curves begin to rise because the gain increases for larger values of the external capacitances. The digitization frequency was 50 MHz and the ramp range setting was 1.

In Table 4, we show the measure noise in actual ADC counts in CDF mode.

BW \ C	10 pF	20 pF	30 pF	40 pF
0	1.9	2.5	2.75	2.7
5	1.4	1.9	2.1	2.4
10	1.25	1.65	1.8	2.1
15	1.15	1.4	1.55	1.78

Table 4 Noise as a function of the external capacitance for CDF mode. All noise values are given in ADC counts.

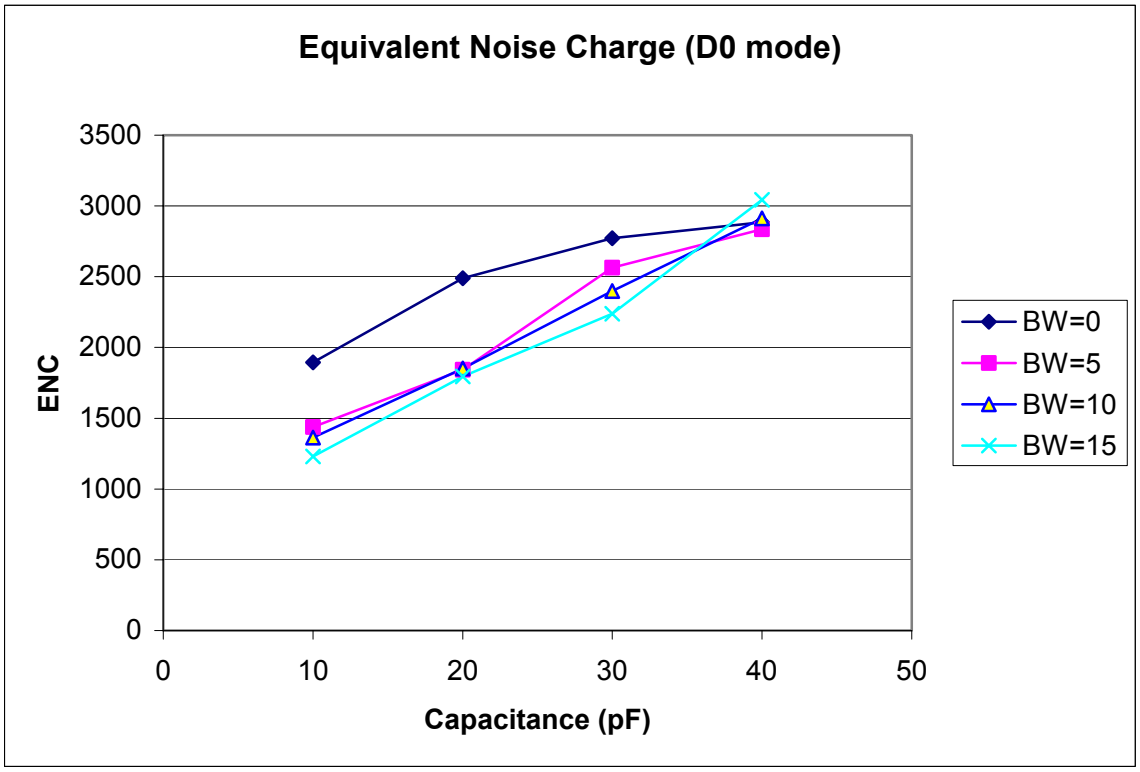

Figure 13 Equivalent Noise Charge (ENC) as a function of the external capacitance in DØ mode. The curves begin to rise because the gain increases for higher values of the external capacitances. The digitization frequency was 50 MHz and the ramp range setting was 1.

InTable 5, we show the measure noise in actual ADC counts in CDF mode.

BW \ C	10 pF	20 pF	30 pF	40 pF
0	1.85	2.35	2.55	2.55
5	1.4	1.7	2.15	2.2
10	1.3	1.6	1.85	2.0
15	1.1	1.4	1.5	1.78

Table 5 Noise as a function of the external capacitance for DØ mode. All values are given in ADC counts.

2.3.2 Operation at 396 ns

We also measured the noise at 396 ns. In Figure 14 and Figure 15 we see the equivalent noise charge for a front end clock of 396 ns. It is important to note that not all channels have the same capacitance. Only channel 0 and channel 127 have the same capacitance of 10 pF and the other channels have a capacitance of 30 pF.

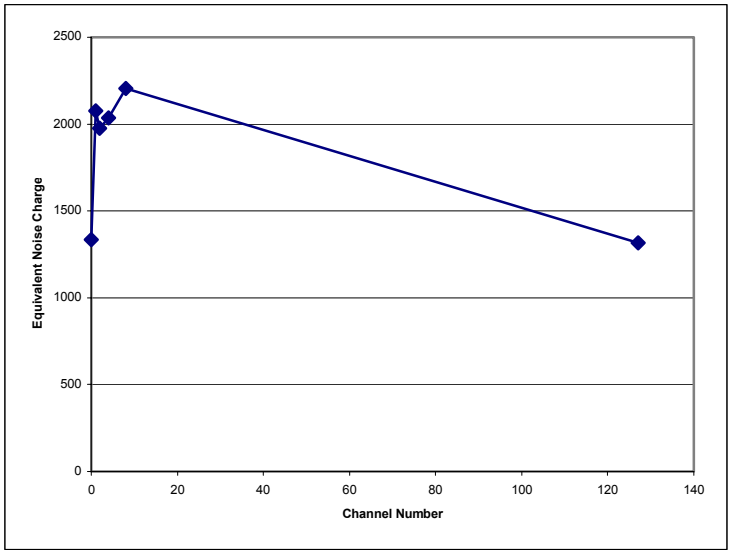

Figure 14 Equivalent noise charge as a function of the channel number. It is important to note that different channels have different capacitances. The following values were used: channel 0, 10 pF; channel 1, 30 pF; channel 2, 30 pF; channel 4, 30 pF; channel 8, 30 pF; channel 127, 10 pF. The digitization frequency was 50 MHz and the ramp range setting was 1.

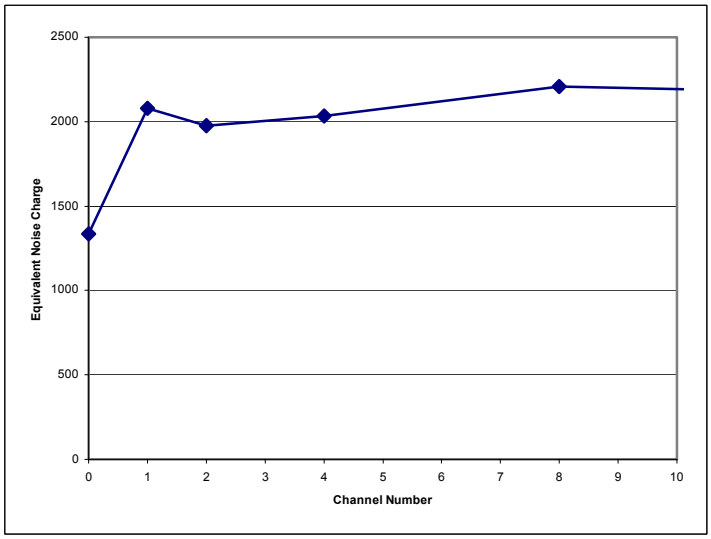

Figure 15 An enlarged view of the equivalent noise charge as a function of channel number. For the data points shown only channel 0 has 10 pF. All other channels have 30 pF. The digitization frequency was 50 MHz and the ramp range setting was 1.

2.3.3 Making Proper Statements About Noise Performance

Analogous to gain comparison between channels with different capacitances, we must choose identical risetimes for each channel. Only then can we make a definitive statement about the noise performance (e.g. S/N). Therefore, changing the risetime or bandwidth settings will give a different noise performance that can be recalculated using Figure 12 and Figure 13.

3 The Pipeline

The preproduction version of the SVX4 has a linear dependence as a function of the cell number pipeline. The average pedestal is larger for higher pipeline cell numbers. The SVX4 version B attempted to correct this problem by enlarging the circuit traces inside the pipeline. From Figure 16 and Figure 17 it is clear that the linear dependence is still present in version B. The variation is only 0.7 ADC counts. This is very small effect and will not affect the overall performance of the chip. The linear dependence acts as a common mode noise contribution to the data and will be removed by the DPS circuitry when operating in the detector. As discussed in Section 4.4, we have confirmed that the dynamic range of the pipeline is greater than 62.5 fC.

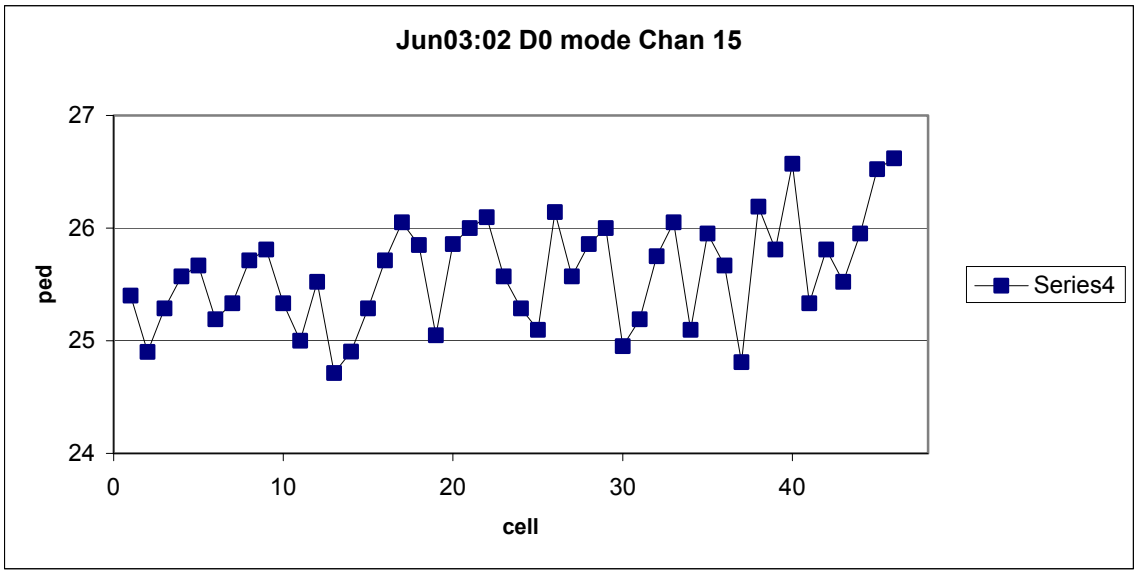

Figure 16 Average pedestal as a function of pipeline cell number for channel 15. It is clear that the linear dependence is still present in the SVX4 version B chip.

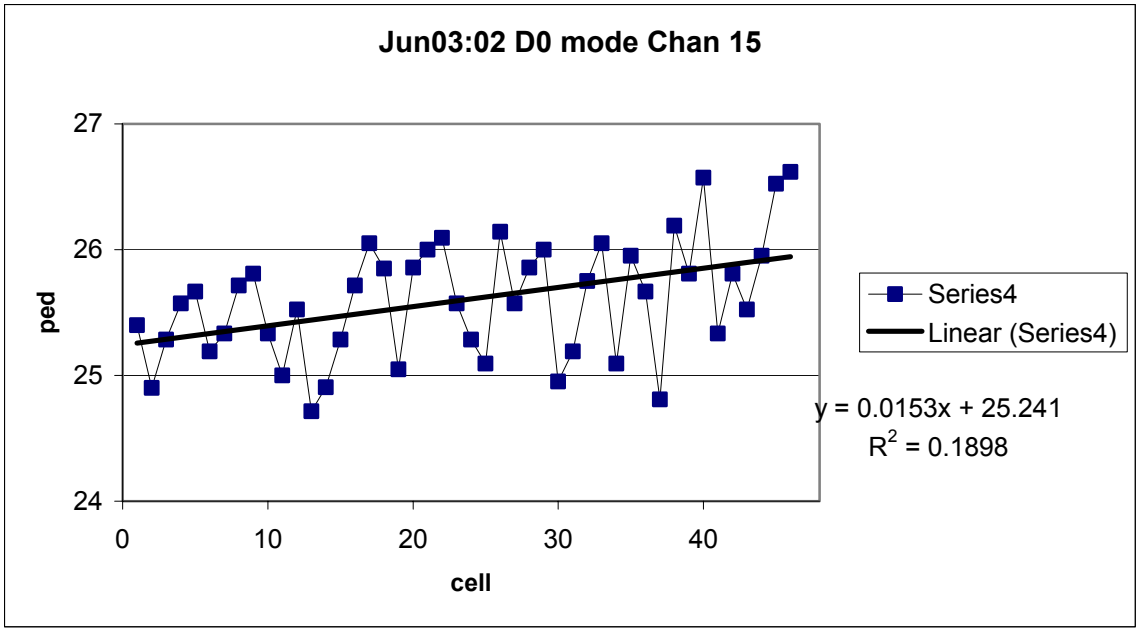

Figure 17 Average pedestal as a function of pipeline cell number for channel 15. We plotted a trend line to show the linear dependence on pipeline cell number.

4 The ADC

The ADC for the SVX4 version B has been redesigned in order to remove the nonuniformity of the pedestal and improve performance. The two most important measurements in the performance of the ADC are the differential nonlinearity and the integral linearity. We also confirmed the proper operation of the pedestal and the ramp for the SVX4 chip.

4.1 Pedestals

The pedestals for the new SVX4 version A and B were adjusted to allow for a larger dynamic range then earlier versions. We measured the pedestal values for the two modes of operation to confirm the change. The values obtained from the chip are shown in Table 6. The graphical representation of this data is shown in Figure 18.

Ramp Pedestal Setting	Pedestal (CDF mode)	Pedestal (DØ mode)
0	193	193
1	176	176.5
2	160	160
3	143	143
4	127	127
5	111	111
6	94.5	95
7	78	78.5
8	62.5	62.5
9	46	46.5
10	30.5	30.5
11	17	17
12	32	32
13	48	48.5
14	63	63
15	150	157

Table 6 Measured pedestal values as a function of the downloaded values for the Ramp Pedestal setting. These values were taken with a Ramp Range setting of 0 and a digitization frequency of 50 MHz. All values are in ADC counts.

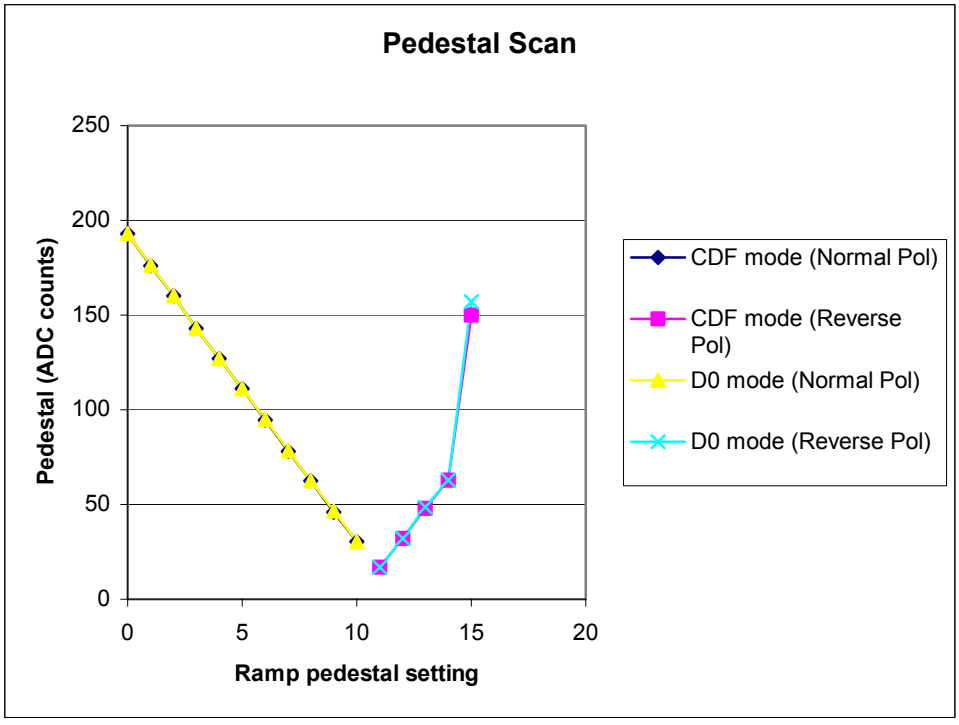

Figure 18 Graphical representation of the pedestal values for the SVX4 version B chip. The Ramp Range value was 0 and the digitization frequency was 50 MHz.

A new feature was added to the SVX4 version B that allows the user to set the pedestal in the ramp down direction with different step widths. It is important to note that for ramp

pedestal settings higher than 10 the ramp direction, pipeline polarity, and comparator polarity must be inverted.
The pedestal nonuniformity no longer exists in the newest versions of the SVX4 chip. All operating ranges where the pedestal was nonuniform have been checked and appear to be linear.

4.2 The Ramp

The ramp was also changed in the newest versions of the SVX4. We confirmed the functionality and the linearity of the new ramp with the following studies below. We downloaded all values of the ramp to the chip and measured the pedestal. In Table 7, we show the pedestal values obtained from the SVX4 for a ramp range scan and in Figure 19 we show the graphical representation of the same data.

Ramp range	Pedestal (CDF mode)	Pedestal (DØ mode)
0	33	33.5
1	78	78
2	78	78.5
3	123	123
4	56	56.5
5	101	101
6	101	101
7	144	145

Table 7 Pedestal values from the SVX4 in CDF and DØ mode for all values of the Ramp Range setting. These pedestals were attained with a Ramp Pedestal setting of 7 and a digitization frequency of 50 MHz. All values are given in ADC counts.

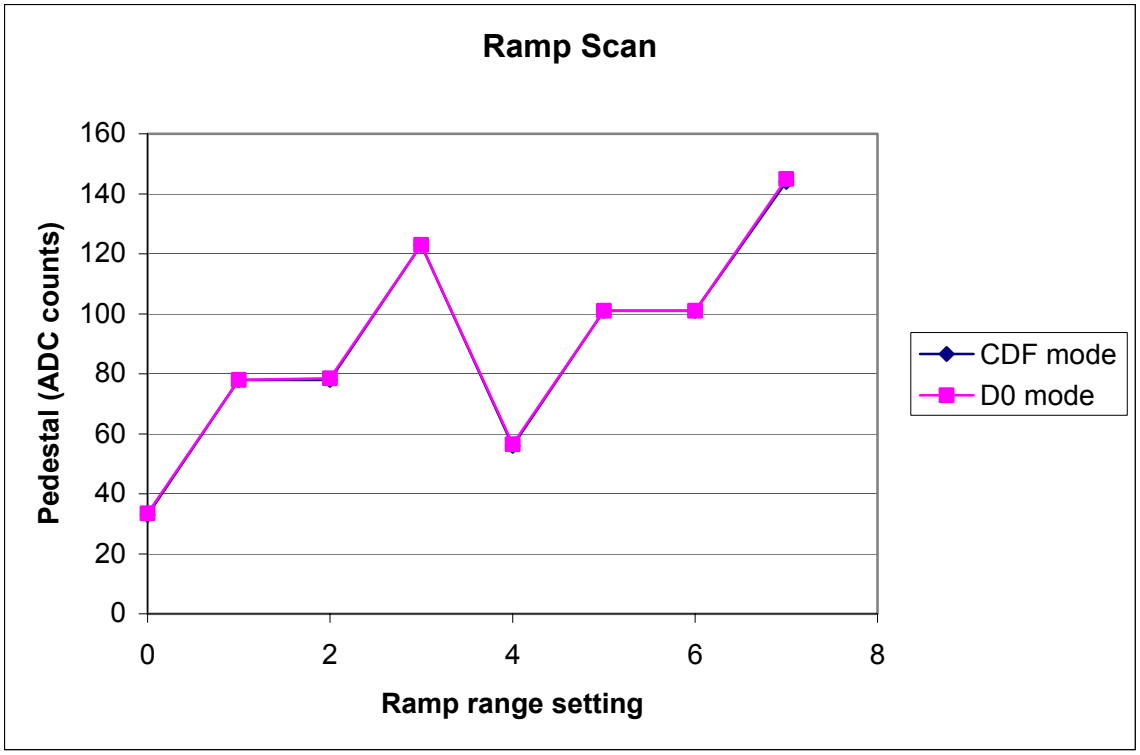

Figure 19 Graphical representation of the pedestals that were obtained by downloading all values for the Ramp Range. A Ramp Pedestal setting of 7 was used and a digitization frequency of 50 MHz.

We also observed and measured the ramp directly by placing a Picoprobe on test pads located on the top of the chip. The ramp output is shown in Figure 20. The first dip in Figure 20 is the ramp obtaining the ramp pedestal setting. The ramp is not released until the digitize cycle occurs. When digitization is about to begin, the ramp is released. This is clearly seen in the figure. Using the oscilloscope, we measured the values of the ramp directly. We give the data in Table 8.

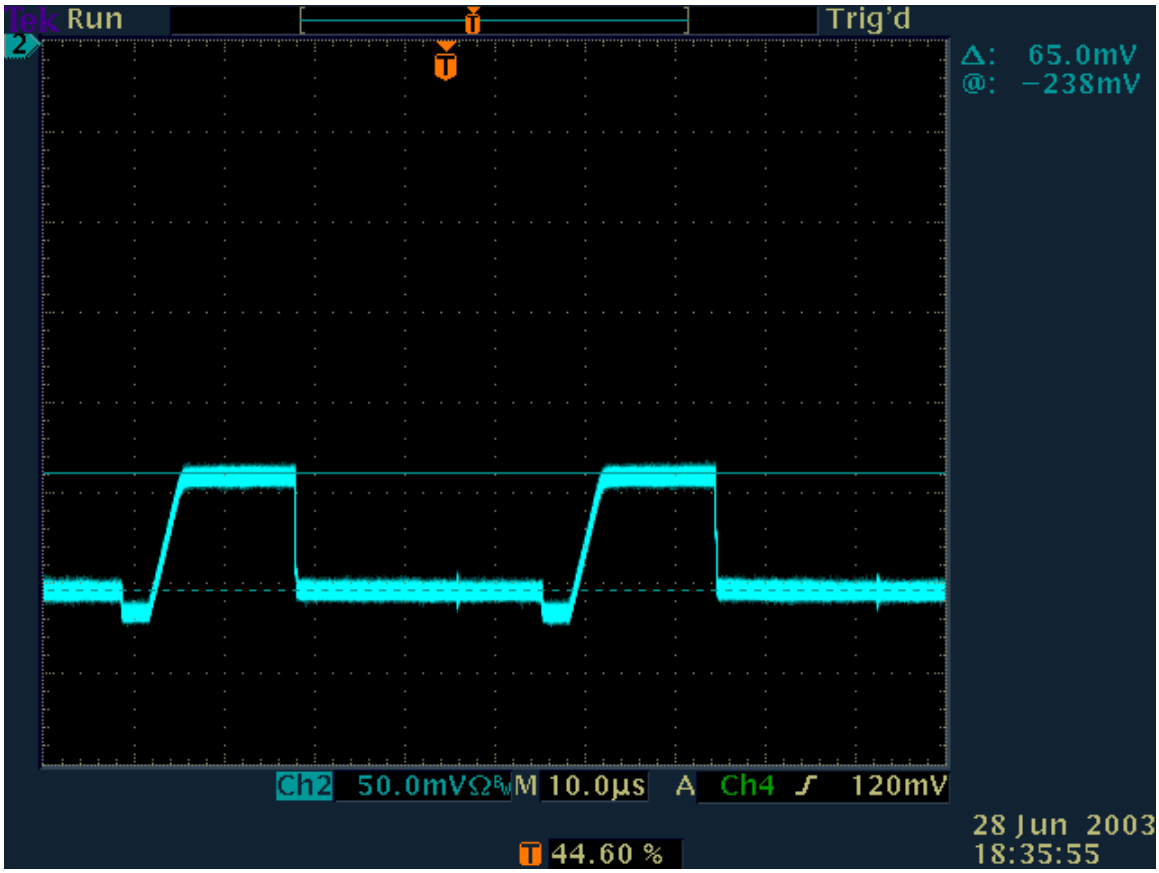

Figure 20 A picture showing the ramp of the SVX4. The Stimulus System was set to Auto-Burst mode which constantly downloads the control pattern in order to make viewing the ramp easier.

Ramp Range	0	1	2	3	4	5	6	7
Slope	23.8	8.1	8.24	5.04	11.82	6.18	6.31	4.12

Table 8 Measured values for the slope of the ramp. We measured these values by placing a picoprobe onto test pads located on the top of the chip. All values are in mV/ns.

4.3 Differential Nonlinearity (DNL)

Since the ADC for the SVX4 version B is new, we wanted to measure the DNL or the asymmetry between the amount of charge that is necessary to flip the least significant bit from 0→1 to 1→0. In Figure 21, we see a picture of the sine wave voltage that was used in the study. In Figure 22, we see the output from the ADC for the sine wave connected to V cal.

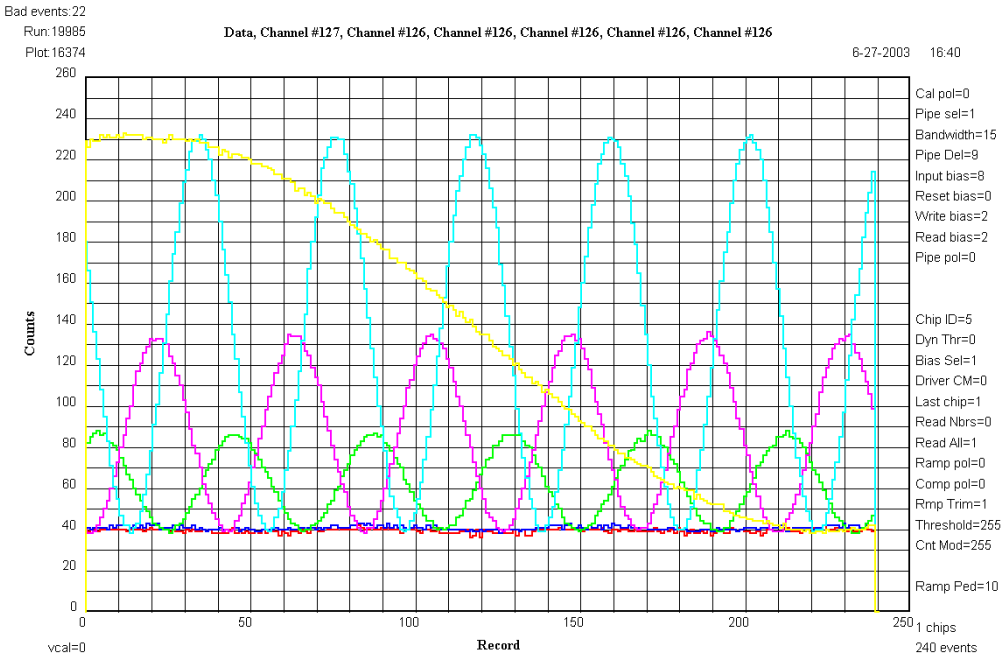

Figure 21 Pedestals as a function of record number which corresponds to time. The sine wave is clearly evident. We plot the variation of the pedestal for four different frequencies. The offset of the sine wave is set so that the lowest value corresponds to the pedestal.

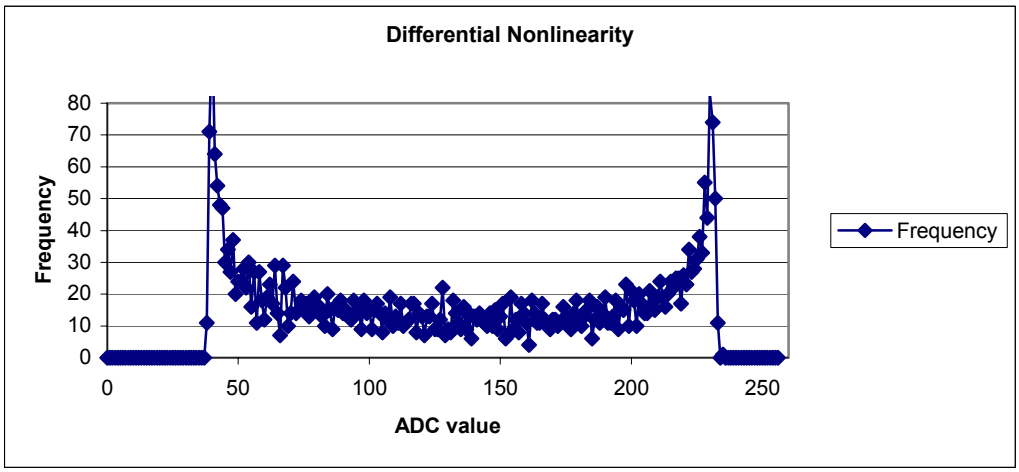

Figure 22 Frequency of ADC output for an input sine wave connected to V cal. The shape of this wave corresponds to the probability for having a specific voltage output from the sine wave.

In Figure 23, we see an expanded region of Figure 22 that is used to estimate the DNL for the SVX4. Adding up all the even bin contributions and odd bin contributions and calculating the normalized difference gives an estimate of the DNL.

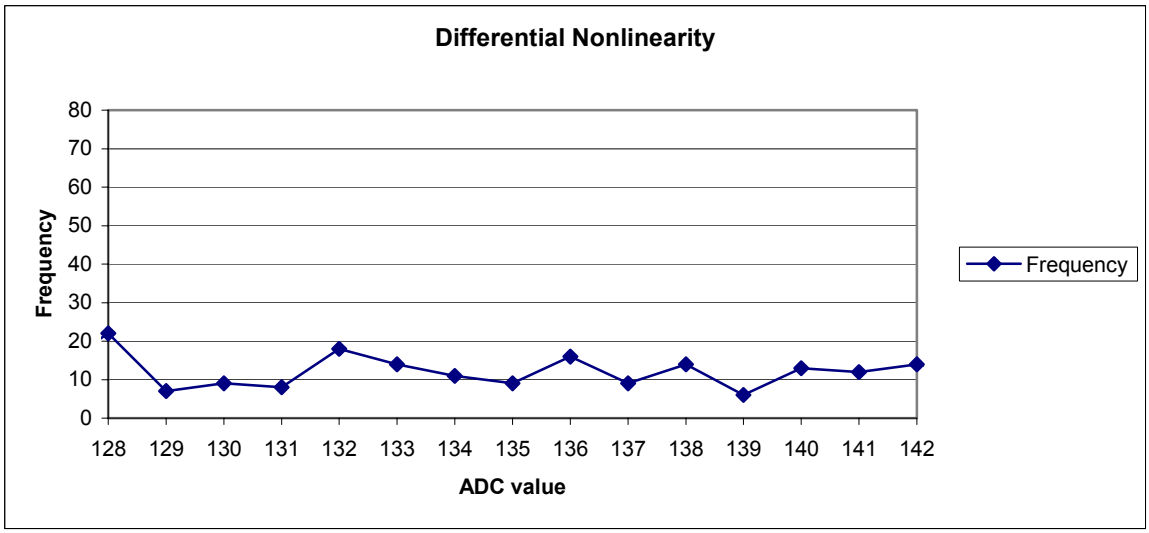

Figure 23 Expanded region of the DNL frequency plot that was used to estimate the DNL. No even-odd effect is seen even though the estimate of the DNL is 24%.

We calculated a DNL of 24%. Though this is a large value we do not see an even-odd effect when we examine the data. A more precise measurement of the DNL has been made on a DØ two chip hybrid with the clocks well tuned has produced a value of the DNL on the order of 5%. Though we have measured a DNL of 24% the specification is smaller than 50% (<0.5LSB), so our measurement shows the ADC satisfies this requirement. Note that we did not tune the clocks to produce the best value for the DNL, but only did a rough measurement to confirm that there are no gross defects in the ADC.

4.4 Integral Linearity

The opposite of the DNL is the integral linearity. We examined the linearity for individual unbonded channels. In Figure 24 and Figure 25, we show the linearity for a single channel of the SVX4 and the residuals or deviation from linearity for this channel. These plots show that the nonlinearity is less than 1%. We did not use a value of 0 mV in the fit because it appears that the V cal circuitry has a slight offset due to the internal V cal circuitry. Assuming an input capacitance of 25fF, the SVX4 is linear up to injected values of the charge of 62.5 fC. This sets a upper lower limit on the pipeline dynamic range which is expected to be on the order of 60 fC.

In Figure 26, we see the linearity and residuals from the PATT03 test stand. The top histogram shows the ADC output as a function of the input voltage or V cal along with the linear fit to the data. The bottom histogram shows the deviation or residuals of the data from the linear fit. For the PATT03 test stand, the deviation is less than 0.4%. Using the measured gain of 1288 electrons/ADC (= 729e × 53MHz/30MHz), it was

determined that the injection capacitor is C=26.7fF (= 129.6 ADC/V × 1288 e/ADC × 1.6E-19 C/e).

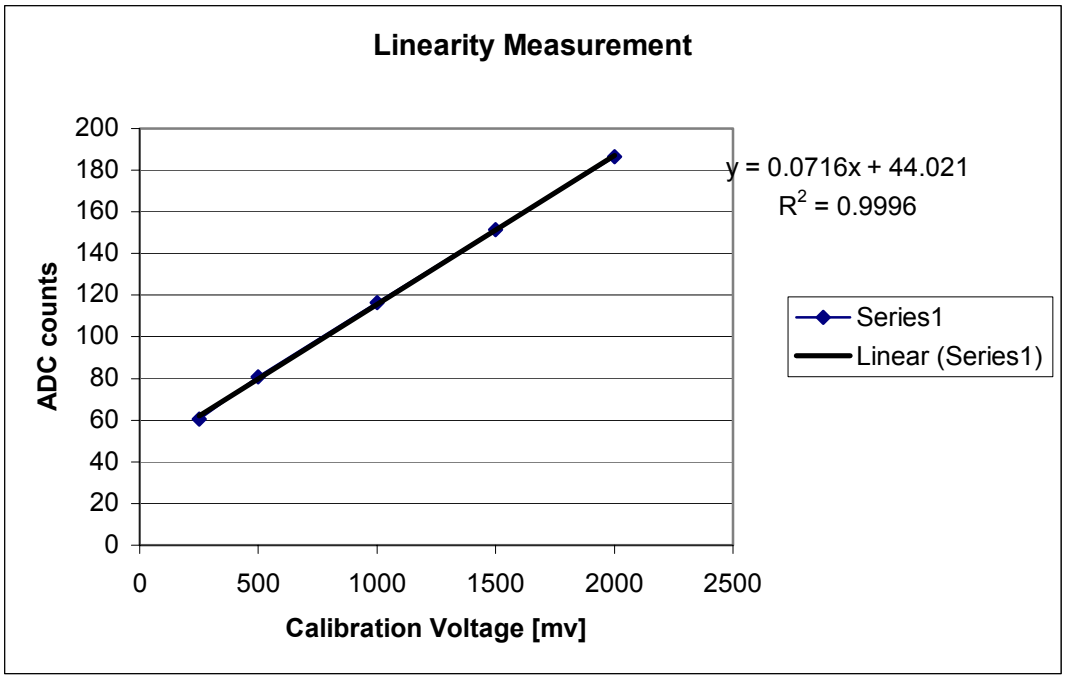

Figure 24 Linearity of a single unbonded channel. Also shown is the linear fit to the data.

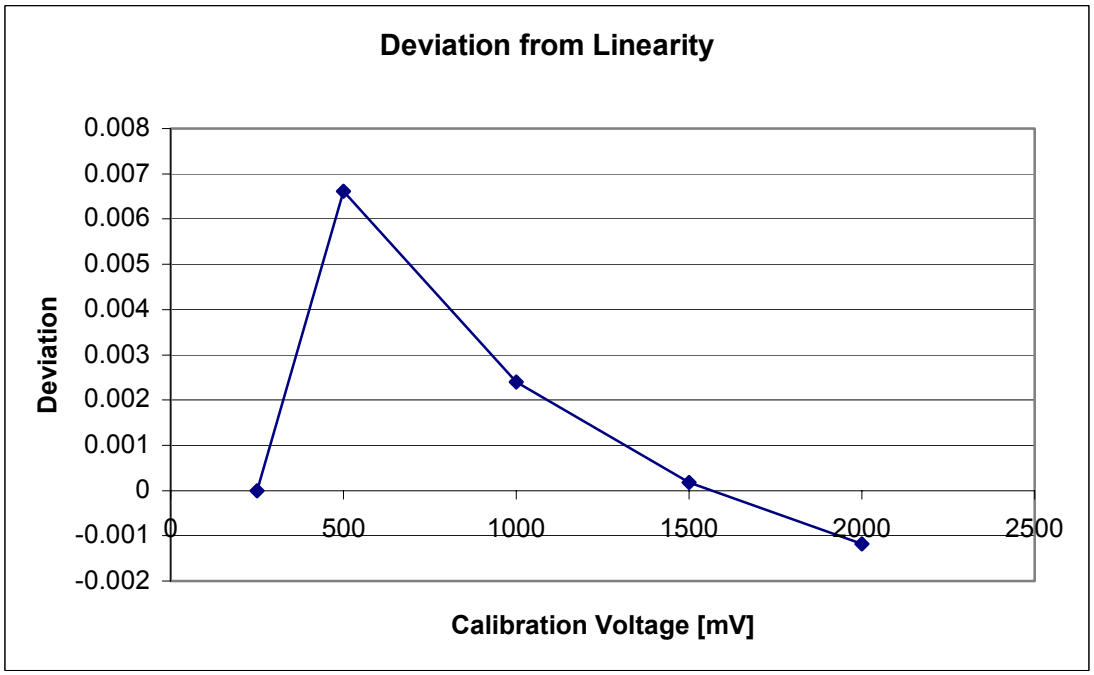

Figure 25 Deviations from linearity for charge injection into a single channel.

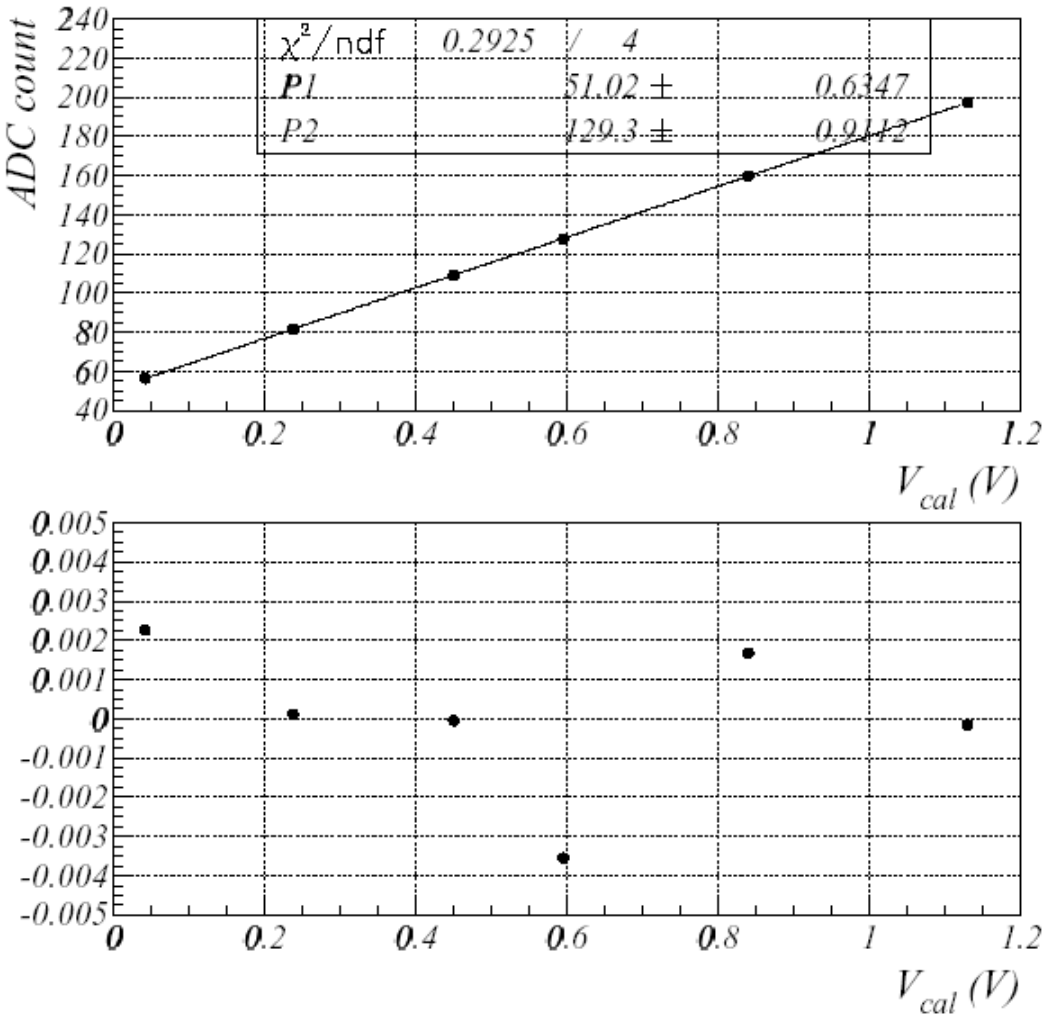

Figure 26 Linearity and residuals for the SVX4 using the PATT03 test stand. The top plot shows the ADC output as a function of the input voltage on V cal. The bottom plot shows the deviation from the fit obtained in the upper histogram. This shows that the deviation is less than 0.4%. This data has been converted from 30 MHz to 53 MHz.

4.5 Margins of Frequency and Duty Cycle in Digitize

We also measured the frequency and duty cycle margins of the SVX4 version B in the digitize cycle on the Stimulus Test Stand. In Figure 27, we show the pedestal as a function of digitization frequency. We see the expected linear as a function of frequency. We found the chip to be operational in the frequency range of 30-60 MHz for all duty cycle values between 30-60%.

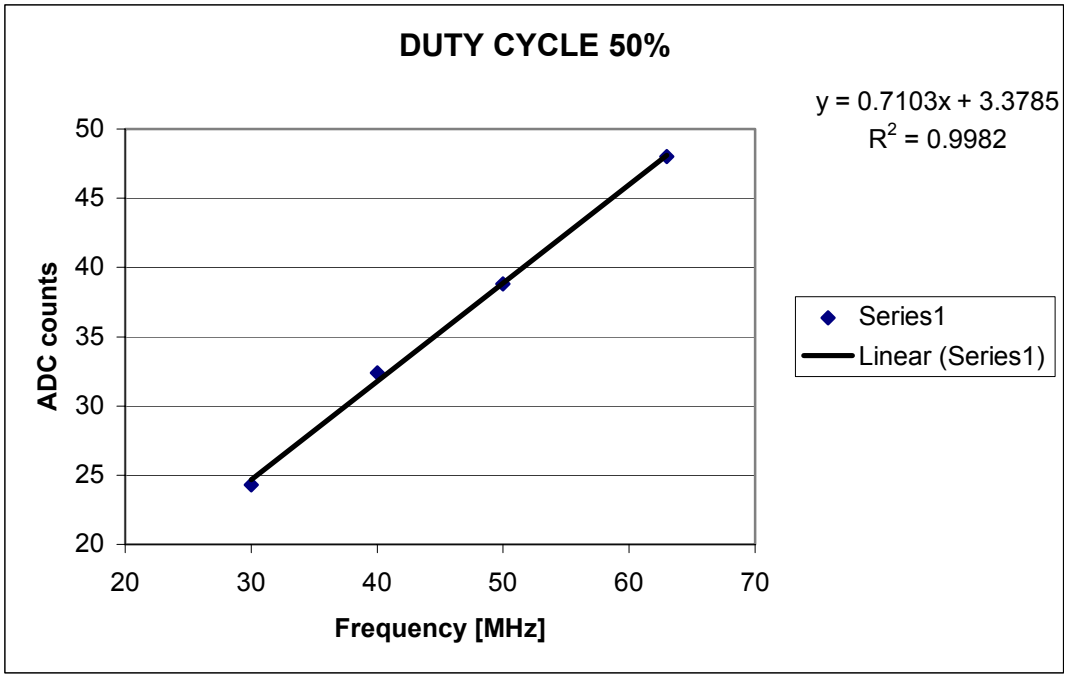

Figure 27 Pedestal as a function of the digitization frequency. The data were taken using a Ramp Pedestal setting of 10 and a Ramp Range setting of 0.

5 Miscellaneous

5.1 DØ Control Pattern

The first versions of the SVX4 had a design feature in the DØ mode: the front-end clock was not gated during digitize. This design feature did not allow the SVX4 chip in DØ mode to place the pipeline cells onto the read amplifier for digitization. This was corrected in the latest version of the SVX4 version A and B where the front-end clock is gated in all modes except readout. We choose to only test version B because it has the newly designed ADC. Note that we did these studies at the nominal AVDD=DVDD=2.5V unless otherwise stated. The latest versions of the chip have a new length of bits in the shift register (192 bits). These bits were the first thing to be confirmed in the latest testing.

In Figure 28, we see the newest DØ mode pattern for the SVX4. This pattern is downloaded to the chip and is functional. In Figure 29, we see the output from the logic analyzer connected to the Stimulus System. It is obvious from the output that the chip is operating normally with the new pattern because the readout of the chip contains the experimental data.

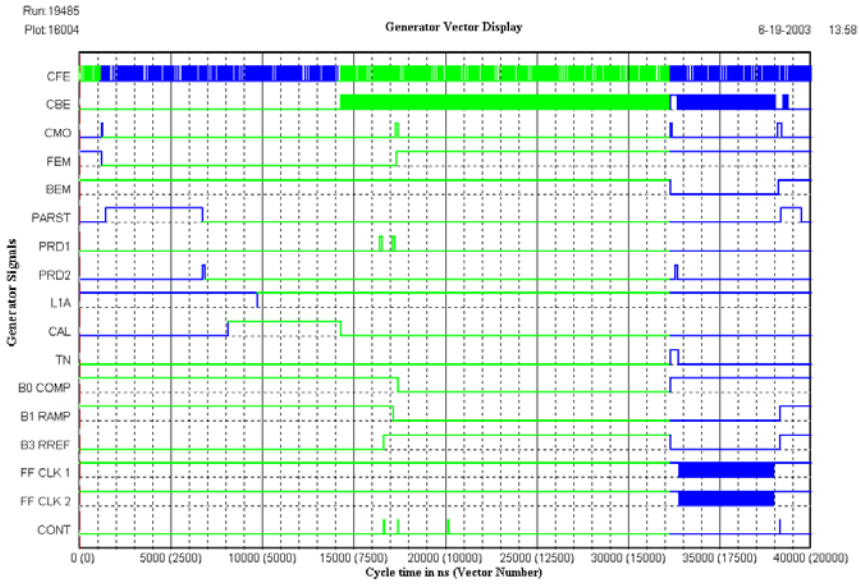

Figure 28 The new DØ mode pattern for the SVX4. This pattern has been confirmed to be functional in DØ mode.

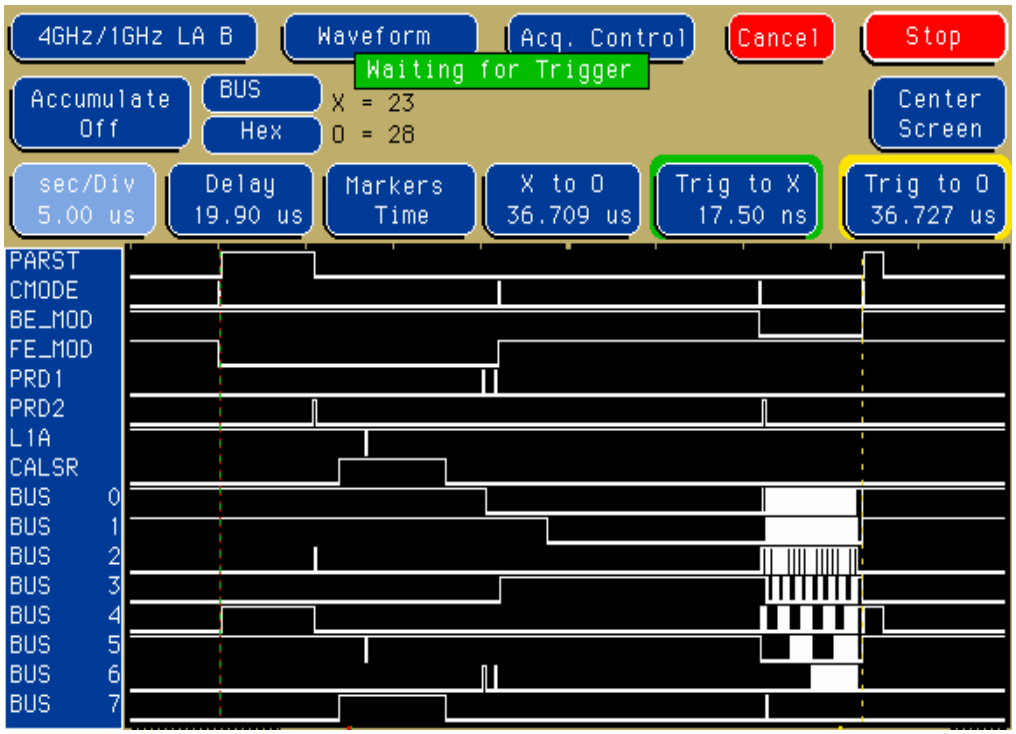

Figure 29 The output from the logic analyzer while in DØ mode. It is clear from the readout that the new control pattern in functional.

5.2 Studies of Voltage Margins Using Integral Linearity

We confirmed the operating voltage range for the SVX4 chip by examining the linearity for different voltage configurations. In Figure 30, we see the linearity for several different voltage configurations. By examining the differences between equal steps in voltage, we confirmed that the SVX4 is linear for the following configurations:

AVDD=DVDD=2.75 V; AVDD=DVDD=2.5 V; AVDD=DVDD=2.25 V; and |AVDD-DVDD|= 0.5 V. The voltage margins for the SVX4 are 2.25 - 2.75 V for both AVDD and DVDD.

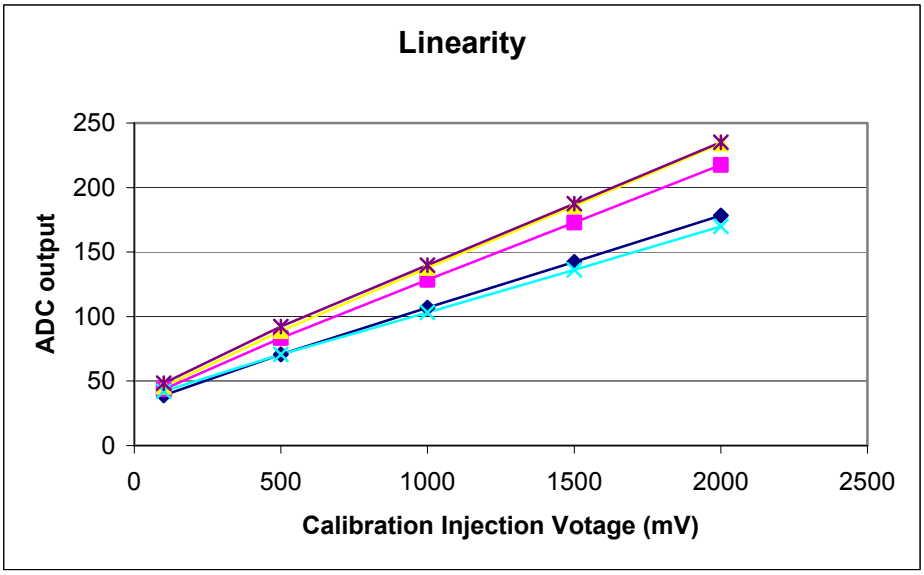

Figure 30 Linearity plots for different values of the supply voltages. The dark blue line is for AVDD=DVDD=2.75 V. The pink line is for AVDD=DVDD=2.25 V. The yellow line is for AVDD=DVDD=2.25 V. The brown line is for AVDD-DVDD=0.5 V and the sky blue line is for DVDD-AVDD=0.5 V. The chip remains lineariy within the required operating range of 2.25-2.75 V for both AVDD and DVDD.

5.3 Dynamical Pedestal Subtraction

Due to the changes in the ADC, the DPS circuitry was also modified. In Figure 31, we show the number of channels needed at pedestal for the DPS circuitry to function properly. We measured V_{th} directly and found a value of V_{th}=1.61 V when the design value is 1.9V.

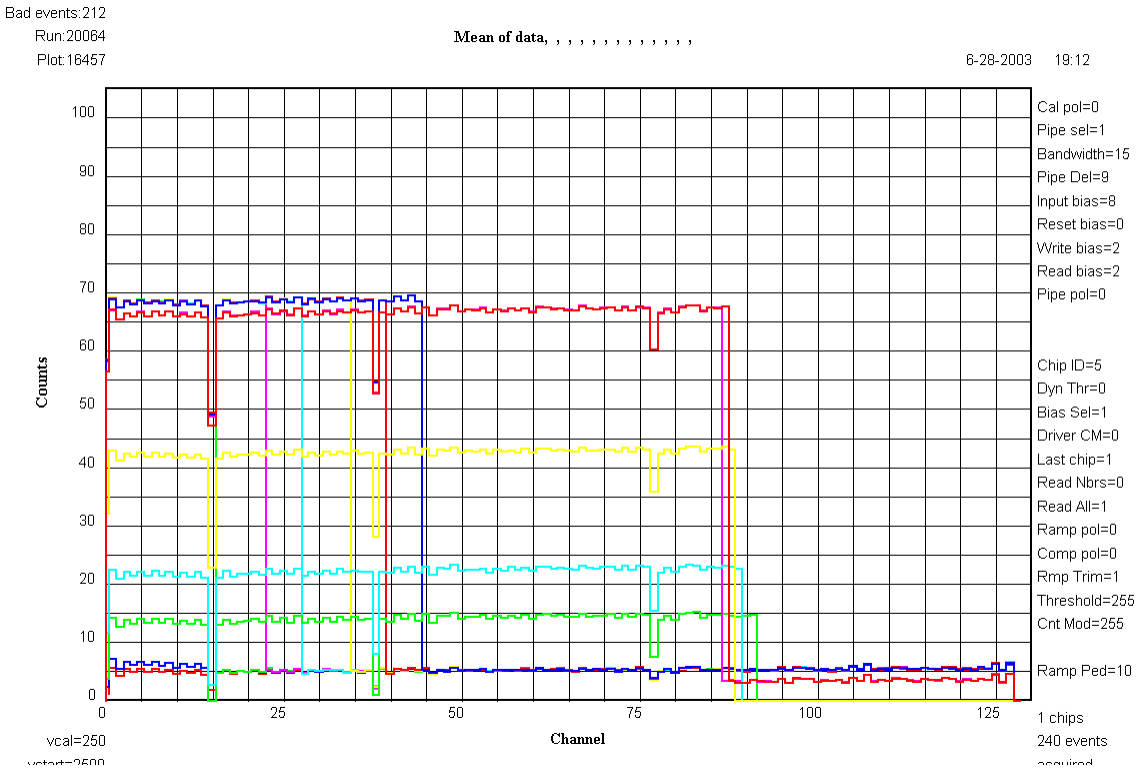

Figure 31 Pedestal values as a function of the number of channels with charge injection with DPS on. The blue line corresponds to 45 channels injected with charge. The red line corresponds to 88 channels injected with charge. The yellow corresponds to 89 channels injected with charge. It can be seen that the gain begins to drop which then shows how many channels are needed at pedestal for the DPS circuitry to work properly (128-88=40). The light blue and light green correspond to 90 and 91 channels at pedestal, i.e. no charged injected.

We have found that 40 channels at pedestal are required for proper operation of the chip with DPS on with the default value of the DPS resistance of V_{Th} = 19 kΩ. In Figure 32, we show the number of channels needed at pedestal as a function of the external resistance. In Figure 33, we show the relative gain and noise as a function of the external resistance. Again, we are only examining a few values in order to observe the overall behavior and not map out the entire range.

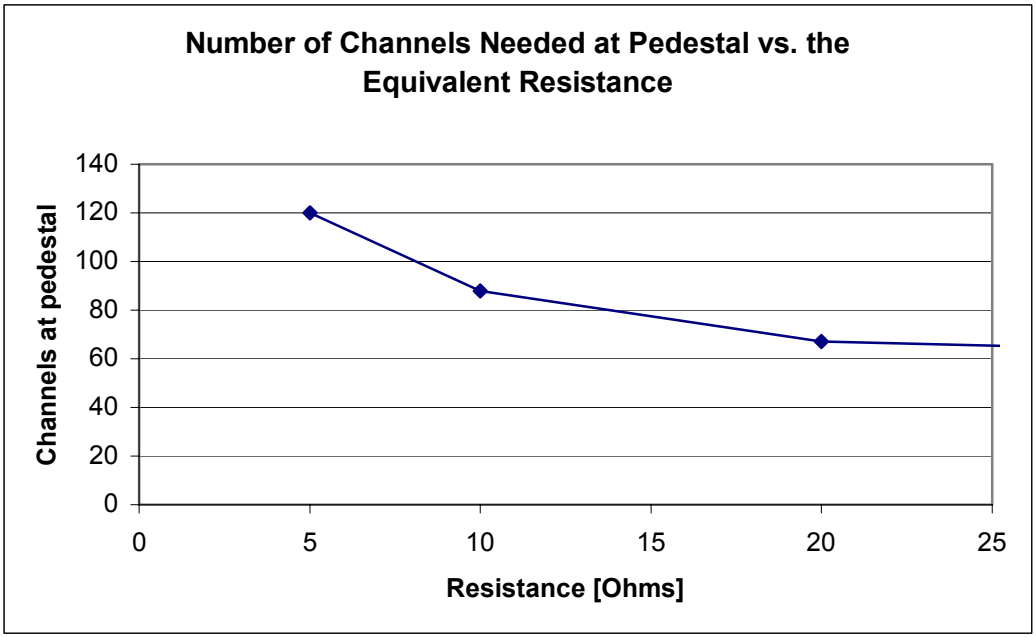

Figure 32 Number of channels needed at pedestal as a function of the external resistance in order for the DPS circuitry to work properly.

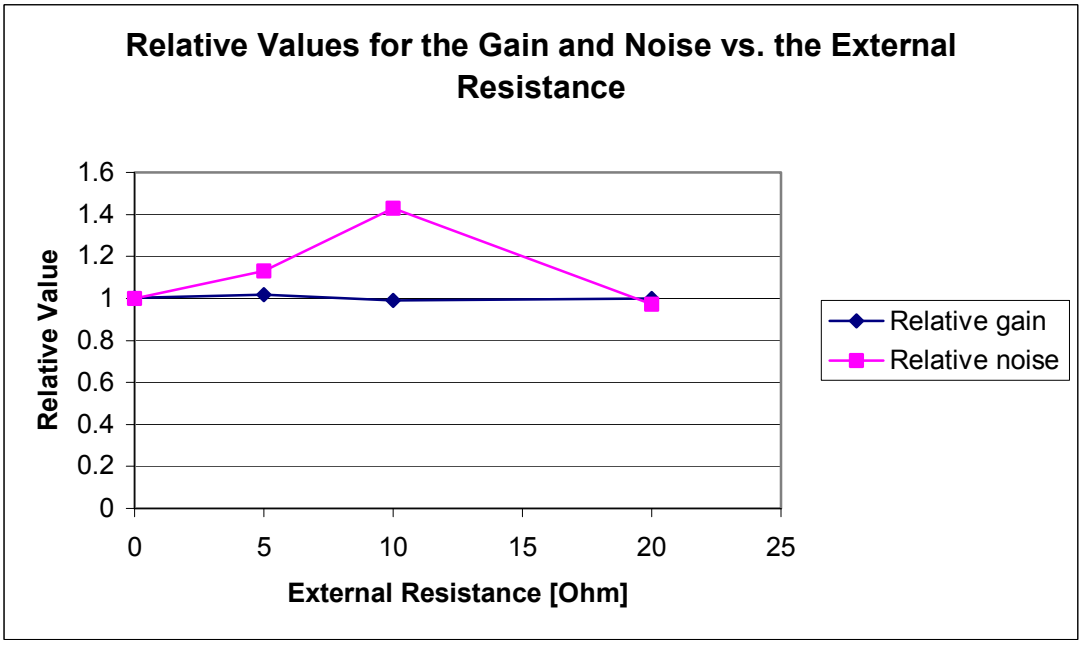

Figure 33 Relative gain and noise as a function of the external resistance.

5.4 Margins of Frequency and Duty Cycle in Readout

We also measured the frequency and duty cycle margins of the SVX4 version B in the readout cycle on the Stimulus test stand. We found the chip is operational in the frequency range of 15-50 MHz for all duty cycle values between 30-70%.

5.5 I_{qui} and Output Drivers

In the earlier versions of the SVX4, the width of the ground line connected to the output drivers resistors was too thin and developed a significant resistance therefore changing the bias voltage of each output driver. For small variations of the I quiescent current, the output drivers stopped functioning. In version B, the width of the ground line was increased to remove this effect. In Figure 34, we show the output from the SVX4 with charge injection on every 10^{th} channel for five different values of the I quiescent current. It is evident that the chip continues to function for large variations of the I quiescent current.

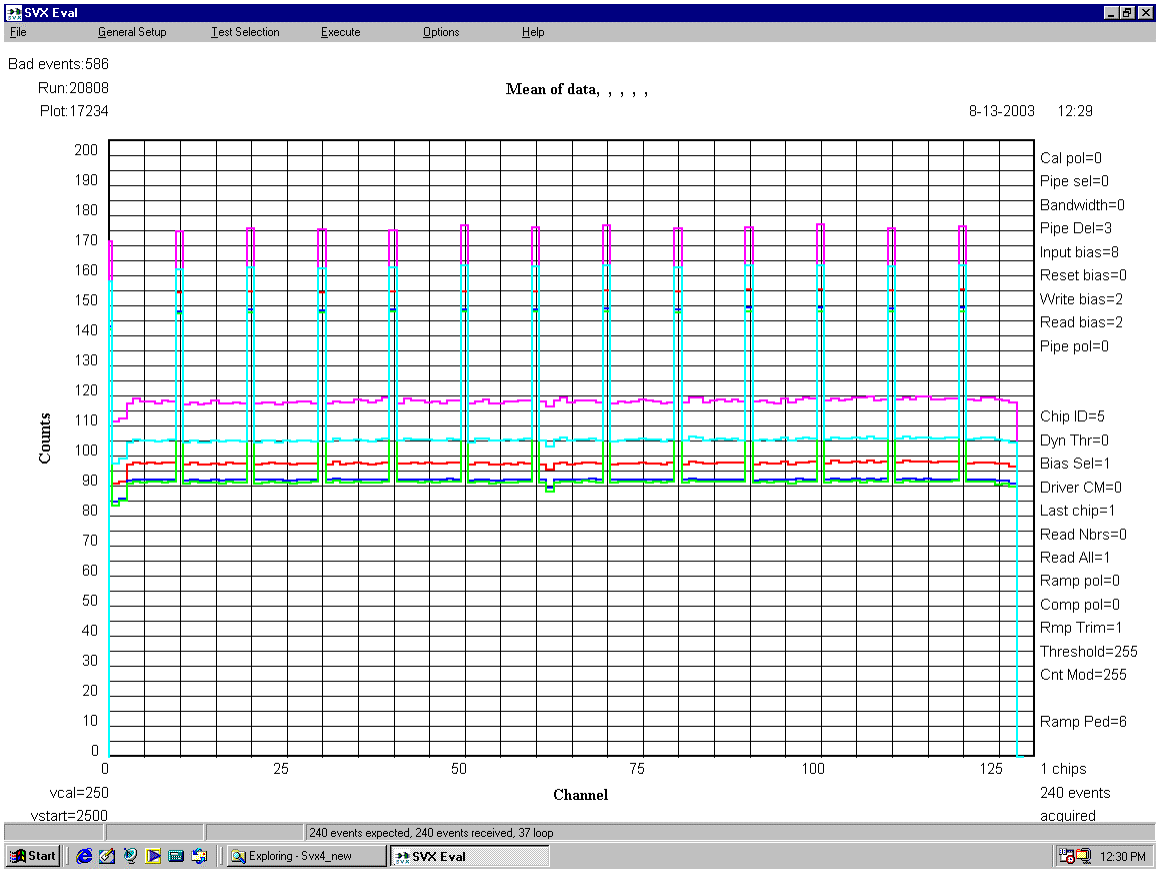

Figure 34 Output from the SVX4 for five different values of I quiescient. The red line is for the nominal value of external resistance of 7.7 kΩ connected to AVDD giving a nominal current I=249μA. The light green line corresponds to a value of I/3. The blue line corresponds to a value of I/2. The light blue line corresponds to a value of 2I and the pink line corresponds to a value of 3I.

6 Conclusions

We have tested the SVX4 Version A/B and have confirmed that all modifications are working well. After analysis of all tests, we are confident that the SVX4 version B satisfies all requirements for full production.

[1] L. Christofek *et al.,* DØ Note 4250.
[2] L. Christofek *et al.,* DØ Note 4252.
[3] L. Christofek *et al.*, DØ Note 4249.