Fermi National Accelerator Laboratory

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SVX3 Six Inch Wafer Failure Report*

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Summary

In 1997 an order was placed with Honeywell for 265 four inch SVX3 wafers. One hundred 4 inch wafers were received by Fermilab in the summer of 1998. After the initial delivery, the processing line at Honeywell was switched to 6 inch wafers. Fermilab changed the balance of its order to 72 six inch wafers. Because scratches occurred on many of the 6 inch wafers during processing, 75 SVX3 wafers were delivered to Fermilab. The wafers came from 5 different lots. Upon receipt of the wafers, Fermilab began to immediately test the 6 inch wafers using the same automated test system and procedure that was used on the 4 inch wafers. It was quickly apparent that there were serious problems on the 6 inch wafers which were not seen on the 4 inch wafers. Honeywell was officially notified of the problem on January 6, 1999.

Beginning in January, a serious effort was begun by Fermilab and LBNL (Lawrence Berkeley National Laboratories) personnel to understand the nature of the problem. Honeywell was continuously updated on the work being done with letters, faxes, email, and phone conversations.

Two related yield issues have been uncovered thus far. The yield on two of the five lots is essentially zero. Two other lots have a large yield hole in the center of the wafer. The mechanism causing the yield hole in the center of wafers is the dominant cause of the failures on the zero yielding lots. It simply appears that the yield hole has grown to 6 inches on the zero yield wafers. The problem with chips has been traced to bad M2-M3 vias. Many of the vias on a chip have a high resistance (in the megohms). The high resistance has been shown to cause high pedestal offsets in the analog pipeline resulting in performance failure. There is other evidence that bad M2-M3 vias are also causing failures in the digital shift register that is used to initially program the SVX3. The tests which have been completed indicate a processing problem on the 6 inch wafers which was not present on the 4 inch wafers.

Wafers from one of the 6 inch lots generally have a high yield and do not exhibit the center of the wafer via problem. Unfortunately all of the wafers from that lot have numerous scratches which cause overcurrent chip failures. Five of the 7 wafers tested from the lot appear to be good except for the scratched dice.

The long term reliability of "good" dice which come from wafers that have bad M2-M3 vias is in question. It is not known if bad vias will recover or good vias go bad with time, temperature and radiation. It has been found that annealing a wafer at 400 °C for 40 minutes decreases the yield on the wafer. This might suggest that a high operating temperature over a period of time may result in other failures.

Testing Approach

Tests to understand the nature of the problem on the 6 inch wafers were done at LBNL and Fermilab. Wafer level testing was done at LBNL and chip level testing was done at

Fermilab. Approximately 5 man-months and $20,000 of outside failure analysis work have been spent on the problem.

All of the 4 inch and 6 inch wafers received from Honeywell were sent to LBNL for wafer level testing on an automated probe station. Dies which pass all the tests are "good". Dies in which all failures are constrained to a single channel and/or a small number (<= 30) of randomly distributed pipeline capacitors are "fair". The "randomly distributed" in the above sentence means that no pipeline cell number can have more than 10 bad pipeline capacitors (out of 128 each cell has) and no good channel can have more than 4 bad pipeline capacitors (out of 46). All dies which are not "good" or "fair" are classified as "bad".

The following is a list of wafer probing tests performed at LBL with some rudimentary description. Tests 1-4 are the most pertinent for this report.

1. AVDD and DVDD CURRENTS. After chip power-up we immediately check that there are no shorts inside the chip. In that case either AVDD or DVDD current can go up to the current limit of their corresponding supplies. We set both limits at 200 mA. If one or both currents hit this limit the die is classified as bad, and the test sequence for this die is aborted. The currents are also checked after some reasonable initialization and acquisition patterns have been run. The AVDD current depends on the preamp current settings. With the settings used for our tests, we reject chips if the AVDD current is below 55 mA or above 110 mA. Due to limitations of our setup, we can not measure the DVDD current while the chip is being read out (it is a tricky measurement because the readout time is short, and the current flows predominantly through the DVDD bypass capacitor). Instead, the DVDD current is measured when the chip just sits there, doing nothing. The chips are rejected if this current is below 4 mA or above 50 mA.
2. SERIAL LINE FUNCTIONALITY. Various sequences of 0s and 1s are sent to the chip shift register in the initialization mode. We check that whatever is sent on the top neighbor line shows up on the bottom neighbor line with the delay equal to the shift register depth. The dies which fail this test are immediately classified as bad and no further tests are performed on them.
3. BASIC READOUT FUNCTIONALITY and CHIP ID. A simple acquire-digitize-readout
   pattern is run with trigger in a known place. The readout stream is checked for errors in chip ids, cell ids, and channel numbers. Several chip ID settings are tried in order to make sure that there are no ID bits or readout bus bits which are stuck at 0 or 1. The dies which fail this test are also classified as bad immediately.
4. PEDESTALS and NOISE. Pedestals and noise are measured for all pipeline capacitors in the chip. This measurement is performed for two different preamp-pipeline polarity settings. The pedestal and the gain adjustment settings are fixed, as well as the pipeline depth. Pipeline capacitors and/or channels are marked as bad if pedestal, noise, or pedestal variations are out of limits. We want to accommodate die-to-die and wafer-to-wafer variations but to reject the chips which have too much noise and/or pedestal non-uniformity. The limit values are selected as a reasonable compromise between these two requirements, with the emphasis rather on allowing good dies to pass than on making bad dies to fail. As such, the noise limit is set to 5 ADC counts which for our clock and ramp resistor settings corresponds to about 5000 electrons. In the wafer testing setup we can not bypass the chips very well because the contacts are made through rather long probe card needles which have non-negligible inductance, and we have to average positive and negative polarity pedestals in order to cancel pedestal shifts produced by the trigger signal. This averaged pedestal has to be between 20 and 45 ADC counts (typical value for good chips is 30 counts with the RMS noise of about 1.3 counts).

5. CALIBRATION MASK. All calibration mask bits are set and calibration charge is injected into all channels simultaneously during the usual acquire-digitize-readout sequence. This is done for two different values of calibration voltage. In such way we can determine if the calibration works for every channel and can get a crude idea about the chip gain. The channels which do not appear to be sensitive to the calibration injection are marked as bad.
6. CHIP ADC LIMITS. During digitization, the ramp is kept at reset. As a result, the comparators which normally latch the ADC counter values never fire, and every channel should latch the value of "counter modulo" instead ("counter modulo"+-1 is also allowed). We go through various "counter modulo" settings and check that there are no bits stuck at 1 or 0 on any of the ADC latches.
7. PEDESTAL ADJUSTMENT. Ramp pedestal settings are stepped from 0 to 15 and the pedestals are measured for several channels with and without charge injection. This test is performed for two different polarity settings. For each die and for each pedestal settings, a median pedestal value is calculated over several selected channels. This value is compared to the median value over the whole wafer (known bad chips excluded). The difference between the chip median and the wafer median should be not more than 30 ADC counts and not less than -15 ADC counts for each pedestal setting. The assumption is, of course, that there are more than 50% of good chips in the sample remaining after removal of obviously bad dies.
8. DYNAMIC COMMON MODE SUPPRESSION. The number of channels with charge injection is changed (by changing calibration mask bits) within the range from about 30 to about 110, while chip is operating with common mode noise suppression turned on. We look at the average pedestal for several control channels. For these control channels the charge injection is always on. When the number of channels with charge injection becomes large, the common mode noise suppression circuit stops working (it is tricked into thinking that the charge injection IS the common mode noise), and it suppresses the control channels. We check when it happens and compare with what we expect for good dies.
9. GAIN. Chip gain is measured by changing calibration voltage in 50 mV steps so that it covers the whole dynamic range of the ADC. The gain is measured for all channels in a single pipeline cell and for all pipeline cells in a single channel. However, when the measurement is performed for all channels, charge is not injected into every channel (we think that the combined capacitance that has to be driven by the calibration voltage line is too large in this case). Instead, the charge is injected into every 10^{th} channel and the measurement is performed 10 times with different calibration mask settings. We require that the gain is between 165 and 330 ADC counts per 1 Volt of the calibration injection voltage (typical good die gain is about 240 ADC counts / 1 V Vcal).
10. PIPELINE DELAY. Pipeline delay is checked for every setting from 1 to 42. The position of the trigger in the pattern is known, and the cell id which comes out is compared with the expected cell id.
11. SPARSIFICATION. Sparsification performance is checked in both "single channel" and "read neighbor" modes, with and without last chip flag. The sparsification threshold is set half-way between the pedestal level and the calibration signal level. The channels which come out are compared with the list of expected channels for several different calibration mask settings.
12. SPARSIFICATION THRESHOLD SCAN. Sparsification threshold is varied for about 20 counts above and below pedestal, and the number of channels which come out is recorded. The result should look like an S-curve. The location of the steepest part of that curve should coincide with the pedestal, and the width should be approximately equal to the chip noise.
13. BOTTOM NEIGHBOR. Transitions on the bottom neighbor line are monitored during digitization and readout in order to make sure that the neighbor logic and the priority passing work.

14. DATA VALID. We do not use data valid to write the chip data in our setup, so we check separately that it behaves as expected during readout.
15. GAIN ADJUSTMENT. The gain adjustment settings are varied from 0 to 255 with step of 10. As a result, the ramp rate and the observed pedestal should change accordingly. Note that we would probably like to start the SVX detector operation with some large value of gain adjustment and then gradually step down because the chip gain increases with accumulated dose.
16. MULTIHIT OPERATION. So far, all the above tests have been done in SVXII mode. In this test we inject 4 triggers first and then perform digitization and readout 4 times. The obtained cell ids are compared with the expected cell ids. We also require that the observed pedestal values from all triggers are between 18 and 55 ADC counts, and that the difference between different triggers is not more than 22 ADC counts.
17. DEADTIMELESS PERFORMANCE. An acquire-digitize-readout pattern is run, and another trigger is inserted into it in various places. This pattern is followed by a digitize-readout sequence for this second trigger. The obtained cell ids are compared with the expected cell ids. The original idea of this test was to look also at pedestals and noise. However, these data turned out to be unreliable during digitization or readout due to the lack of appropriate bypassing.

Data integrity is checked in each test for every readout. This means that chip id, cell id, and channel numbers should come out right every time. For every test we perform not just a single acquisition, but a number of them. The number of acquisitions varies from 5 to 50, depending on the test length and complexity. The setup runs at 30 MHz, and the ramp reference resistor is 100K.

The above tests are performed sequentially. If a chip fails tests #1, 2 or 3, the chip is unusable, the failure is recorded and the test is stopped.

Tests at Fermilab were conducted on mounted individual chips which were identified as bad chips from the wafer testing at LBNL. The testing at LBNL identified which of the 128 channels on a chip were bad and which of the 46 cells within a channel were bad. That information was used at Fermilab to probe some test pads already on the chip with a Picoprobe. Many other pads, however, had to be added to numerous chips using a Focused Ion beam (FIB). The high density of the circuitry on the SVX3 made adding pads to various points very difficult.

Wafer Level Testing

Honeywell told Fermilab that there would be 140 dice per 6 inch wafer. Lot #8 has 140 dice per wafer. Wafers from all remaining lots have 134 dice per wafer (58 wafers). The change was made without informing Fermilab. The change was apparently made to allow Honeywell the option of using two different steppers. Unfortunately, that means that Fermilab received 348 less dice (58 x 6) or about 2.5 wafers less than originally expected.

Over twenty of the 6 inch SVX3 wafers have been tested at LBNL. Yields for each of the wafers are shown on Wafer Quality Maps in Appendix A. There is a wide variation in yield between lots as shown in the following list:

Lot	Wafer	Good die %	Good + fair die %	Scratched die	Unscratched good die %
8	1	55.0	63.6	18	61.5%
8	3	12.9	25.0	8	13.6
8	4	61.4	70.7	18	70.5
8	6	56.4	67.1	18	64.7
8	11	37.1	53.6	17	42.2

8	15	60.0	68.6	17	63.1
8	17	32.9	57.1	17	37.4
9	2	39.6	54.5		
9	3	30.6	47.8		
9	5	61.2	69.4		
10	1	0.7	2.2	3	---
10	2	0.0	0.0	2	---
10	8	1.5	3.0		
10	10	0.0	1.5	4	---
10	18	3.7	11.2	1	---
11	3	0.0	0.7	12	---
11	5	0.7	0.7	7	---
11	11	0.0	1.5	4	---
11	18	3.0	7.5	7	---
11	20	0.0	0.7	21	---
12	4	44.8	55.2		
12	11	38.1	47.0		
12	12	44.0	58.2		
12	15	38.1	49.3		

The wafers from lot #8 generally have good yield. The predominant failure mode is overcurrent/undercurrent which occurs on nearly every scratched die. There is a random distribution of other failures that are probably due to various defects. Wafer #3 has a very bad yield and wafer #17 has a "yield hole" in the center of the wafer.

Wafers from lots #10 and #11 have essentially zero yield. Although there are a few scratches on these wafers, the scratches do not significantly affect the overall yield. It will be shown later that using other quality measurements, lot #11 is probably worse than lot #10.

Wafers from lots #9 and #12 have a moderately good yield. However, all of the tested wafers have a significant "yield hole" in the center of the wafer except for one wafer (lot #12, wafer #12). The large variation in yield across a wafer is very unusual. The zero yield in the center of the wafer is contrary to a normal yield pattern where the yield is high in the center and drops as the dice get close to the wafer edge.

Because of the low and unusual yield patterns for lots #9 - #12, the test data was examined to determine the predominant cause of failed chips. It was quickly apparent that most chips were rejected due to Test #4, the Pedestal Test. Results of the Pedestal Tests for all wafers are shown on Capacitor Quality Maps presented in Appendix B.

A large portion of the SVX3 chip is comprised of an array of capacitors. The array has 128 channels with 46 capacitors in each channel for a total of 5888 capacitors . The capacitors are used to form 128 analog delay lines. Each capacitor stores a sample voltage which is read out at a later time. For no input signal, the signal level (pedestal) on each capacitor of a good chip is essentially the same. On a bad chip, the pedestal voltages vary dramatically. Random bad cells in the array are shown in black while bad cells in a bad channel are shown in red on the plots in Appendix B. It is shown later that the cause of many of the bad channels is probably the same as the random bad cells.

The Capacitor Quality Maps for lots #9 and #12 show a higher number of bad pedestals in the center of the wafer and the number of bad pedestals approaching zero as the die gets closer to the edge of the wafer. Thus there is a "yield hole" in the center of the wafer. For lot #10 the same pattern can be seen. The difference is that the "yield hole" has grown to the diameter of the wafer resulting in essentially zero yield. Lot #11 is just as bad as lot #10 except that the dice in the center of the wafers have failed an additional test. This is indicated by the "No inf." dice. Dice that fail tests 1-3 are rejected immediately and test #4 is never performed resulting in "No inf.". It turns out that the cause of the second yield hole inside the pedestal yield hole is also probably the same as the pedestal yield problem.

To help further examine the failure modes and in particular the failures in the center of the wafers from Lot #11, plots of "Types of Die Failures " were made for all the tested wafers. See Appendix C. The plots for lot #11 show that a significant number of dice in the center of each wafer have failed Test #2, the Serial Line Functionality test. Before the SVX3 can be operated, a long serial bit pattern of 1's and 0's must be downloaded to program the chip. If the shift register does not work, the chip fails the Serial Line test and the chip is declared DOA. As mentioned, the Serial Line failure and Pedestal Failures can be explained by the same mechanism.

Although the wafer test data is helpful, it can not by itself pin down the source of the problem. It was decided to focus on a failure mode that might be easily analyzed on the bench with other diagnostic equipment. The easiest fault to study is the random pedestal fault which appears on some of the 5888 cells on an SVX3 chip. Random Bad Cell Maps are shown in Appendix D for all the wafers. It is readily apparent that all the wafers from lots 10 and 11 have very large numbers of random faults. Wafers from lots 9 and 12 have smaller numbers of random faults. Several chips from lot 9 were selected for study on the bench so that both good and bad cells could be easily examined.

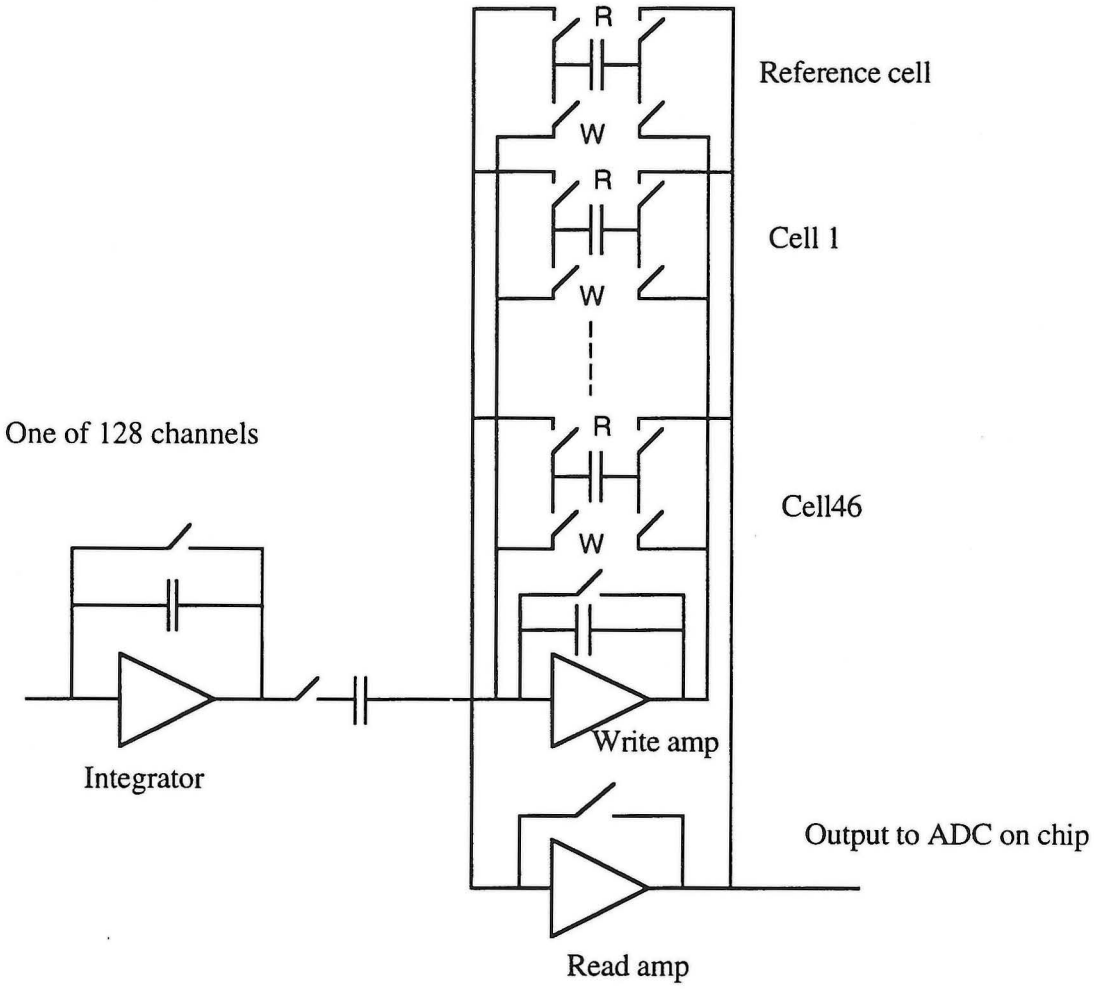
Chip Level Testing

Wafer #2 from lot 9 was diced and chips with random pedestal failures selected for board testing. Individual dice were wirebonded to a test board. After initializing the chip using the serial shift register, operation of the pipeline was studied using existing test points. Additional test points were then added to the chips using Focused Ion Beam (FIB) Techniques and further studies done using a digital oscilloscope and semiconductor analyzer. It was the chip level testing which uncovered the M2-M3 via problem.

A brief explanation of the section of the chip causing the pedestal problems is necessary. Each SVX3 chip has 128 identical channels each with a 46 cell deep analog pipeline as shown below. There is an extra pipeline storage cell in each channel which is used as a reference cell for pedestal subtraction. The output of the integrator is fed to the pipeline. The difference between when a cell is written and when it is read provides a delay which is typically about 4 usecs. The pipeline is dual ported and has separate write and read amplifiers for simultaneous write and read operation. Each storage cell has 2 NMOS write switches and 2 NMOS read switches. The storage capacitor (200 fF) is formed from Poly-M1-M2. Writing to a cell is performed by switching its capacitor into the write amplifier feedback loop, quickly resetting it before the arrival of the signal from the integrator, and then switching it out after the signal has settled. Reading the cell is performed by switching the desired capacitor into the feedback loop of the read amplifier.

With no input to the channel, ideally zero charge is stored on each cell in the pipeline and then read out a few microseconds later via the on chip ADCs. The value read out is called the pedestal. On a good chip, the pedestals are uniform from cell to cell and channel to

channel with a value of about 30 counts. On a bad chip the pedestals have a very large variation. The pedestals can be either higher or lower than the nominal value. Plots are shown in Appendix E for good, fair and bad chips.



Simplified Schematic of One Pipeline Channel

The SVX3 chip was built with test pads at the output of the read amplifier. By looking at the Read Amplifier output with a Picoprobe, it was clear that there was a problem with the readout cycle on many chips. In order to more clearly see the problem, the read amplifier was run slowly, first putting the reference cell capacitor into the feedback loop and then a "bad cell" into the feedback loop. Scope traces for 4 different cells are shown in Figure 1. Examine trace #1. When the reference cell is placed in the feedback loop, the read amplifier quickly rises to its steady state value. A short time later when the bad cell is placed in the feedback loop, the Read Amplifier overshoots its steady state level and slowly returns to its proper level. In normal operation, only a short time is allowed for the read amplifier to settle resulting in the overshoot level being sampled and a large pedestal offset being read out. The reason for the large overshoot is a large resistance in series with the read switches and the 0.2 pf capacitor. The value of the series resistance can be calculated from the settling time constant on the bad cells, and knowing that C=0.2 pf. For trace #1 the

resistance is 10 Mohms, trace #2 is 5 Mohms, and trace #4 is less than 1 Mohm. Note that for trace #3 the time scale is different and the resistance is about 100 Mohms. For comparison, the resistance in series with a good cell such as the reference cell is essentially zero.

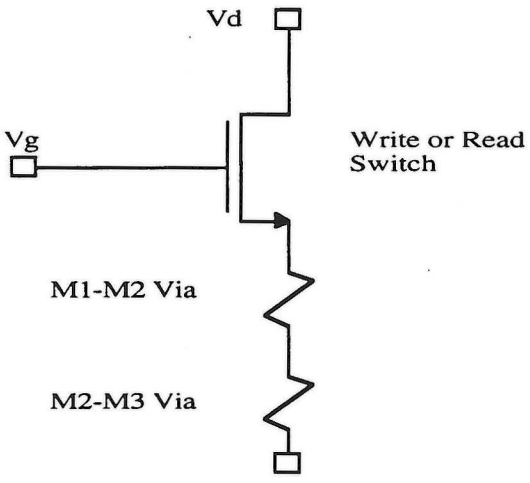
By putting test pads on the output of the Write amplifier, the same overshoot phenomenon could be observed in the Write Amplifier in other cells with bad pedestals. Figure 2 shows the output of the Write amplifier after a reset release and after injecting a charge. In a normal cell, the amplifier output would quickly reach the correct value without an overshoot. The simulation of the write operation shown in Figure 3 shows a good correlation between measurement and calculation. In the simulation three different resistor values were placed in series with the switches in the Write Amplifier (0, 10 Mohms, and 100 Mohms). The trace on Figure 2 shows about 100 Mohms in series with the feedback capacitor. All of the pedestal offset problems can be explained by a high resistance in series with either the W or R switches.

The amplifier overshoot problem was never seen for both the write and read amplifiers in the same cell. Therefore, it was concluded that there was no problem with the capacitors which were common to both operations. The problem had to be in the write (W) and read (R) switches or the vias.

Figure 4 is a layout of the critical area for one pipeline cell containing the R and W switches and the associated vias. A portion of one storage capacitor is shown on the left and another storage capacitor on the right. The switches control the capacitor on the left.

At one point, bad transistors were thought to be the problem. The poly connections to the W and R transistor gates were cross sectioned and a break and a crevice in one poly trace were found. Honeywell later showed that the cross section had been performed too close to the edge of the poly trace and there was no problem. Afterwards attention shifted to the vias that connect the R and W switches to the Write bus and Read bus.

Numerous test pads were added to several chips to study the high impedance problem. It was found that adding the test pads or the process of making a measurement could sometimes change the fault. This problem made trouble shooting extremely difficult and costly.



Transistor/Via Test

At one point a test pads were added to several channels so a combined transistor and via characteristic could be examined with a parameter analyzer. A one shot plot of a good transistor/via characteristic is shown in Figure 5. The program starts with Vg= 1 V and after each curve Vg is increased by 0.5 V up to 5 V. After testing the good cell, the parameter analyzer was connected to a known bad transistor/via and the single shot set of curves shown in Figure 6 were generated. Note the characteristic is very different . Figure 7 is a blowup of Figure 6 which shows very low transistor current until Vg= 3.5 V and Id reaches 1 mA. After that Id jumps up to 214 uA as shown in Figure 6 and then the rest of the characteristic appears relatively normal. It was found that near the origin the slope of all the I/V curves was about 33 Mohms and decreasing as drain current is increased.

The "bad" transistor/via was run a second time on the parameter analyzer and the problem was found to be completely gone as shown in Figure 8. It appears that the process of running a small amount of current through the transistor and vias corrected the fault, at least temporarily. Figure 9 shows operation of the read amplifier before the single shot test with the parameter analyzer and after the second shot was completed. The before portion of figure 9 is very similar to Figure 1.

Figure 10 and 11 show the low current characteristic of another bad transistor/via. The characteristic can be explained by a large resistor in series with the transistor. The resistor is 48 Mohms at low currents and decreases at higher currents.

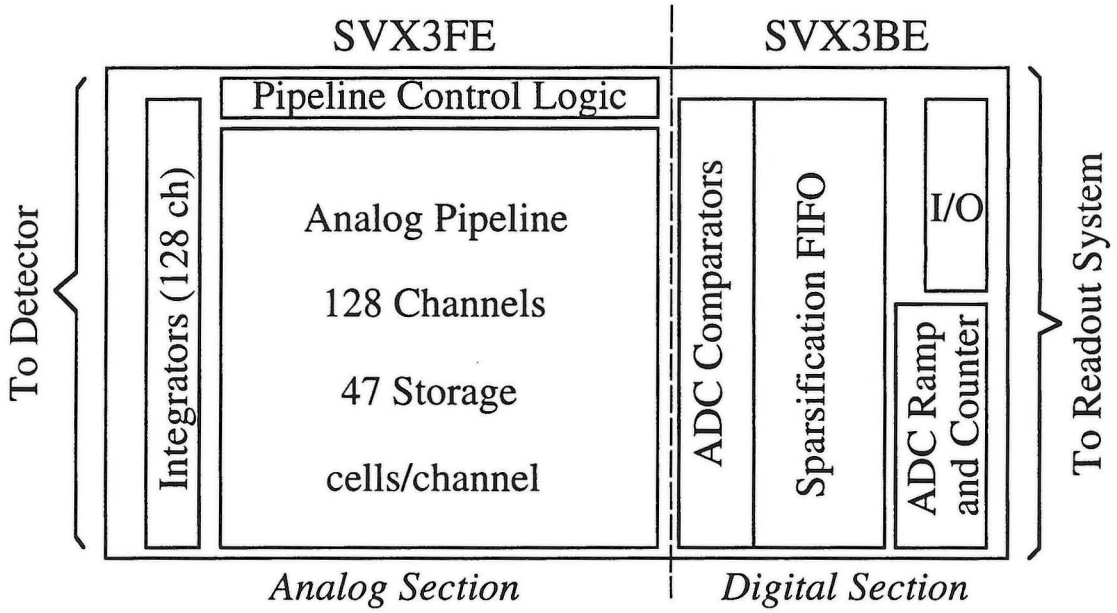
It was decided to try and measure the via resistance by turning the read switch completely on by applying 5 V to the gate and using the programmable current source in the parameter analyzer. The resultant curve shown in Figure 12 shows a resistance which starts out about 50 Mohms and decreases with current. The test was repeated in Figure 13 but at a higher current level. Around 125 nA the curve becomes irregular suggesting that something was beginning to change. When an attempt was made to run the curve again, it was found that the problem was gone and a completely normal transistor/via characteristic was present as shown in Figure 14. Figure 15 shows the read amplifier output before and after the transistor/via problem was corrected. The problem had gone away!

The last test where the transistor was fully turned on and the series resistance was measured strongly suggested that the high resistance was probably in one of the M1-M2 or M2-M3 vias. Figure 4 shows that each of the two R and two W switches are connected to the Read and Write buses through a pair of M1-M2 and M2-M3 vias. Since M2-M3 vias are used primarily in the area of the pipeline and most of the failures are occurring in the pipeline area, it was thought that the M2-M3 vias were the most likely problem. Test pads were placed on a different bad cell. One pad was placed on one side of the M2-M3 via and another pad was placed on the other side. Figure 16a shows a significant voltage across a bad via during normal operation. After a short time the via resistance went to zero and the voltage across the via was zero as shown in Figure 16b. It should be noted that the process of measuring the via voltage caused about 1 uA to flow through the via (1 V/ 1Mohm). Based on previous measurements it was assumed that the small measurement current again cleared the via. The same via measurement was done on a second cell as shown in Figure 17. Unfortunately only the before waveform showing voltage across the via is available.

At this point there is very strong evidence that the M2-M3 vias have a high impedance which can be cleared by running some current through them. Unfortunately under normal operation, very small currents pass through the vias in the pipeline cells and there is no evidence that the vias will clear themselves.

M2-M3 Via Distribution in the SVX3

Essentially all of the M2-M3 vias on the SVX3 chip are located in the analog sections of the chip. A simplified floor plan of the chip is shown below. The analog pipeline has 4 vias per cell for a total of 23552 vias per chip (4/cell x 46 cells/channel x 128 channels/chip). If any one of the 4 vias in a cell fails there should be a random cell failure which would show up as a black area on the Pipeline Quality Map.



SVX3 Floorplan

There are 14 M2-M3 vias per channel outside the pipeline in circuitry common to a given channel (Reference cell, Integrator, Write amplifier, and Comparator). Every one of these vias has not been studied in great detail. However, if any one of these vias fails, all of the 46 cells in a channel could look bad. These cells would show up as red on the Pipeline Quality Map. Under some conditions, some other random faults can show up as red on the Pipeline Quality Maps also. The main point is that a single bad via outside the pipeline has a large leverage which can show up as a lot of bad cells. Thus it is not surprising to see a larger red section than black section on many of the Pipeline Quality Maps.

There are three M2-M3 vias in each of 46 cells in the pipeline digital logic section. If one of these vias was open there could be a pipeline failure. This is a relatively small number of vias and a detailed analysis has not been done.

There is a larger number of M2-M3 vias in the serial shift register which is used to initially program the chip. The serial shift register runs vertically along the input side of the chip between the detector pads and the integrators. There are 7 M2-M3 vias in each of the 151 cells for a total of 1057 M2-M3 vias. If one of the vias fails, the chips is dead. The vias are for clock signals and power connections which essentially carry little or no current. Some or all of these vias are potential failure points. Thus it would not be surprising to see serial shift register failures begin to occur in chips where there are a large number of bad

pipeline cells as shown on the Capacitor Quality Maps for lots 10 and 11. This appears to be the case in lot #11. The five Capacitor Quality Maps for lot #11 shows a very large number of bad cells in the center of the wafer. Wafers 3, 5, 11, and 20 show another failure mechanism occurring. By looking at the Types of Die Failures for wafers 3, 5, 11, and 20 in lot 11, it is seen that all of the chips in the center of the wafer are failing the serial shift register test. Outside the yield hole caused by the serial shift register failures, there are predominately chips with bad pedestals. The bad pedestal count gets smaller as the individual dice get closer to the edge of the wafer. The failed shift register suggests that bad vias are also causing failures in digital portions of the chip.

Analysis has been done on the number of bad cells as a function of location on the chip for all channels on both good and bad wafers. Figure 18 shows a very interesting phenomenon for the bad wafers. (Left and right die simply refer to reticule location). There is a linear increase in the failure rate of bad cells on a chip from cell 0 to cell 46. Cell 46 is at the integrator side of the chip. This seems to indicate that there is a significant dependence on layout similar to what might be seen on processes that have layout density rules. The cause of the variation is unknown at this time. It does suggest however, that M2-M3 vias located in other areas such as test structures off the chip may have very different failure rates.

Wafer Annealing Test

One of the wafers from a lot with moderate yield was annealed by Honeywell to see if the chip yield would change. Wafer #15 from lot #12 was chosen since it had a yield of 38.8% with a yield hole in the center caused by bad cells in the pipeline. After annealing, the wafer was retested at LBNL. The Die Quality Maps, the Pipeline Quality Maps, the Type of Die Failure Maps, and the Random Bad Cell Maps for before and after annealing are shown in Appendix F. The Die Quality Maps show that there is a significant decrease in yield after annealing. Annealing caused the yield of good dice to decrease from 39% to 18% and the yield of good+fair dice to decrease from 50% to 31%. A breakdown is given here for all of the dice.

good -> fair	11 dice
good -> bad	18
fair -> bad	10
bad -> good	1
bad -> fair	1
fair -> good	0
No change	93

An interesting observation can be made from the Types of Die Failure Maps before and after annealing. None of the pre-annealing failures due to over/under current, and basic readout problems changed after annealing. This shows a certain degree of repeatability in the test setup.

The Capacitor Quality Maps show that there is a large increase in the number of bad pipeline cells. The increase is dramatically apparent by looking at the Random Bad Cell Maps before and after annealing. These two maps show that the yield hole has gotten larger and deeper. Here is a vertical sample of dice through the center of the wafer before and after annealing.

Die	Bad cells before	Bad cells after
3	0	0
8	0	0
14	0	0
21	0	0
29	14	18
38	57	78
47	108	157
56	135	187
64	---	---
71	32	37
79	---	---
88	81	142
97	19	31
106	3	8
114	0	0
121	0	0
127	0	0
132	0	1

It is very clear that the center of the wafer was bad and the number of bad cells was about 50% higher after annealing.

Root Cause

The root cause of the bad M2-M3 vias is unknown. Construction of a M2-M3 via is a reasonably complicated process. After the aluminum M2 is deposited, a metal glue layer is put down, followed by a TiW barrier material. Afterwards the via is filled with tungsten. On top of the tungsten is another glue layer and TiW layer. The aluminum M3 layer is then deposited. A problem could occur at any of these interfaces.

Several suspect M2-M3 (and M1-M2) vias to Write switches were cross sectioned using FIB techniques. Figure 19 shows where the vias are located on the layout. Figure 20 shows a cross section through 2 M1-M2 vias and 2 M2-M3 vias. The right hand via shows a small white region under the M2-M3 via. The right hand M2-M3 via is blown up in Figure 21. A different set of vias is shown cross sectioned in Figure 22. There appears to be a fine white line at the bottom of the left hand M2-M3 via. It is not known if these discolorations are a problem or not.

One of the early hypotheses from Honeywell was that there was a redeposition of photoresist into vias during a plasma etching step. Figure 23 shows what that might look like using Transmission Electron Microscope (TEM). Honeywell has proposed examining several vias using TEM to study the problem. Since the chance of finding a bad via by chance is relatively low and the cost of TEM analysis is high, a chip with bad vias in known locations was sent to Honeywell for analysis. Results are not yet available.

Comparison to 4 Inch Wafers

Considerable analysis has been done on the chips from the 4 inch wafers as well as the 6 inch wafers. The pedestal failure pattern seen in the center of most of 6 inch wafers simply does not exist on the 4 inch wafers. The average yield for all 4 inch wafer dice is shown in

Figure 24. The percentage of a reticule location shown in green represents the percentage of good dice at that location for all the wafers. It should be noted that there is a relatively uniform yield pattern across the wafer with a slight decrease near the wafer edge as would be expected.

A breakdown of yield information for the 4 inch wafers is given here:

1st Honeywell batch (15 wafers, 14 probed)
Good Dice: 50.1%
Good+Fair dice: 59.6%

2nd Honeywell batch (100 wafers, 100 probed)
Good Dice: 50.6%
Good+Fair dice 62.5%

All 4 inch wafers combined:
Dice probed: 5906 (100 %)
Good Dice 2987 (50.6%)
Good+Fair dice 3672 (62.2%)

The yield distribution across all 114 of the 4 inch wafers is shown in Figure 25. There are 52 dice per wafer. The lowest yielding wafer was 15.4%. The median yield was 50%. This distribution can be used to establish the yield pattern for SVX3 wafers. Wafers which lie below a reasonable lower limit could/should be rejected.

The yield for the 6 inch wafers from lot #8 (neglecting the scratches) appears to higher than the yield for the 4 inch wafers. The yield on all the other lots has been seriously degraded by a systematic but unknown mechanism. If the problem causing the yield hole on the 6 inch wafers can be corrected, the 6 inch wafer yield should be consistently higher than the 4 inch wafers.

Acknowledgments

This report would not be possible without the outstanding work done by Igor Volobouev at LBNL. All of the wafer level plots as well as other significant contributions came from Igor. In addition, identification of the M2-M3 via problem from chip testing came primarily from Tom Zimmerman at Fermilab. His tireless efforts brought many loose ends together and provided the direction needed to solve the puzzle .

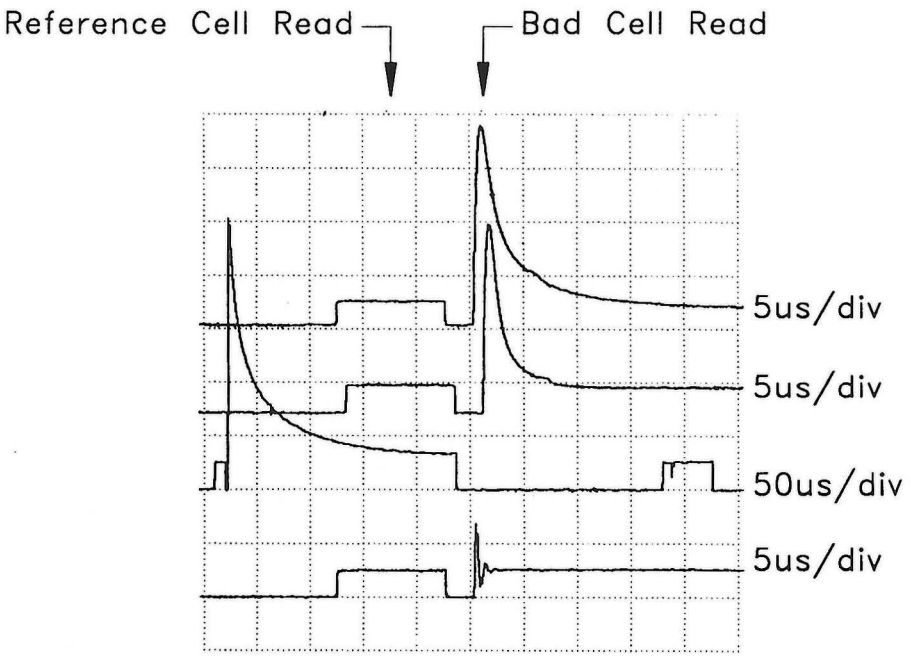
Conclusion

A large and costly effort was mounted to identify the yield problem on the Honeywell 6 inch wafers. It is clear that the problem did not exist on the 4 inch wafers. We believe that the problem lies with the M2-M3 vias. The problem was studied in the analog pipeline since most of the failures occurred in the pipeline and the pipeline was the easiest place to sort out the problem. It is believed that the M2-M3 via problem causes failures in other parts of the circuit but at a lower rate. Use of M2-M3 vias is critical to the Fermilab design as it would be to most other High Energy Physics Projects. It is critical that Honeywell find and correct the problem.

FIGURES

DIE 48
READ AMPLIFIER OUTPUT on "bad" channel/cell

Ch. 46 cell 30
Ch. 13 cell 41
Ch. 49 cell 39
Ch. 51 cell 30



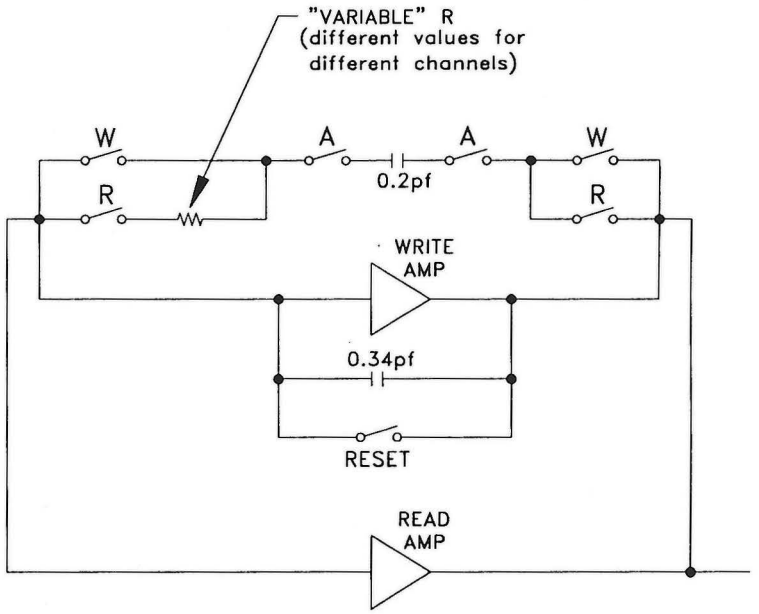
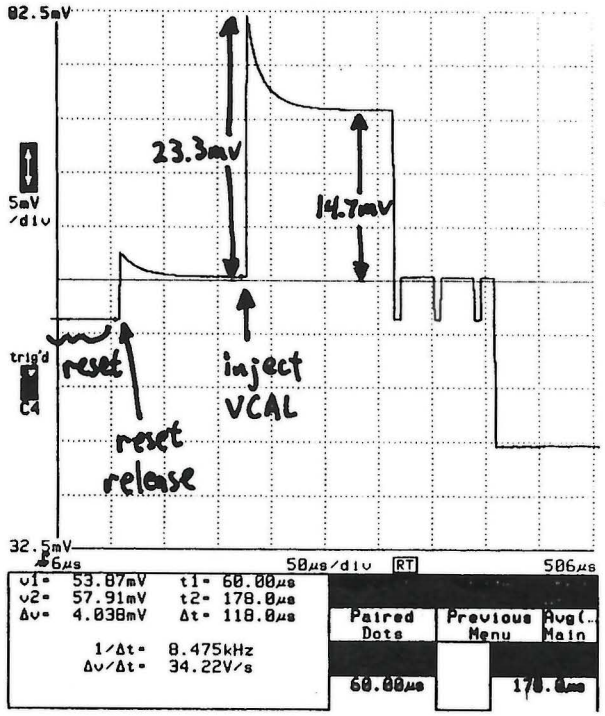
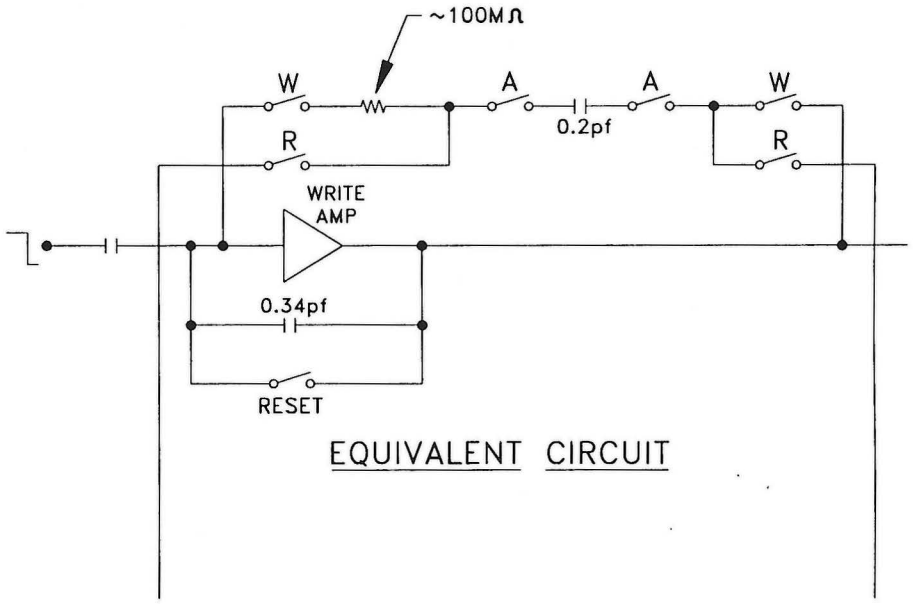


Figure 1

DIE 48
CH. 46 CELL 43
WRITE AMPLIFIER OUTPUT on "bad" channel/cell





EQUIVALENT CIRCUIT

Figure 2

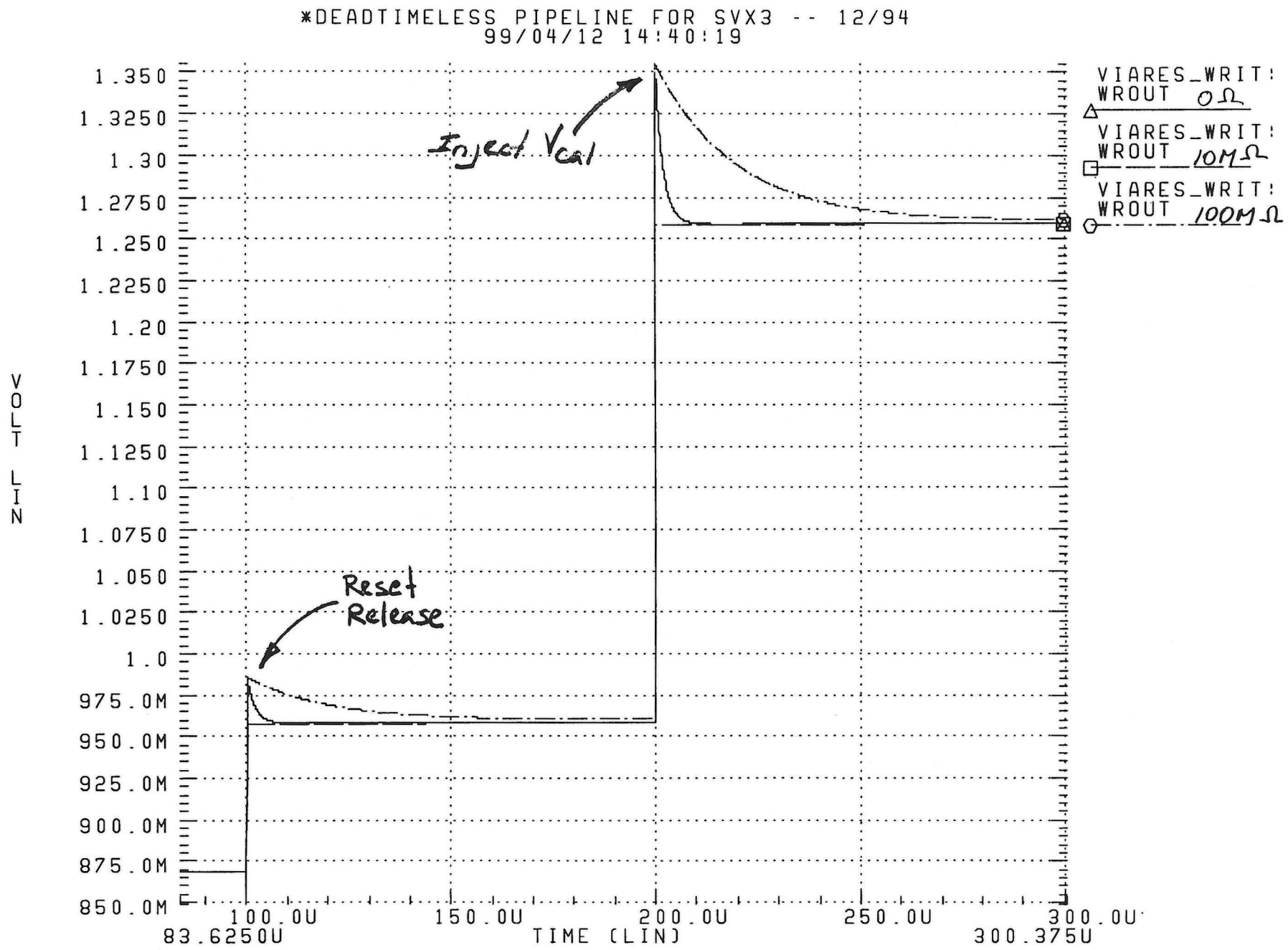

*DEADTIMELESS PIPELINE FOR SVX3 -- 12/94
99/04/12 14:40:19
VIARES_WRIT:
WROUT 0Ω
VIARES_WRIT:
WROUT 10MΩ
VIARES_WRIT:
WROUT 100MΩ
Inject Vcal
Reset
Release
1.350
1.3250
1.30
1.2750
1.250
1.2250
1.20
1.1750
1.150
1.1250
1.10
1.0750
1.050
1.0250
1.0
975.0M
950.0M
925.0M
900.0M
875.0M
850.0M
VOLT LIN
100.0U
150.0U
200.0U
250.0U
300.0U
83.6250U
TIME (LIN)
300.375U

Figure 3

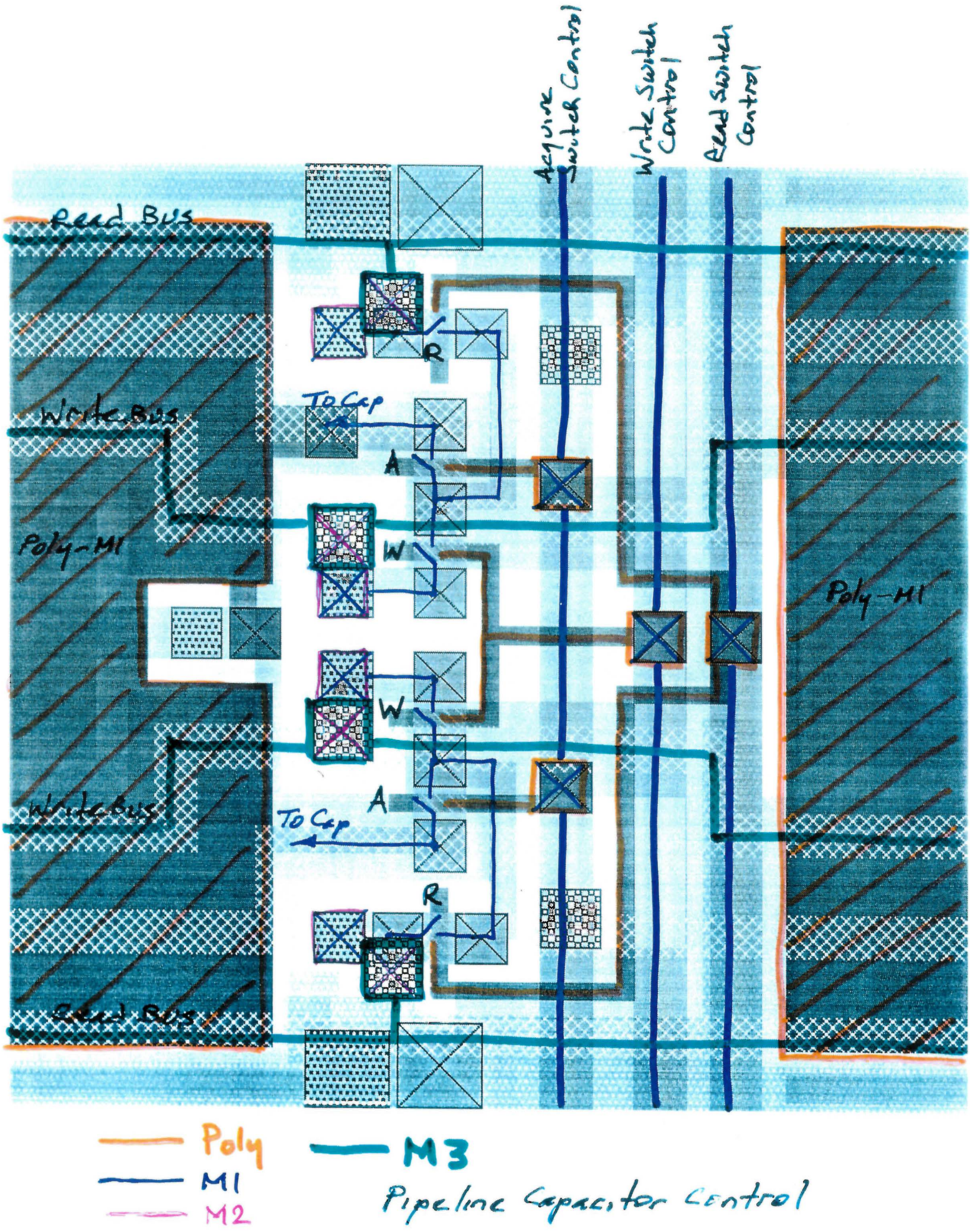

Acquire Switch Control
Write Switch Control
Read Switch Control
Read Bus
Write Bus
Poly-M1
R
To Cap
A
W
W
A
To Cap
R
Write Bus
Read Bus
Poly-M1
Poly
M3
M1
M2
Pipeline Capacitor Control

Figure 4

Figure 5

Good Cell, Ch 31, cell 15
Wafer 92, Ch. # 39

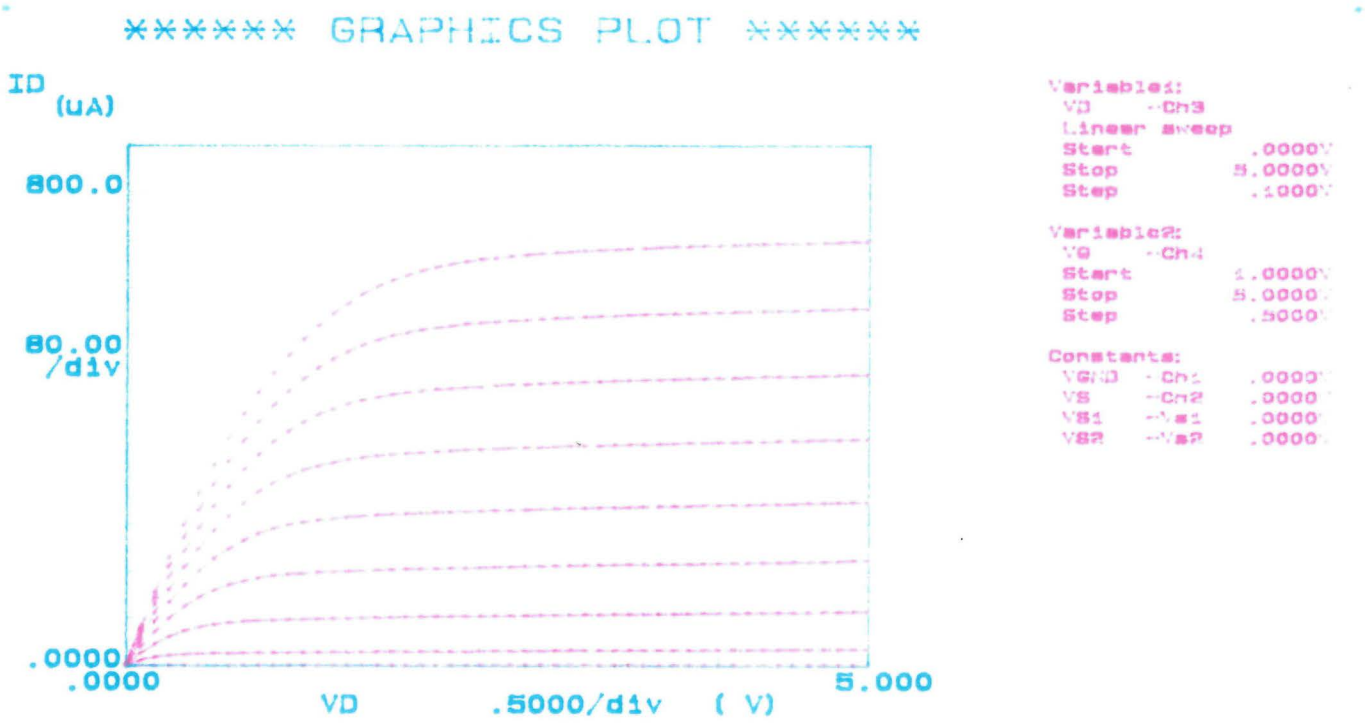


Figure 6

Bad cell Ch36 cell 30
First single shot - shows faulty operation

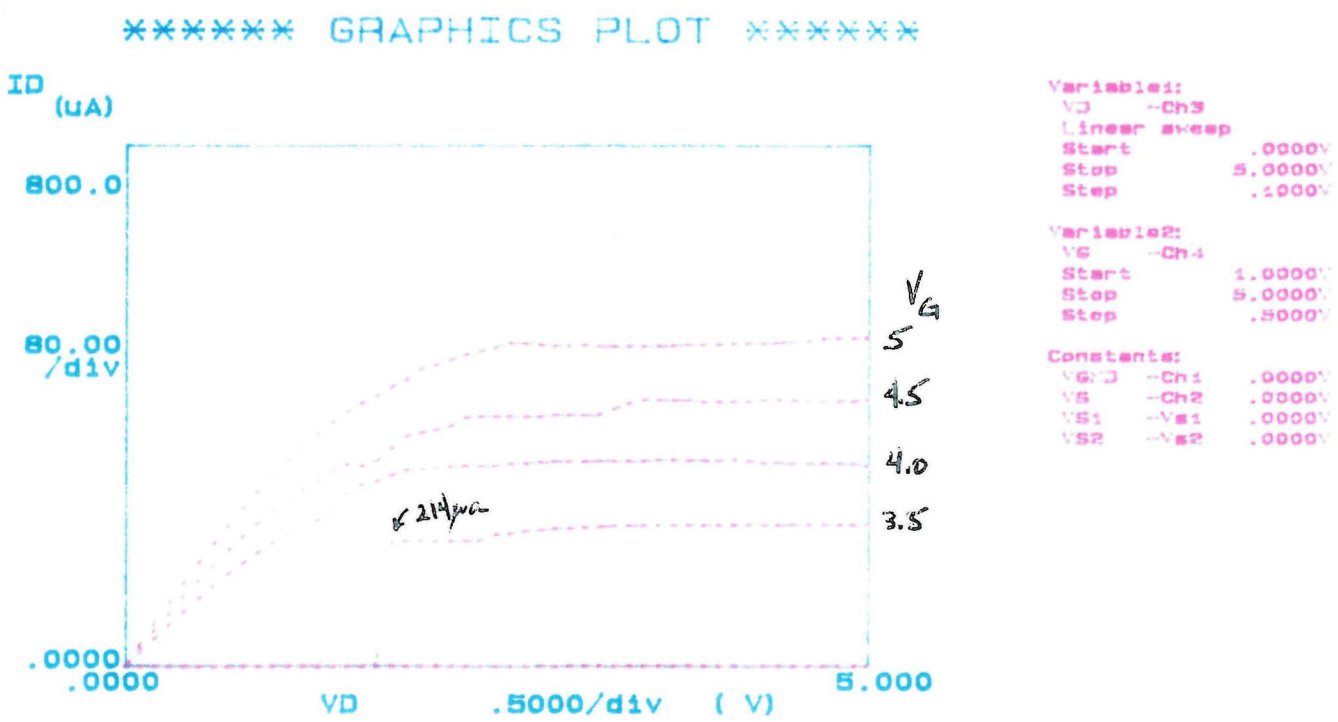


Figure 7

Bad cell ch 36 cell 30
First single shot blowup

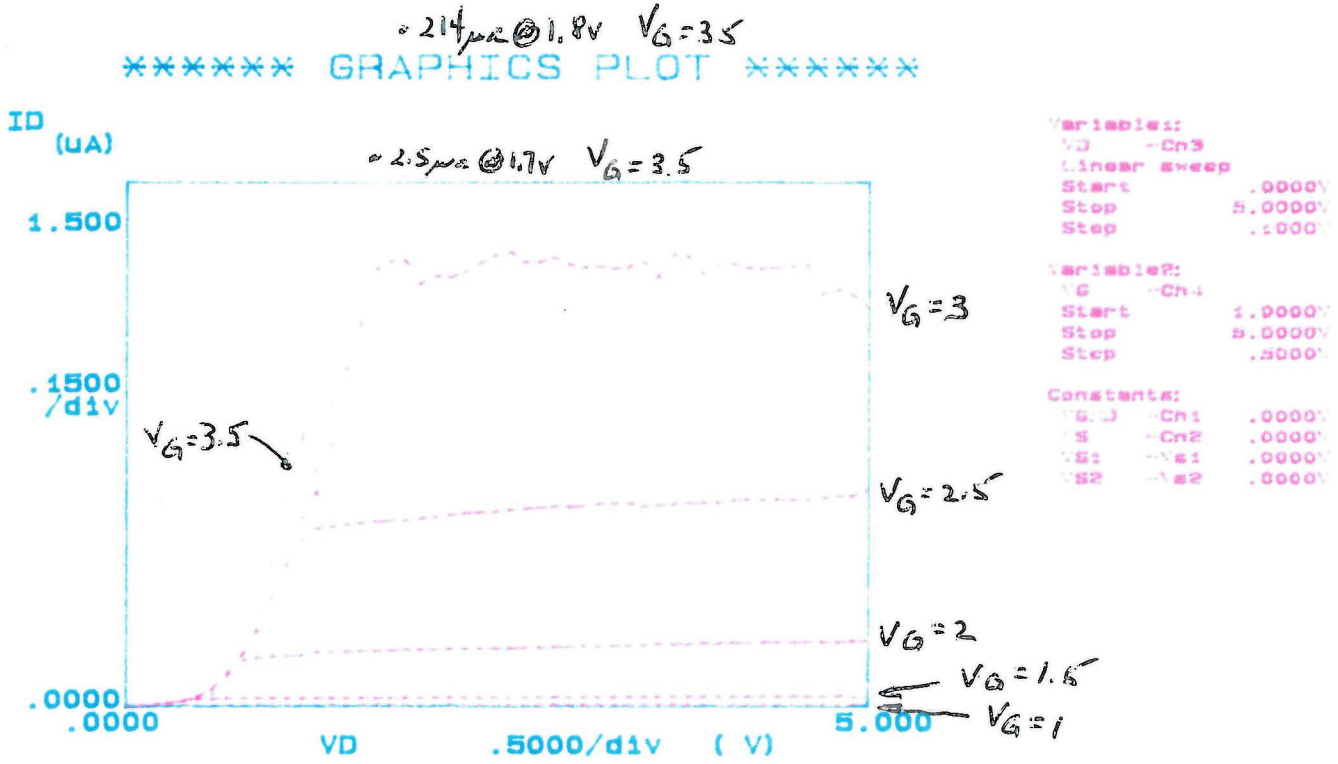


Figure 8

Bad cell ch 36 cell 30
second
~~first~~ slot - transistor now working.

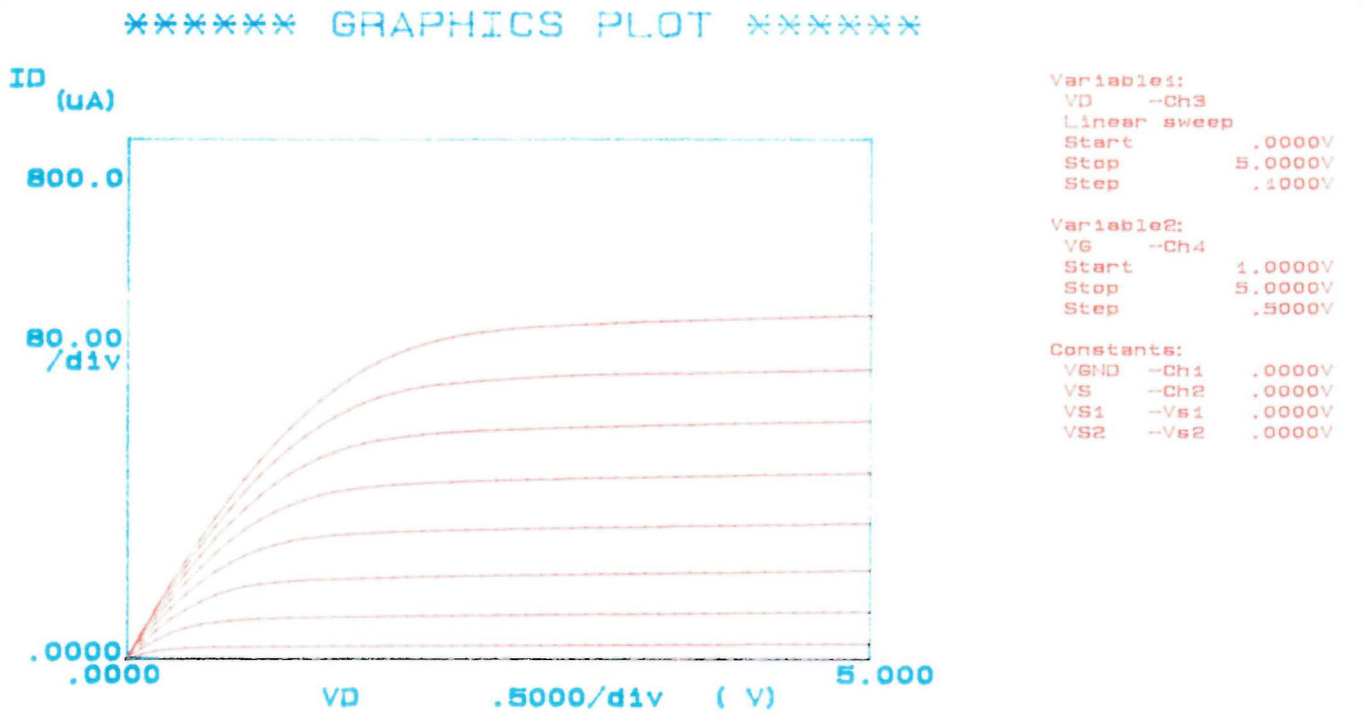
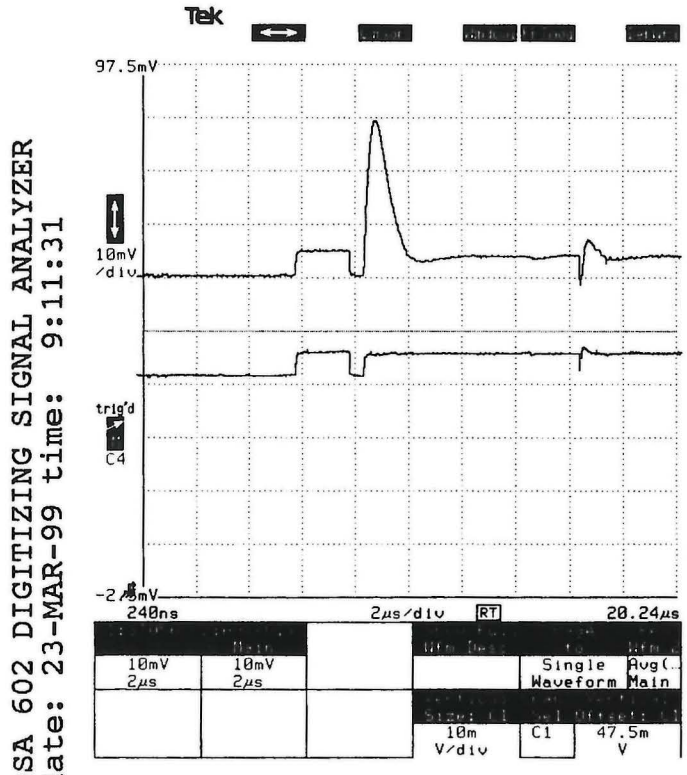


Figure 9



Wafer 92 Chip #39
Channel 36, Cell 30

← Before single shot on parameter analyzer

← After 2 single shots on parameter analyzer.

Figure 10

Wafer 92 Chip #39

Bad cell Ch 55 cell 22

Low current test shows faulty behavior

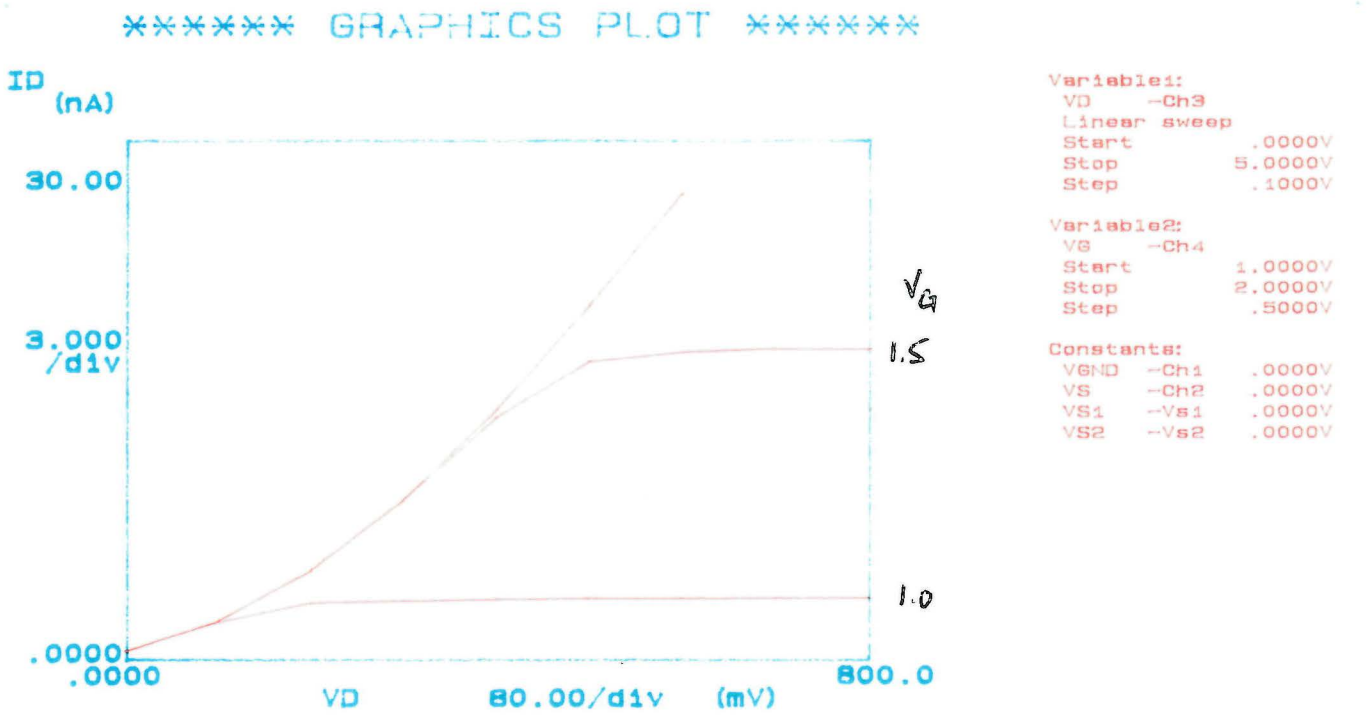


Figure 11

Wafer 92 Chip #39
Bad cell ch 55 cell 22
Low current test shows faulty behavior.

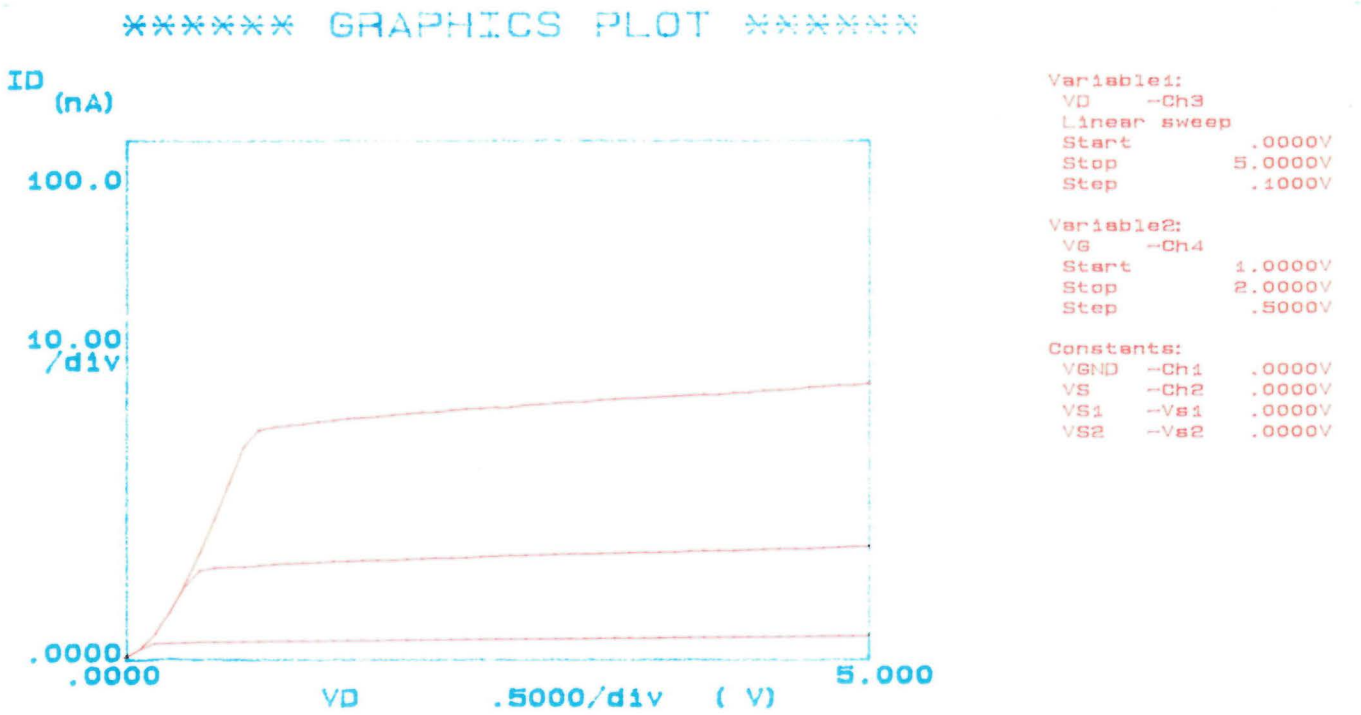
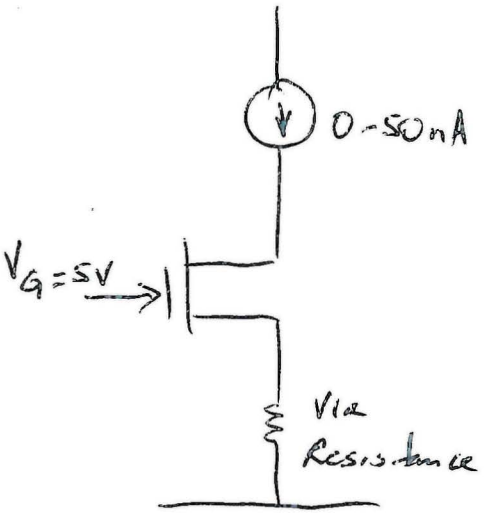


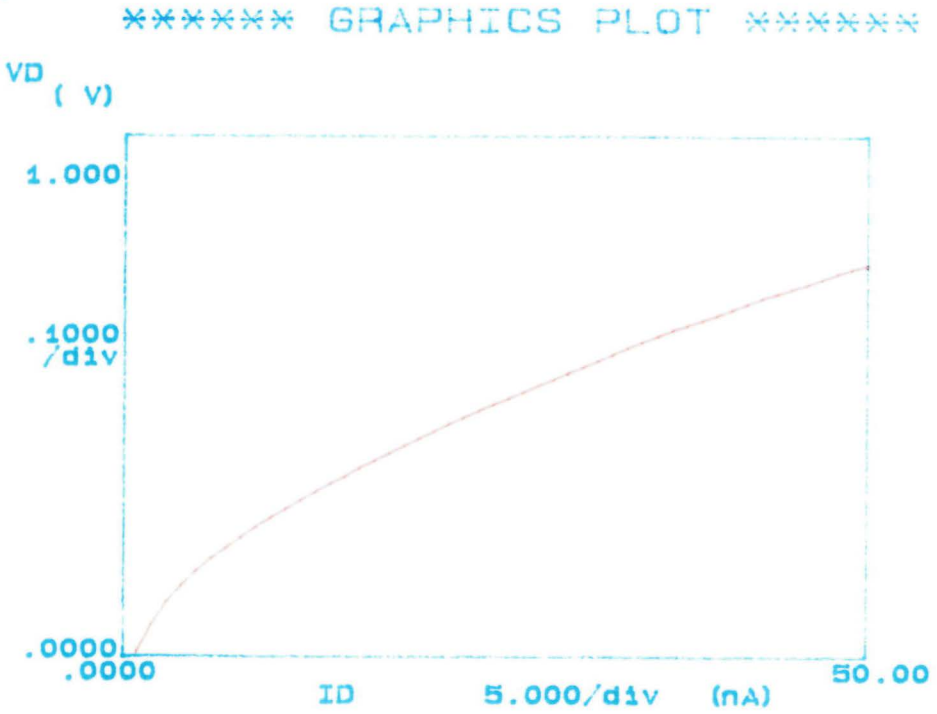
Figure 12

Wafer 92 Chip #39

Bad cell ch 55 cell 22

Measure current dependent via resistance.





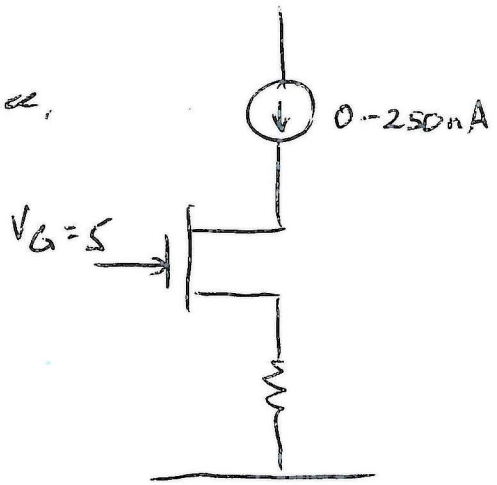
Variable1:
ID -Ch3
Linear sweep
Start .000 A
Stop 50.00nA
Step 1.000nA

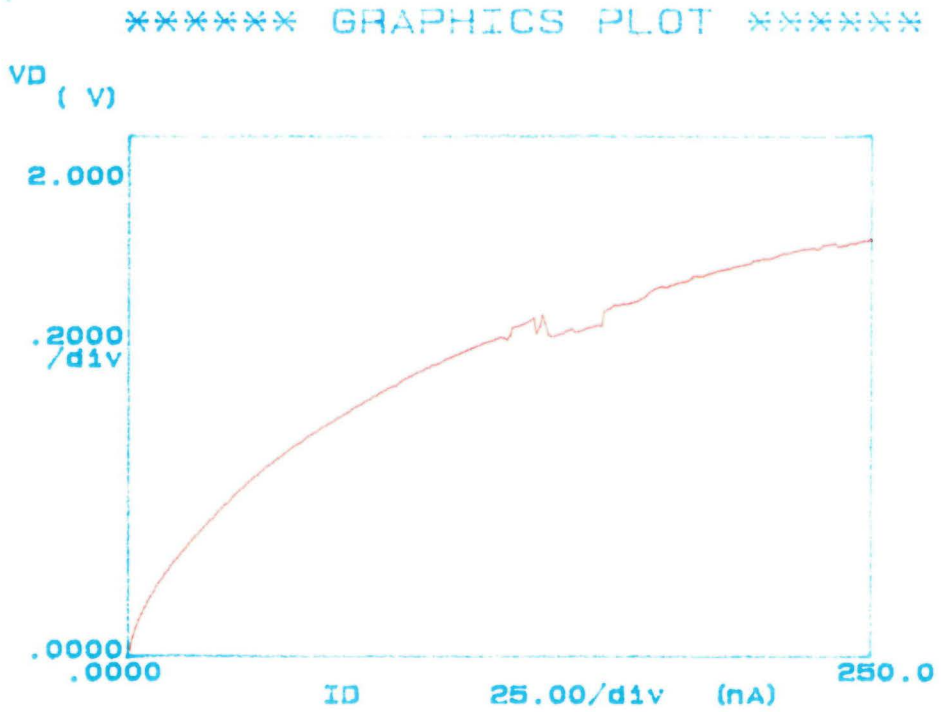
Constants:

VGND	-Ch1	.0000V
VS	-Ch2	.0000V
VG	-Ch4	5.0000V
VS1	-Vs1	.0000V
VS2	-Vs2	.0000V

Figure 13

Wafer 92 Chip #39
Bad cell ch 55 cell 22
Measure current dependent via resistance.
Via healed after end of test.





Variable1:
ID --Ch3
Linear sweep
Start .000 A
Stop 250.0nA
Step 1.000nA

Constants:
VGND --Ch1 .0000V
VS --Ch2 .0000V
VG --Ch4 5.0000V
VS1 --Vs1 .0000V
VS2 --Vs2 .0000V

Figure 14

Wafer 92 Chip #39

Bad cell ch 55 cell 22

Characteristic after via is heated.

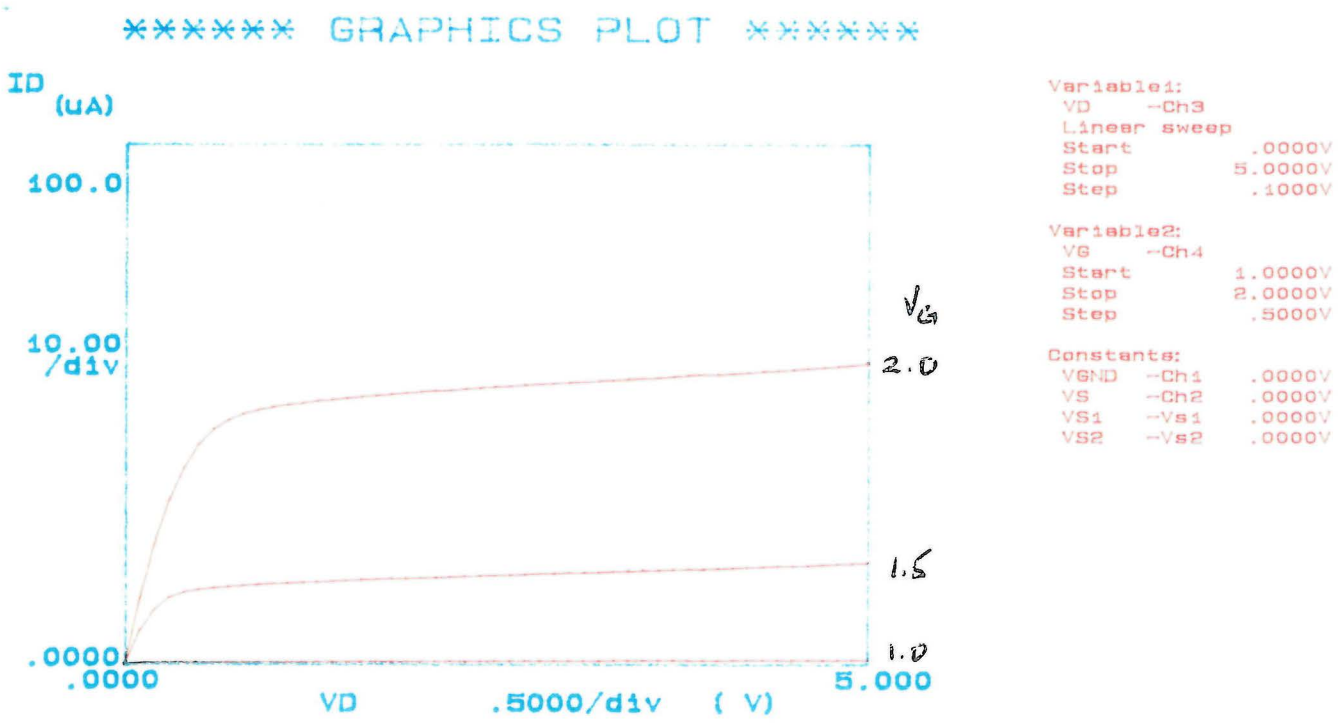
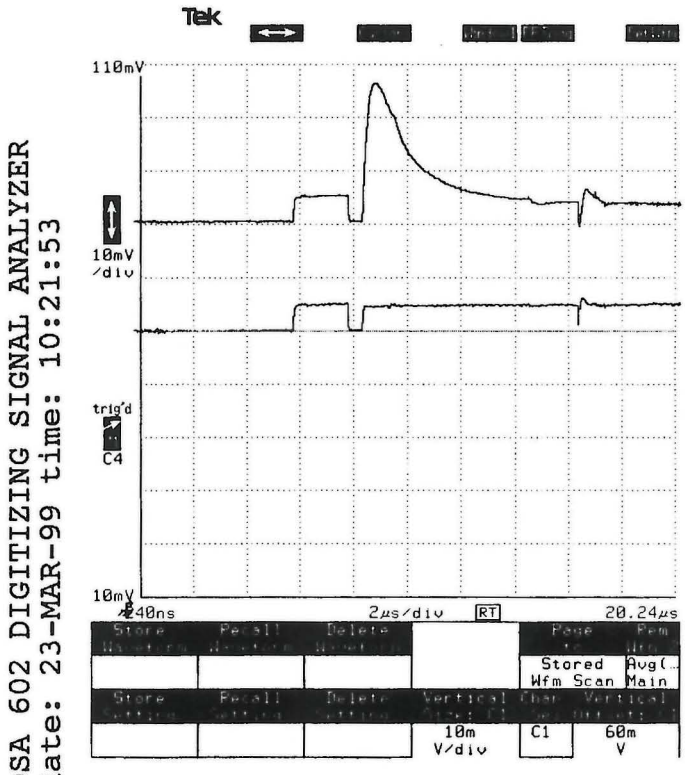


Figure 15

Wafer 92 Chip #39
Chamel 55 cell 22

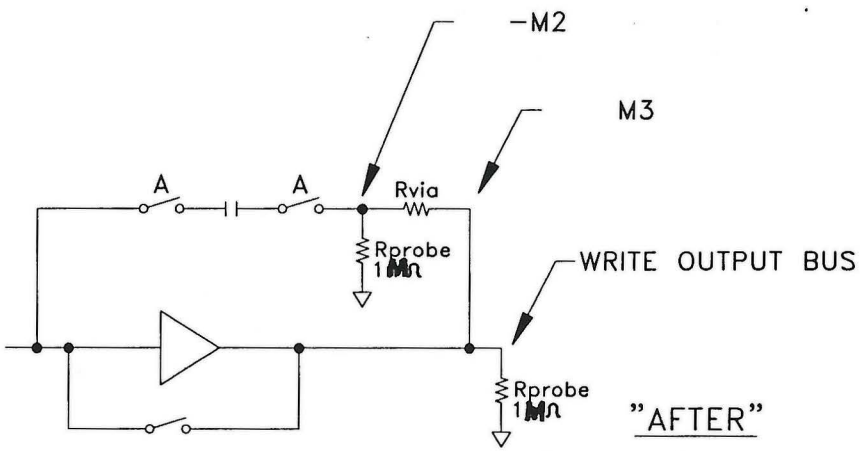


← Before via is fixed

← After via is fixed

DIE #87, Ch. 86, cell 37

Waveforms acquired with picoprobe (R=1MΩ, 20:1)



"BEFORE"

(a)

Aquisition in "bad" cell

"AFTER"

(b)

Aquisition of "formerly bad" cell

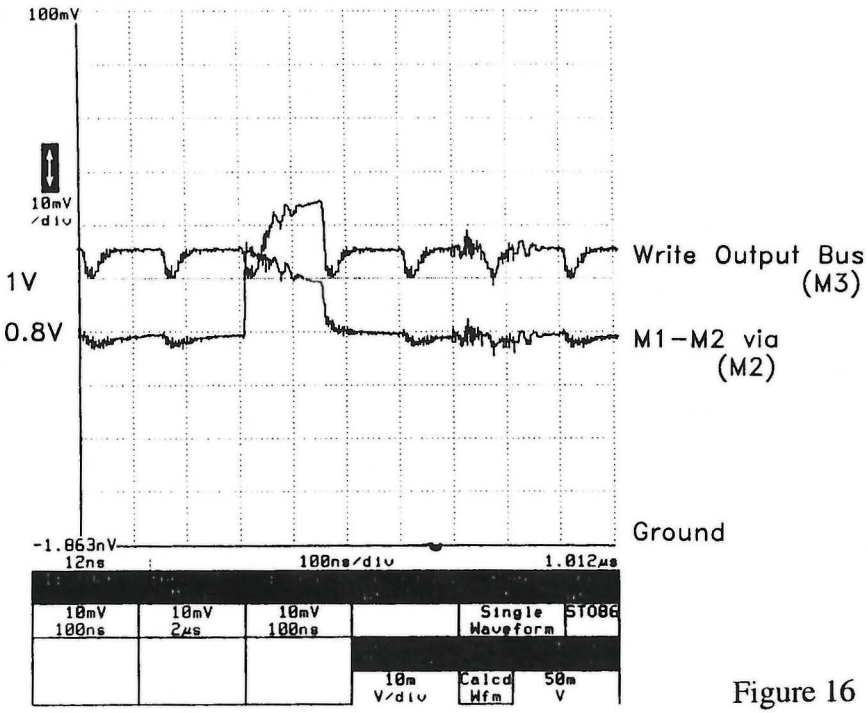
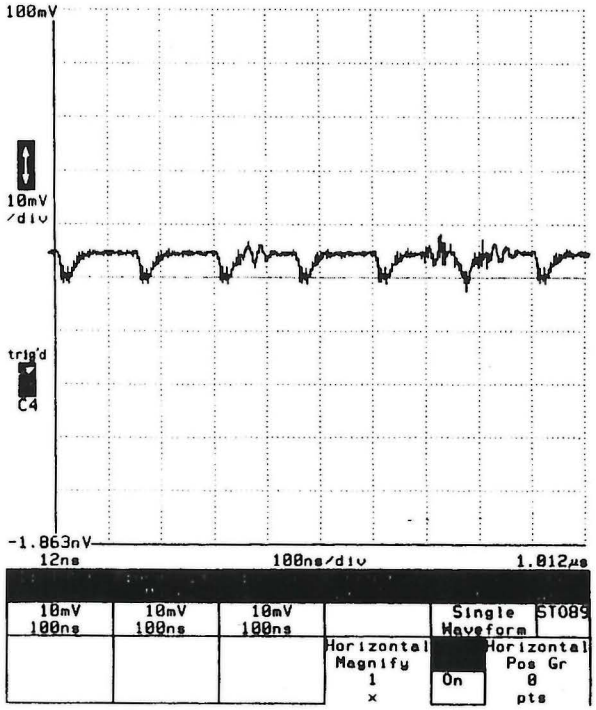


Figure 16



DIE #87, Ch. 33, cell 41

"BEFORE"

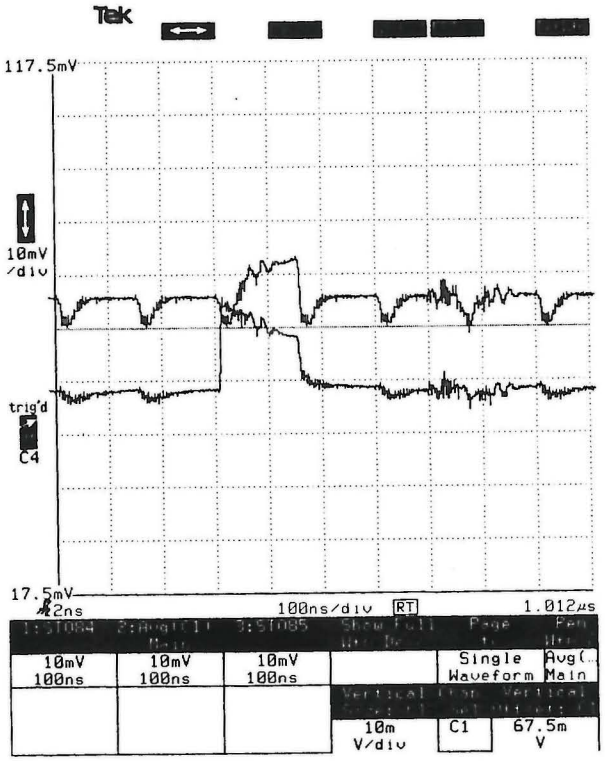


Figure 17

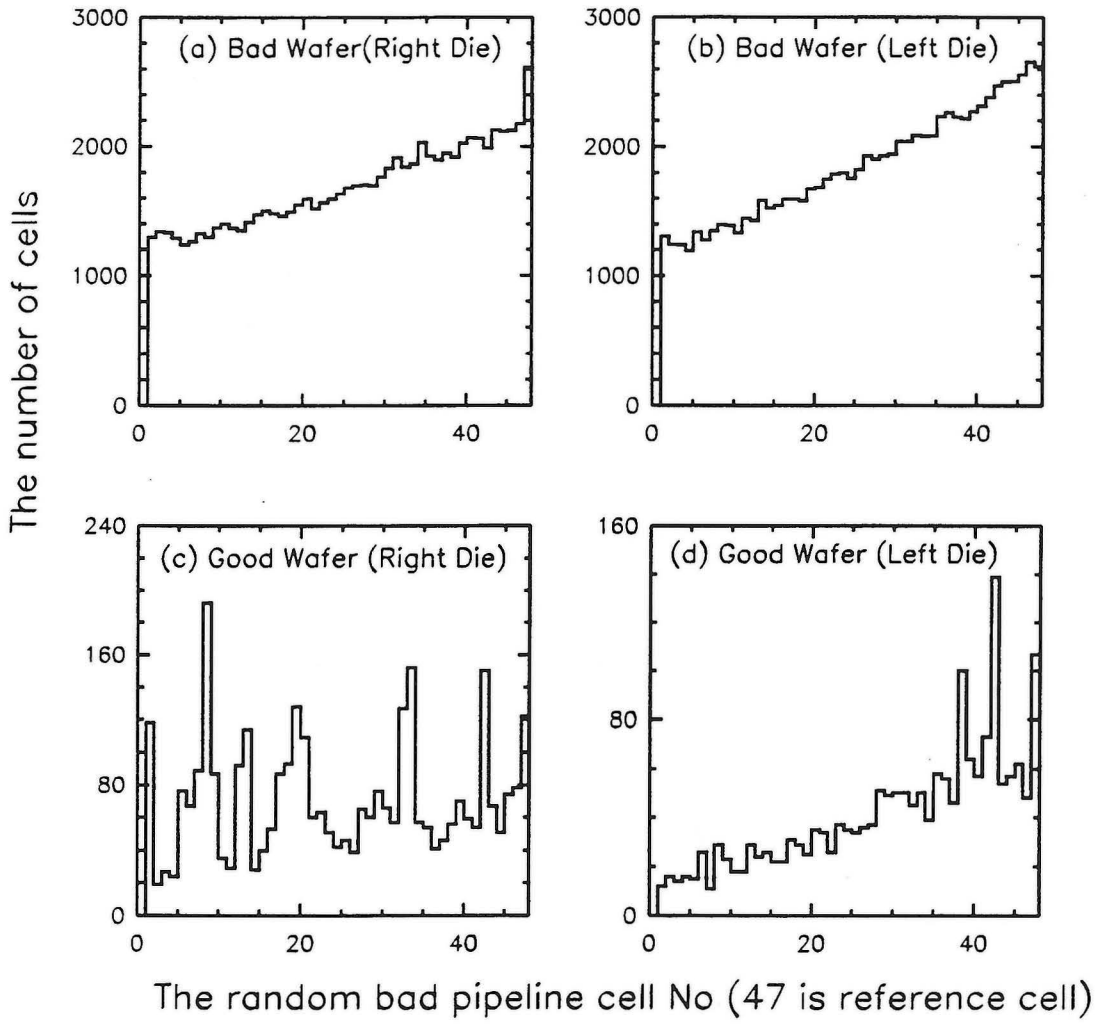


Figure 6: The distribution of all random failing capacitors as a function of pipeline cell number for all the dies (a) bad wafer(right die) (b) bad wafer(left die) (c) good wafer(right die) and (d) good wafer(left die). The bin 47 is the number of failed reference capacitors.

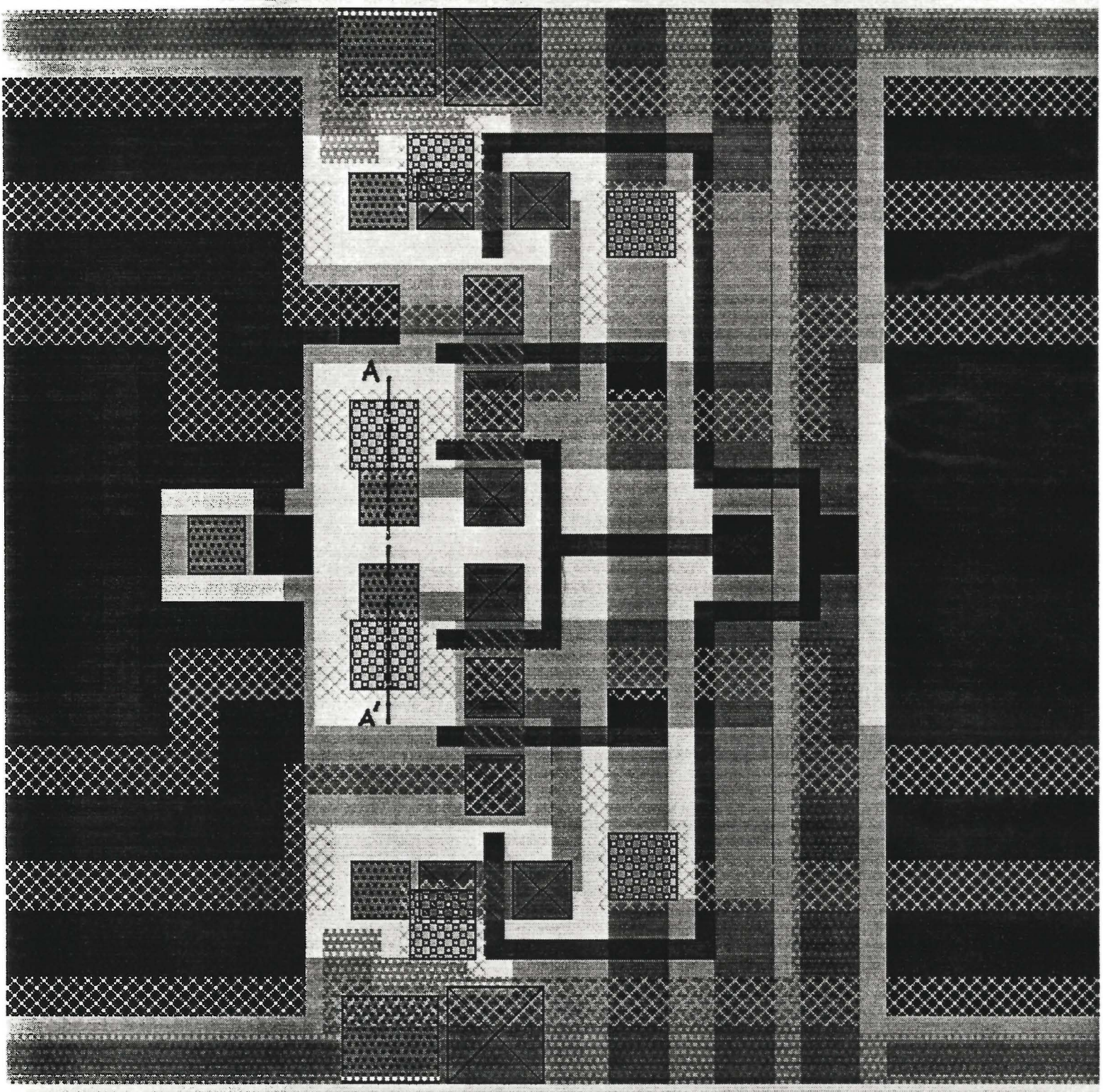


Figure 19

Layout 3

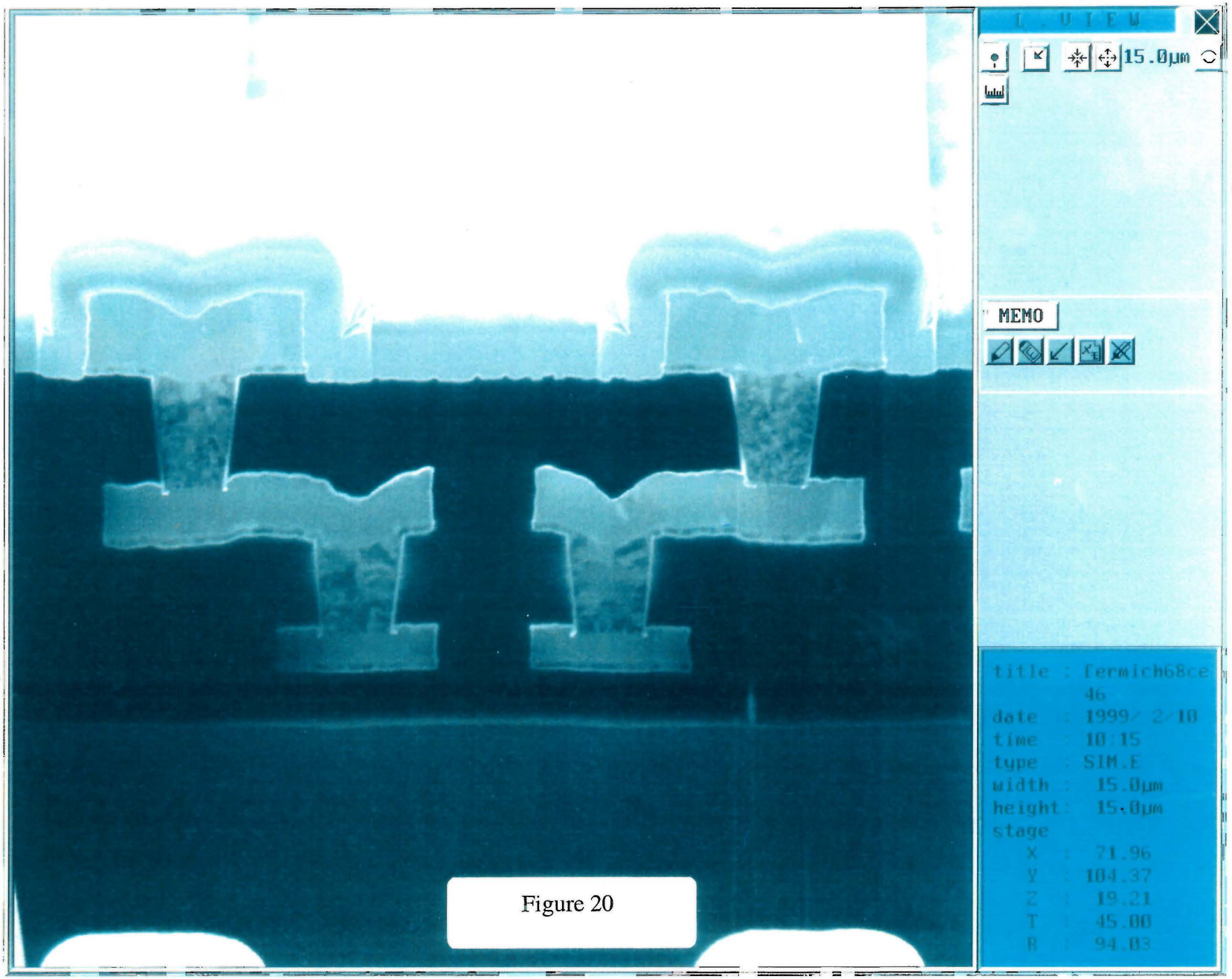


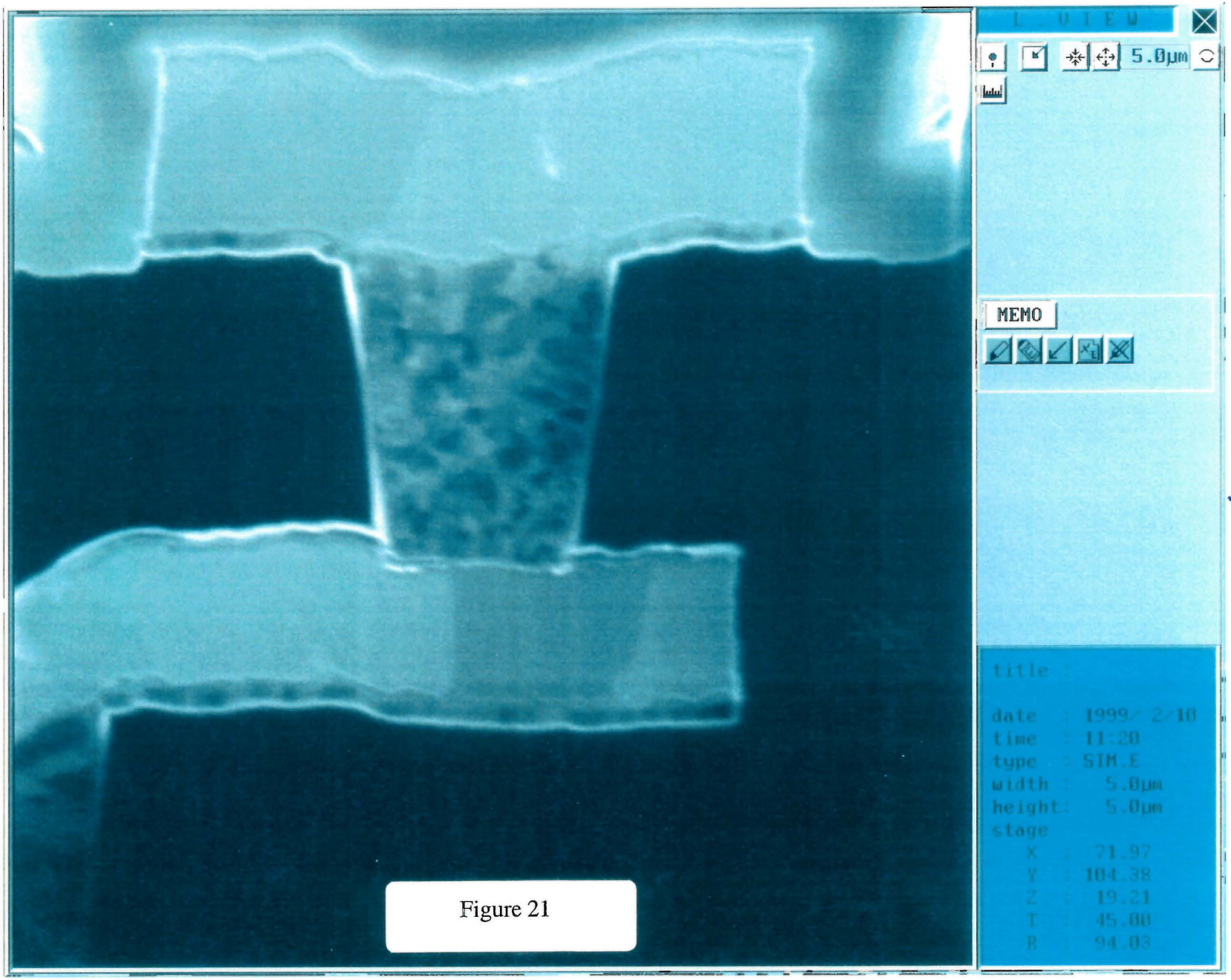
Figure 20

Lot #9
Wafer #2
Chip #48
Channel #68
Cell #46

Section A-A'

Channel 63 Cell 46
Wafer 2 Chip 48

Photo 1



M3 →

M2 →

Lot #9
Wafer #2
Chip #48
Channel #68
Cell #46

Section A-A'

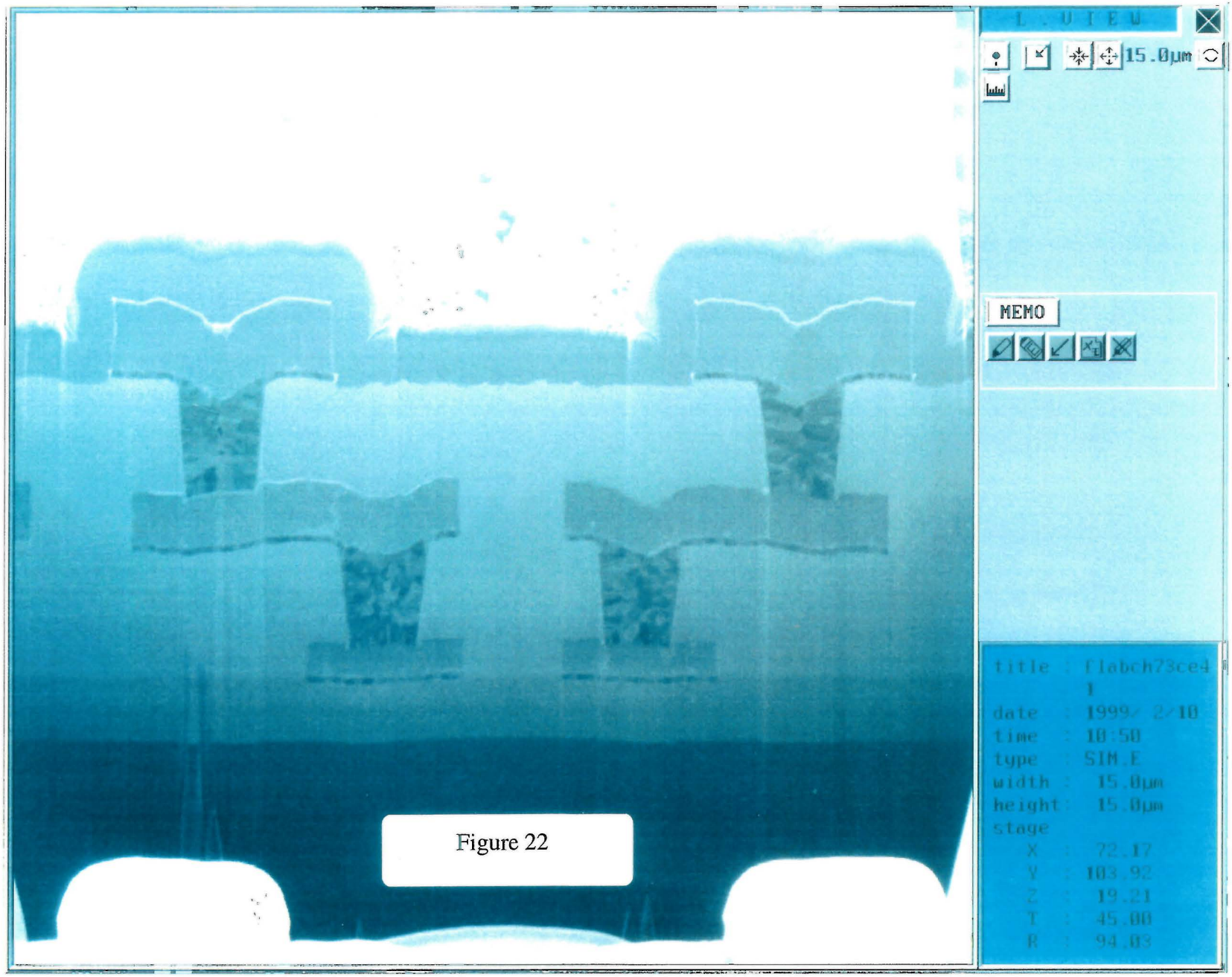
Figure 21

Channel 68
Cell 46
Wafer 2
Chip 48

Photo 2

Write BUS

Write BUS



M3 →

M2 →

M1 →

Figure 22

Lot #9
Wafer #2
Chip #48
Channel #73
Cell #41

Section A-A'

Channel 73 Cell 41
Wafer 92 Chip 48

Photo 3

Figure 23

Precision Cross-Sections

Failure analysis often requires XTEM analysis of a single small localized site on an IC. Figure 4 pinpoints delamination due to the presence of residual photoresist as the cause of an electrically-open contact.

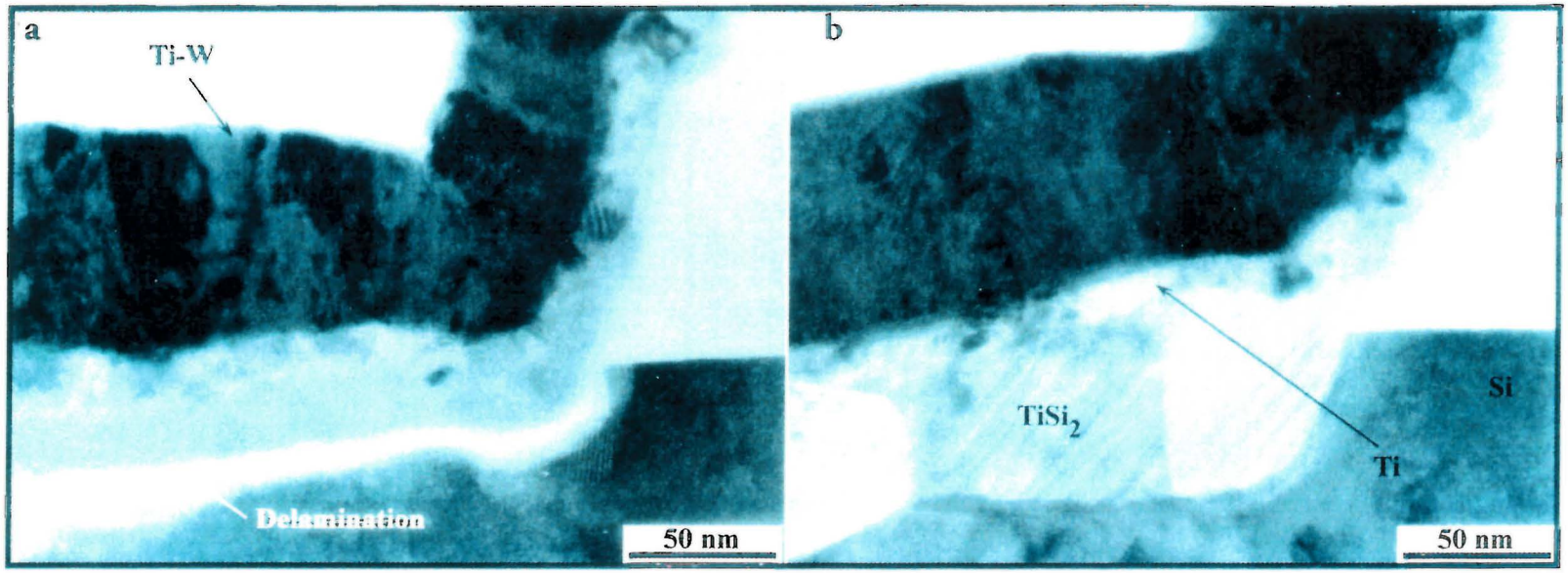


Fig. 4: Precision XTEM of a 1 µm **a)** electrically-open contact. **b)** good contact for comparison.

For sales or more information, contact Accurel Headquarters:

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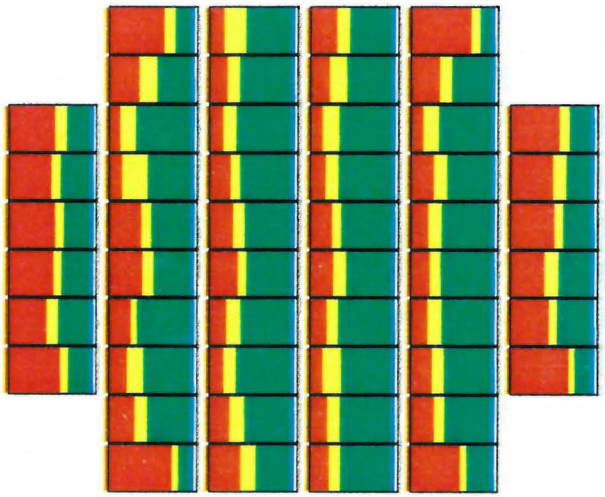
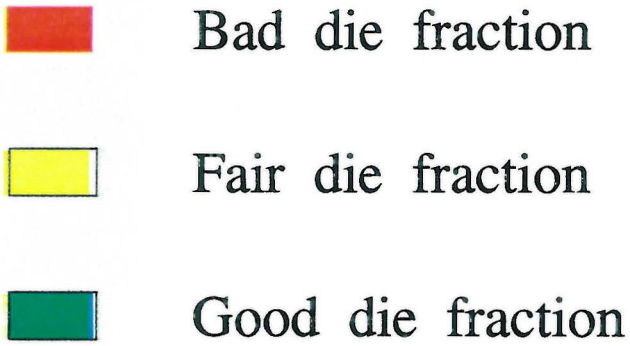
Materials Analysis Group, A Division of Accurel:

350 Potrero Avenue Sunnyvale CA 94086
Office: 408/737-9700 Fax: 408/737-9791

Cumulative die quality map for 114 4-in SVX3D wafers from Honeywell

Date: 03/01/99





Good die yield is 50.6 %

Good + fair die yield is 62.2 %

Figure 24

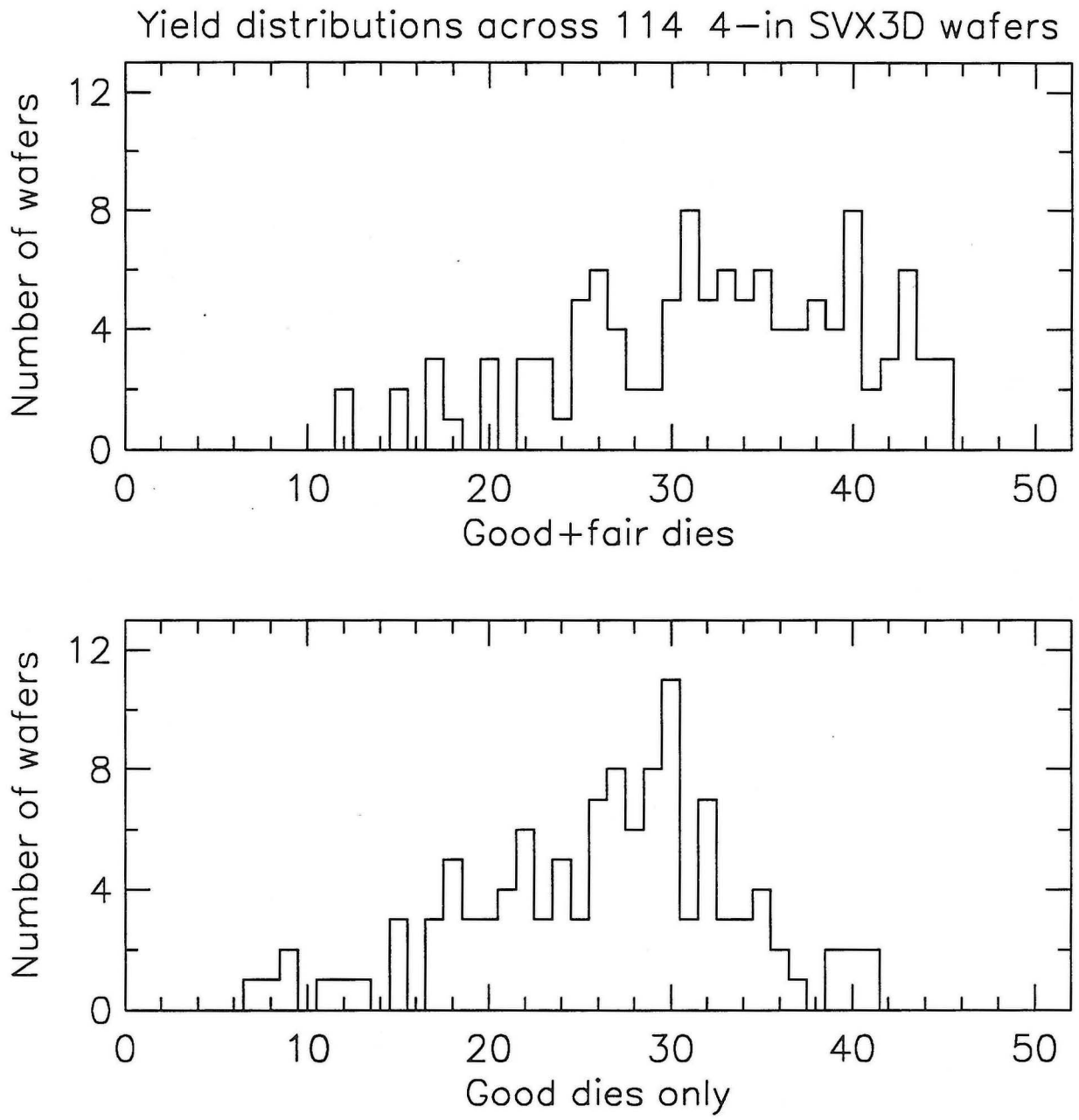

Yield distributions across 114 4−in SVX3D wafers
Number of wafers
12
8
4
0
0
10
20
30
40
50
Good+fair dies
Number of wafers
12
8
4
0
0
10
20
30
40
50
Good dies only

Figure 25

APPENDIX A

Appendix A

Die Quality Maps
(Wafer Yield Maps)

Lot	Wafer
8	1
8	3
8	4
8	6
8	11
8	15
8	17
9	2
9	3
9	5
10	1
10	2
10	8
10	10
10	18
11	3
11	5
11	11
11	18
11	20
12	4
12	11
12	12
12	15

Note: "X" indicates scratched dice.

Quality maps for the 6-in Honeywell SVX3D wafers

Click on the wafer number to get its quality map in Postscript. Pipeline quality maps for the 6-in wafers are here , and maps of die failure types are here .

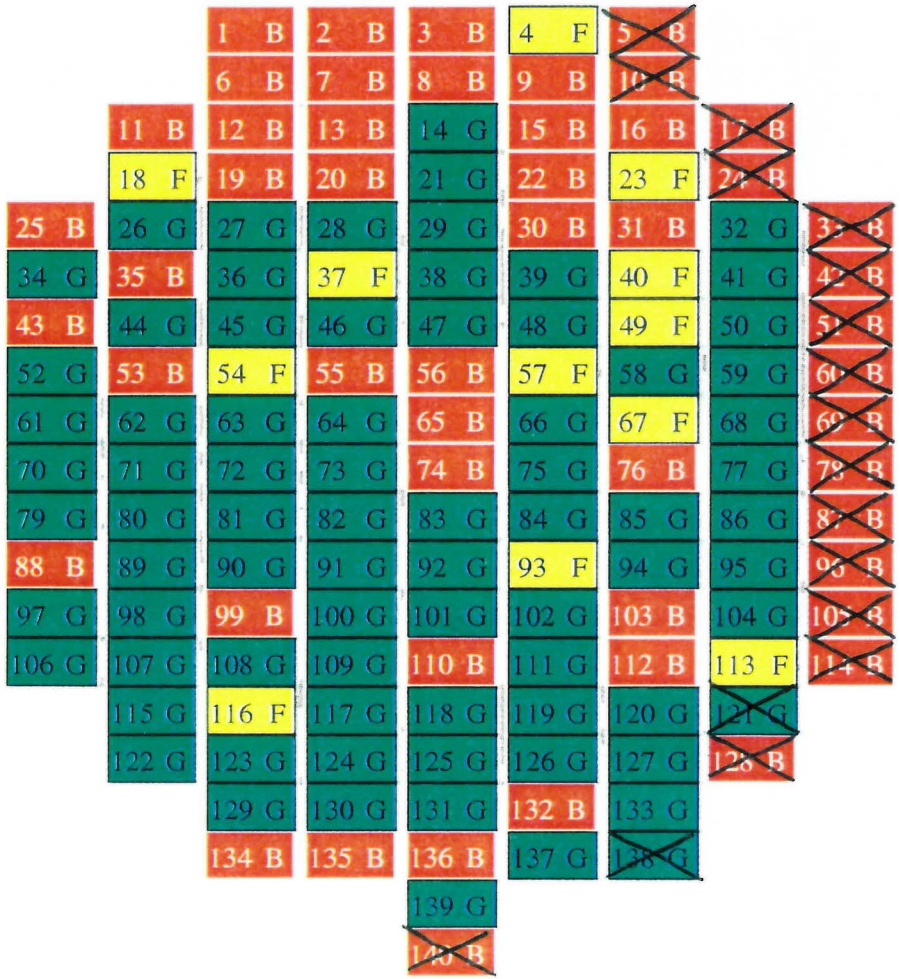
Wafer #	Manufacturer #	Good die yield (%)	Good+fair die yield (%)
69	Y21316-11-20	0.0	0.7
70	Y21316-08-03	12.9	25.0
72	Y21316-10-08	1.5	3.0
74	Y21316-09-03	30.6	47.8
76	Y21316-12-04	44.8	55.2
80	Y21316-12-15	38.8	50.0
81	Y21316-11-03	0.0	0.7
82	Y21316-12-11	38.1	47.0
83	Y21316-11-18	3.0	7.5
85	Y21316-08-04	61.4	70.7
87	Y21316-08-01	55.0	63.6
89	Y21316-10-02	0.0	0.0
91	Y21316-10-01	0.7	2.2
92	Y21316-09-02	39.6	54.5
93	Y21316-09-05	61.2	69.4
137	Y21316-12-12	44.0	58.2
138	Y21316-11-11	0.0	1.5
140	Y21316-08-17	32.9	57.1
141	Y21316-08-06	56.4	67.1
142	Y21316-08-11	37.1	53.6
143	Y21316-08-15	60.0	68.6
144	Y21316-11-05	0.7	0.7
145	Y21316-10-18	3.7	11.2
146	Y21316-10-10	0.0	1.5

These 6-in wafers were not backgrinded and backplated

Questions? E-mail to igv@kfesg.lbl.gov

Die quality map for wafer 87 s/n: Y21316-08-01 (not backplated)

Date: 01/14/99



B Bad die

F Fair die

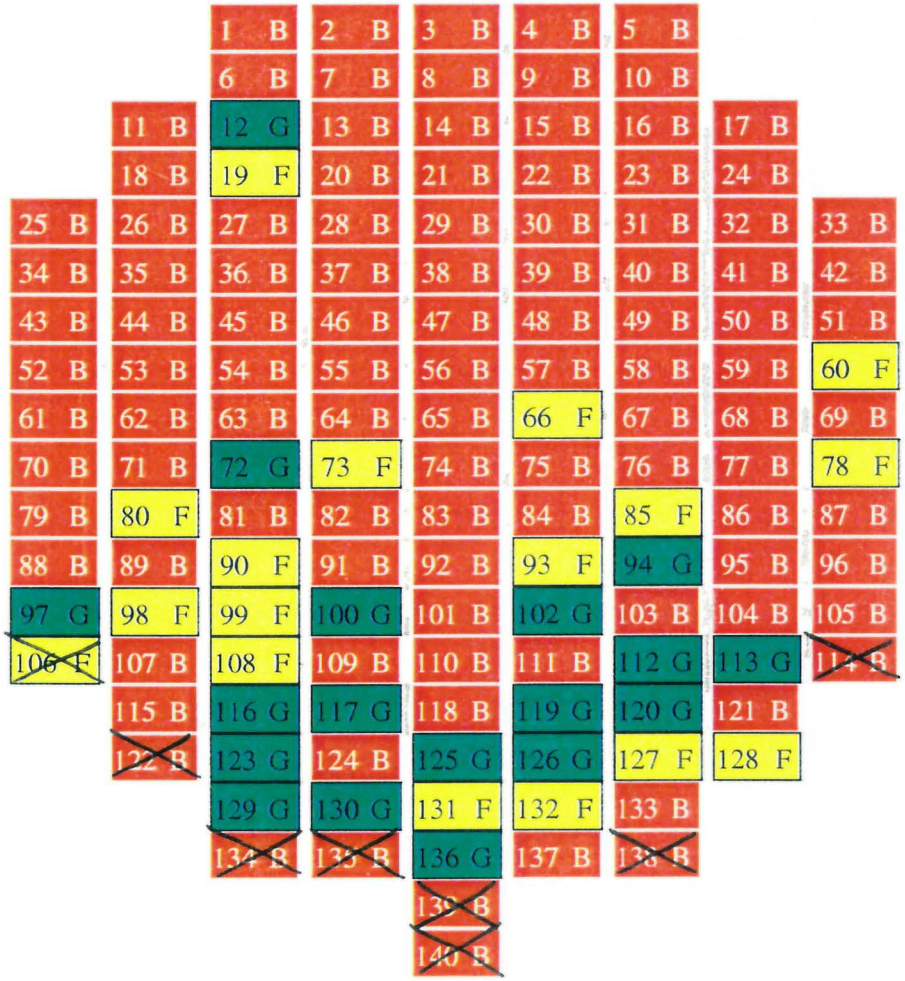
G Good die

N No info

* Manually tagged

Die quality map for wafer 70 s/n: Y21316-08-03 (not backplated)

Date: 12/18/98



B Bad die

F Fair die

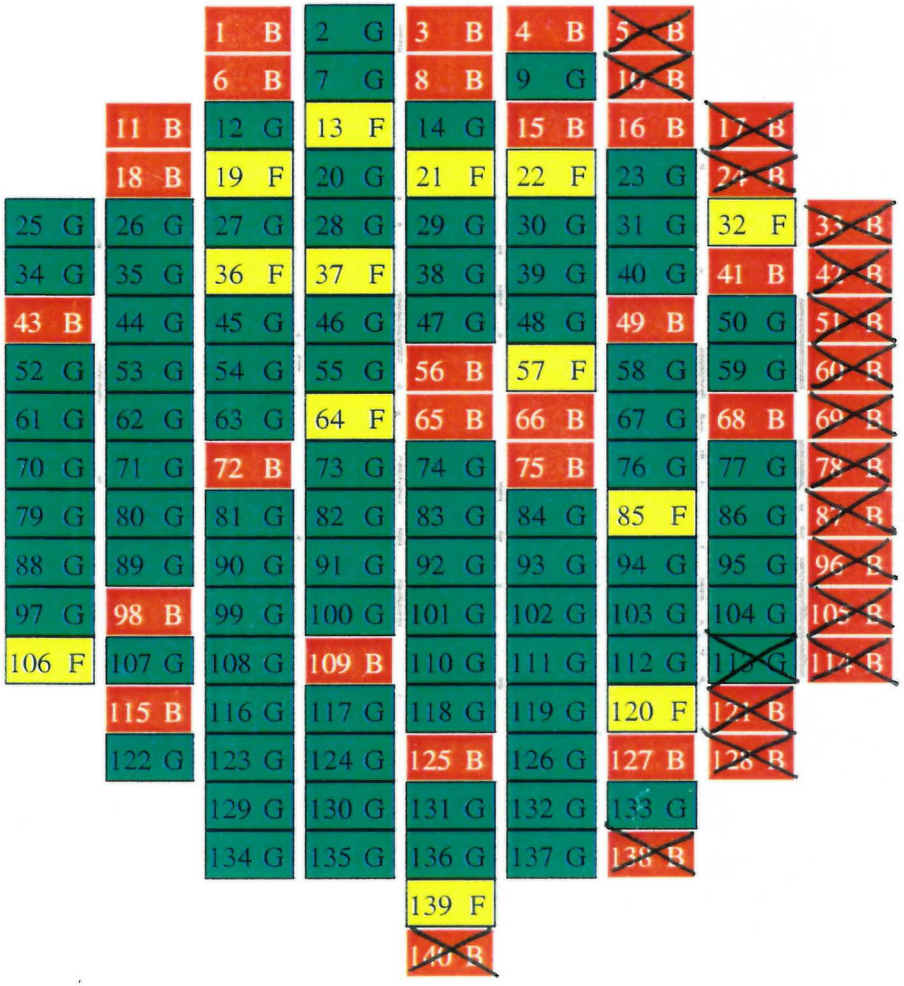
G Good die

N No info

* Manually tagged

Die quality map for wafer 85 s/n: Y21316-08-04 (not backplated)

Date: 01/14/99



B Bad die

F Fair die

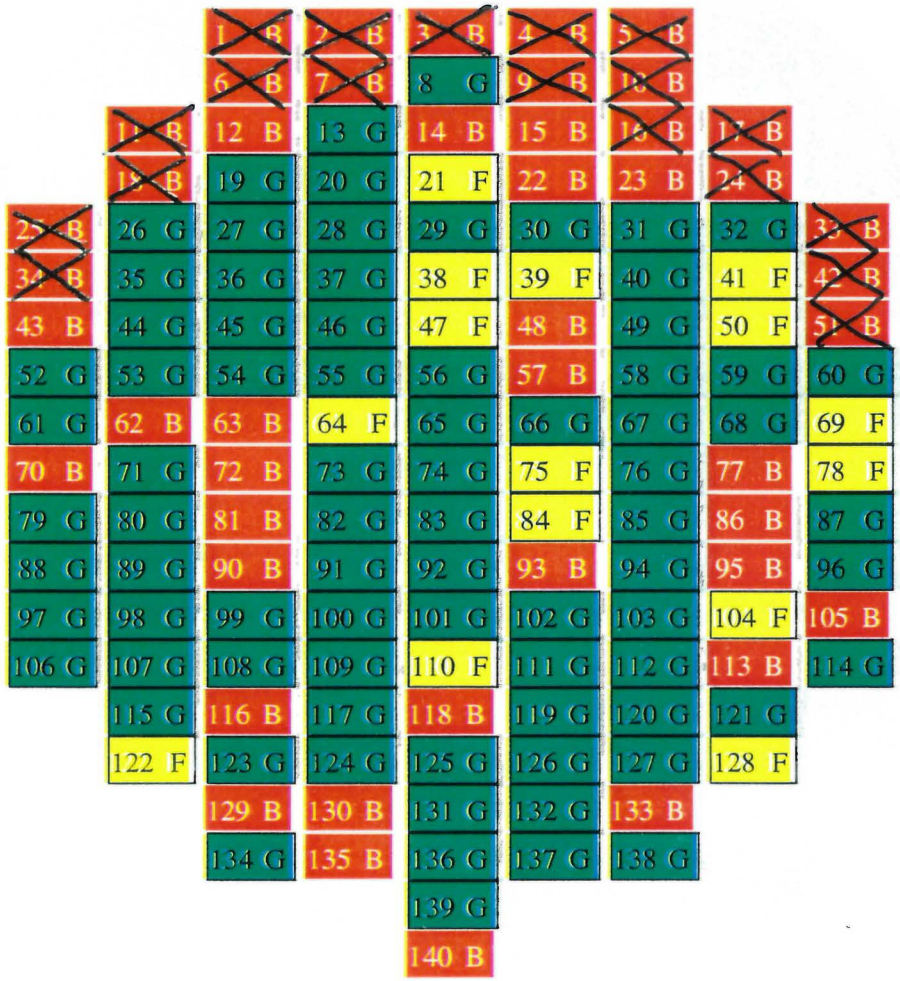
G Good die

N No info

* Manually tagged

Die quality map for wafer 141 s/n: Y21316-08-06 (not backplated)

Date: 03/24/99



B Bad die

F Fair die

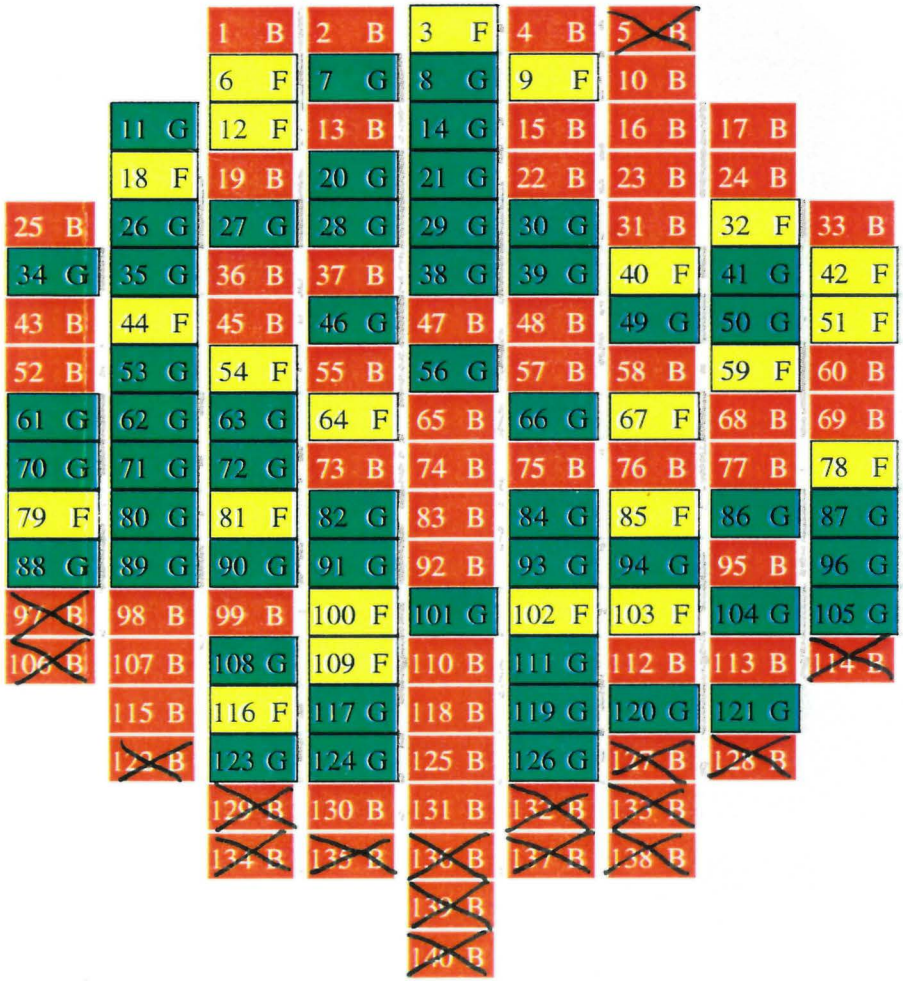
G Good die

N No info

* Manually tagged

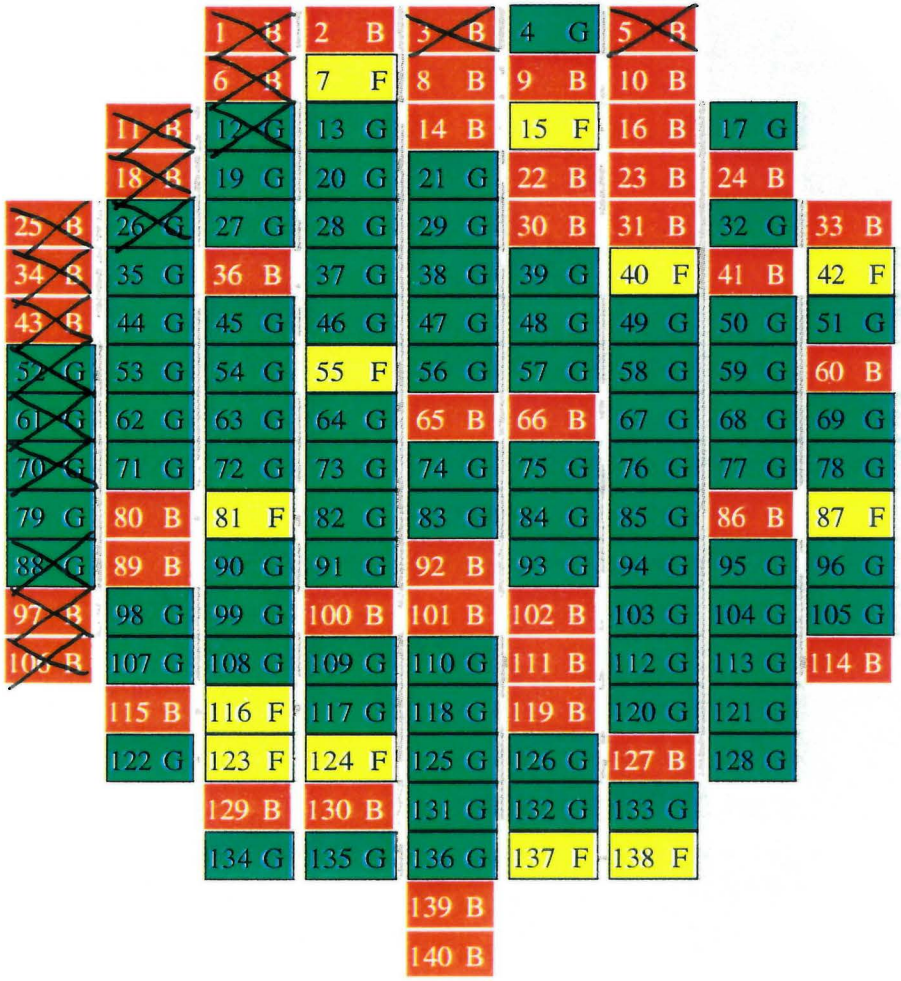
Die quality map for wafer 142 s/n: Y21316-08-11 (not backplated)

Date: 03/25/99



Die quality map for wafer 143 s/n: Y21316-08-15 (not backplated)

Date: 03/26/99



B Bad die

F Fair die

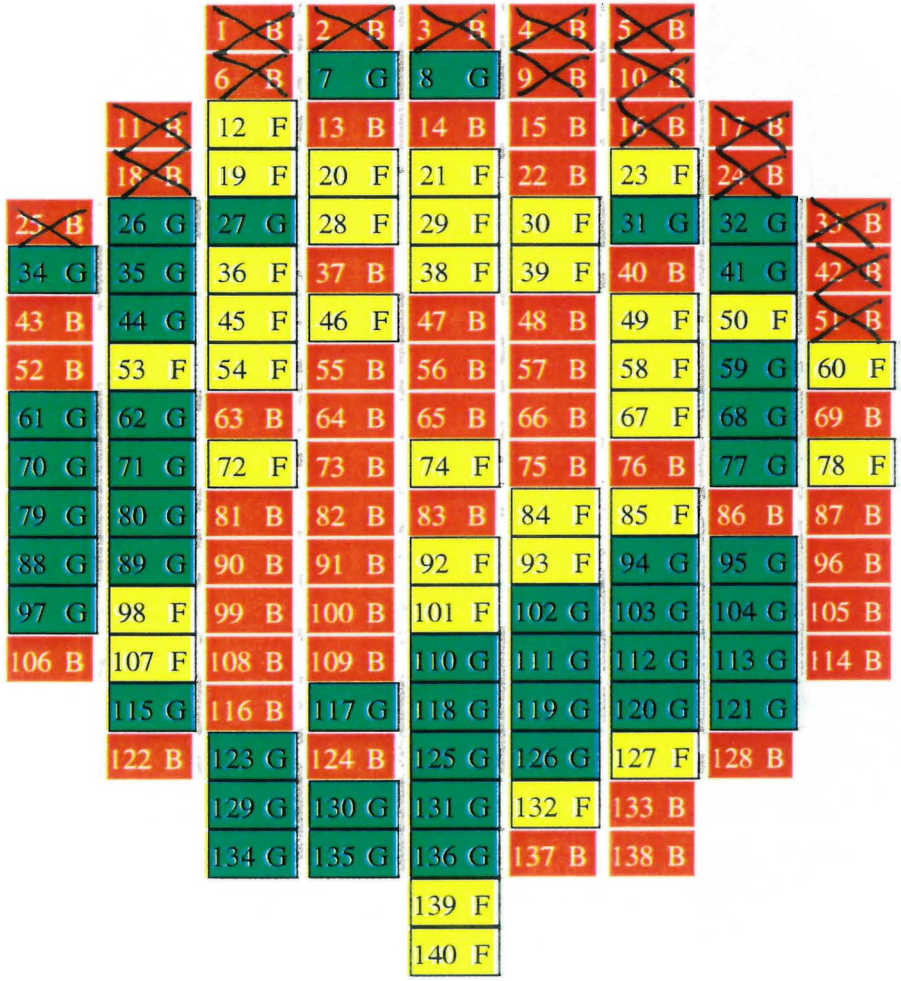
G Good die

N No info

* Manually tagged

Die quality map for wafer 140 s/n: Y21316-08-17 (not backplated)

Date: 03/23/99



B Bad die

F Fair die

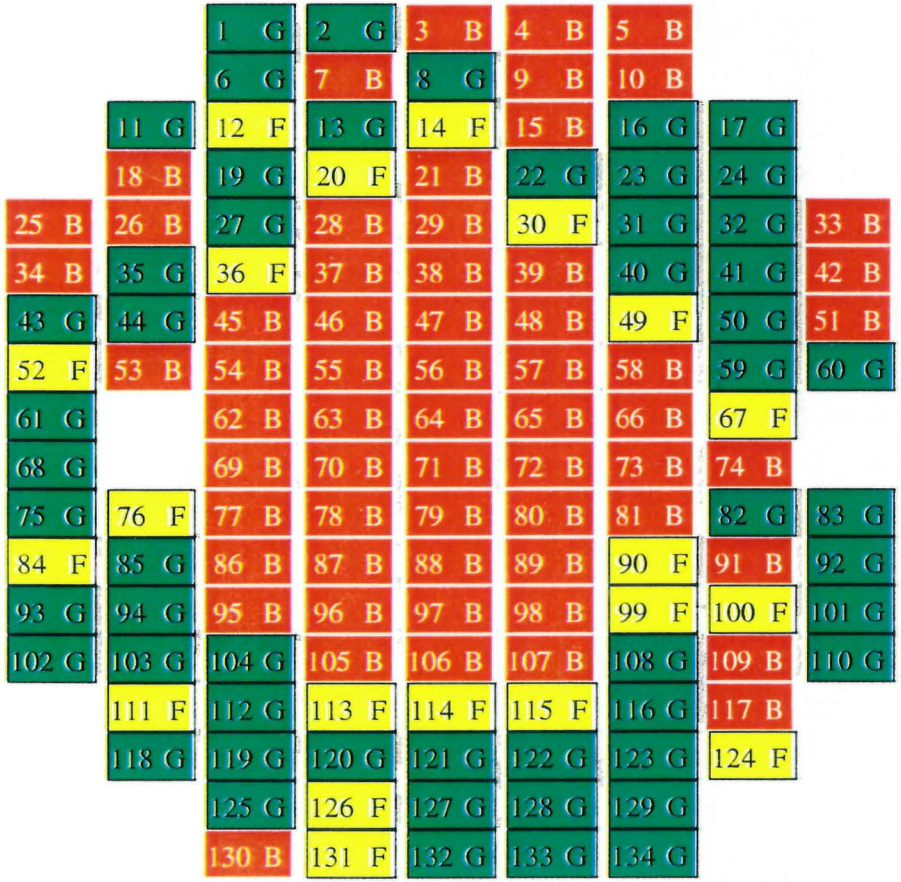
G Good die

N No info

* Manually tagged

Die quality map for wafer 92 s/n: Y21316-09-02 (not backplated)

Date: 01/19/99



B Bad die

F Fair die

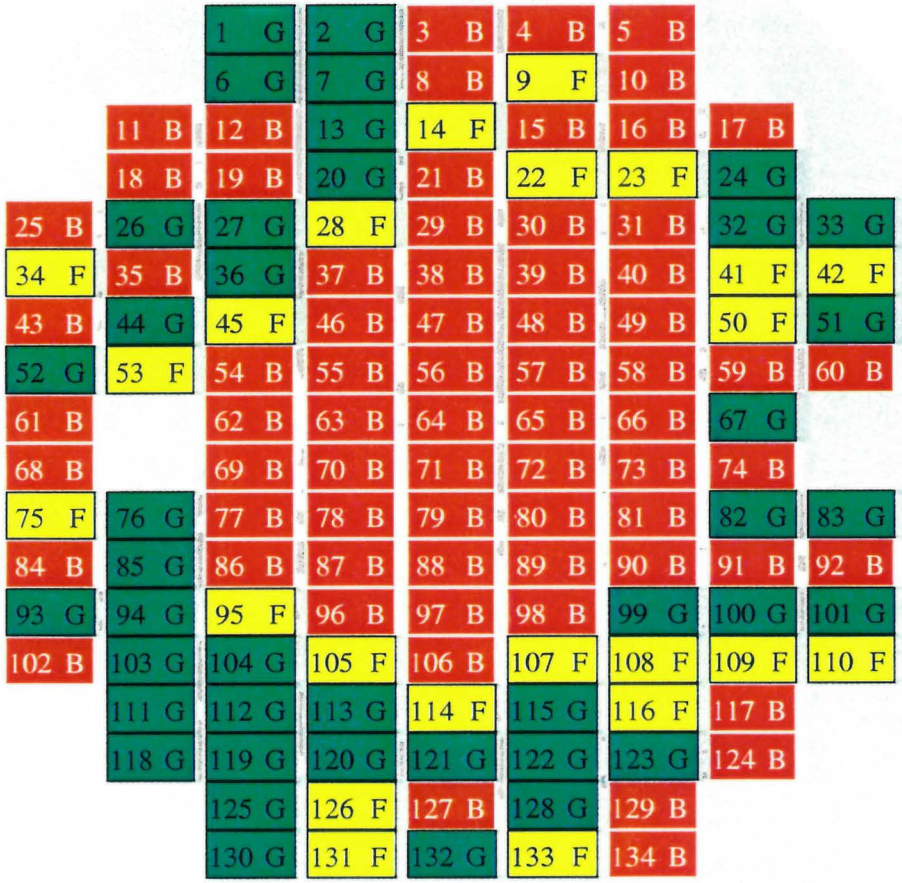
G Good die

N No info

* Manually tagged

Die quality map for wafer 74 s/n: Y21316-09-03 (not backplated)

Date: 12/23/98



B Bad die

F Fair die

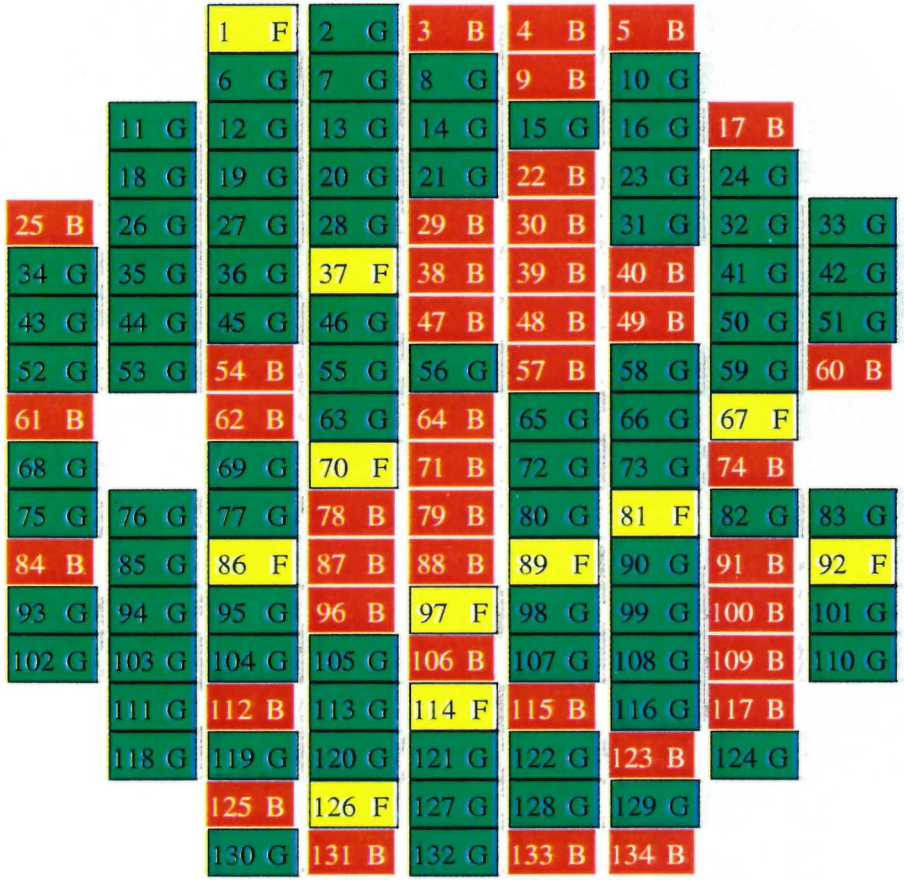
G Good die

N No info

* Manually tagged

Die quality map for wafer 93 s/n: Y21316-09-05 (not backplated)

Date: 01/19/99



B Bad die

F Fair die

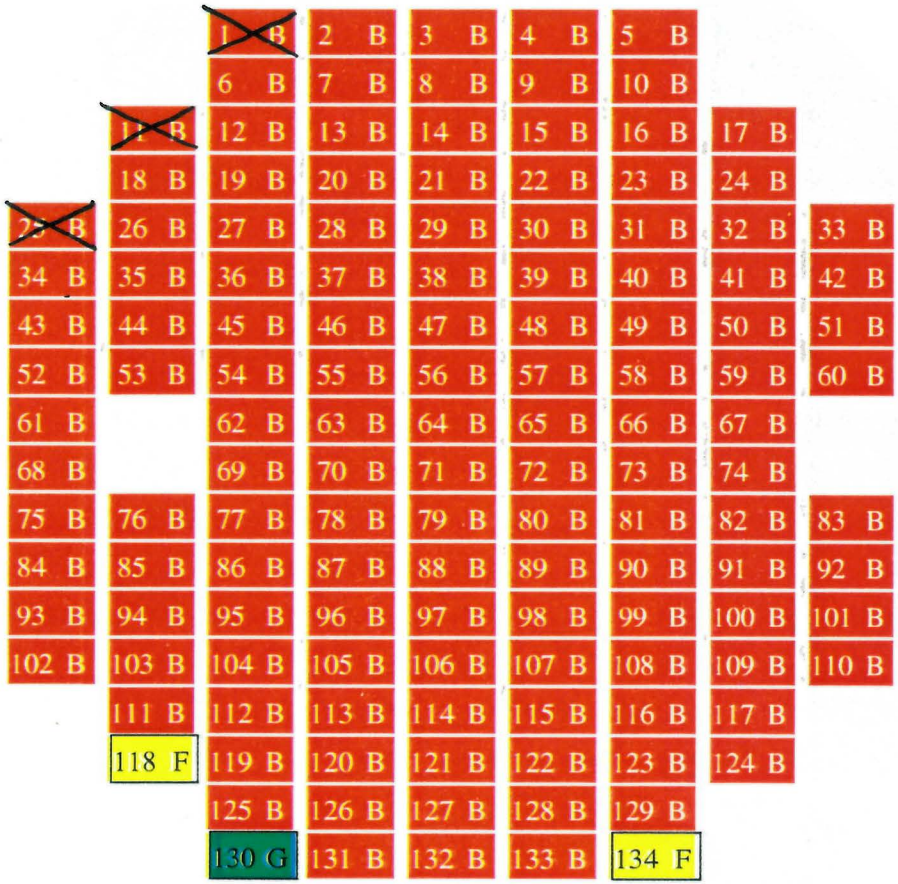
G Good die

N No info

* Manually tagged

Die quality map for wafer 91 s/n: Y21316-10-01 (not backplated)

Date: 01/19/99



B Bad die

F Fair die

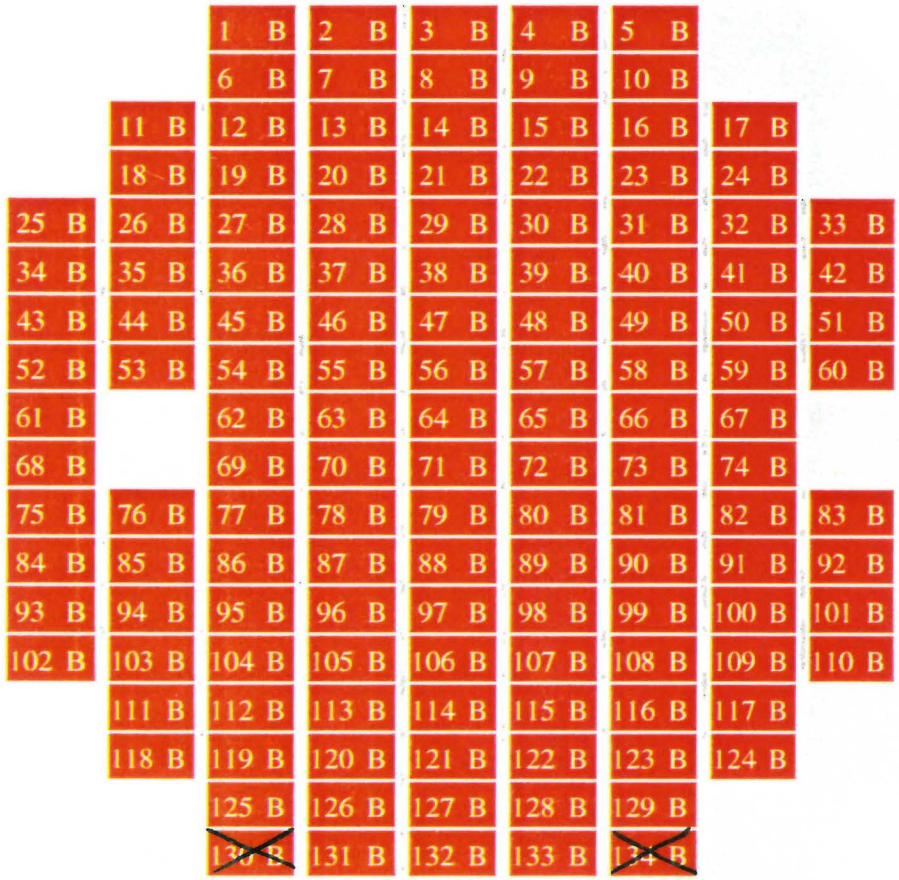
G Good die

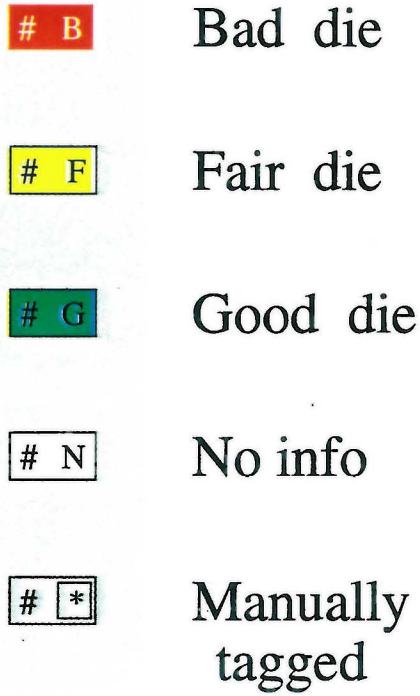
N No info

* Manually tagged

Die quality map for wafer 89 s/n: Y21316-10-02 (not backplated)

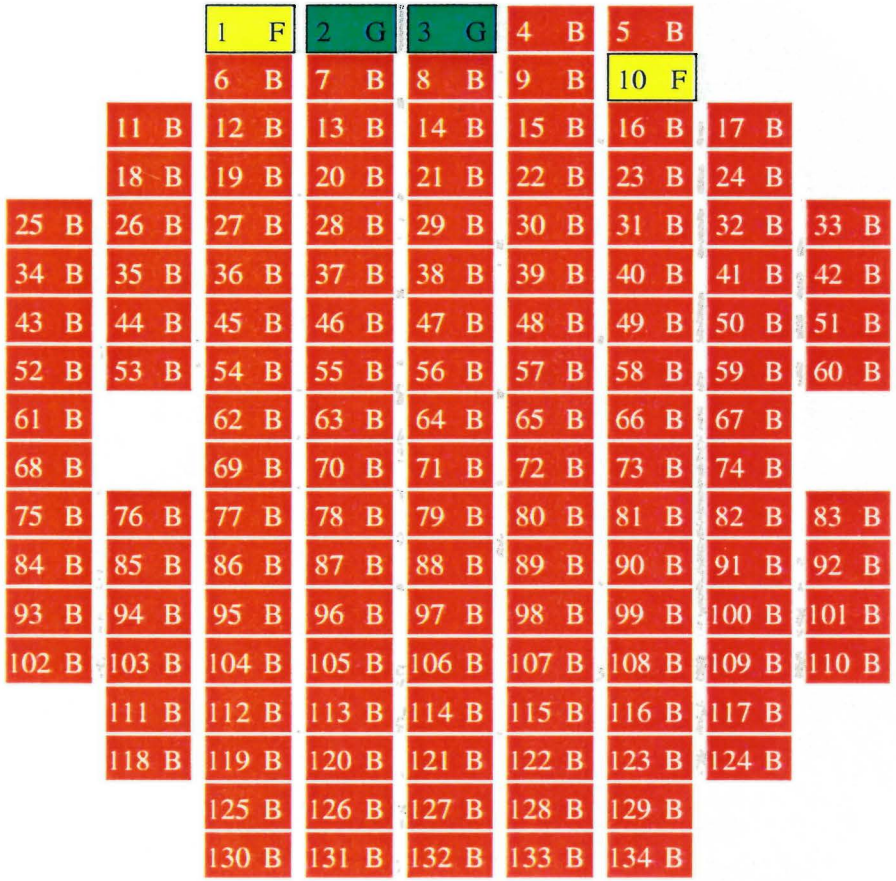
Date: 01/19/99





Die quality map for wafer 72 s/n: Y21316-10-08 (not backplated)

Date: 12/22/98



B Bad die

F Fair die

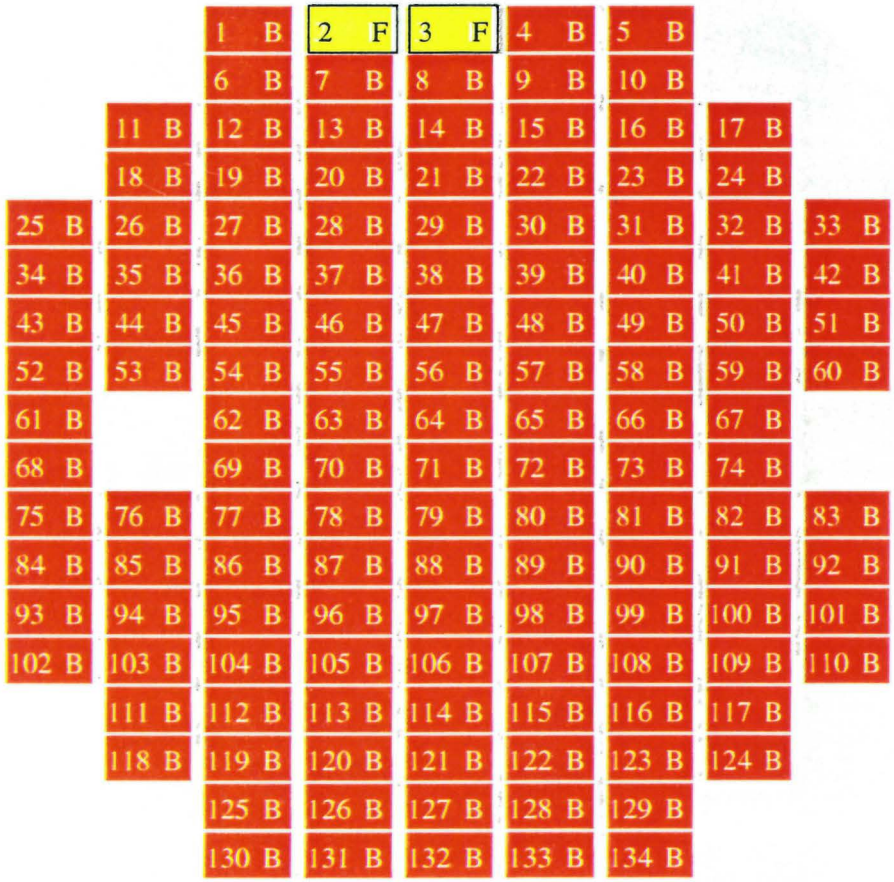
G Good die

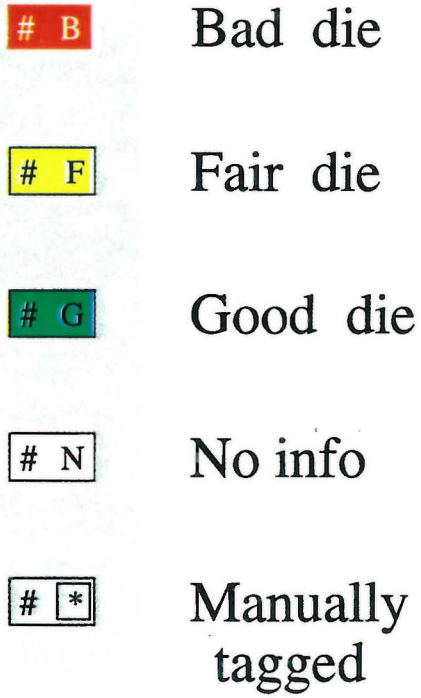
N No info

* Manually tagged

Die quality map for wafer 146 s/n: Y21316-10-10 (not backplated)

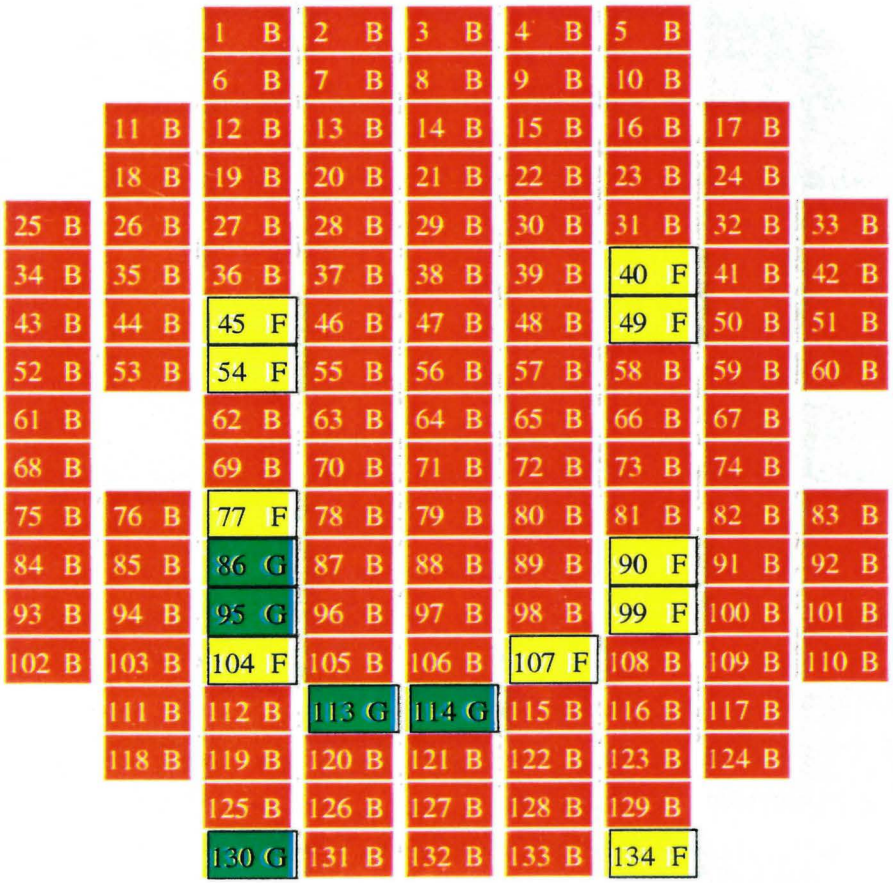
Date: 04/14/99

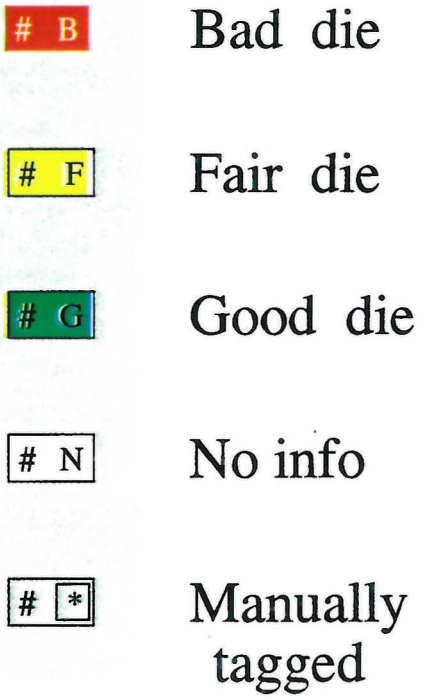




Die quality map for wafer 145 s/n: Y21316-10-18 (not backplated)

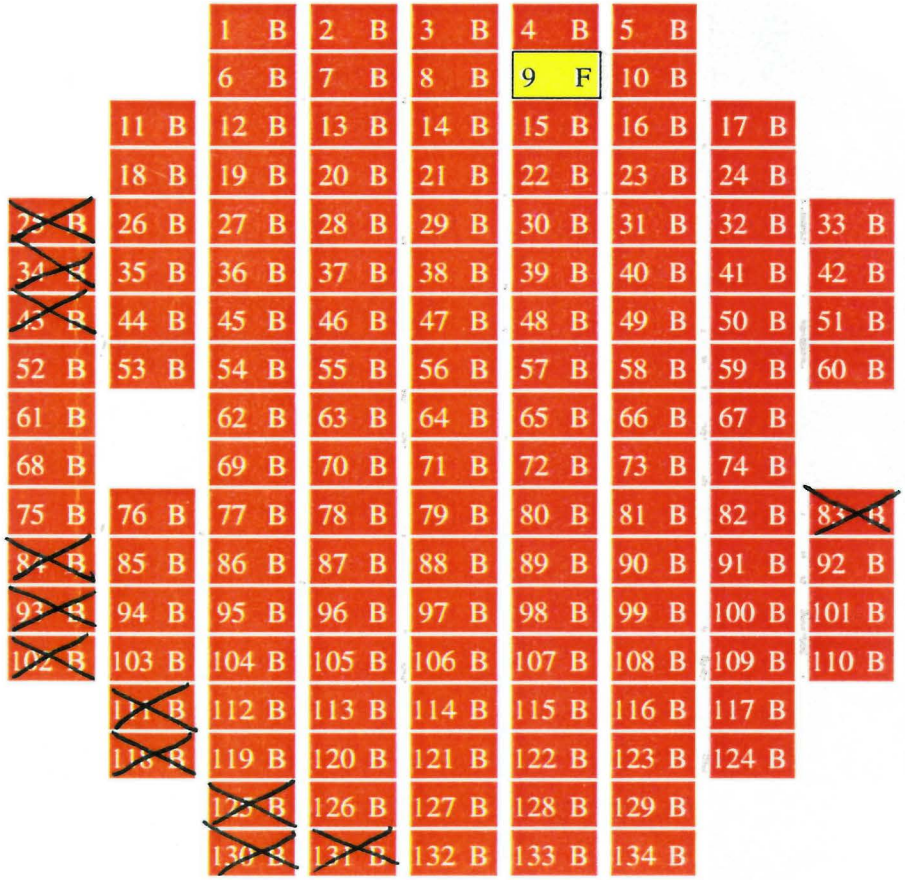
Date: 04/13/99





Die quality map for wafer 81 s/n: Y21316-11-03 (not backplated)

Date: 01/12/99



B Bad die

F Fair die

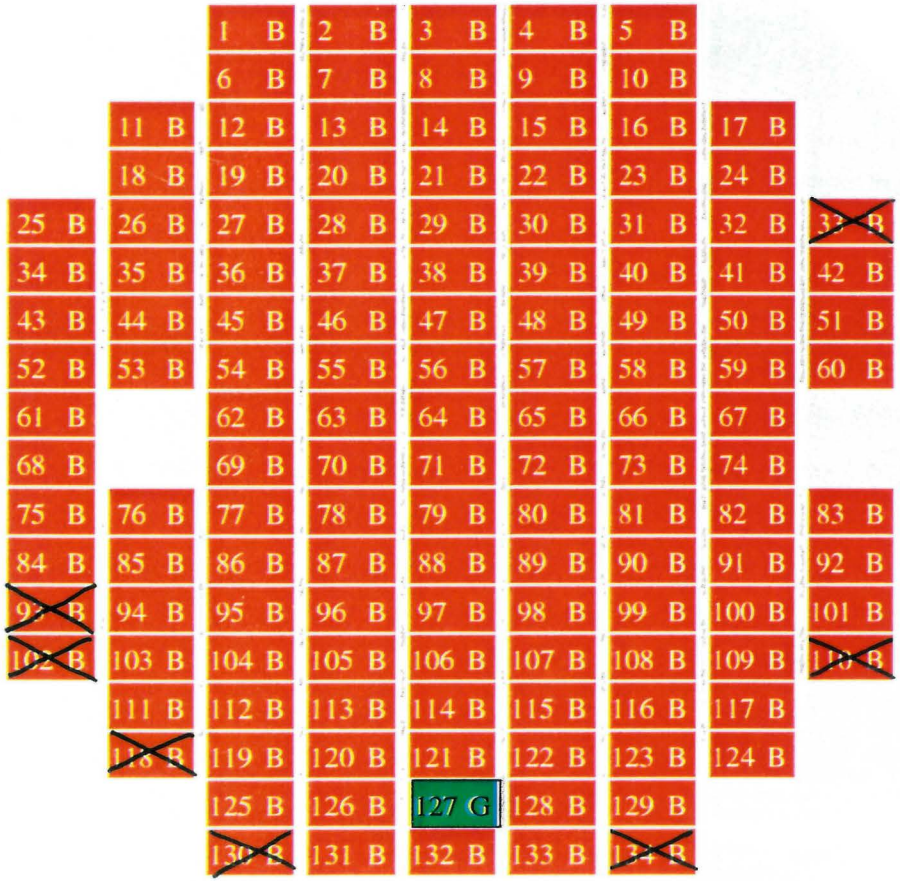
G Good die

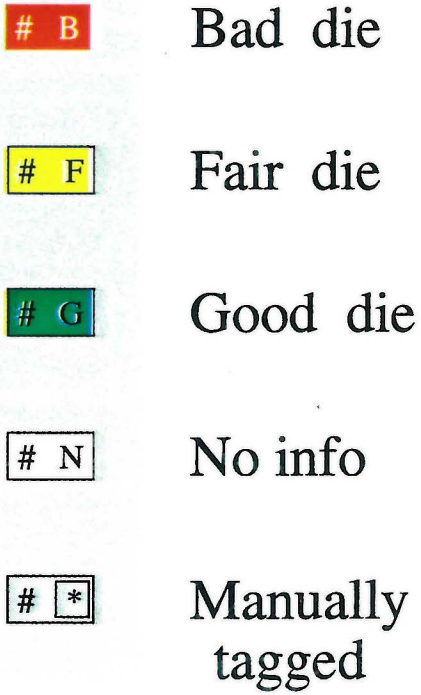
N No info

* Manually tagged

Die quality map for wafer 144 s/n: Y21316-11-05 (not backplated)

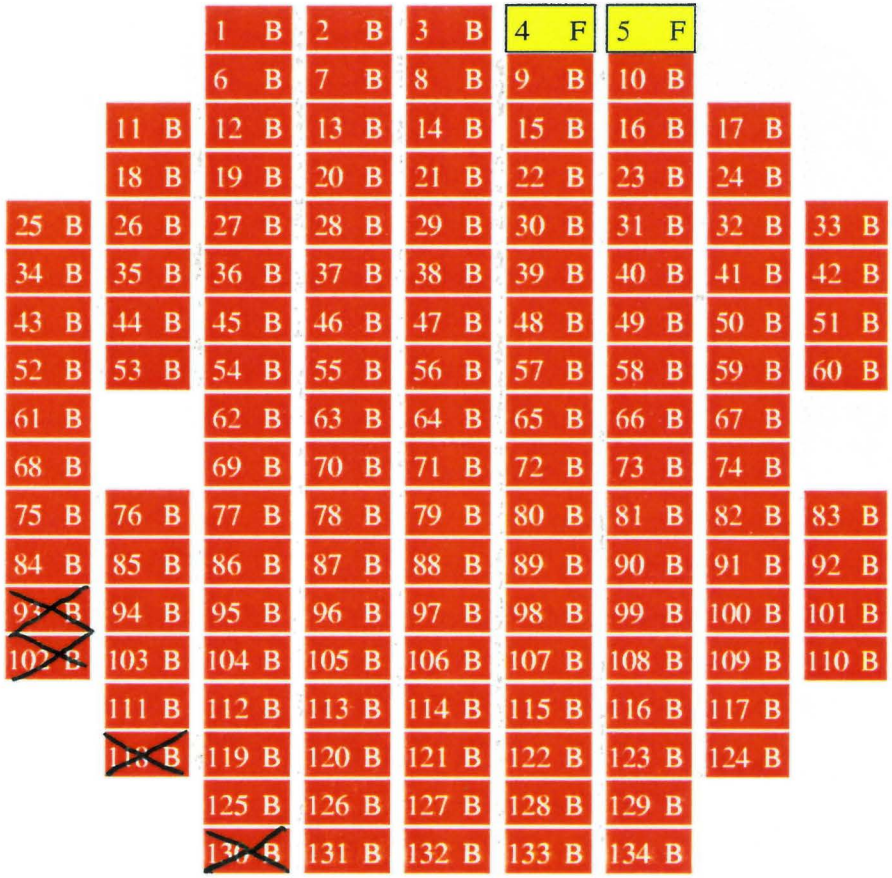
Date: 04/09/99





Die quality map for wafer 138 s/n: Y21316-11-11 (not backplated)

Date: 03/18/99



B Bad die

F Fair die

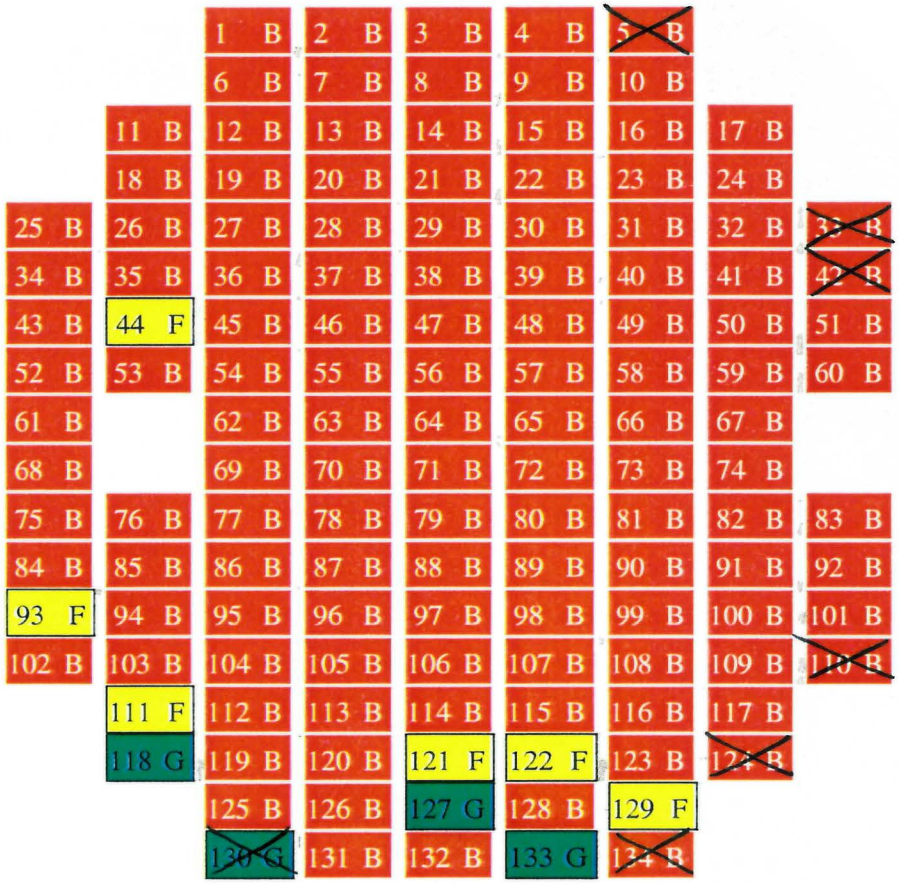
G Good die

N No info

* Manually tagged

Die quality map for wafer 83 s/n: Y21316-11-18 (not backplated)

Date: 01/12/99



B Bad die

F Fair die

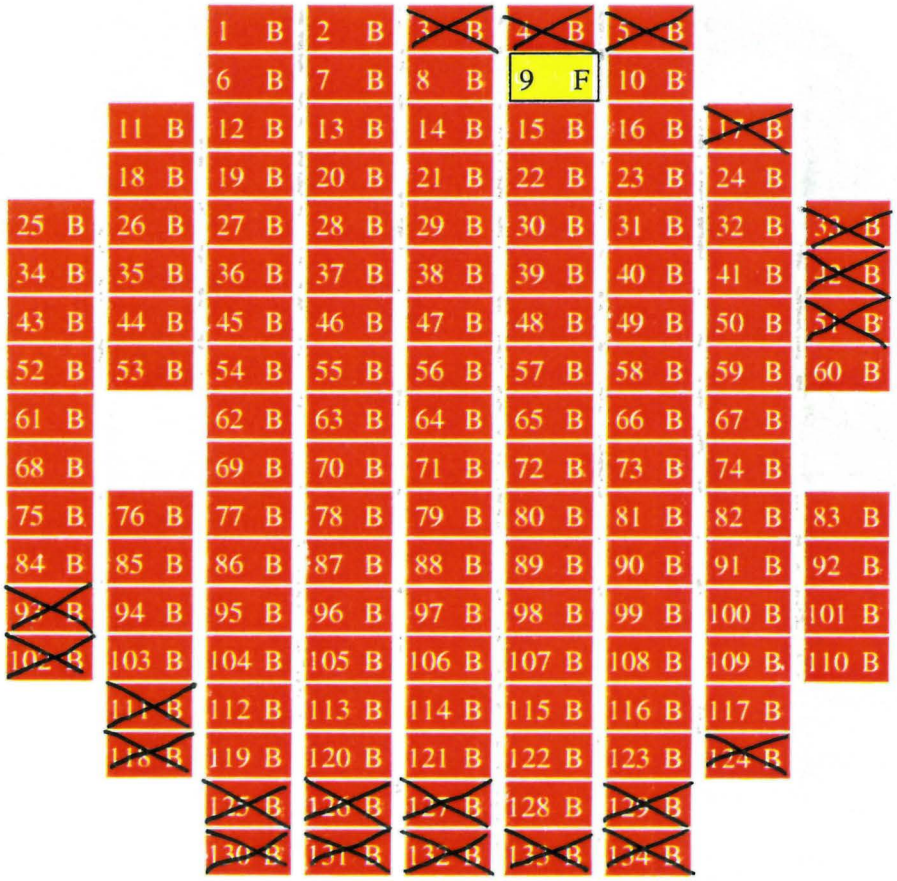
G Good die

N No info

* Manually tagged

Die quality map for wafer 69 s/n: Y21316-11-20 (not backplated)

Date: 12/17/98



B Bad die

F Fair die

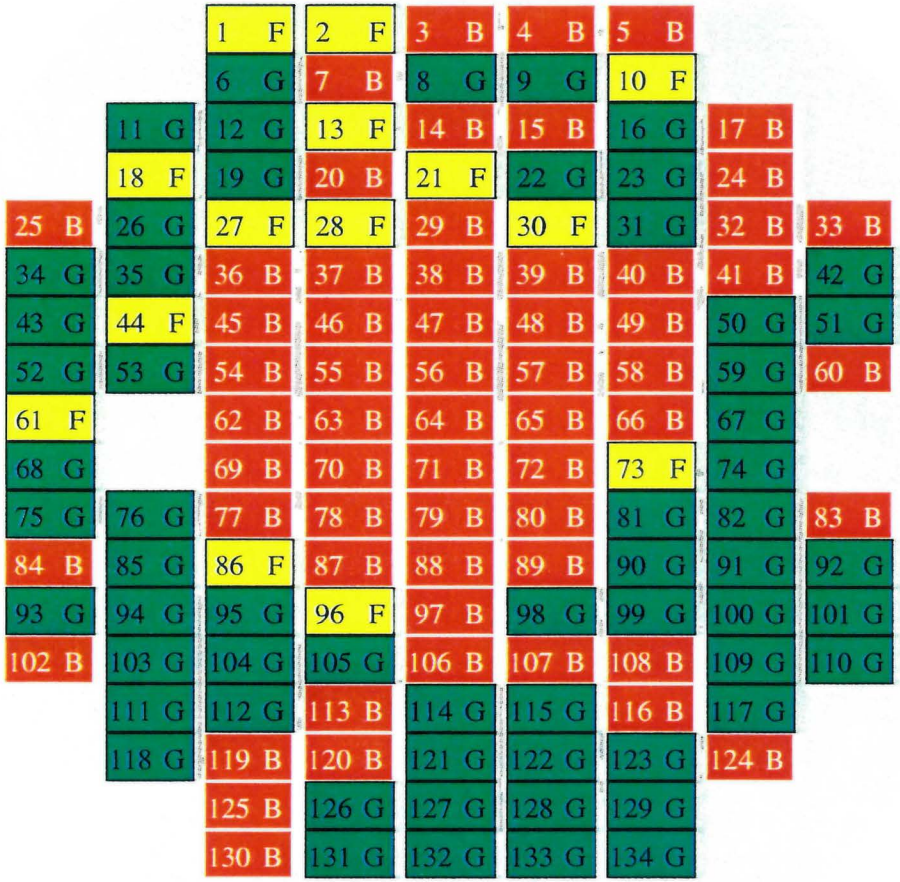
G Good die

N No info

* Manually tagged

Die quality map for wafer 76 s/n: Y21316-12-04 (not backplated)

Date: 01/05/99



B Bad die

F Fair die

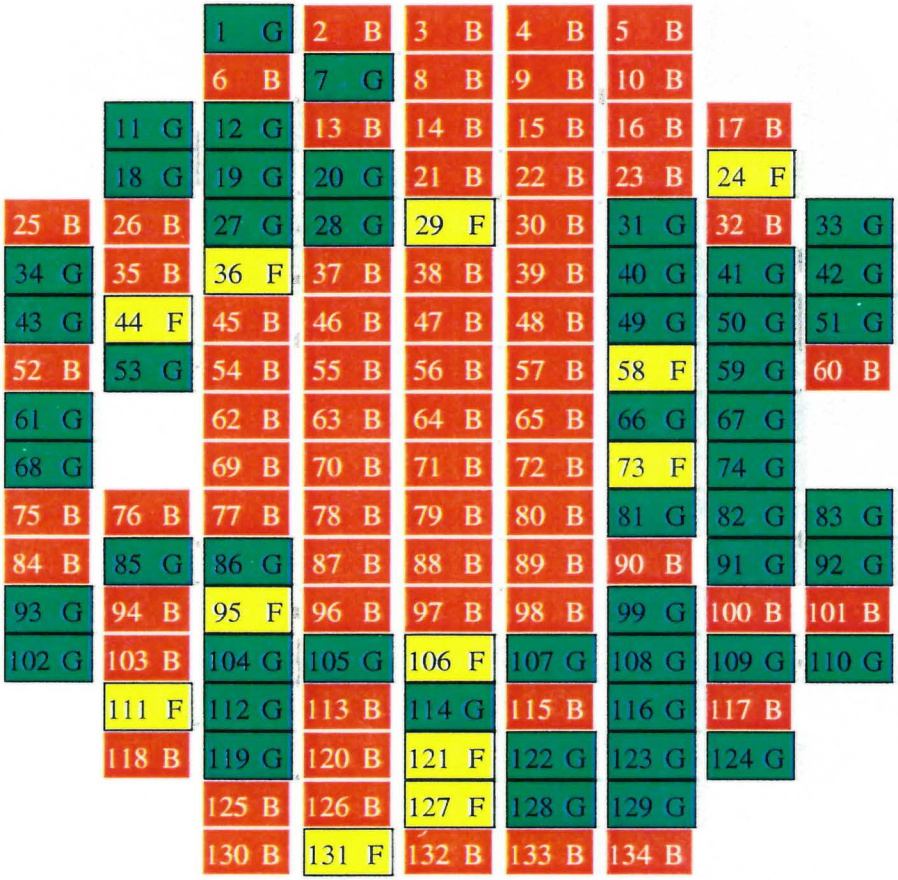
G Good die

N No info

* Manually tagged

Die quality map for wafer 82 s/n: Y21316-12-11 (not backplated)

Date: 01/12/99



B Bad die

F Fair die

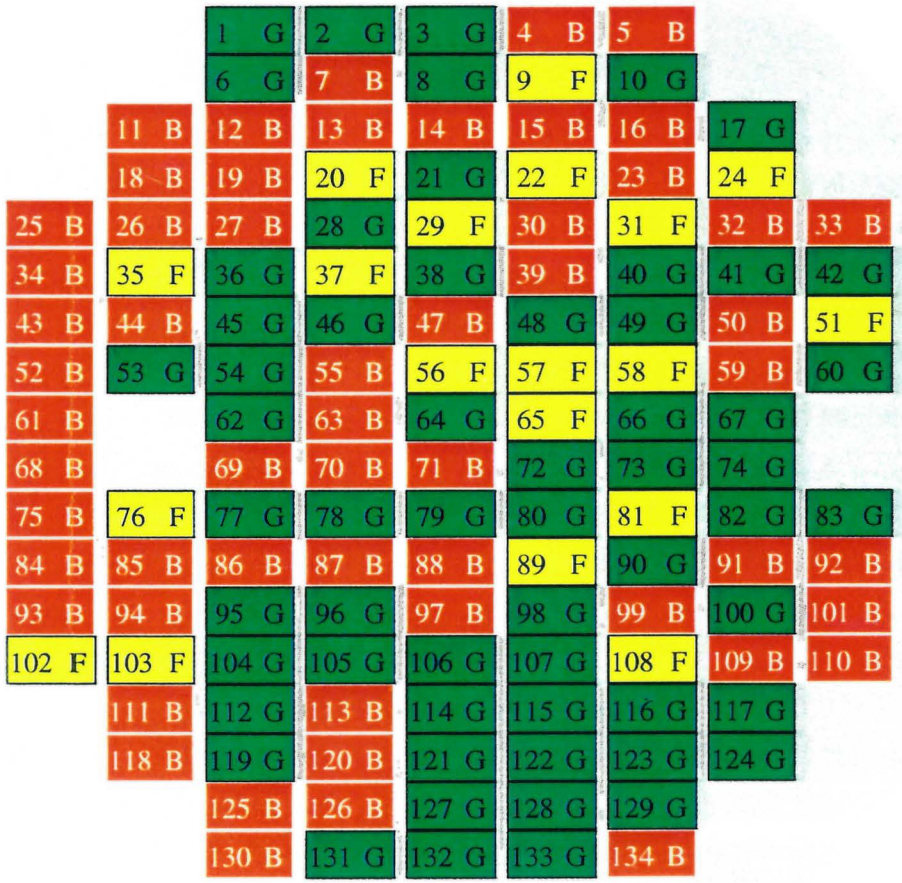
G Good die

N No info

* Manually tagged

Die quality map for wafer 137 s/n: Y21316-12-12 (not backplated)

Date: 03/18/99



B Bad die

F Fair die

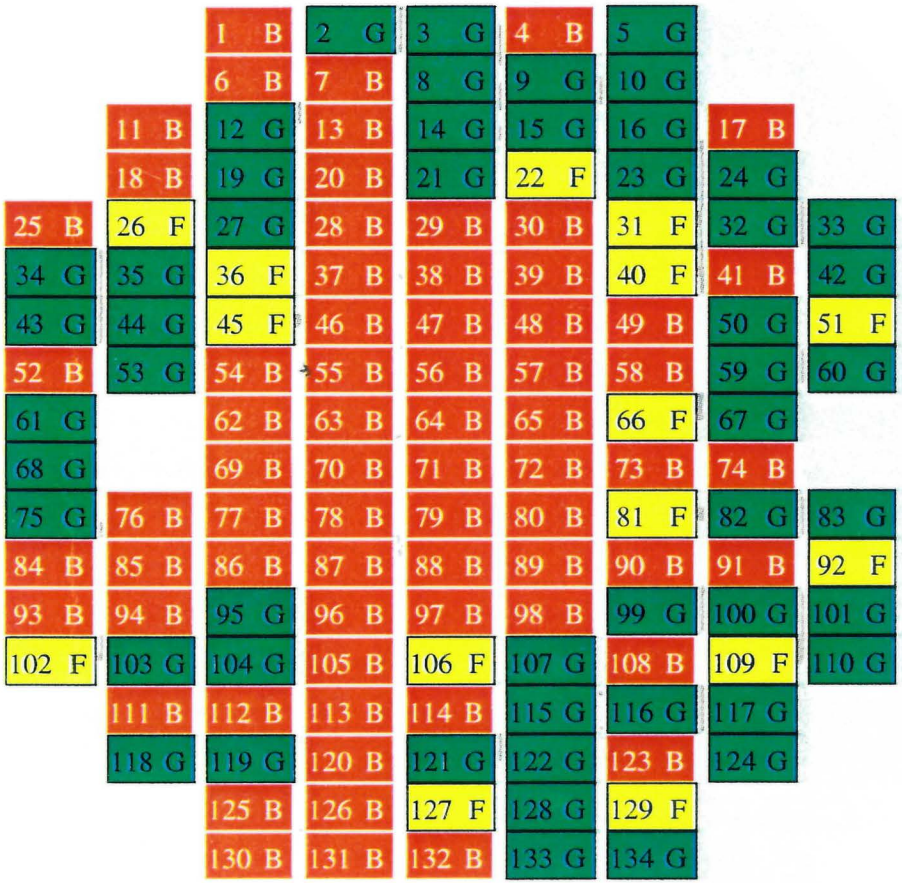
G Good die

N No info

* Manually tagged

Die quality map for wafer 80 s/n: Y21316-12-15 (not backplated)

Date: 01/12/99



B Bad die

F Fair die

G Good die

N No info

* Manually tagged

APPENDIX B

Appendix B

Capacitor Quality Maps
(Capacitor Pedestal Problem Map)

Lot	Wafer
8	1
8	3
8	4
8	6
8	11
8	15
8	17
9	2
9	3
9	5
10	1
10	2
10	8
10	10
10	18
11	3
11	5
11	11
11	18
11	20
12	4
12	11
12	12
12	15

Pipeline quality maps for the 6-in Honeywell SVX3D wafers

Click on the wafer number in the table below to get its pipeline quality map in Postscript. Standard 6-in wafer quality maps are here.

Only pedestal/noise and calibration mask tests are used to create the maps linked to this page.

In these maps the fractions of bad pipeline cells are represented with rectangles in the middle of the dies. The area of these rectangles is proportional to the total number of bad cells. The whole die area corresponds to all 5888 cells in the pipeline. If all or almost all pipeline cells are bad in a given channel then it is perhaps the preamp or the reference cell (or some other channel circuitry) which doesn't function properly. As such, the middle rectangles are color coded. The red area is proportional to the number of pipeline cells associated with bad channels (for these plots a channel is bad if more than 90% of its pipeline cells didn't pass the tests). The black area is proportional to the number of bad cells which are not associated with bad channels. Such cells are usually distributed more or less randomly across the pipeline.

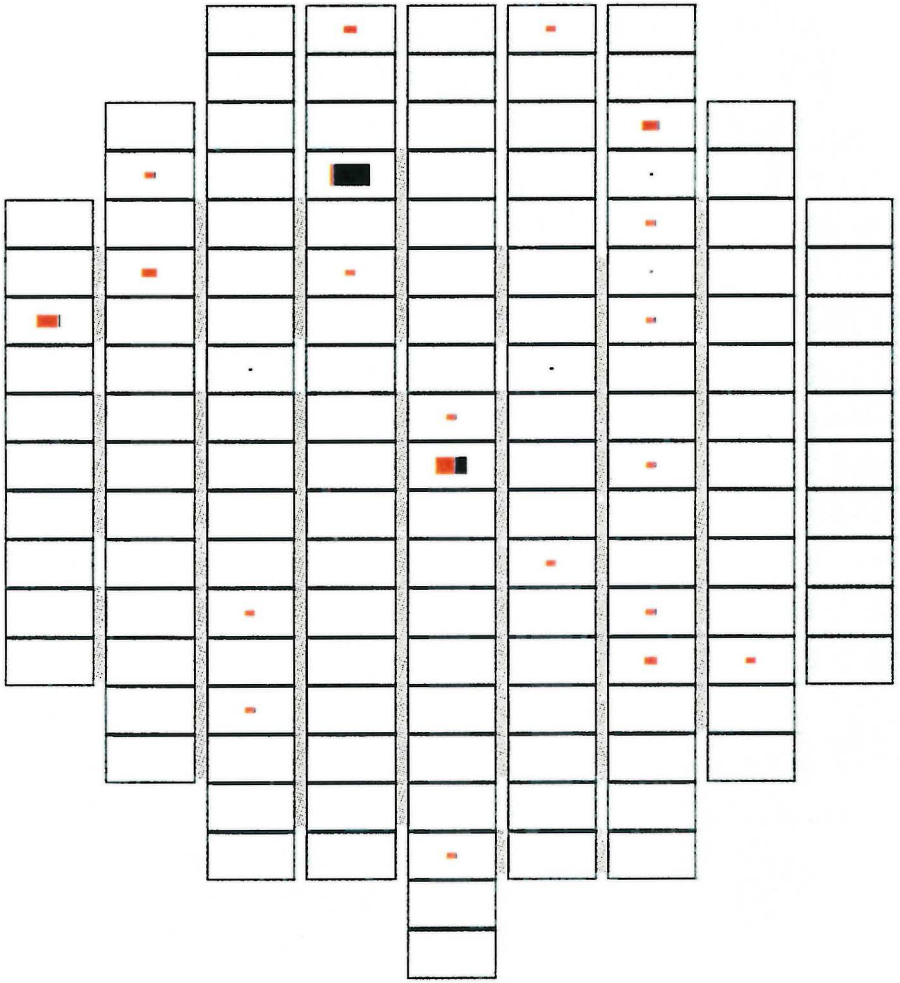
The "no info" dies are those dies which were rejected by the testing procedure before the pedestal/noise measurements.

Wafer #	Manufacturer #
69	Y21316-11-20
70	Y21316-08-03
72	Y21316-10-08
74	Y21316-09-03
76	Y21316-12-04
80	Y21316-12-15
81	Y21316-11-03
82	Y21316-12-11
83	Y21316-11-18
85	Y21316-08-04
87	Y21316-08-01
89	Y21316-10-02
91	Y21316-10-01
92	Y21316-09-02
93	Y21316-09-05
137	Y21316-12-12
138	Y21316-11-11
140	Y21316-08-17
141	Y21316-08-06
142	Y21316-08-11
143	Y21316-08-15
144	Y21316-11-05
145	Y21316-10-18
146	Y21316-10-10

Questions? E-mail to igv@kfesg.lbl.gov

Capacitor quality map for wafer 87 s/n: Y21316-08-01 (not backplated)

Date: 01/15/99



Caps in bad channels

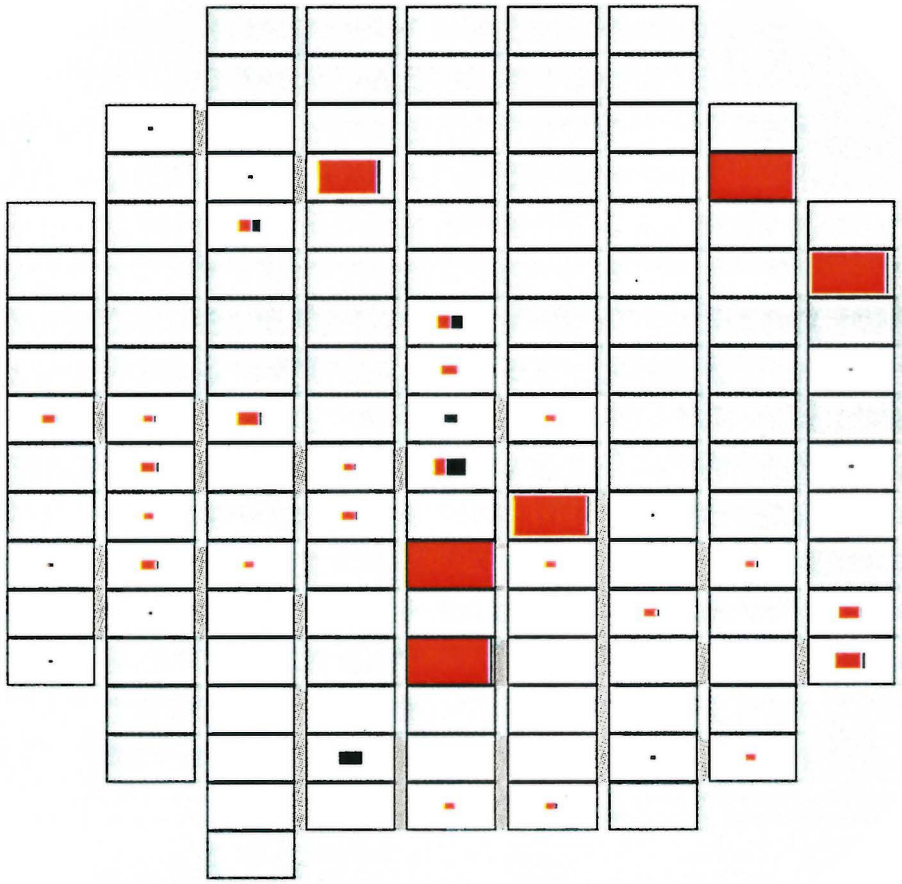
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 70 s/n: Y21316-08-03 (not backplated)

Date: 01/14/99



Caps in bad channels

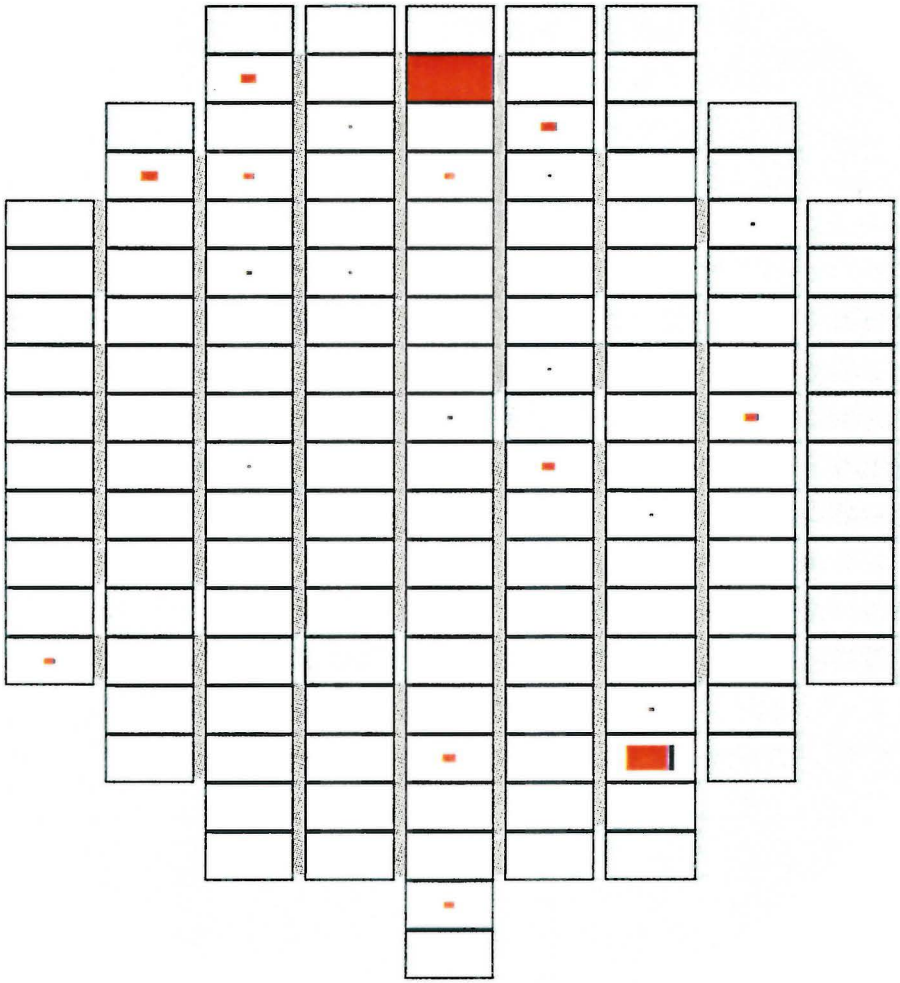
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 85 s/n: Y21316-08-04 (not backplated)

Date: 01/14/99



Caps in bad channels

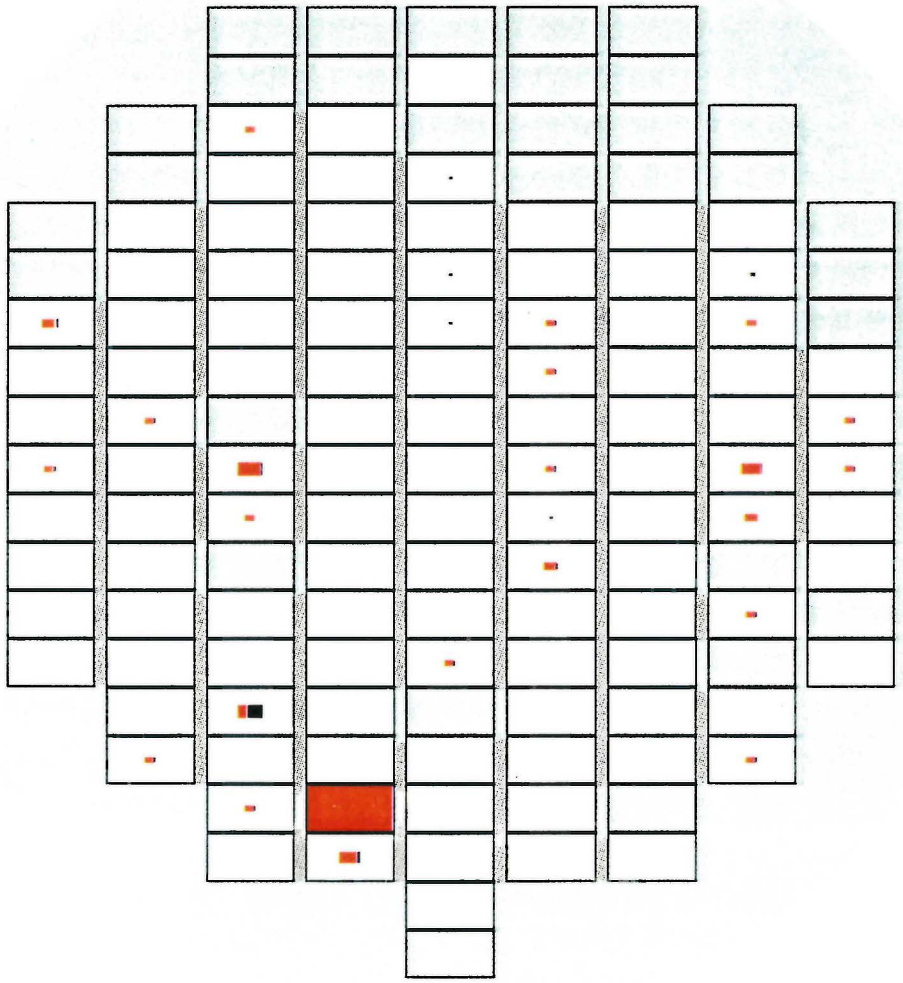
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 141 s/n: Y21316-08-06 (not backplated)

Date: 03/24/99



Caps in bad channels

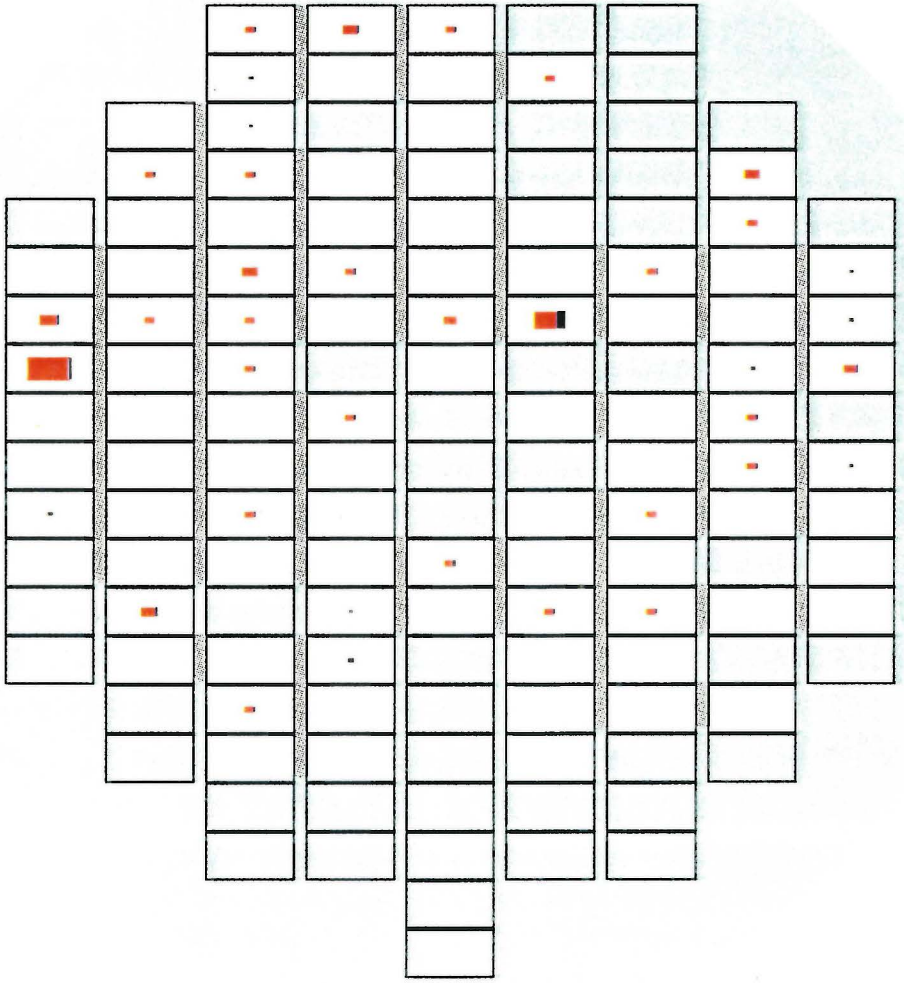
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 142 s/n: Y21316-08-11 (not backplated)

Date: 03/25/99



Caps in bad channels

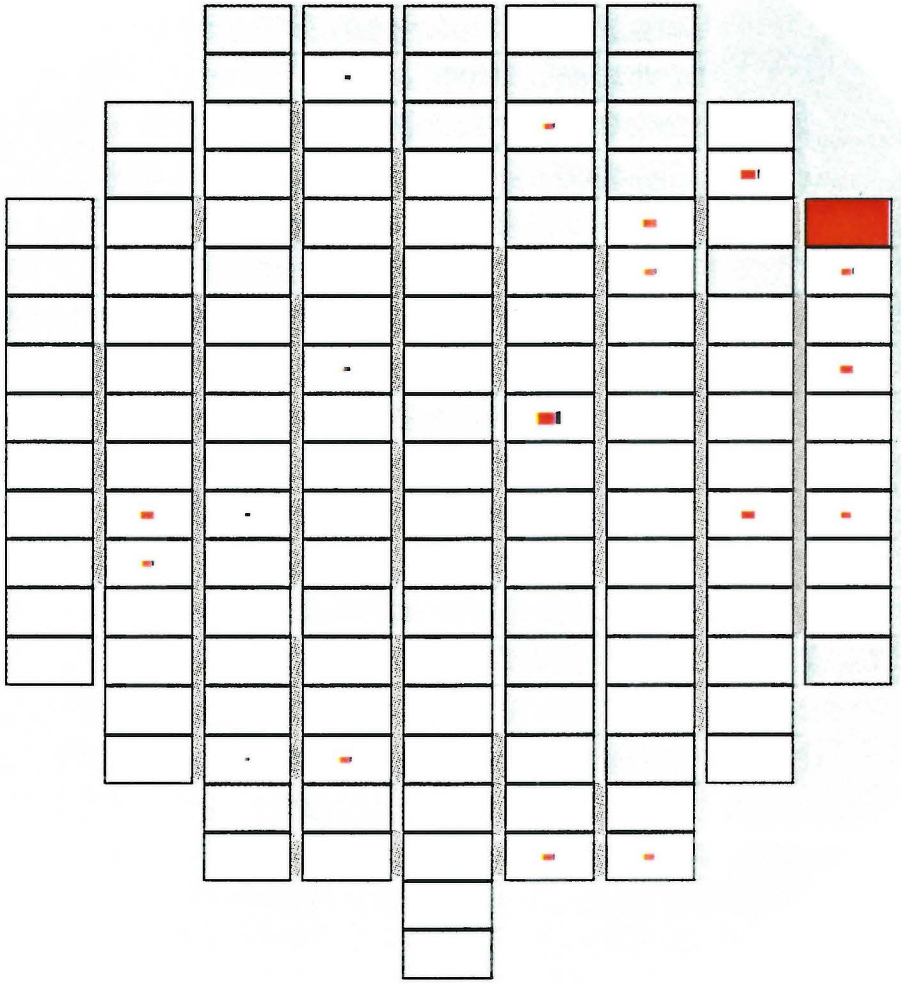
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 143 s/n: Y21316-08-15 (not backplated)

Date: 03/26/99



Caps in bad channels

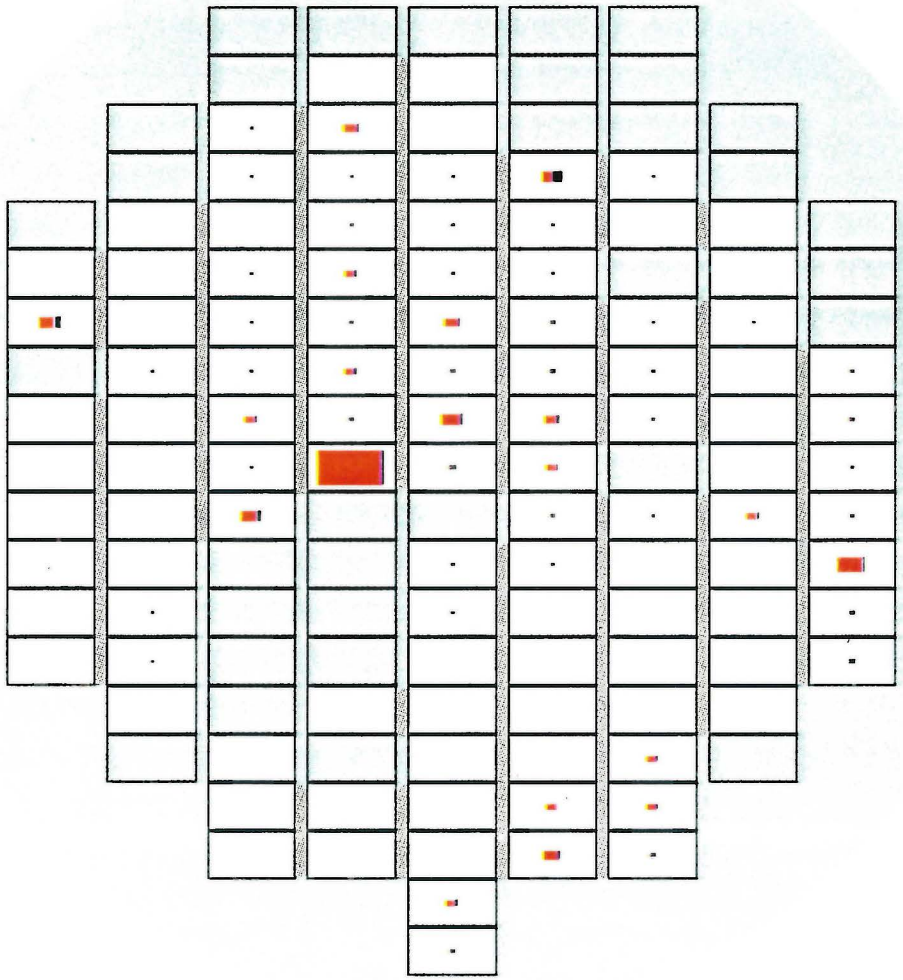
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 140 s/n: Y21316-08-17 (not backplated)

Date: 03/23/99



Caps in bad channels

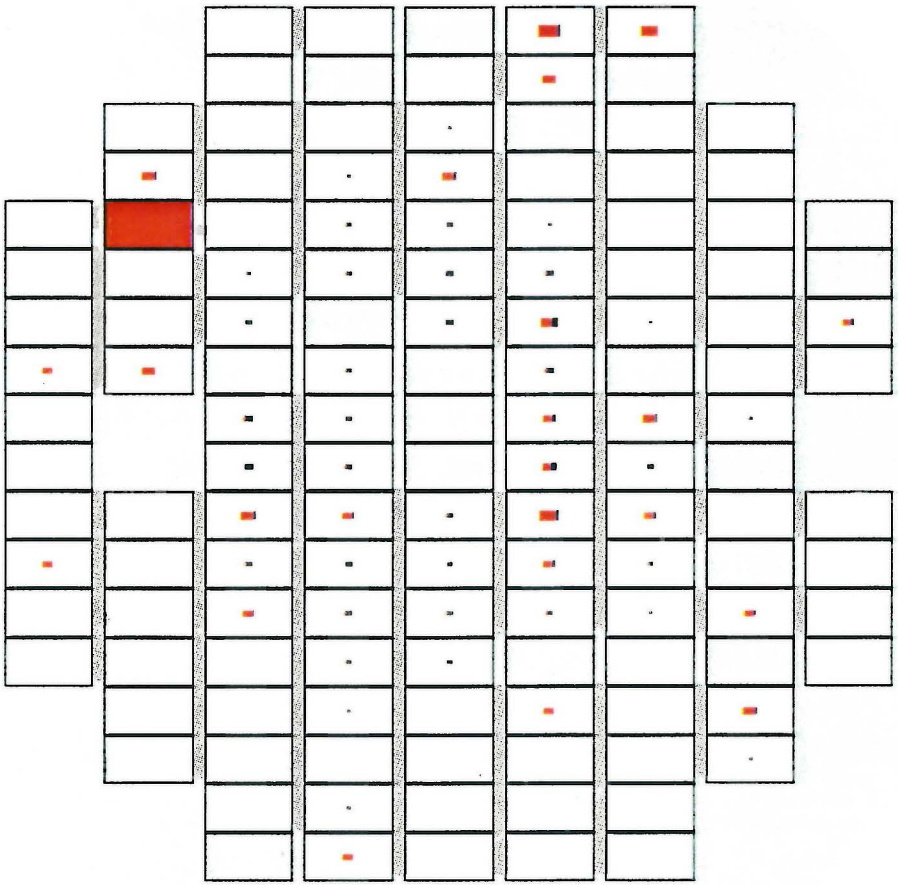
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 92 s/n: Y21316-09-02 (not backplated)

Date: 01/19/99



Caps in bad channels

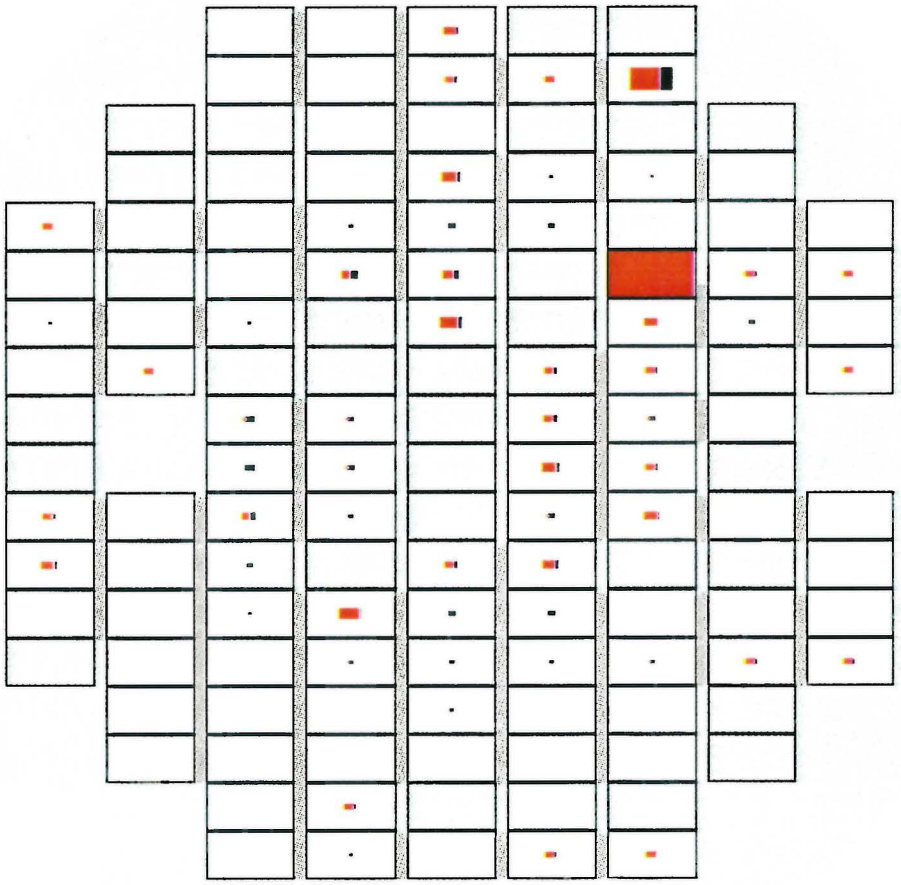
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 74 s/n: Y21316-09-03 (not backplated)

Date: 01/14/99



Caps in bad channels

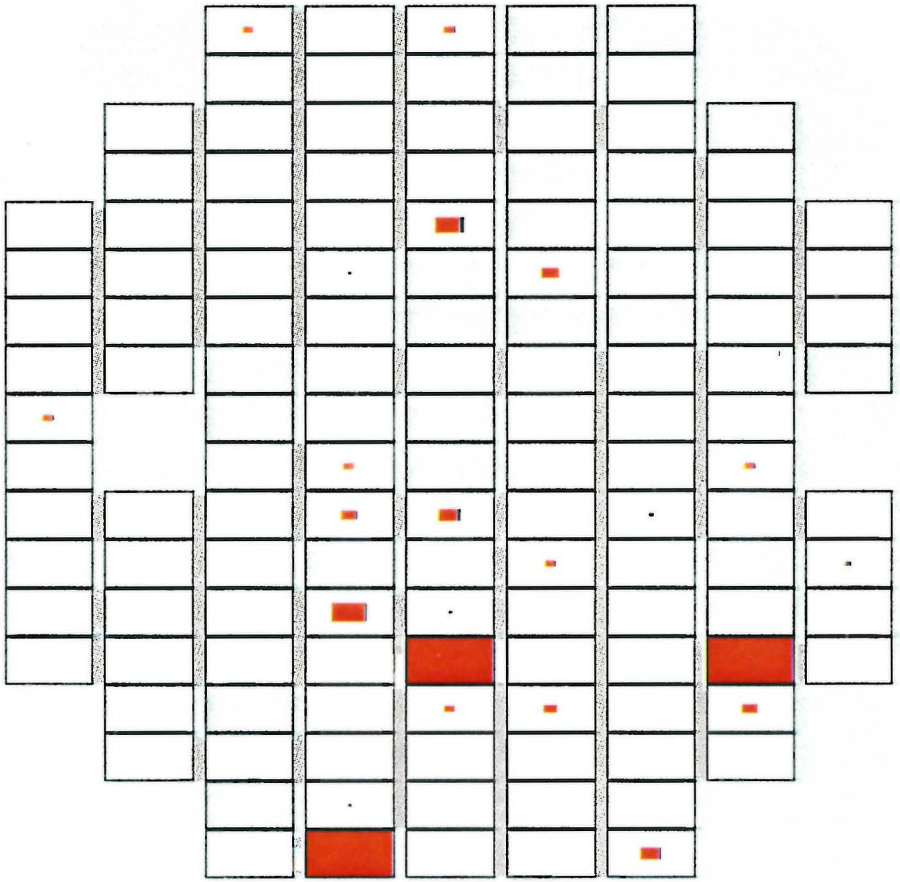
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 93 s/n: Y21316-09-05 (not backplated)

Date: 01/19/99



Caps in bad channels

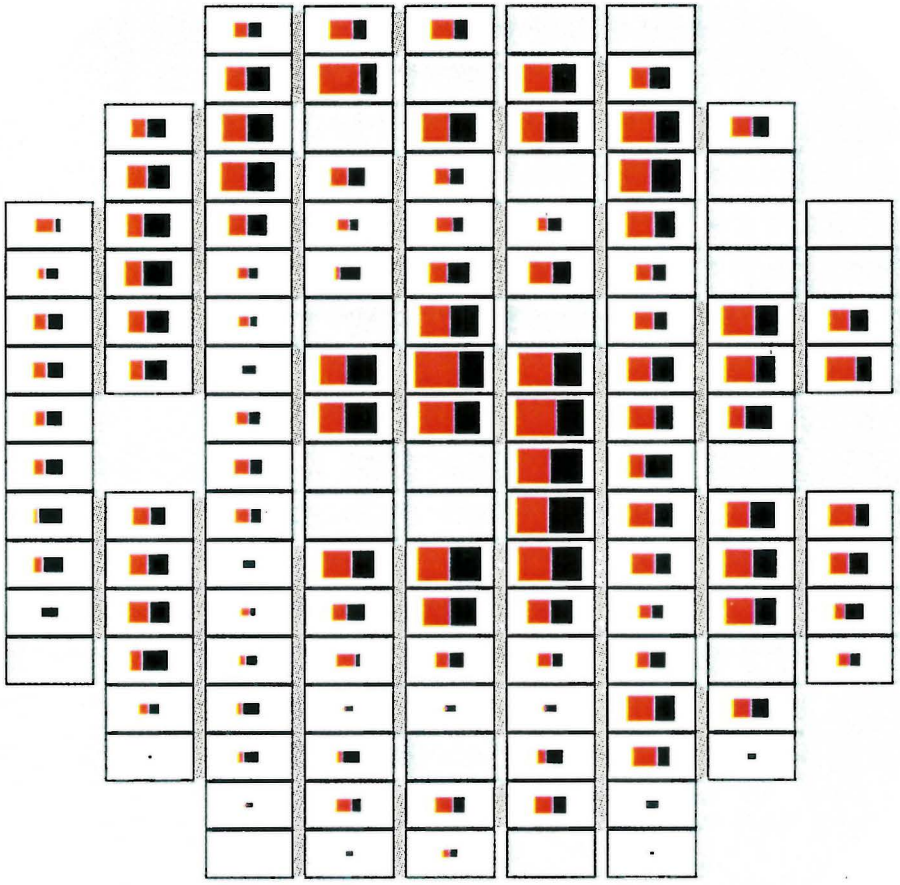
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 91 s/n: Y21316-10-01 (not backplated)

Date: 01/19/99



Caps in bad channels

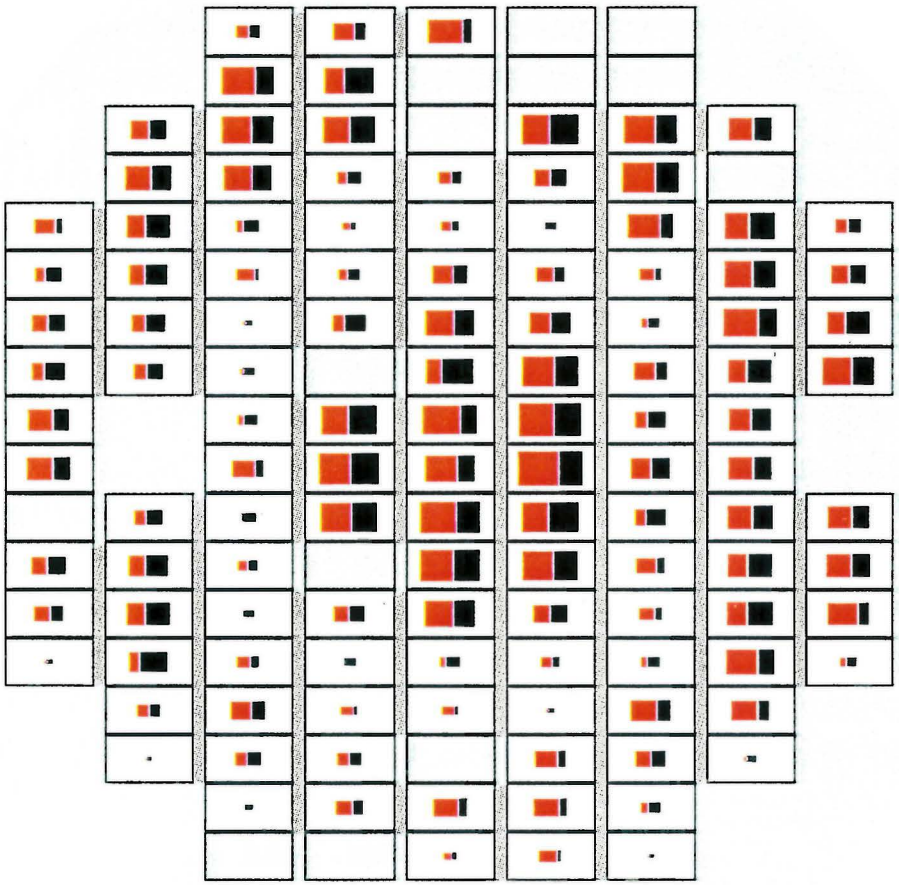
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 89 s/n: Y21316-10-02 (not backplated)

Date: 01/19/99



Caps in bad channels

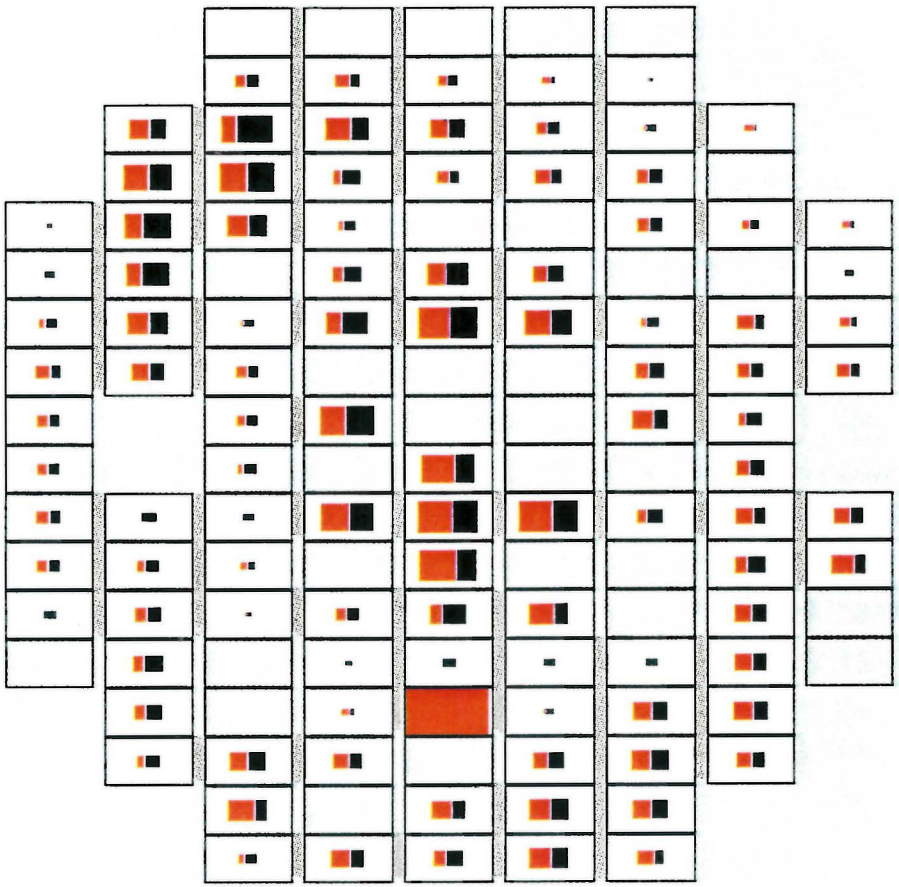
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 72 s/n: Y21316-10-08 (not backplated)

Date: 01/14/99



Caps in bad channels

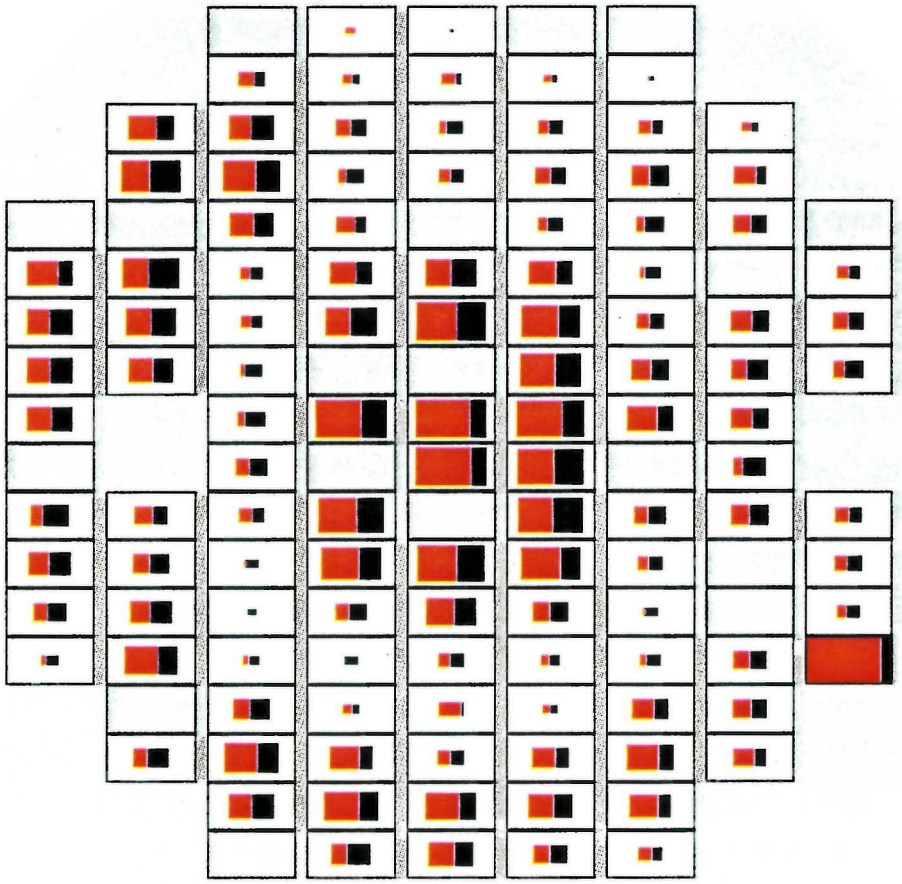
Bad caps in random locations

Good caps

No info

Pipeline quality map for wafer 146 s/n: Y21316-10-10 (not backplated)

Date: 04/14/99



Cells in bad channels

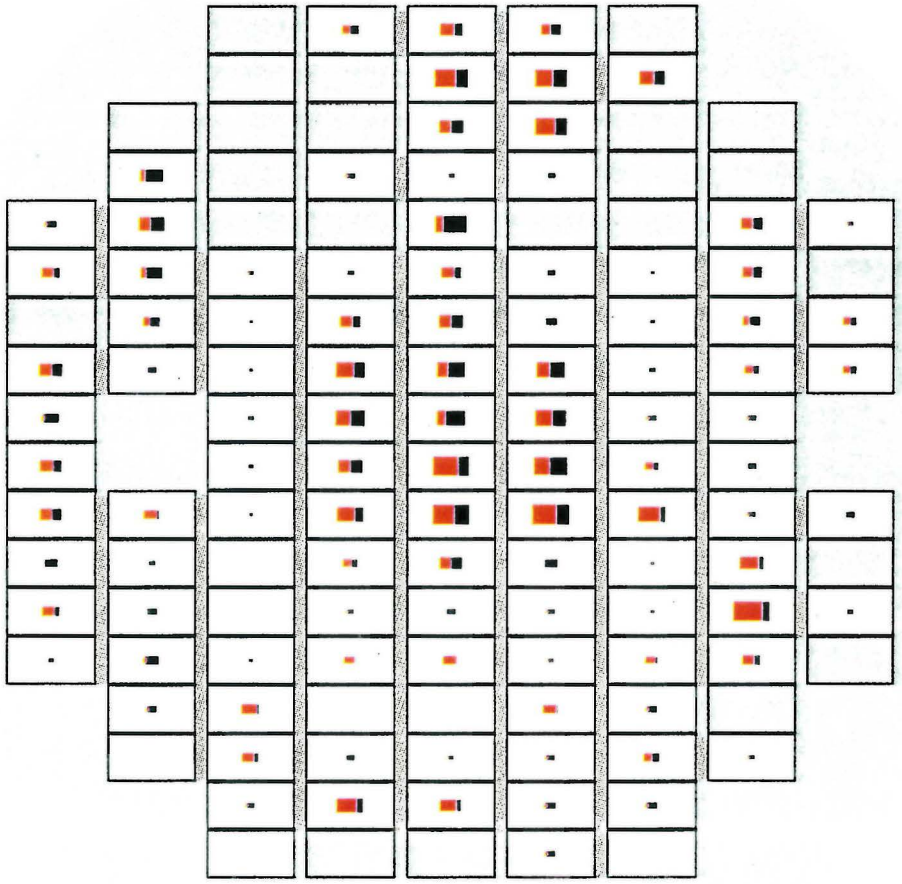
Bad cells in random locations

Good cells

No info

Pipeline quality map for wafer 145 s/n: Y21316-10-18 (not backplated)

Date: 04/13/99



Cells in bad channels

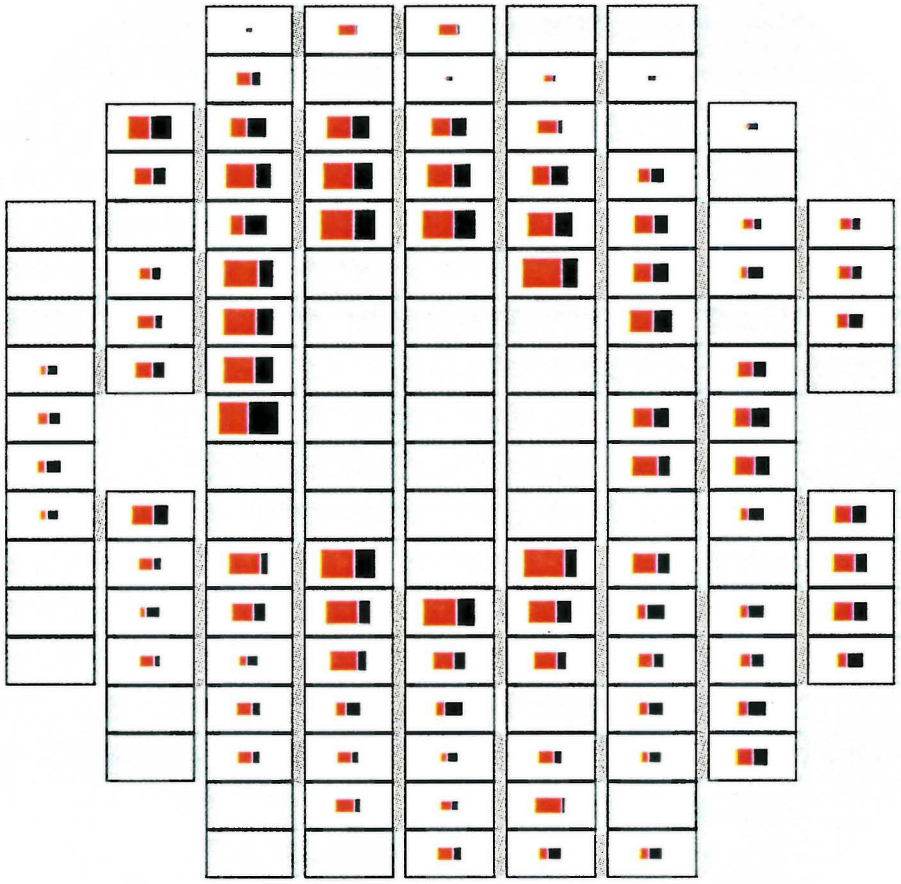
Bad cells in random locations

Good cells

No info

Capacitor quality map for wafer 81 s/n: Y21316-11-03 (not backplated)

Date: 01/14/99



Caps in bad channels

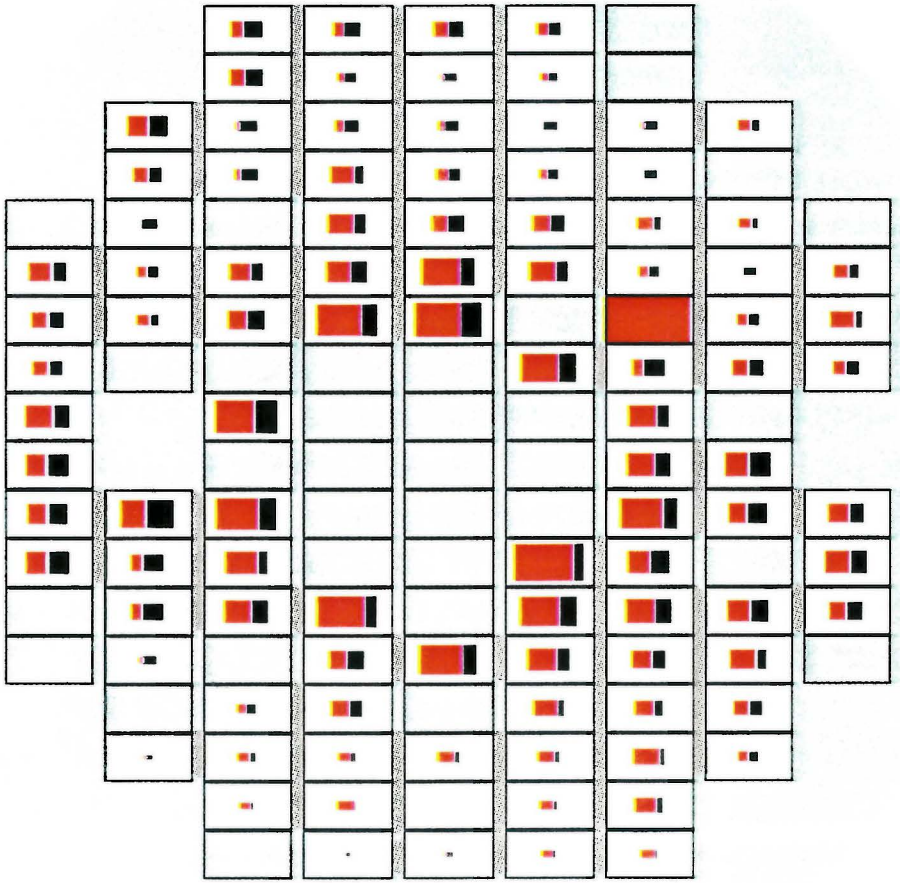
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 144 s/n: Y21316-11-05 (not backplated)

Date: 04/09/99



Caps in bad channels

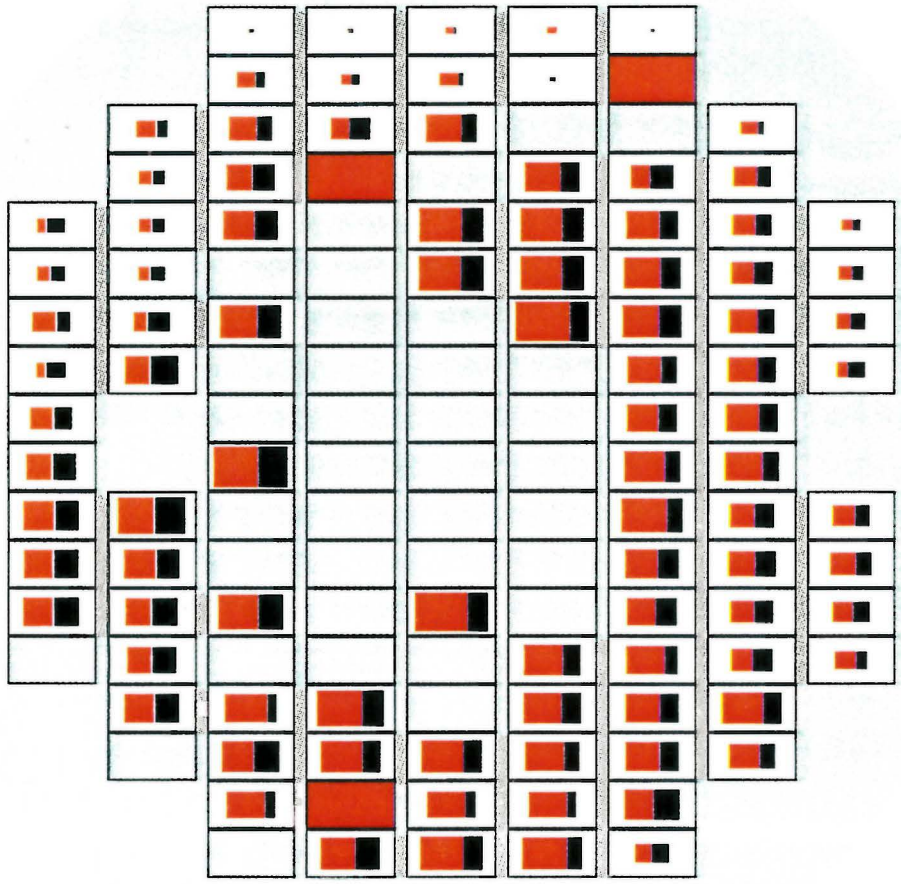
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 138 s/n: Y21316-11-11 (not backplated)

Date: 03/18/99



Caps in bad channels

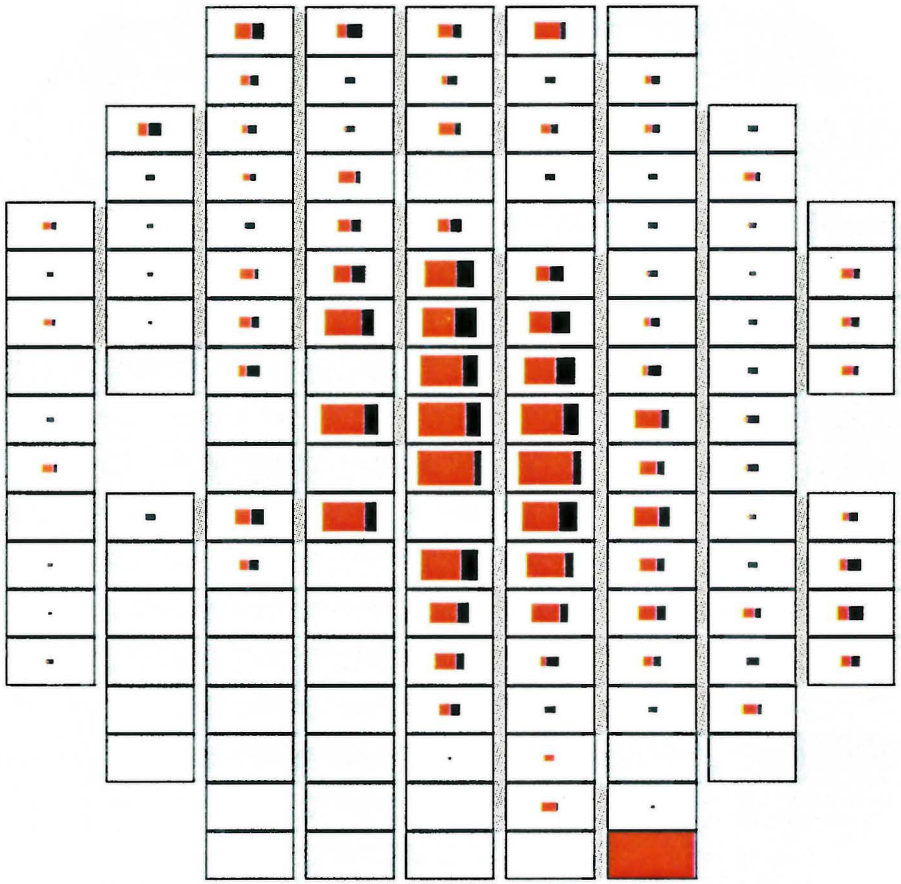
Bad caps in random locations

Good caps

No info

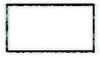
Capacitor quality map for wafer 83 s/n: Y21316-11-18 (not backplated)

Date: 01/14/99

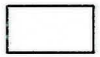


Caps in bad channels

Bad caps in random locations



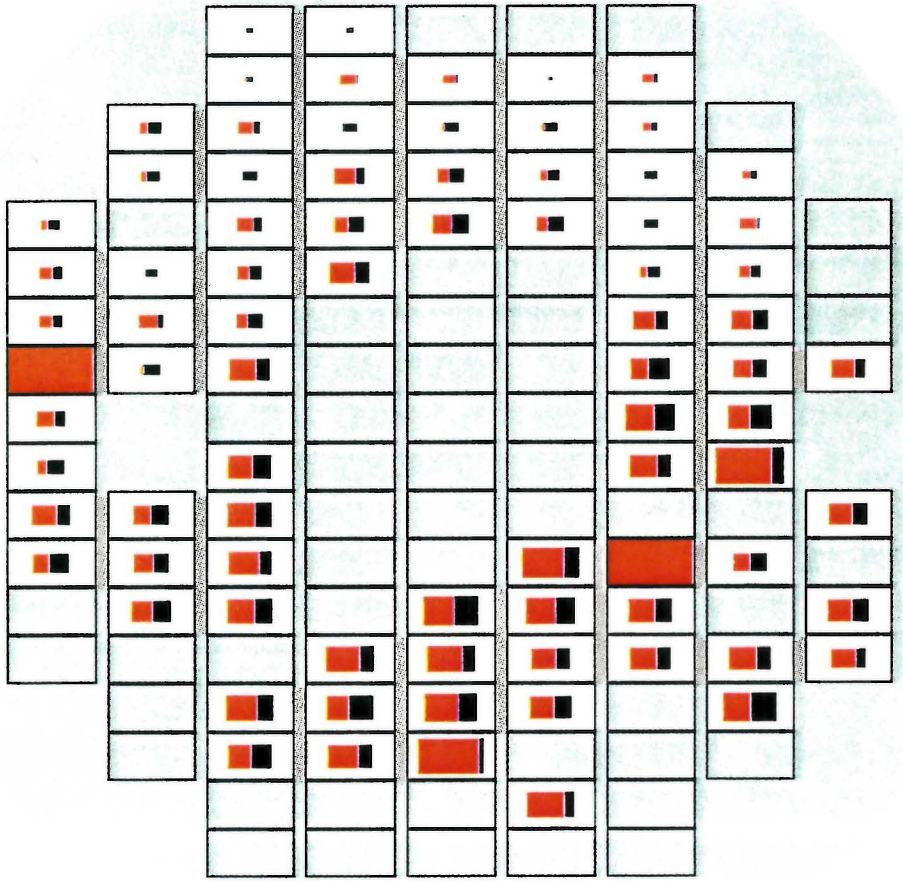
Good caps



No info

Pipeline quality map for wafer 69 s/n: Y21316-11-20 (not backplated)

Date: 04/09/99



Cells in bad channels

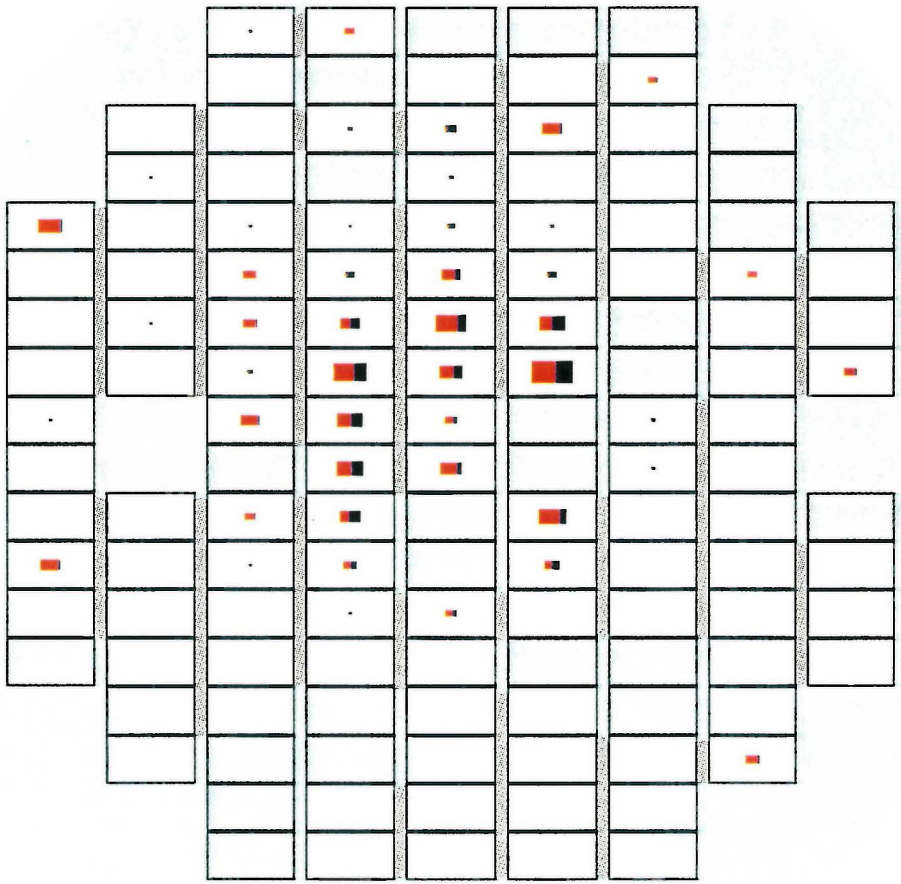
Bad cells in random locations

Good cells

No info

Capacitor quality map for wafer 76 s/n: Y21316-12-04 (not backplated)

Date: 01/14/99



Caps in bad channels

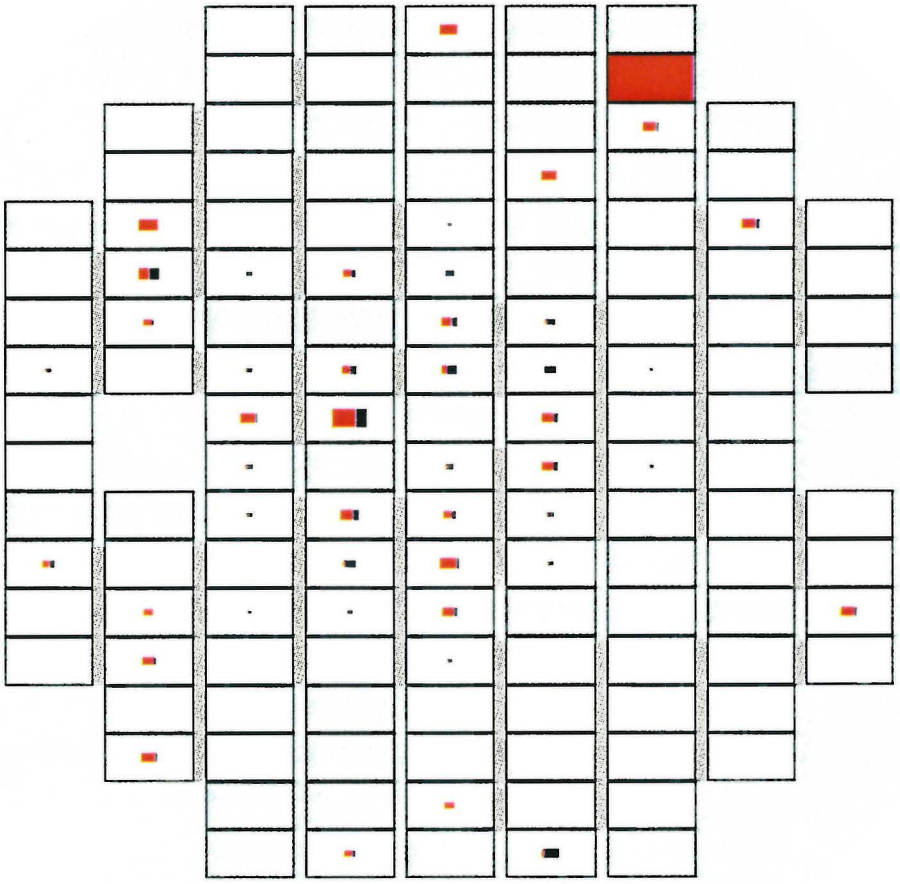
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 82 s/n: Y21316-12-11 (not backplated)

Date: 01/14/99



Caps in bad channels

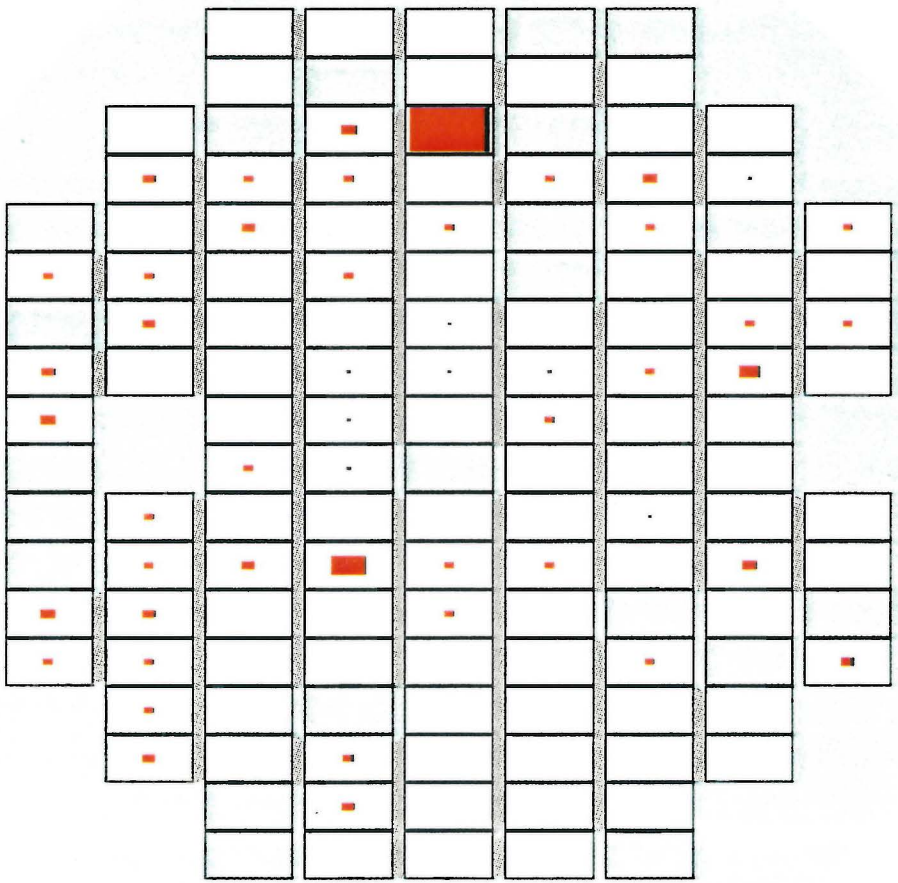
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 137 s/n: Y21316-12-12 (not backplated)

Date: 03/18/99



Caps in bad channels

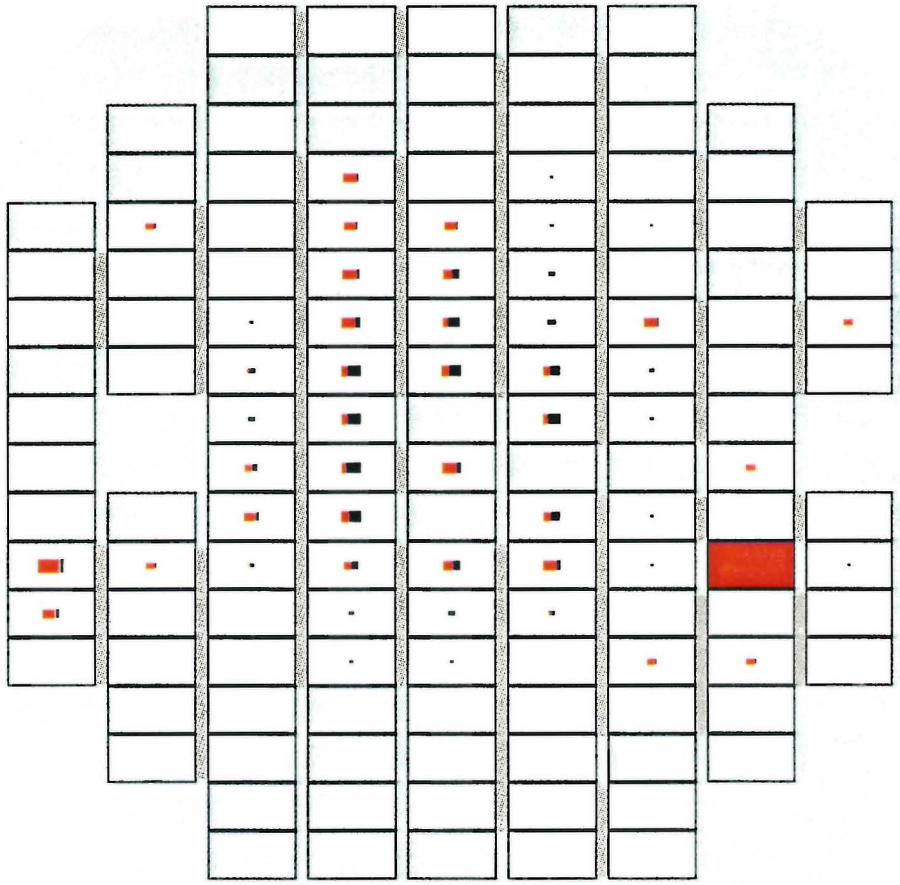
Bad caps in random locations

Good caps

No info

Capacitor quality map for wafer 80 s/n: Y21316-12-15 (not backplated)

Date: 01/14/99



Caps in bad channels

Bad caps in random locations

Good caps

No info

APPENDIX C

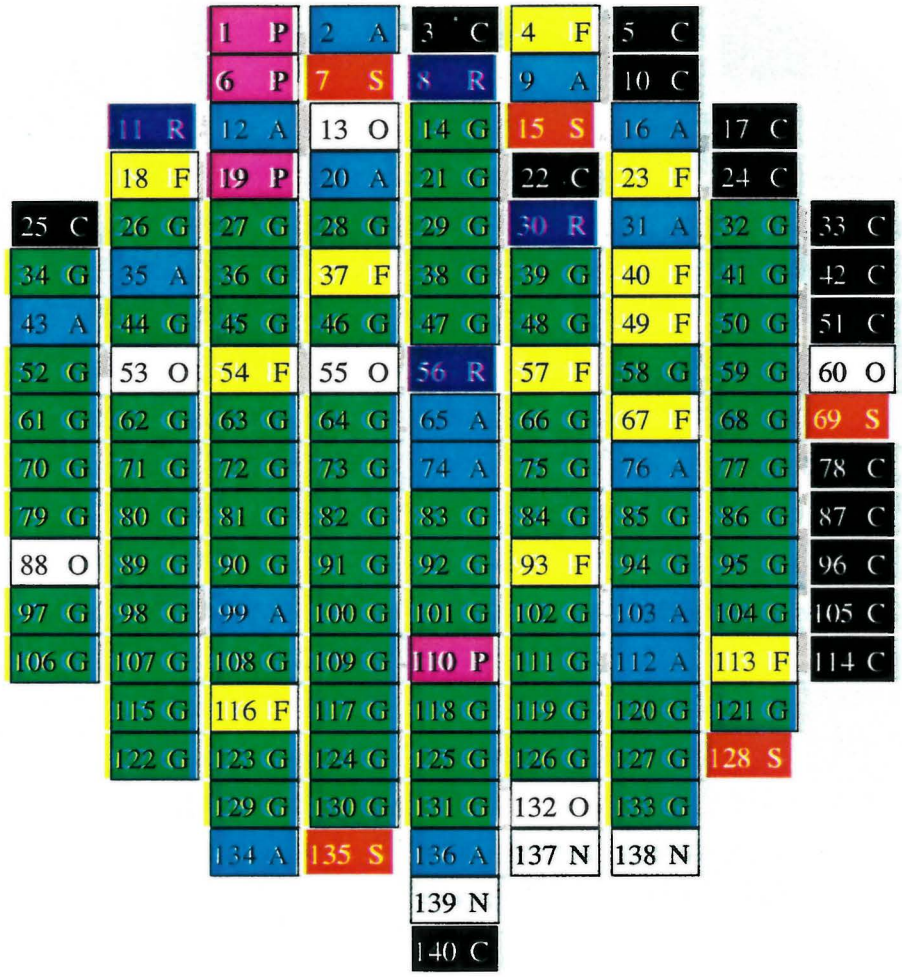
Appendix C

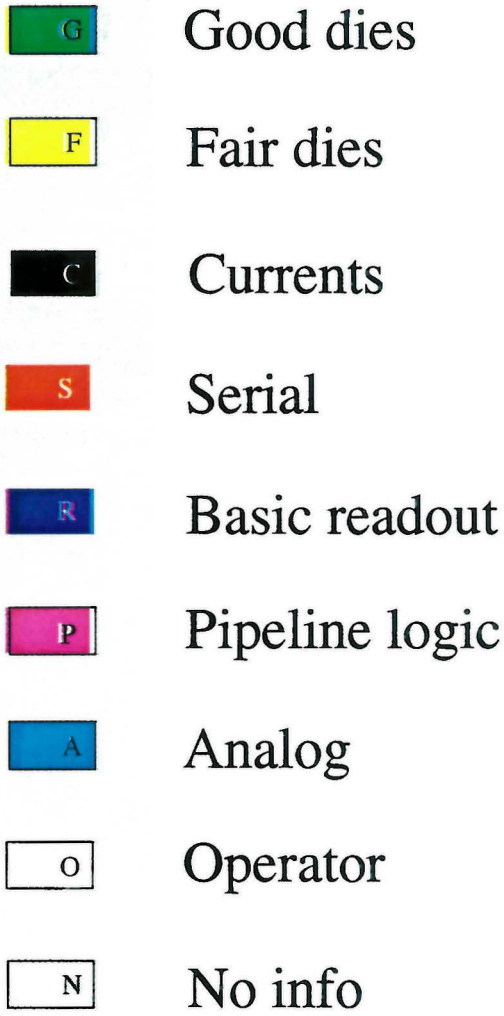
Types of Die Failure Maps

Lot	Wafer
8	1
8	3
8	4
8	6
8	11
8	15
8	17
9	2
9	3
9	5
10	1
10	2
10	8
10	10
10	18
11	3
11	5
11	11
11	18
11	20
12	4
12	11
12	12
12	15

Types of die failures for wafer 87 s/n: Y21316-08-01 (not backplated)

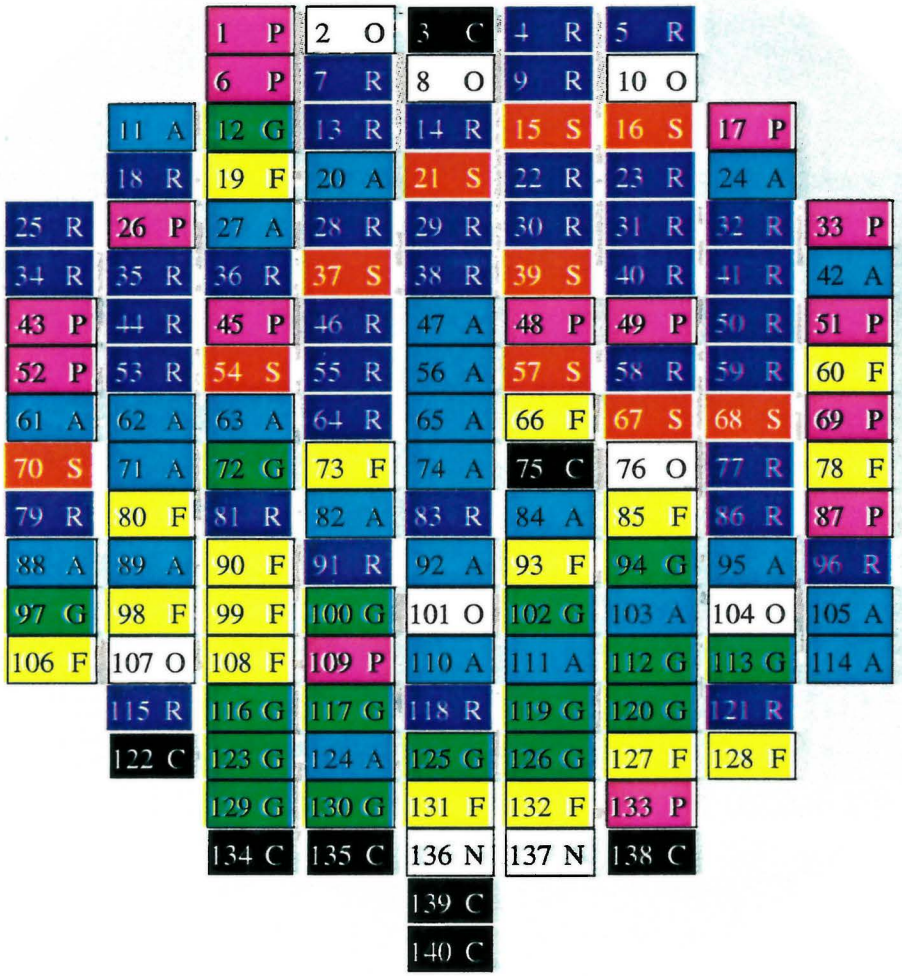
Date: 04/05/99

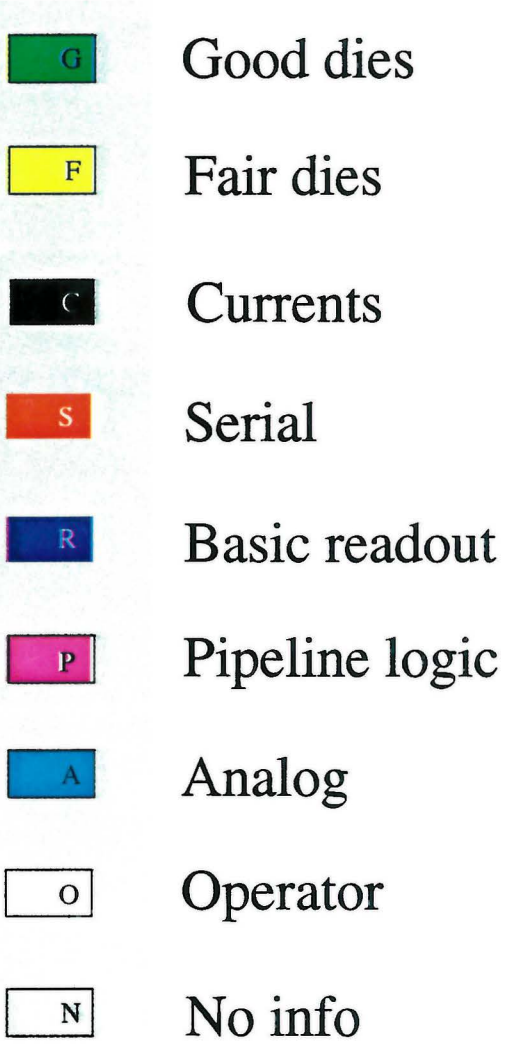




Types of die failures for wafer 70 s/n: Y21316-08-03 (not backplated)

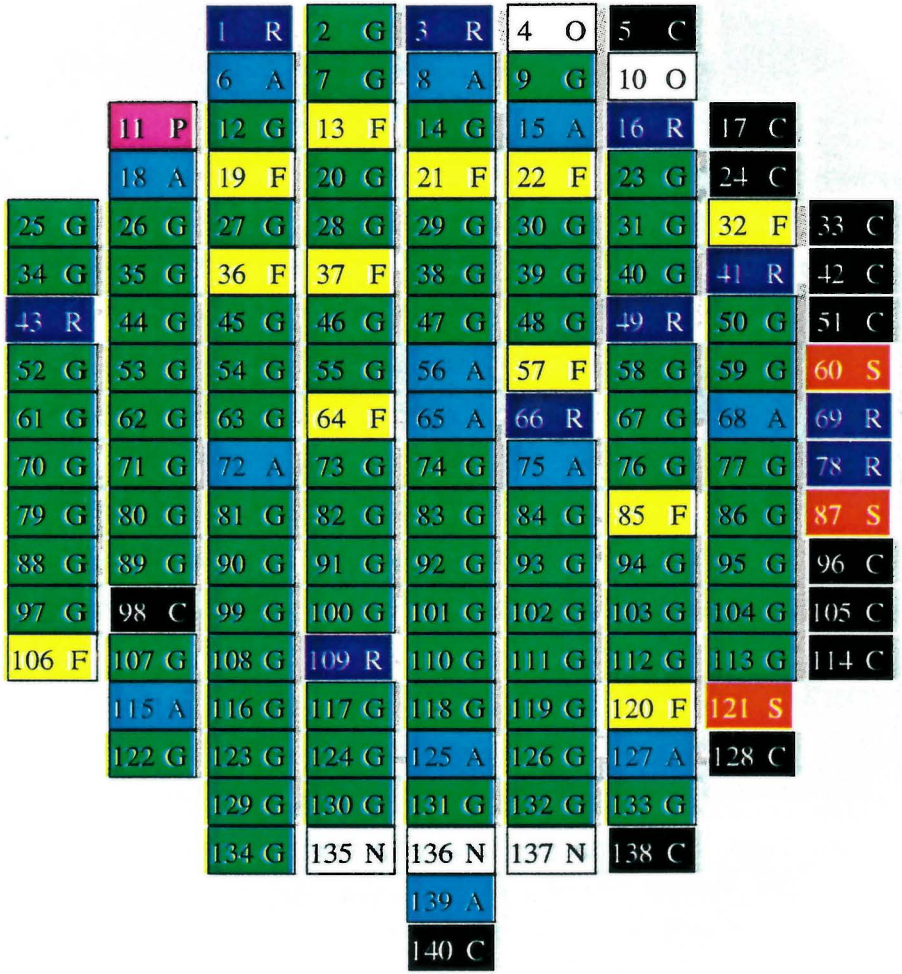
Date: 04/05/99

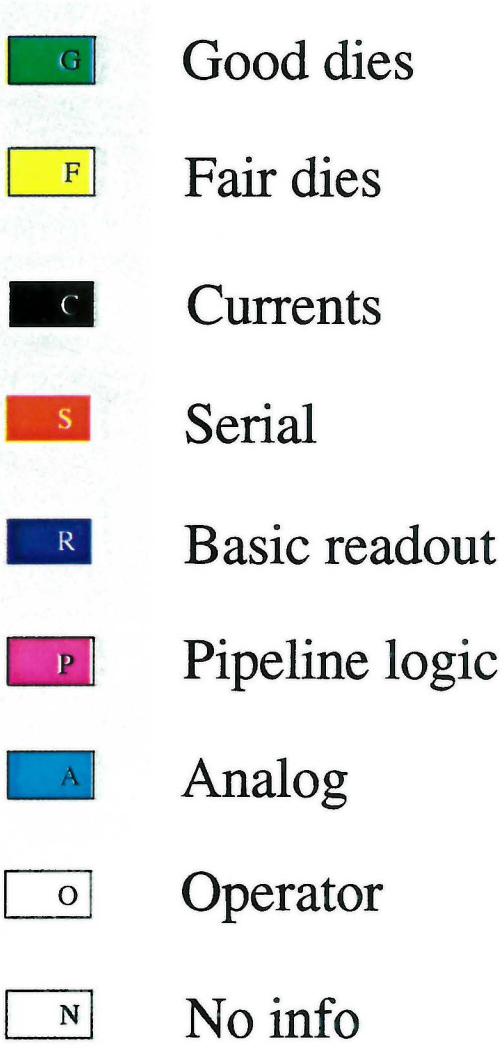




Types of die failures for wafer 85 s/n: Y21316-08-04 (not backplated)

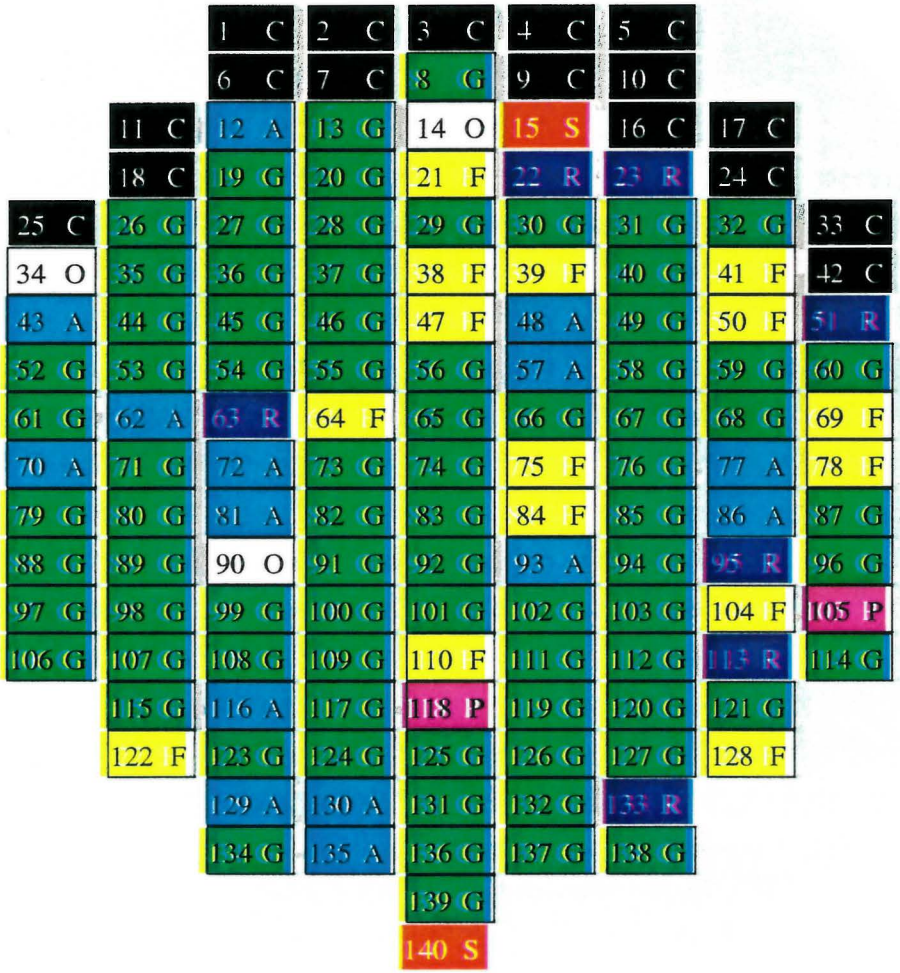
Date: 04/05/99

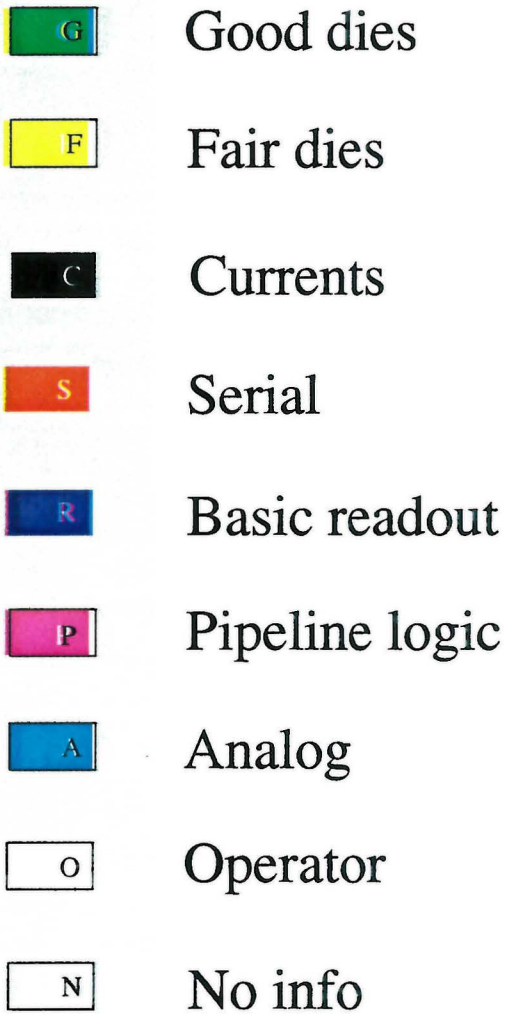




Types of die failures for wafer 141 s/n: Y21316-08-06 (not backplated)

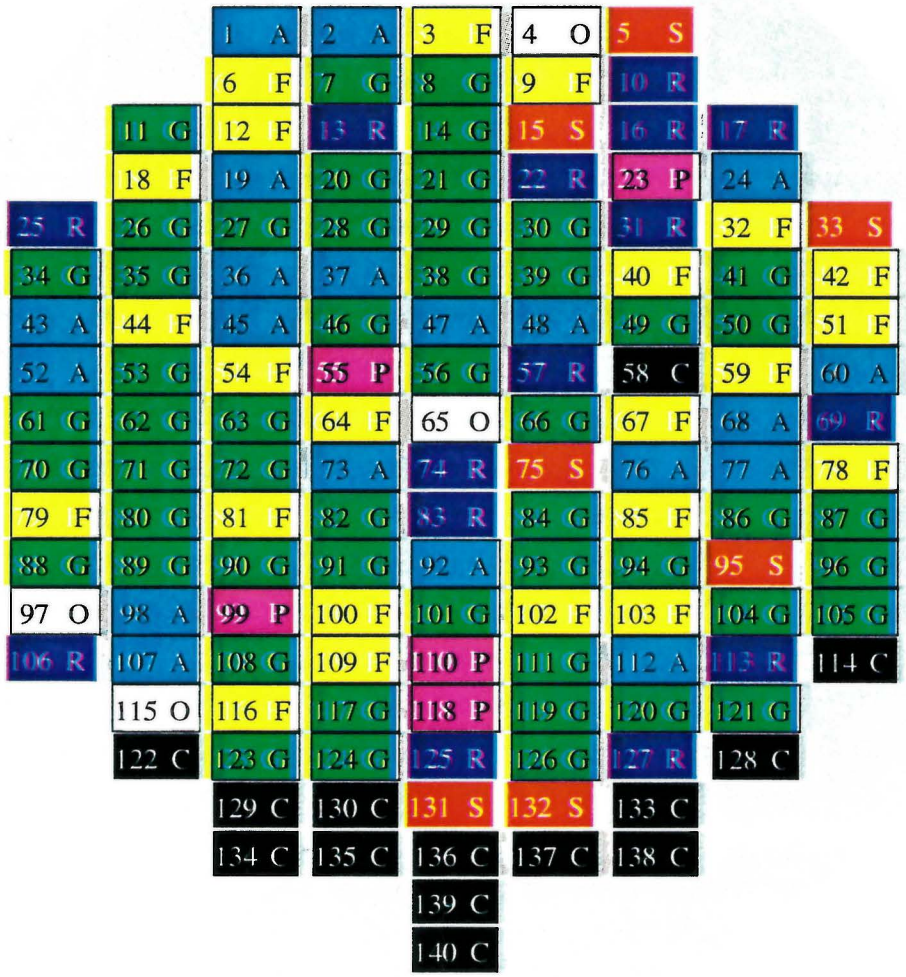
Date: 04/05/99

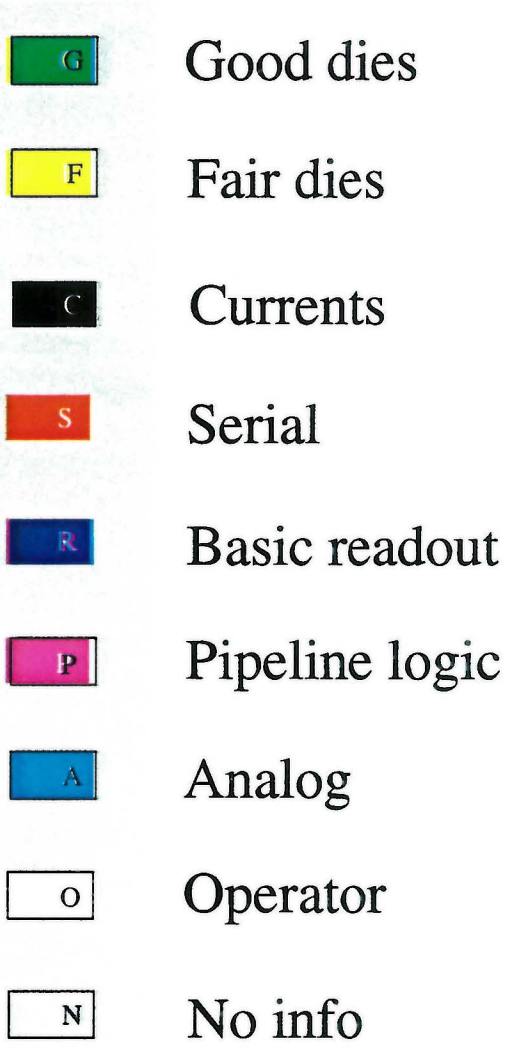




Types of die failures for wafer 142 s/n: Y21316-08-11 (not backplated)

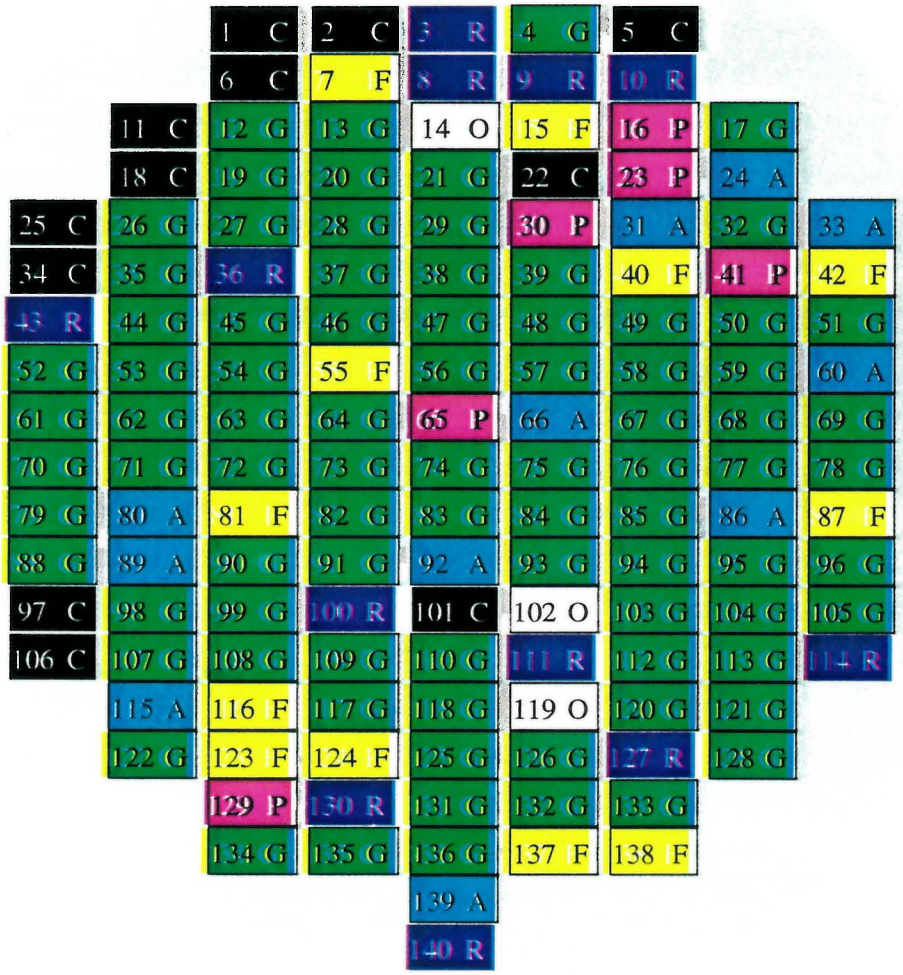
Date: 04/05/99





Types of die failures for wafer 143 s/n: Y21316-08-15 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

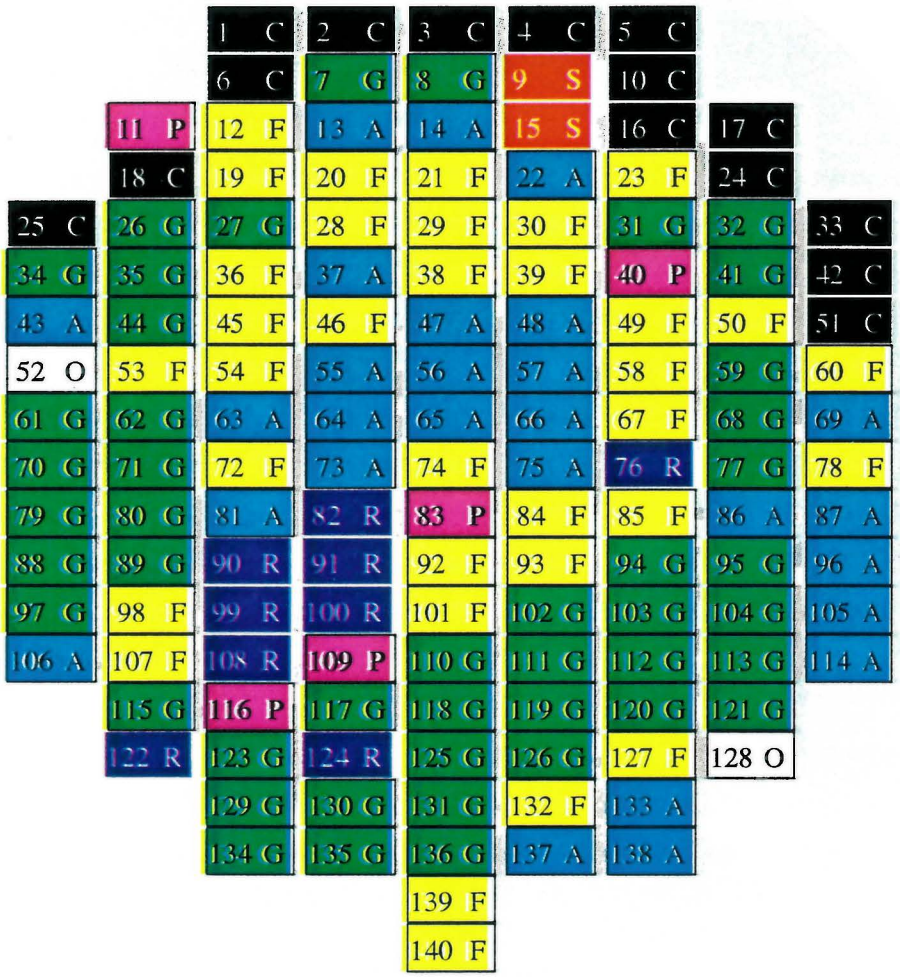
A Analog

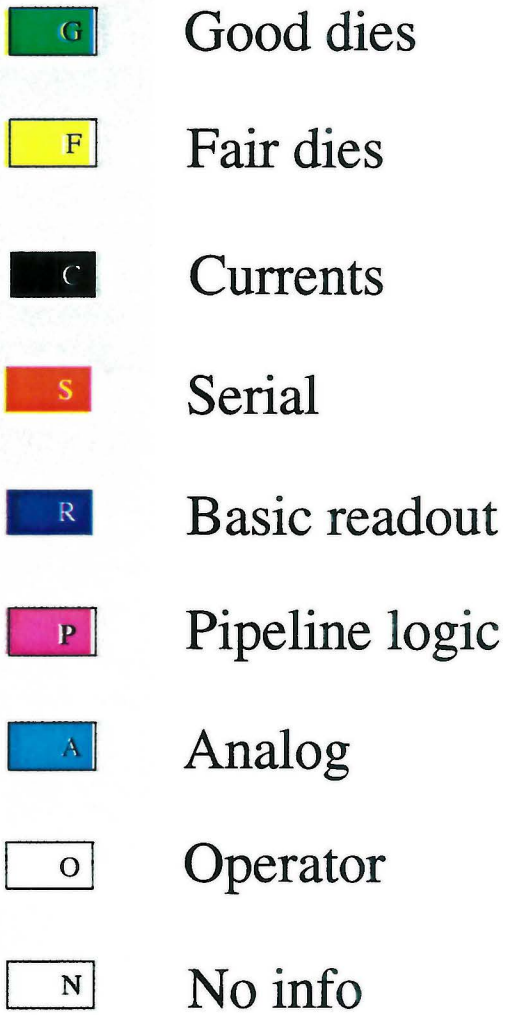
O Operator

N No info

Types of die failures for wafer 140 s/n: Y21316-08-17 (not backplated)

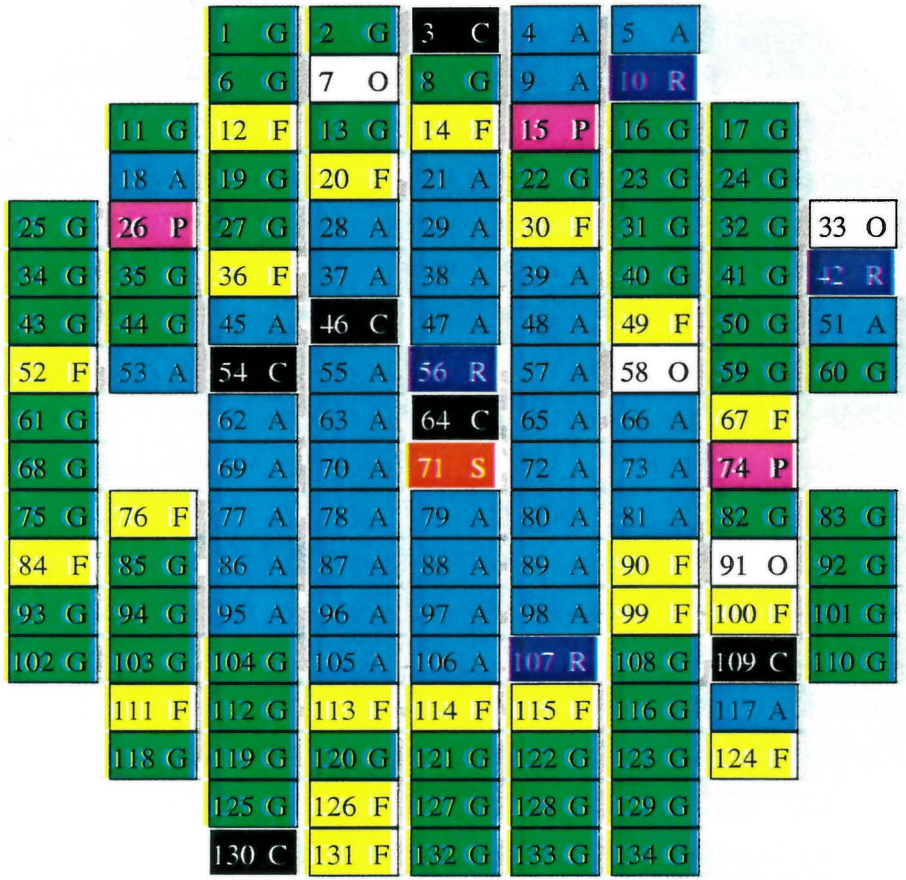
Date: 04/05/99





Types of die failures for wafer 92 s/n: Y21316-09-02 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

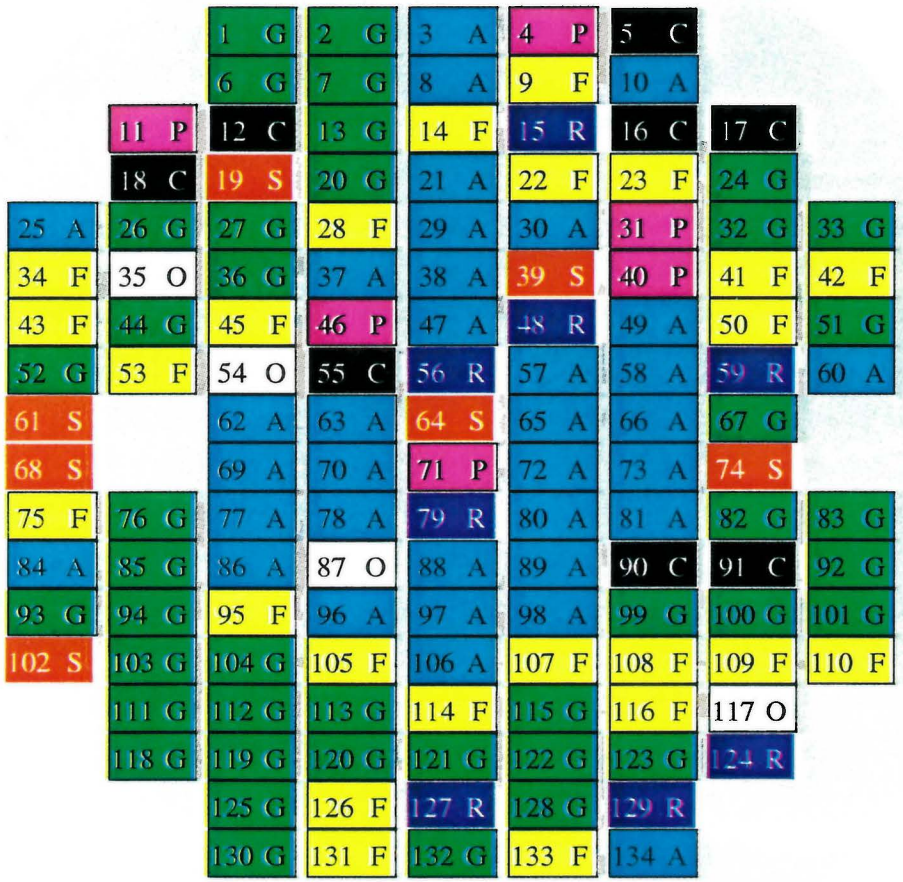
A Analog

O Operator

N No info

Types of die failures for wafer 74 s/n: Y21316-09-03 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

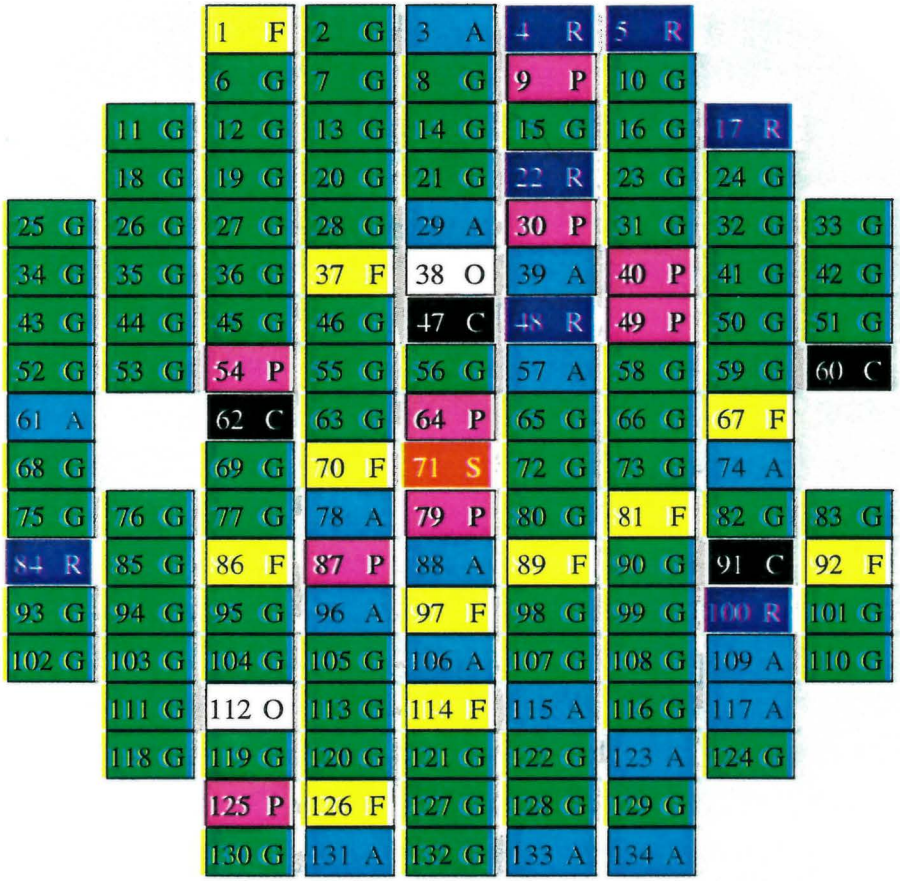
A Analog

O Operator

N No info

Types of die failures for wafer 93 s/n: Y21316-09-05 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

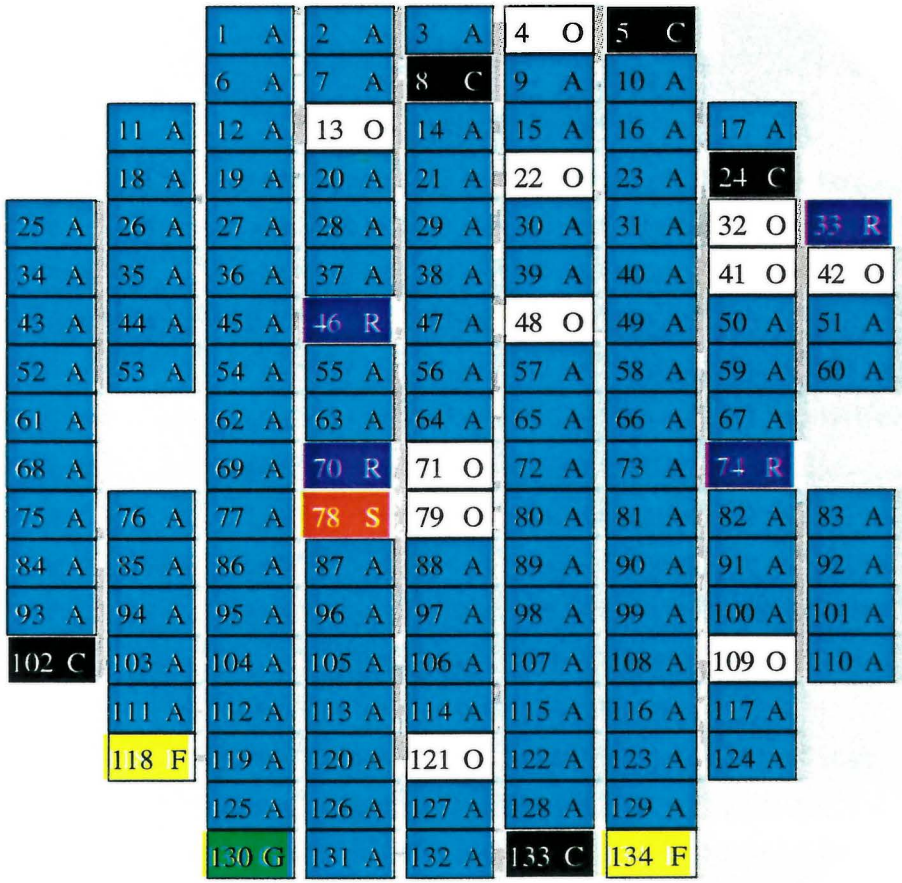
A Analog

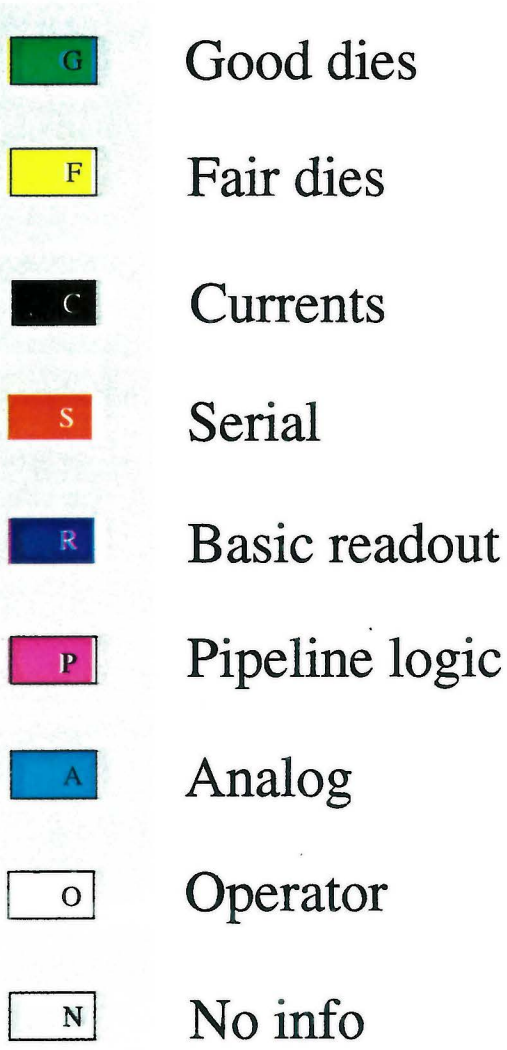
O Operator

N No info

Types of die failures for wafer 91 s/n: Y21316-10-01 (not backplated)

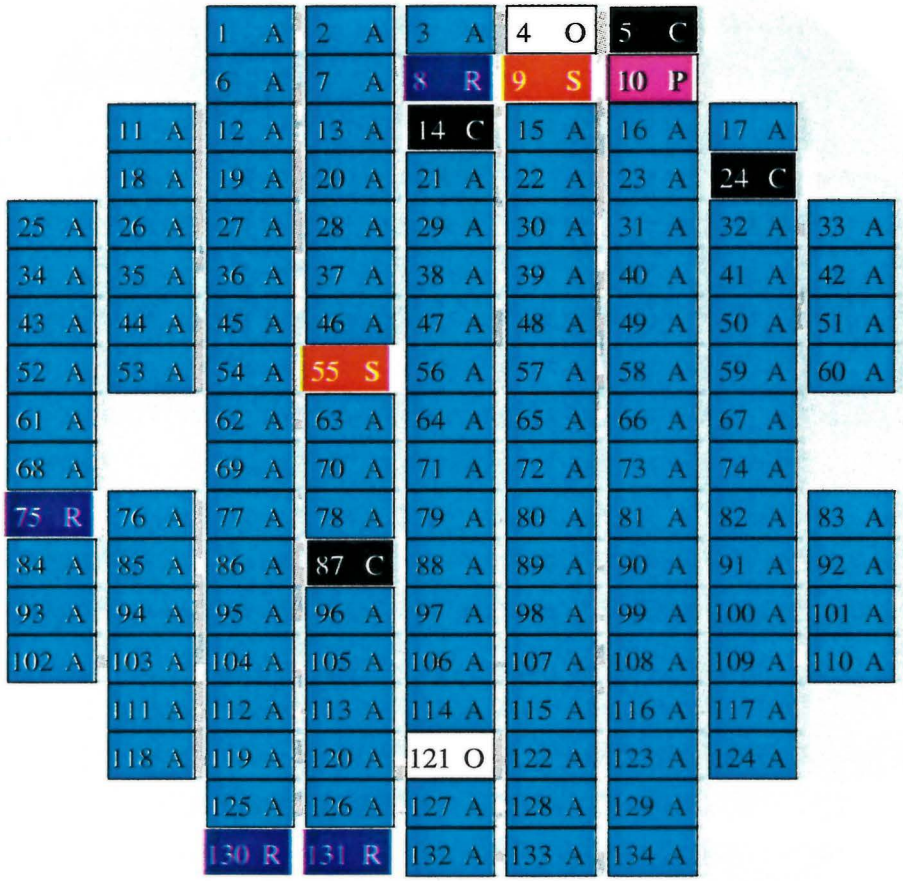
Date: 04/05/99

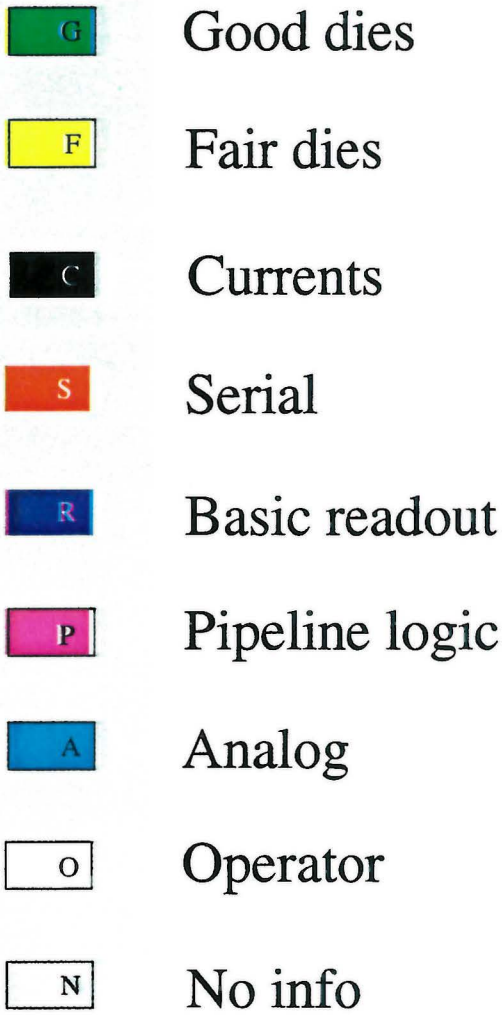




Types of die failures for wafer 89 s/n: Y21316-10-02 (not backplated)

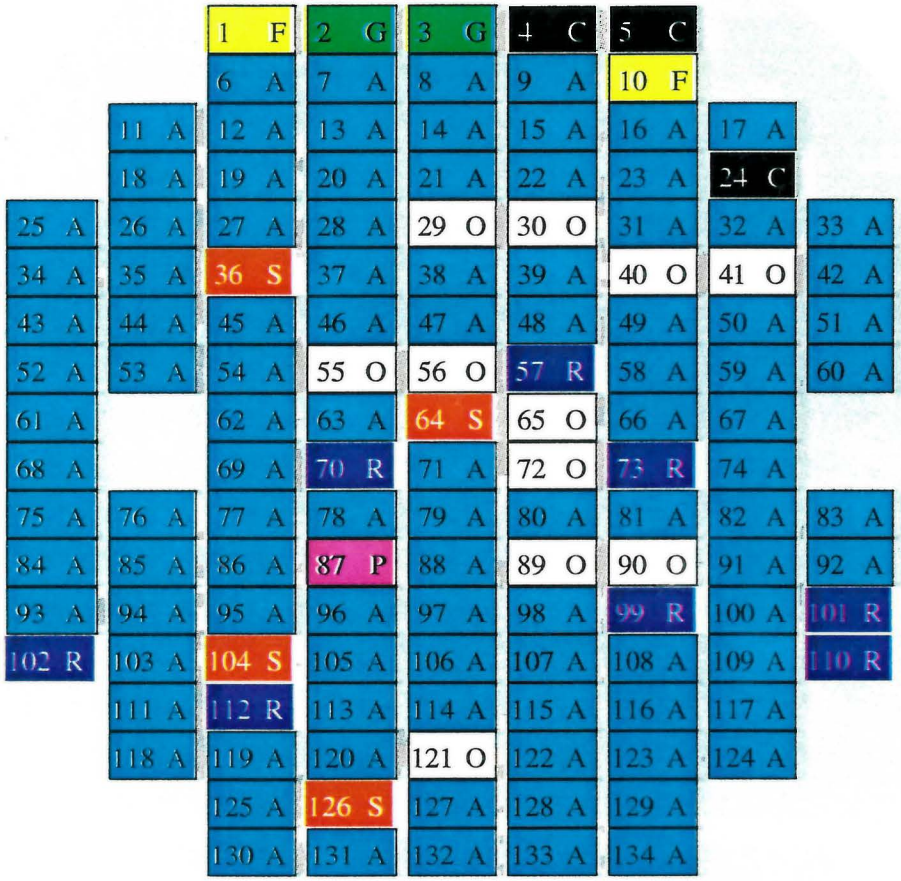
Date: 04/05/99





Types of die failures for wafer 72 s/n: Y21316-10-08 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

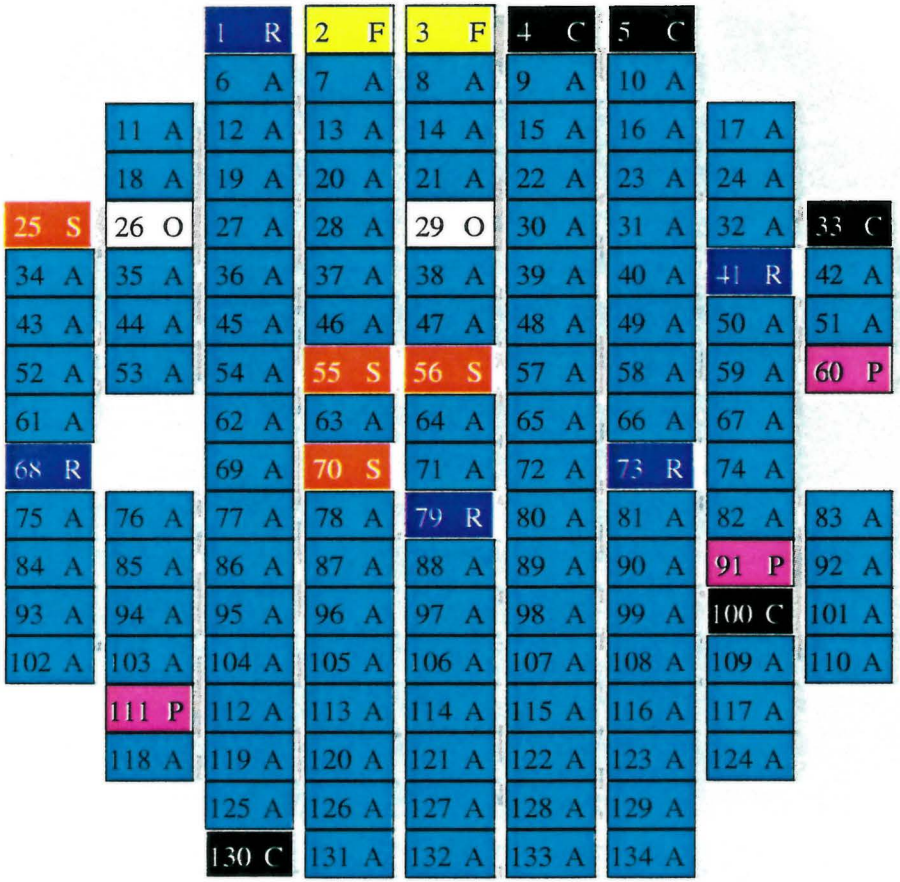
A Analog

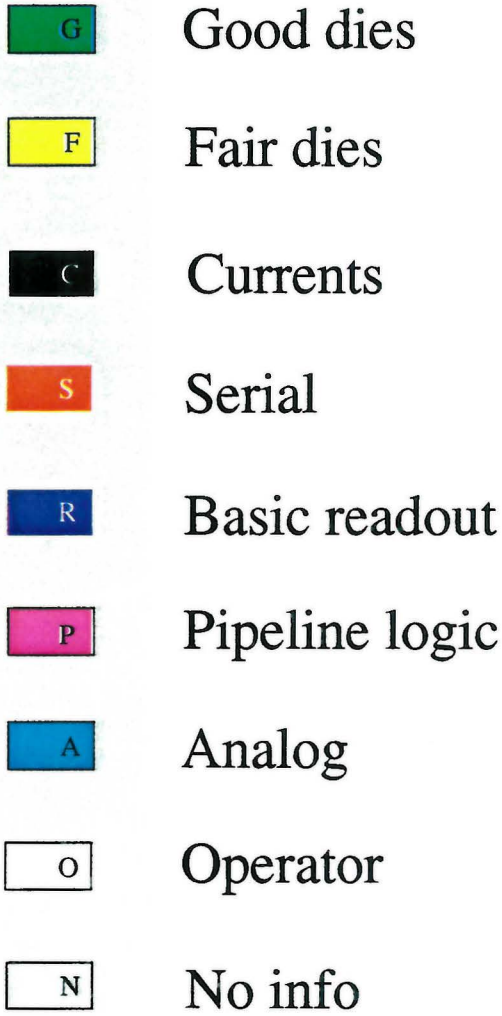
O Operator

N No info

Types of die failures for wafer 146 s/n: Y21316-10-10 (not backplated)

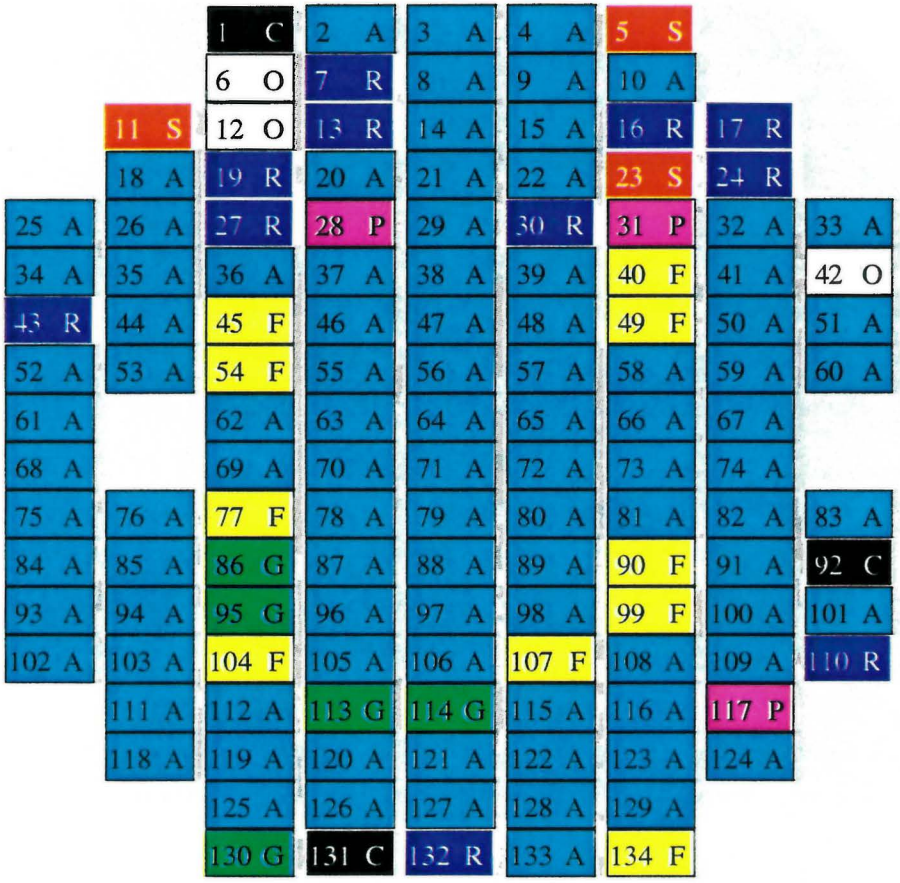
Date: 04/14/99





Types of die failures for wafer 145 s/n: Y21316-10-18 (not backplated)

Date: 04/13/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

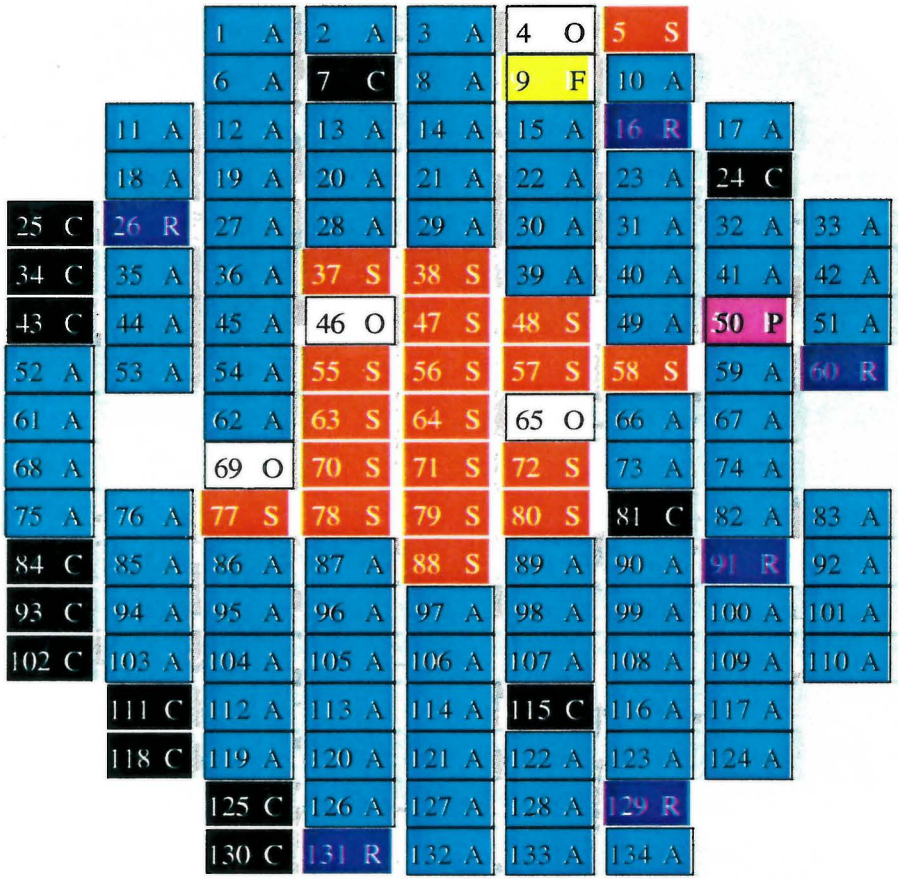
A Analog

O Operator

N No info

Types of die failures for wafer 81 s/n: Y21316-11-03 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

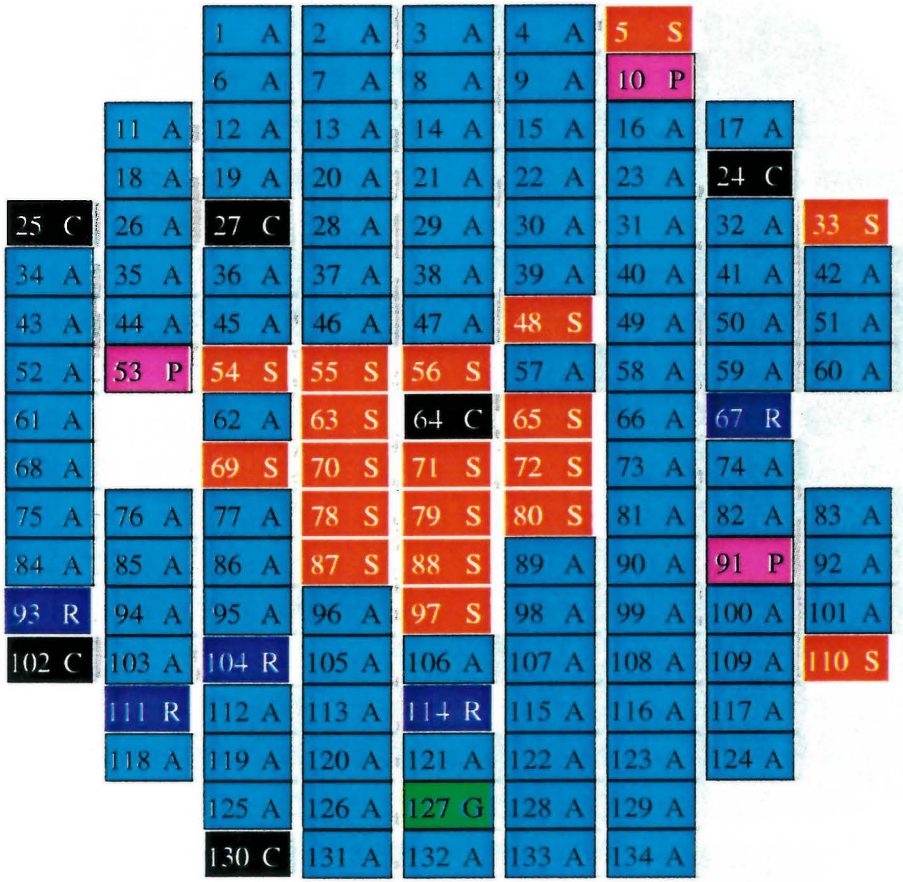
A Analog

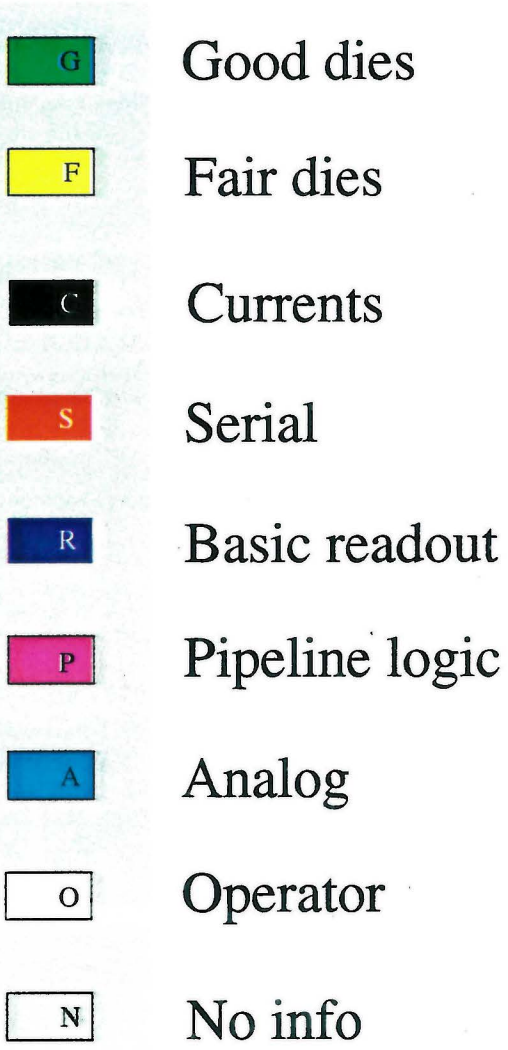
O Operator

N No info

Types of die failures for wafer 144 s/n: Y21316-11-05 (not backplated)

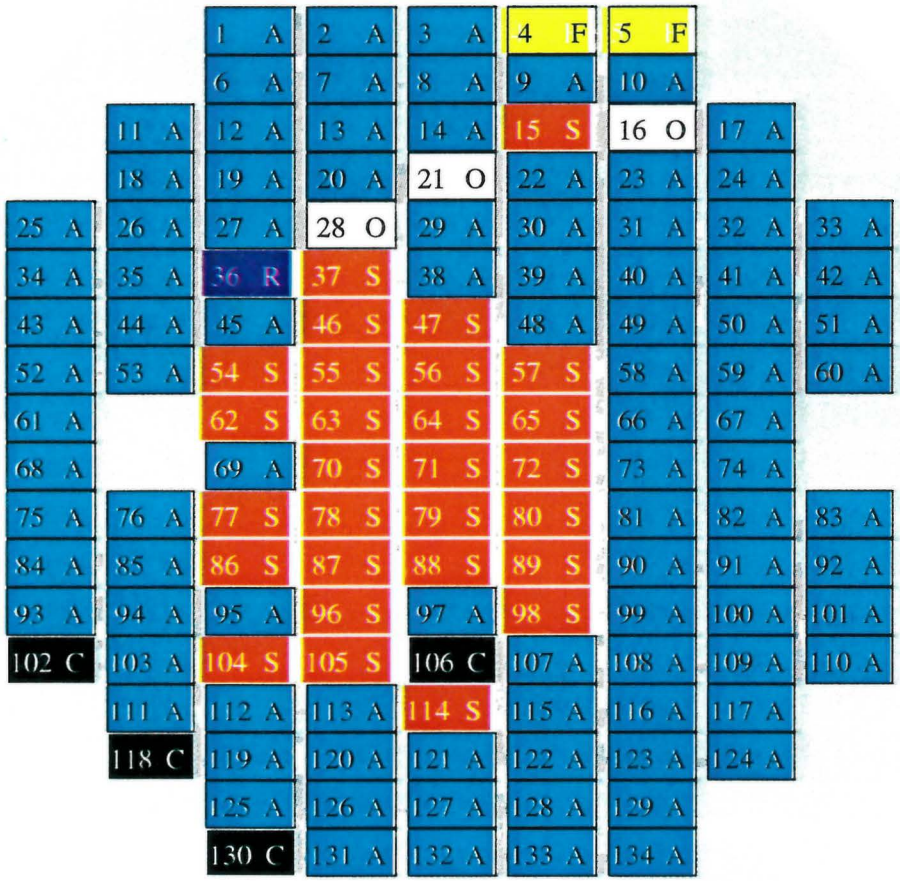
Date: 04/09/99





Types of die failures for wafer 138 s/n: Y21316-11-11 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

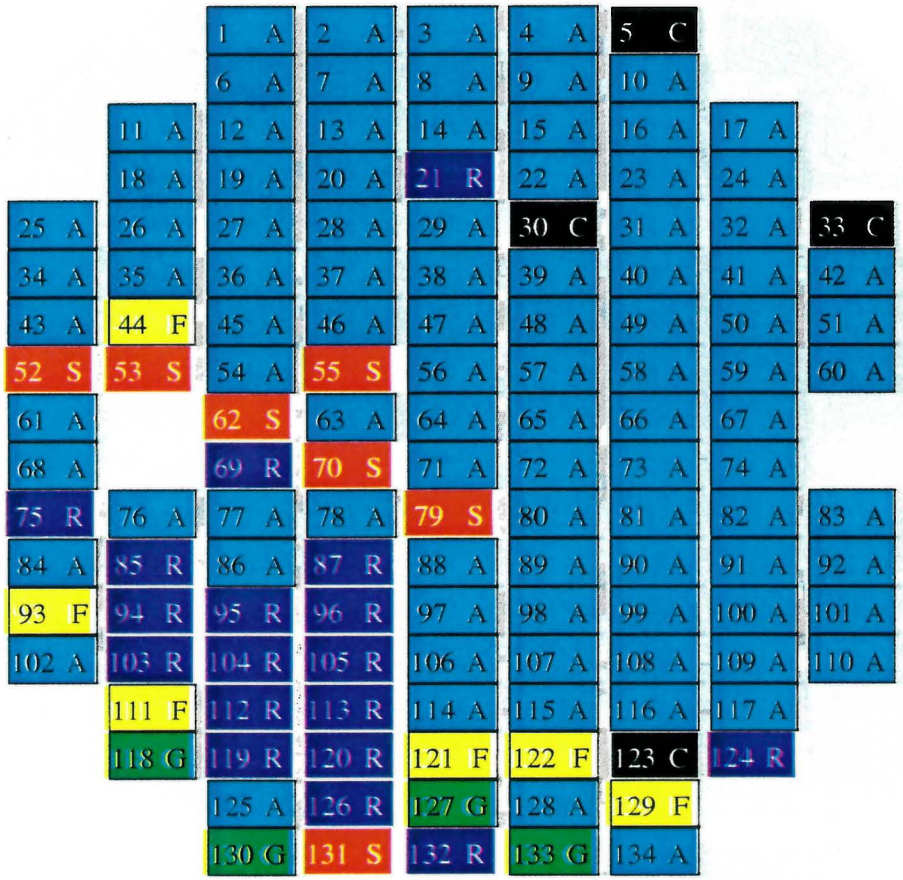
A Analog

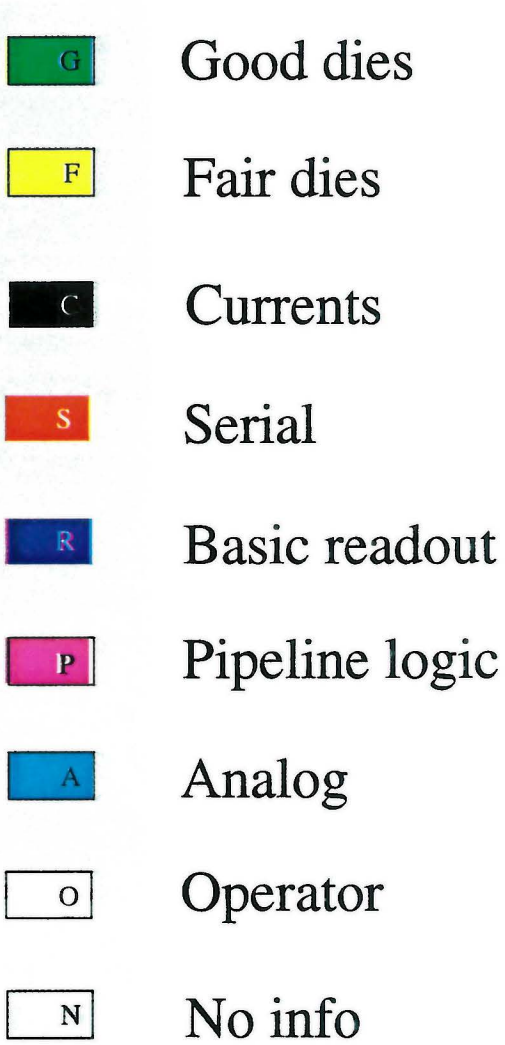
O Operator

N No info

Types of die failures for wafer 83 s/n: Y21316-11-18 (not backplated)

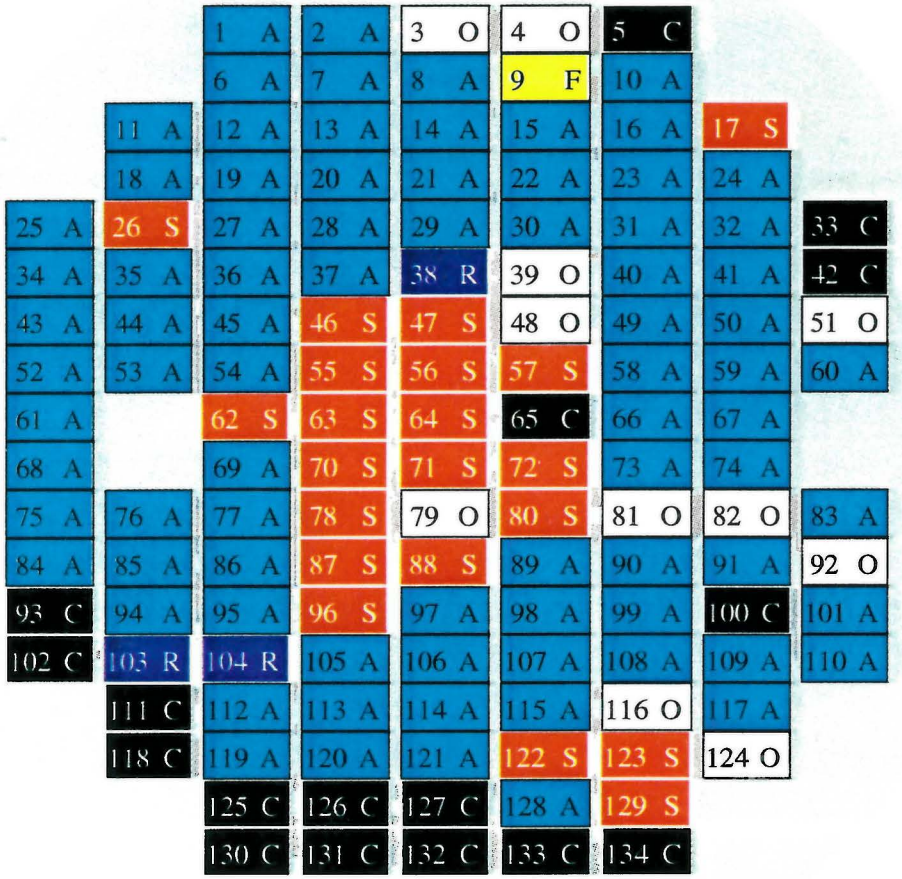
Date: 04/05/99

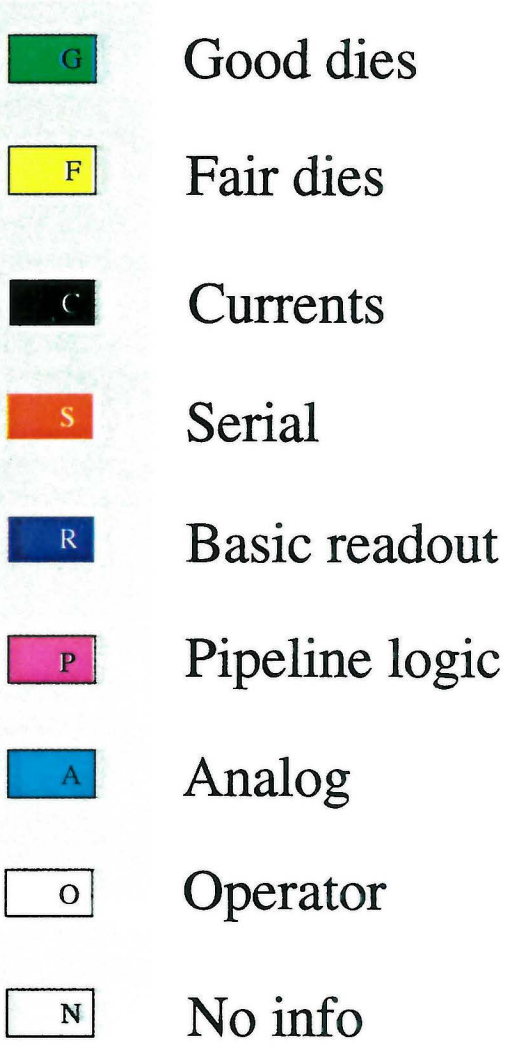




Types of die failures for wafer 69 s/n: Y21316-11-20 (not backplated)

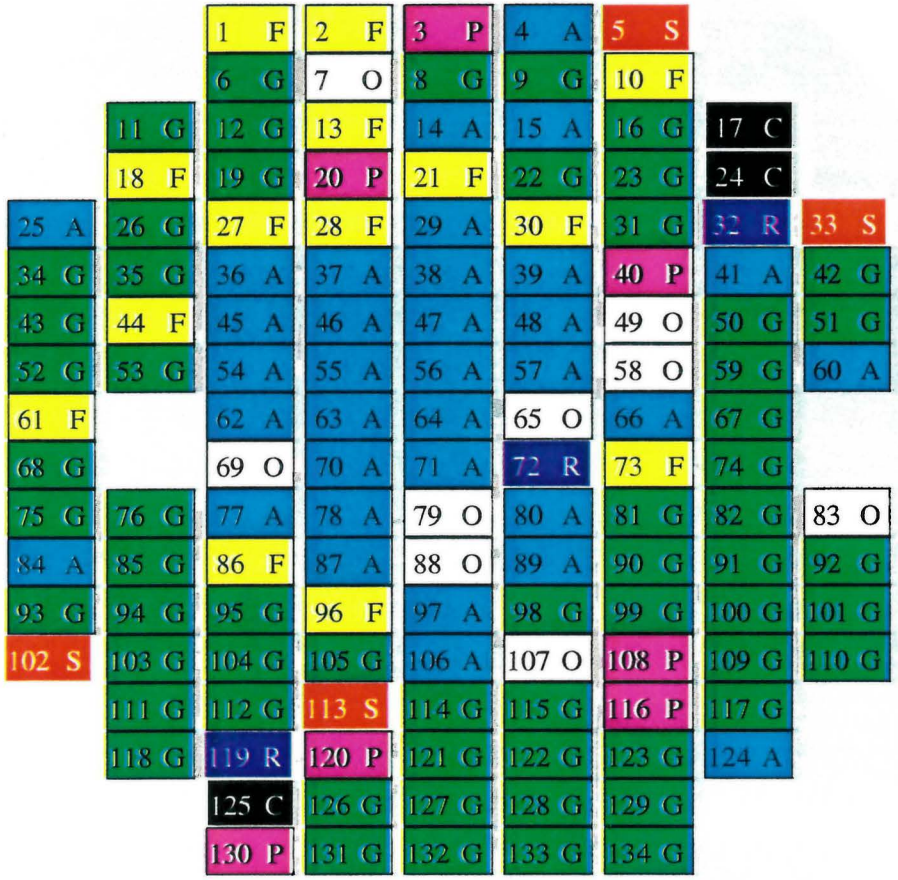
Date: 04/05/99





Types of die failures for wafer 76 s/n: Y21316-12-04 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

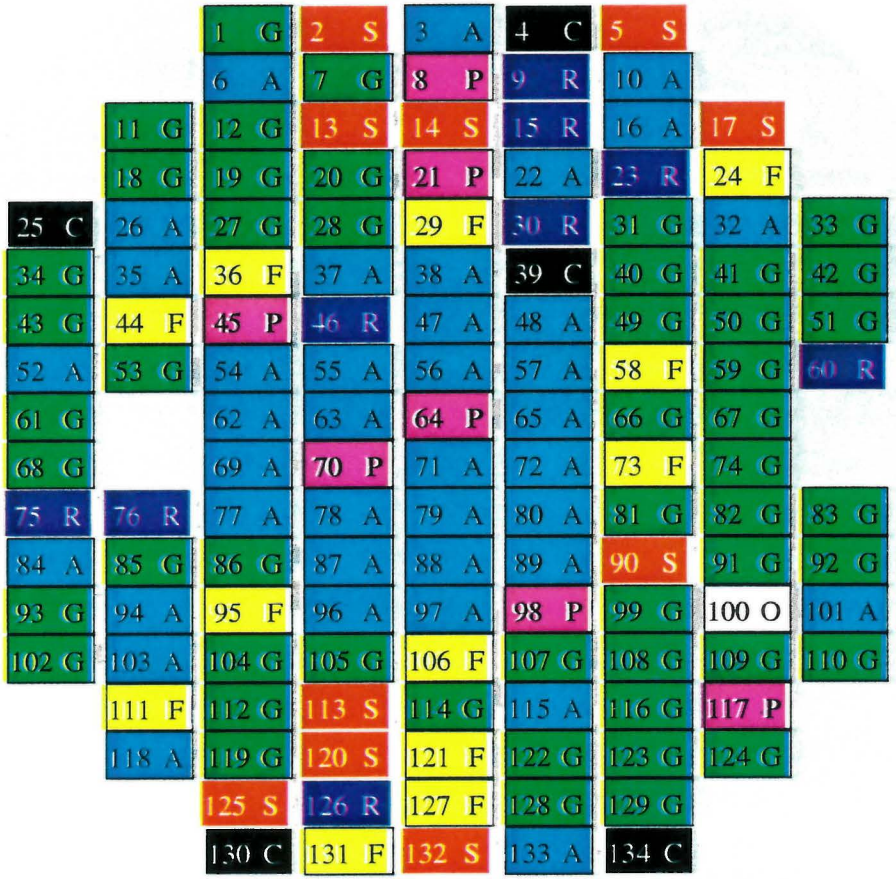
A Analog

O Operator

N No info

Types of die failures for wafer 82 s/n: Y21316-12-11 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

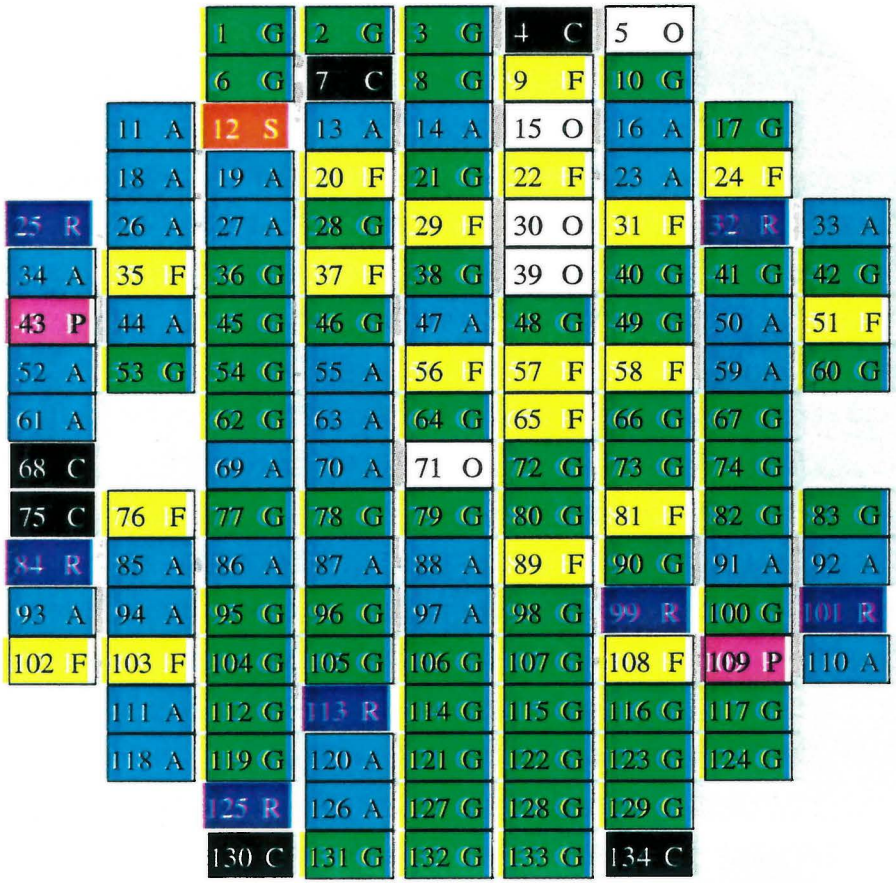
A Analog

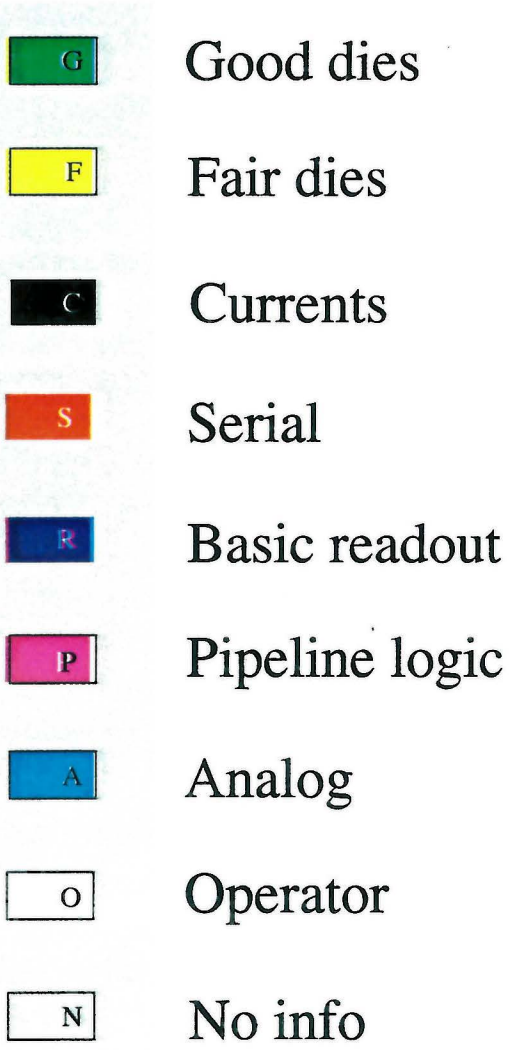
O Operator

N No info

Types of die failures for wafer 137 s/n: Y21316-12-12 (not backplated)

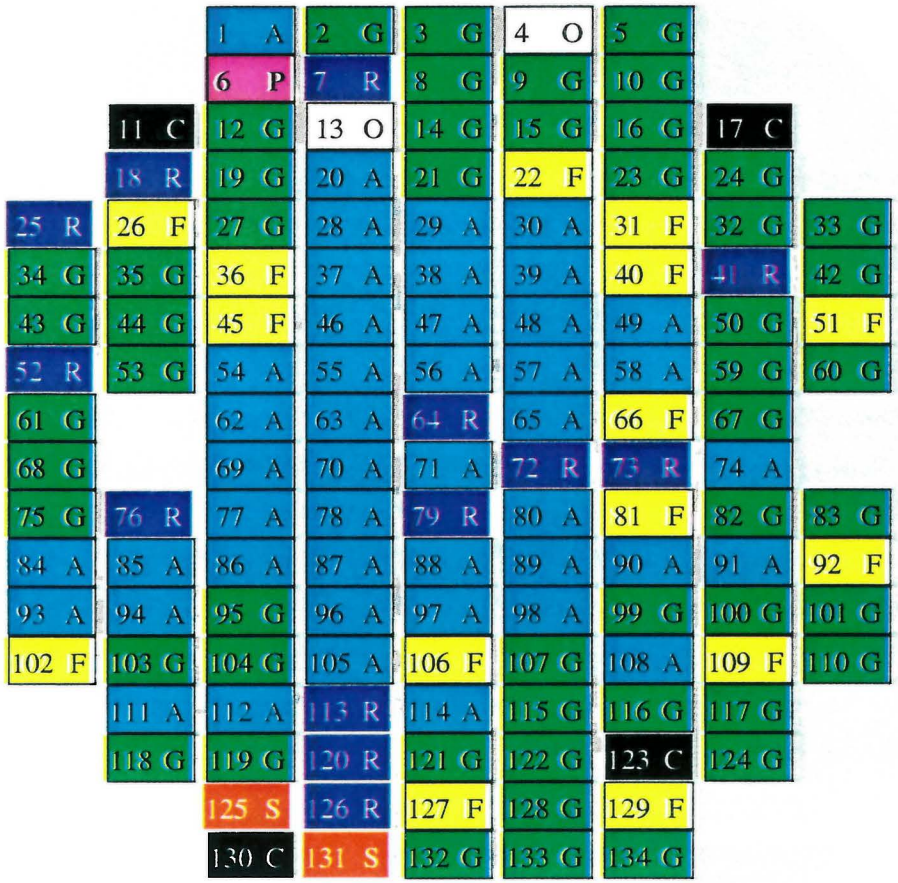
Date: 04/05/99

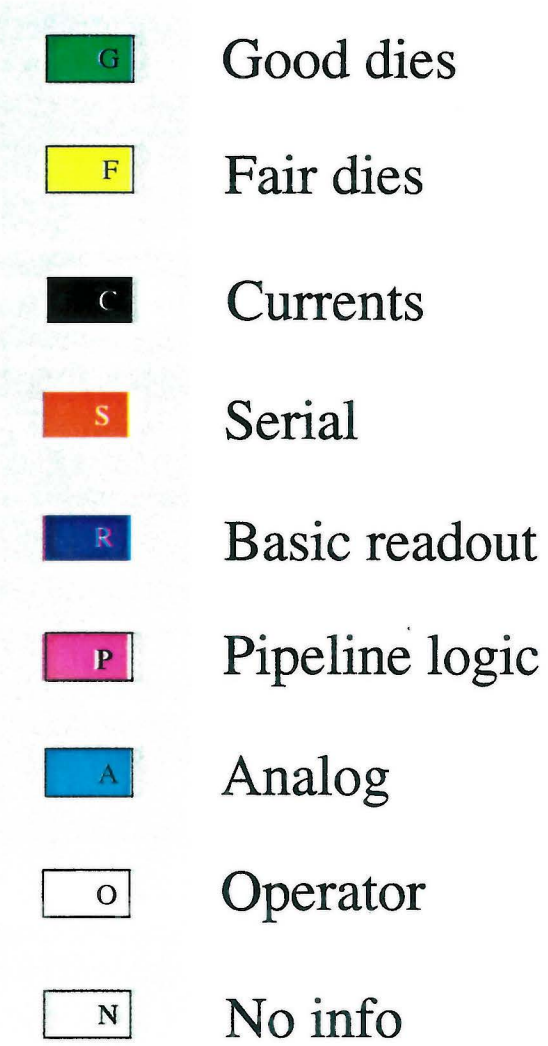




Types of die failures for wafer 80 s/n: Y21316-12-15 (not backplated)

Date: 04/05/99





APPENDIX D

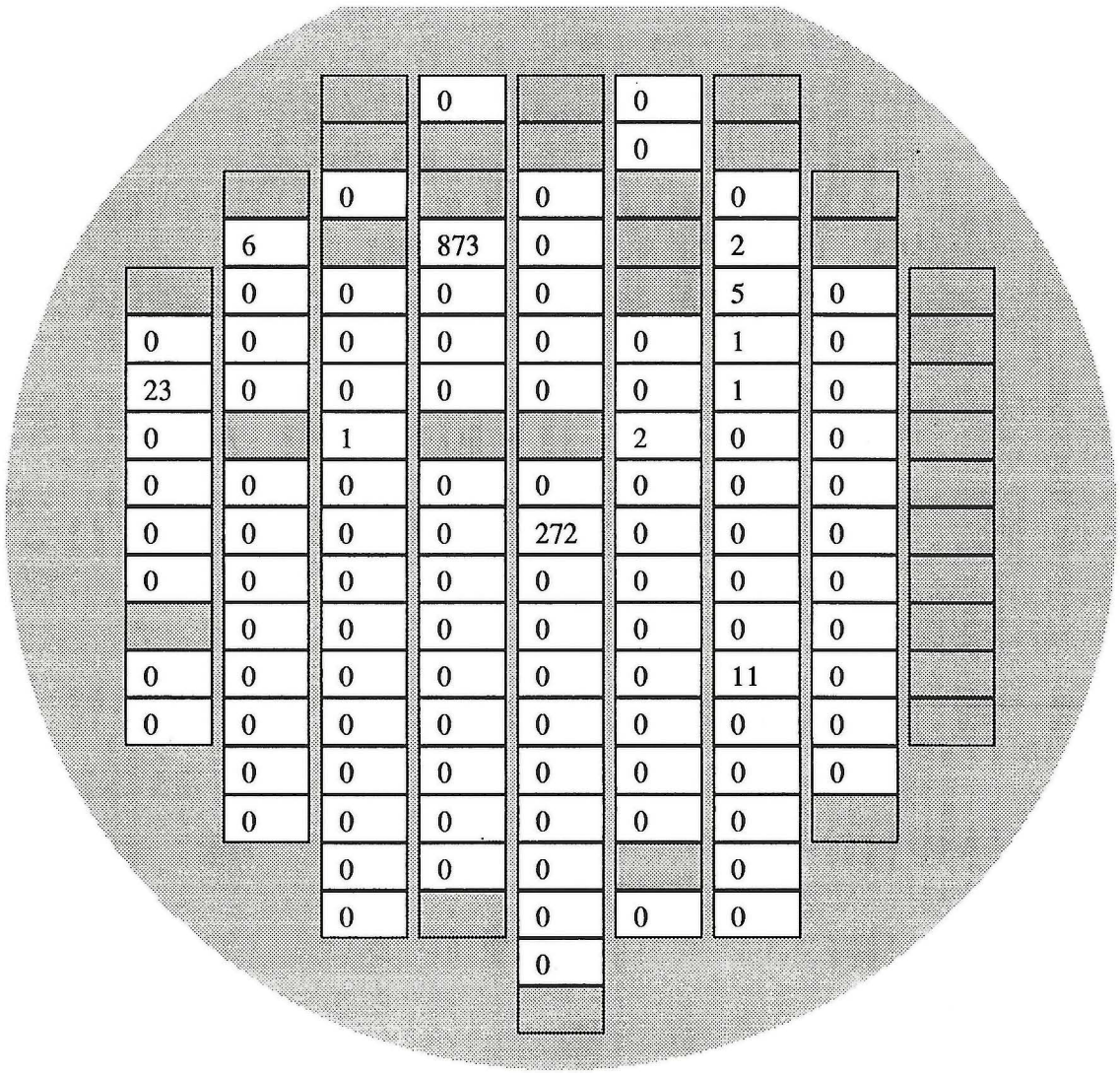
Appendix D

Random Bad Cell Maps

Lot	Wafer
8	1
8	3
8	4
8	6
8	11
8	15
8	17
9	2
9	3
9	5
10	1
10	2
10	8
10	10
10	18
11	3
11	5
11	11
11	18
11	20
12	4
12	11
12	12
12	15

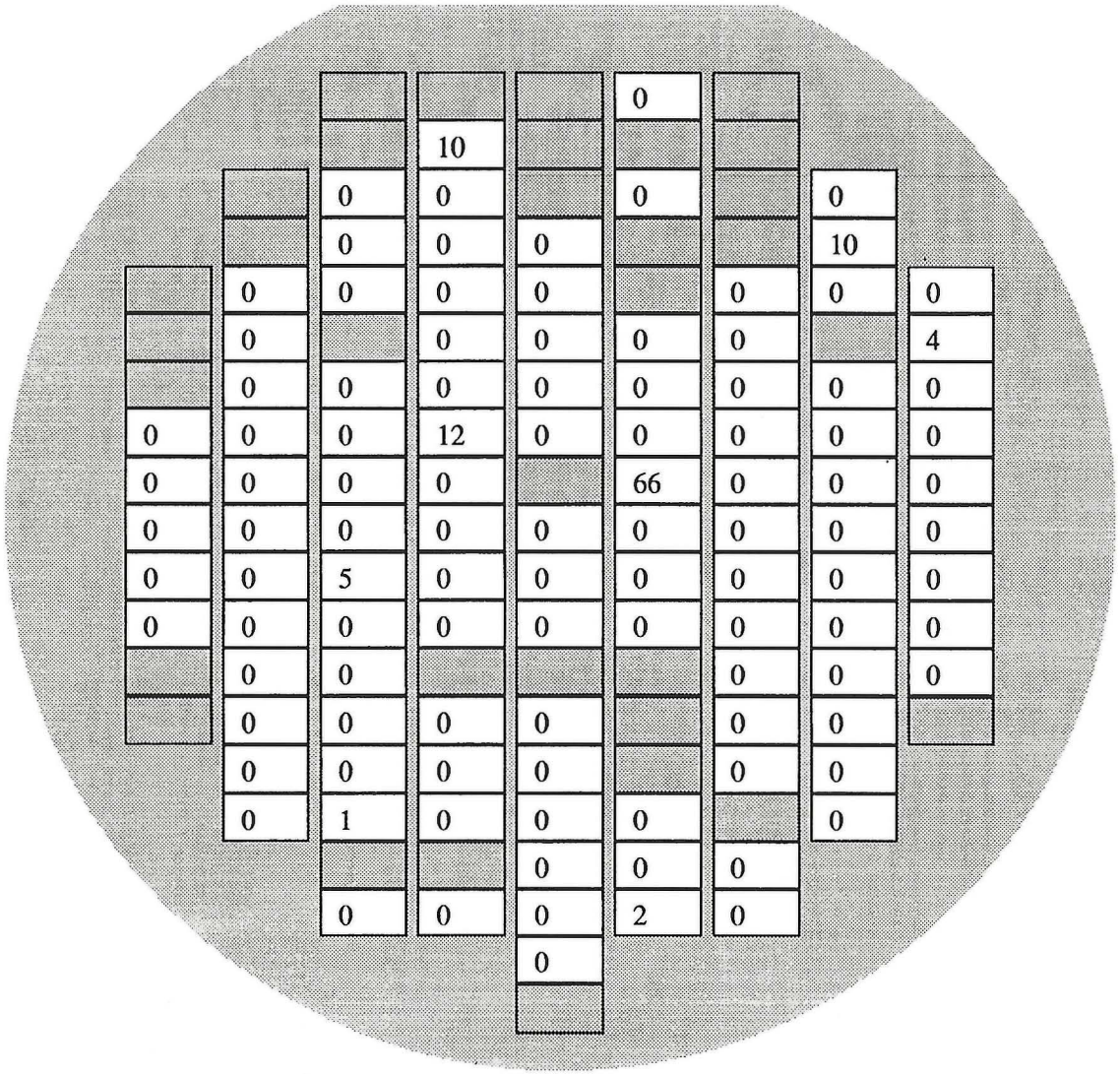
Random bad cell map for wafer 87 s/n: Y21316-08-01 (not backplated)

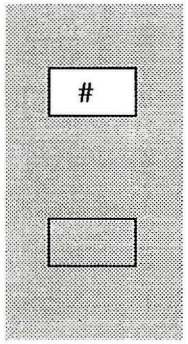
Date: 04/09/99



Random bad cell map for wafer 143 s/n: Y21316-08-15 (not backplated)

Date: 04/09/99



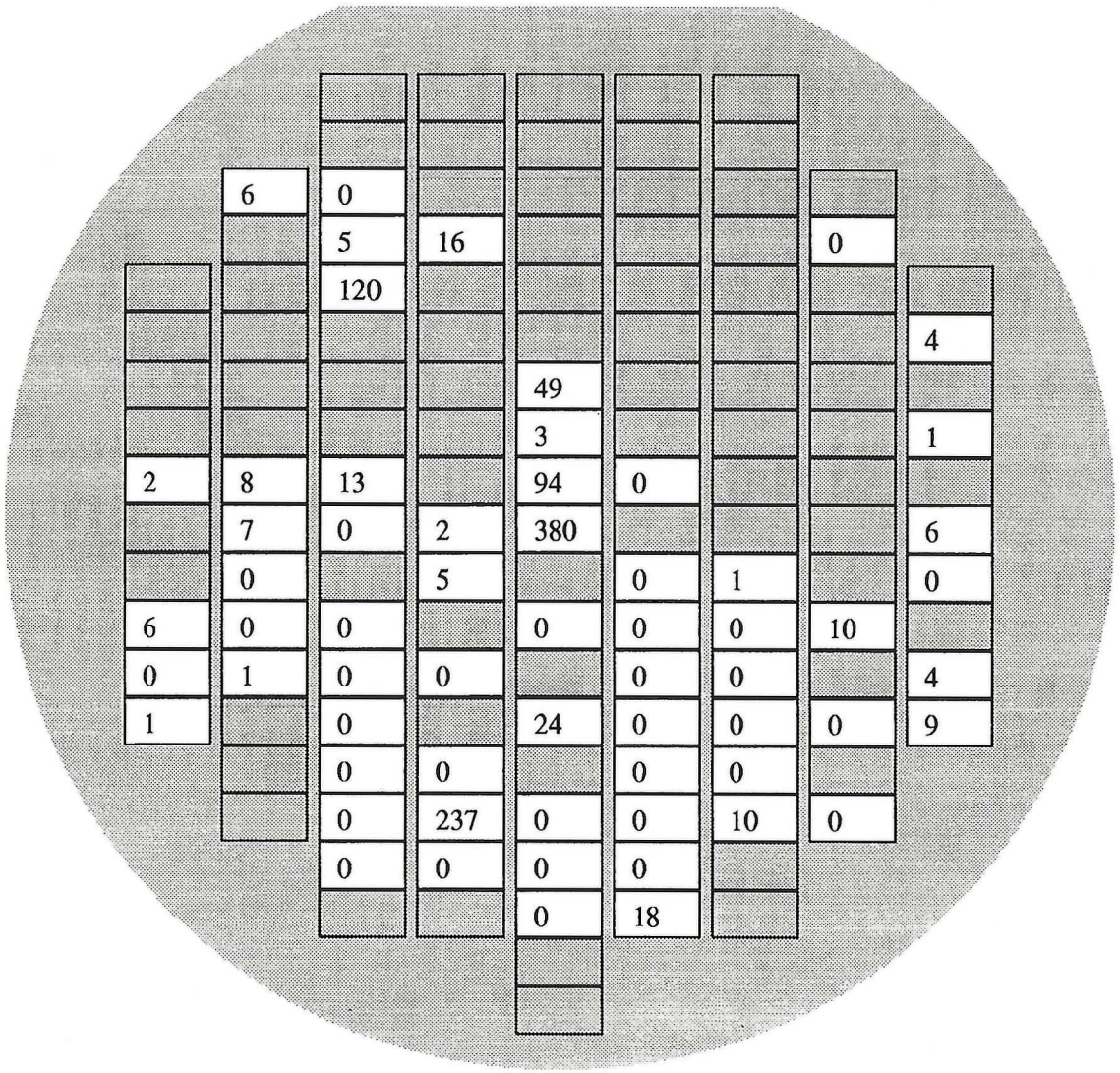


Number of bad cells in random locations

No info

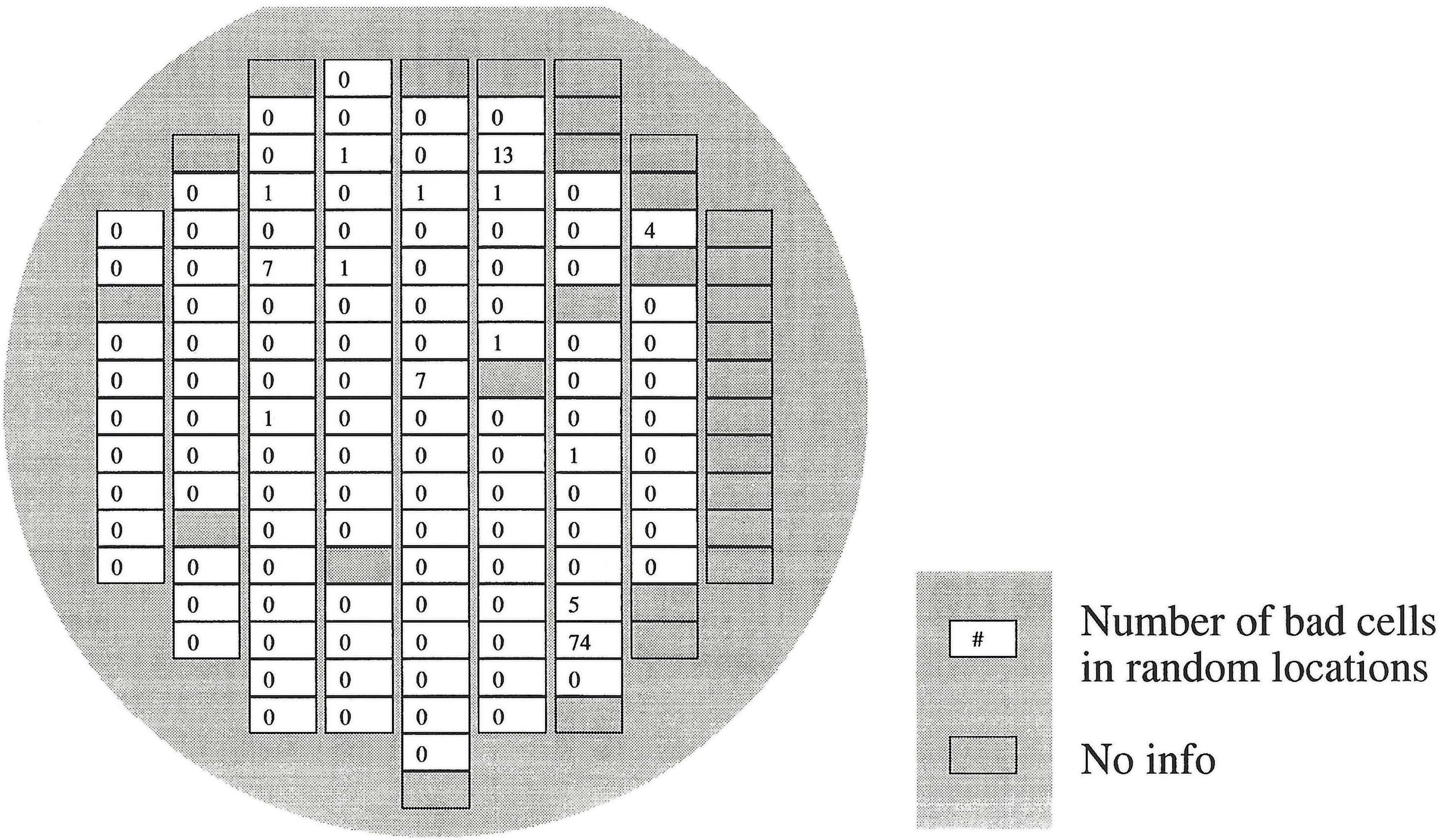
Random bad cell map for wafer 70 s/n: Y21316-08-03 (not backplated)

Date: 04/09/99



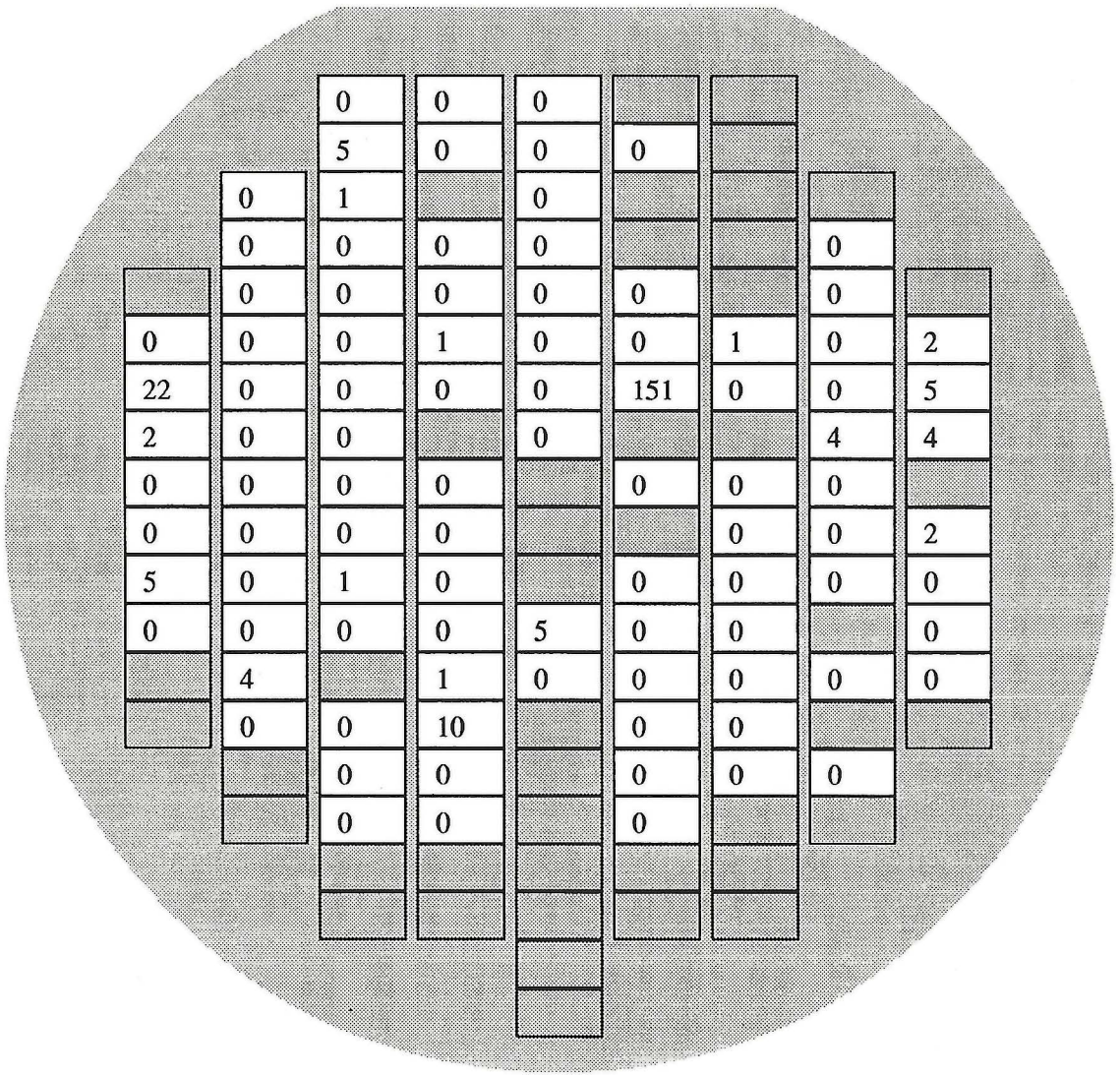
Random bad cell map for wafer 85 s/n: Y21316-08-04 (not backplated)

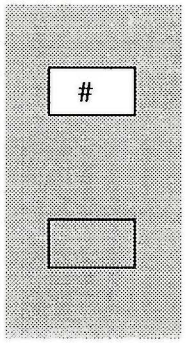
Date: 04/09/99



Random bad cell map for wafer 142 s/n: Y21316-08-11 (not backplated)

Date: 04/09/99



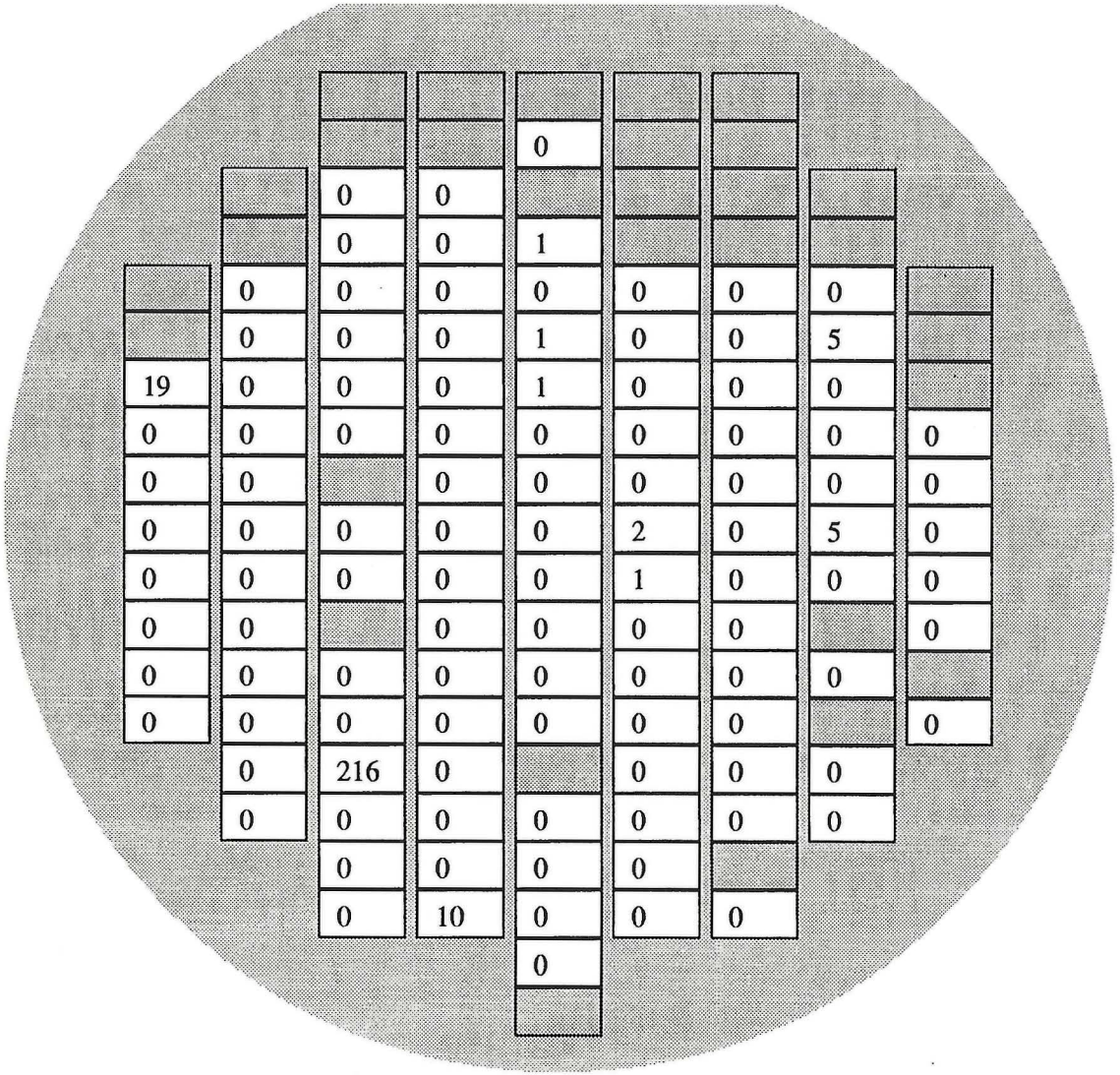


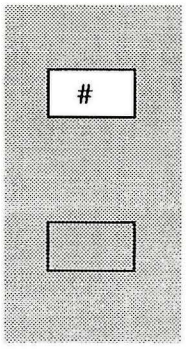
Number of bad cells in random locations

No info

Random bad cell map for wafer 141 s/n: Y21316-08-06 (not backplated)

Date: 04/09/99



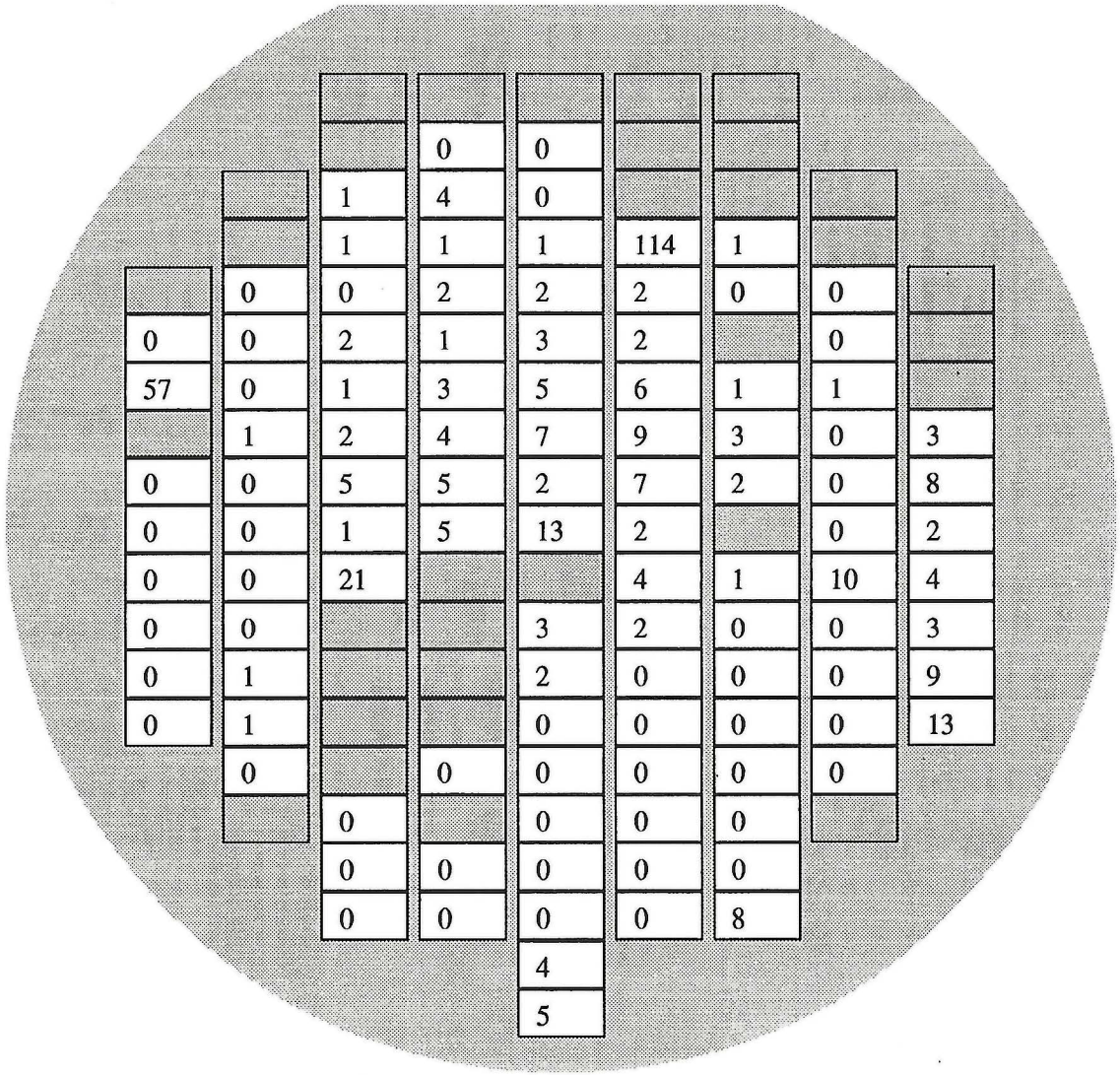


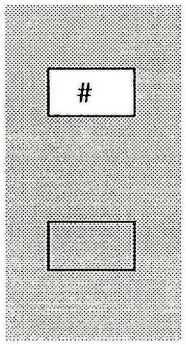
Number of bad cells in random locations

No info

Random bad cell map for wafer 140 s/n: Y21316-08-17 (not backplated)

Date: 04/09/99



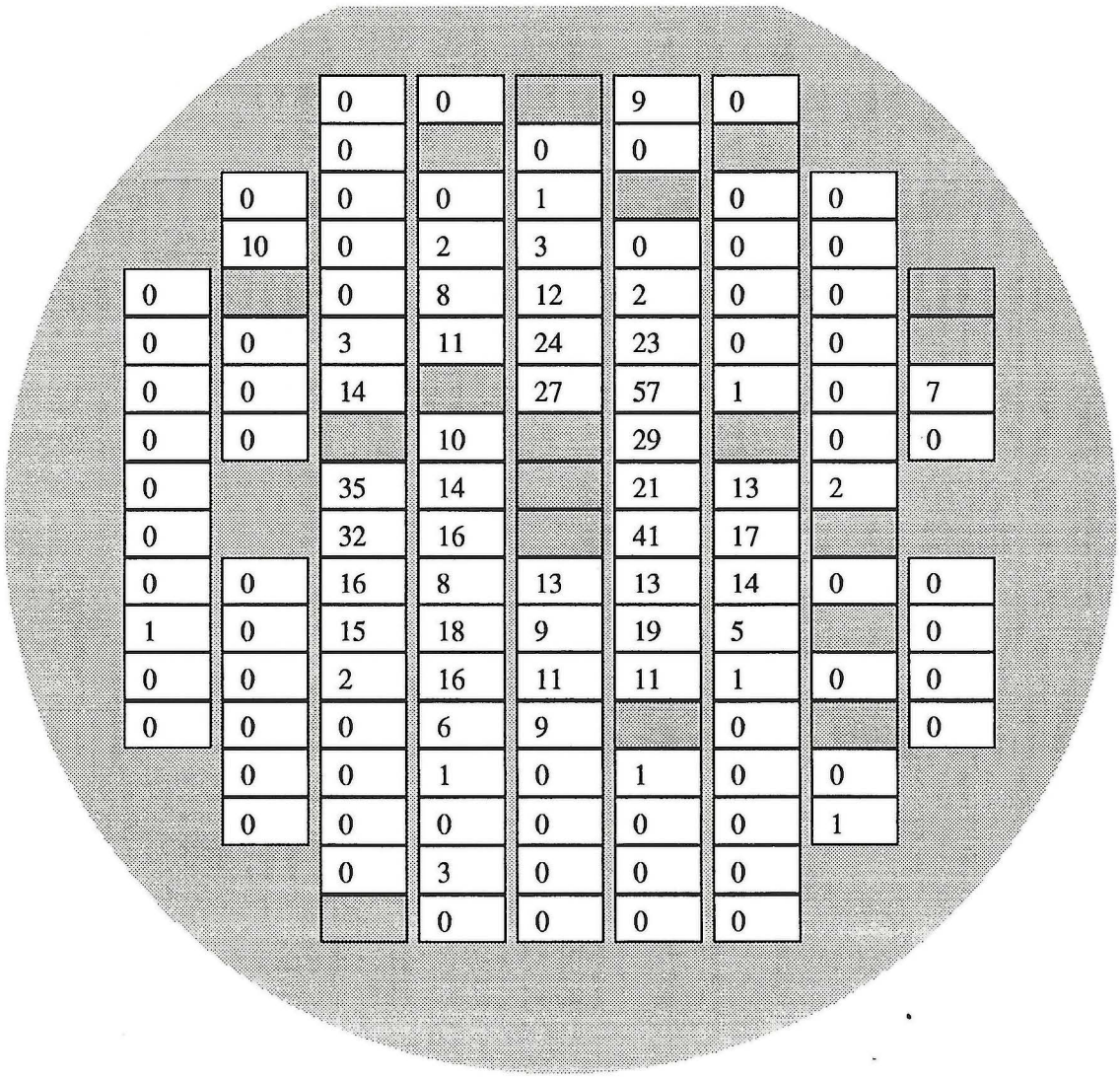


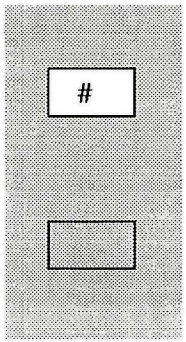
Number of bad cells in random locations

No info

Random bad cell map for wafer 92 s/n: Y21316-09-02 (not backplated)

Date: 04/09/99



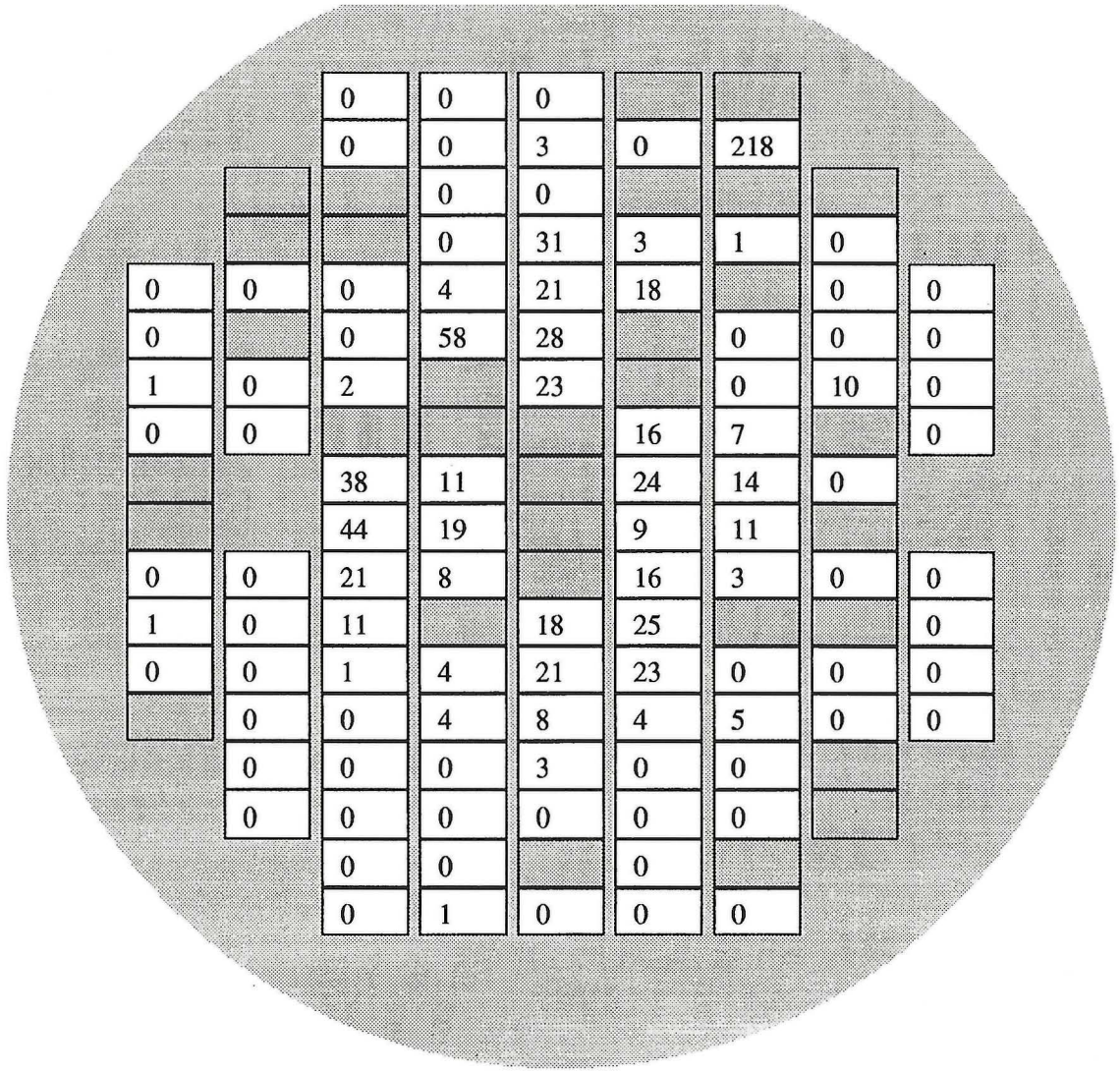


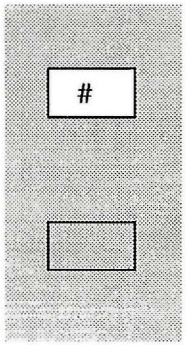
Number of bad cells in random locations

No info

Random bad cell map for wafer 74 s/n: Y21316-09-03 (not backplated)

Date: 04/09/99



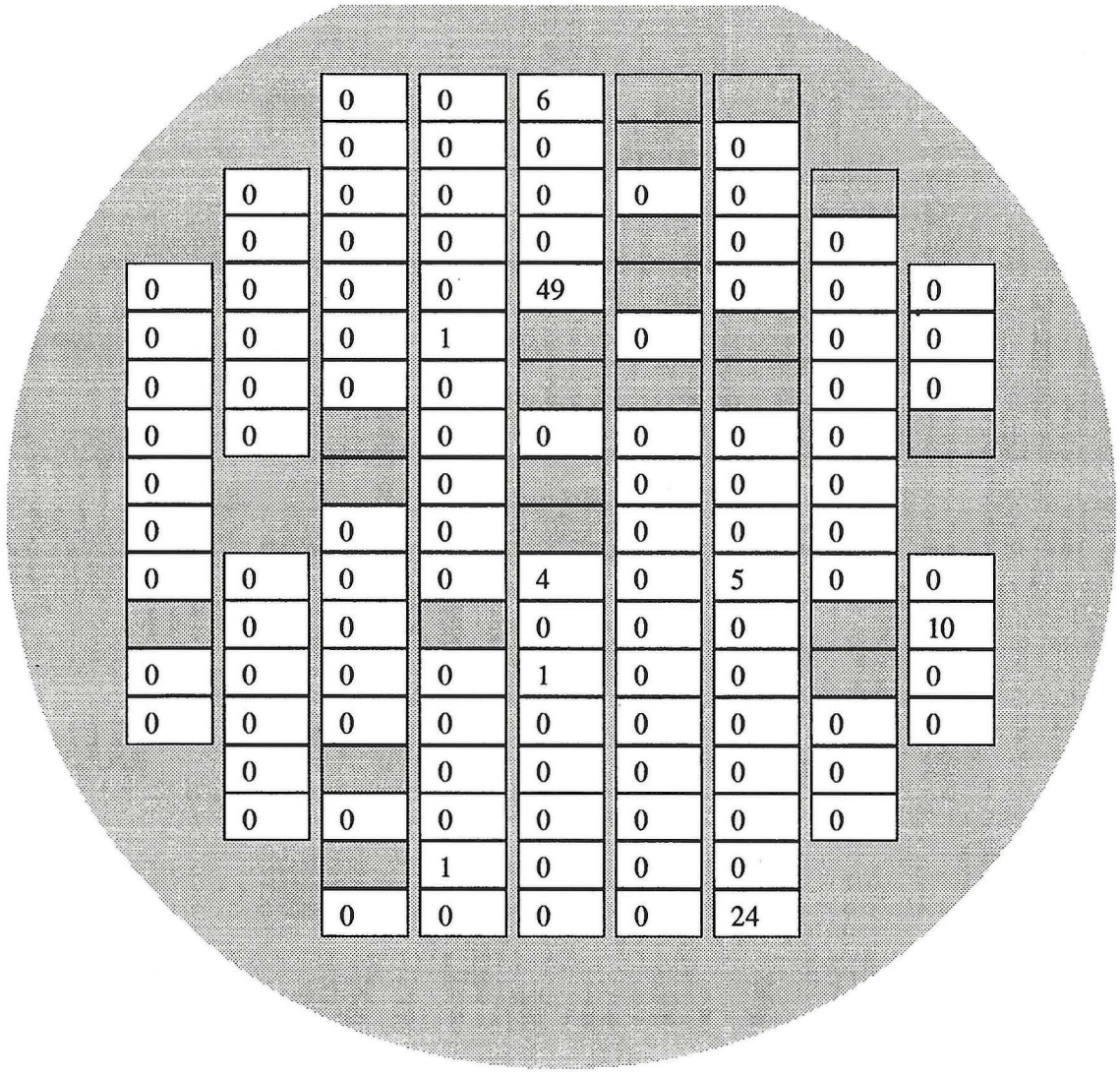


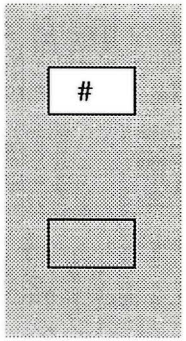
Number of bad cells in random locations

No info

Random bad cell map for wafer 93 s/n: Y21316-09-05 (not backplated)

Date: 04/09/99



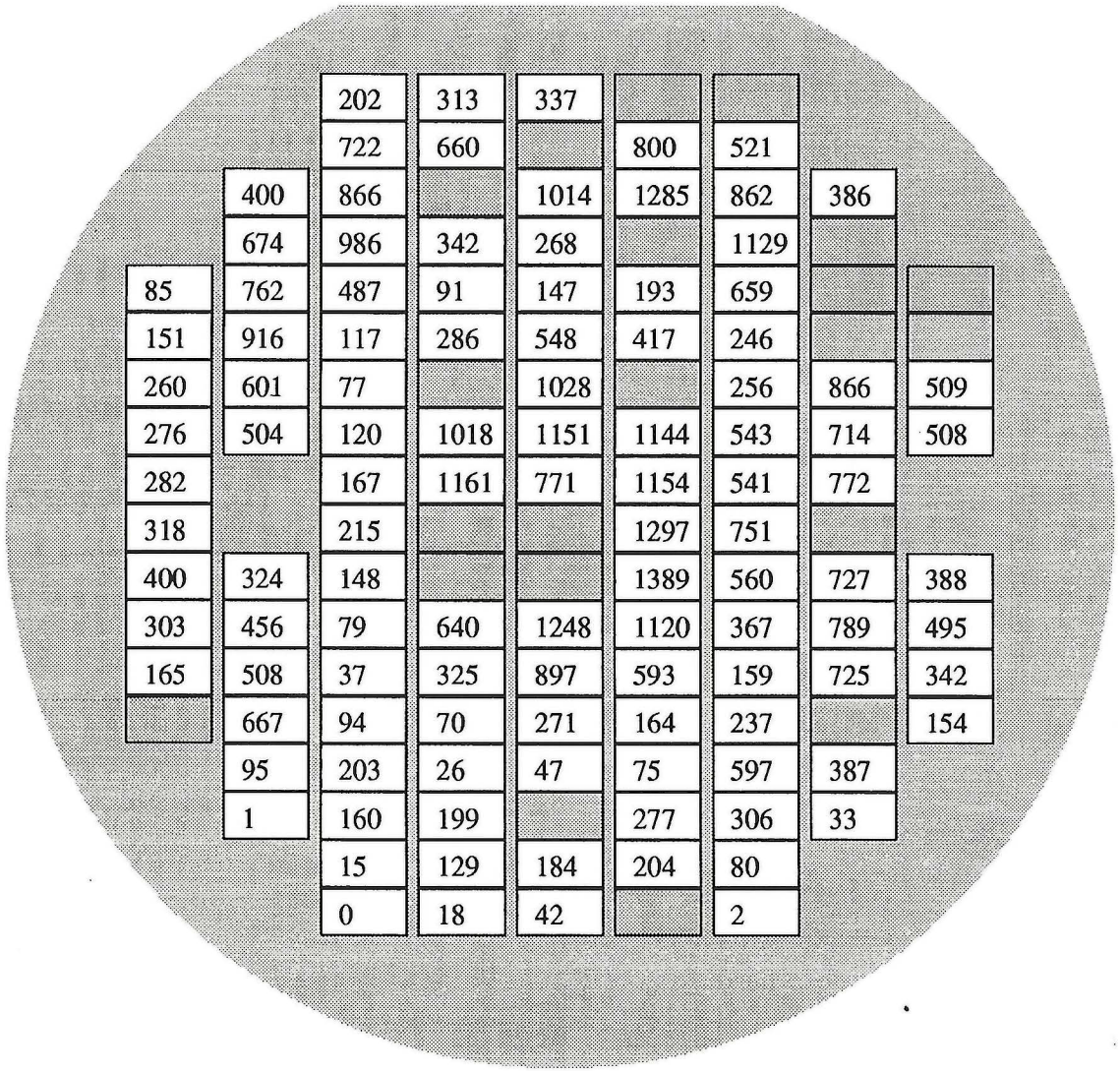


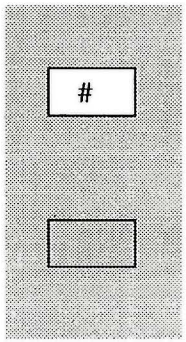
Number of bad cells in random locations

No info

Random bad cell map for wafer 91 s/n: Y21316-10-01 (not backplated)

Date: 04/09/99



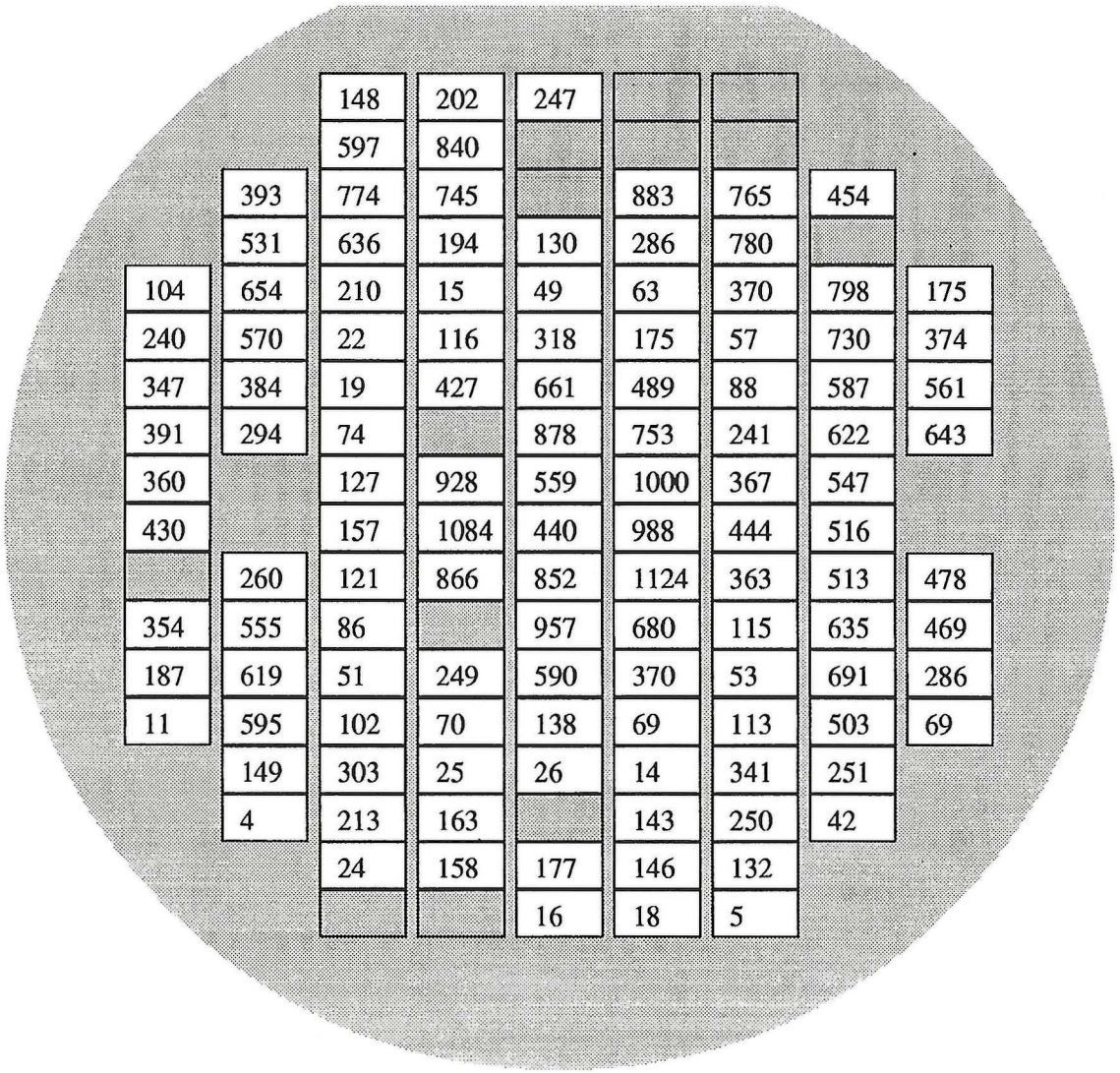


Number of bad cells in random locations

No info

Random bad cell map for wafer 89 s/n: Y21316-10-02 (not backplated)

Date: 04/09/99

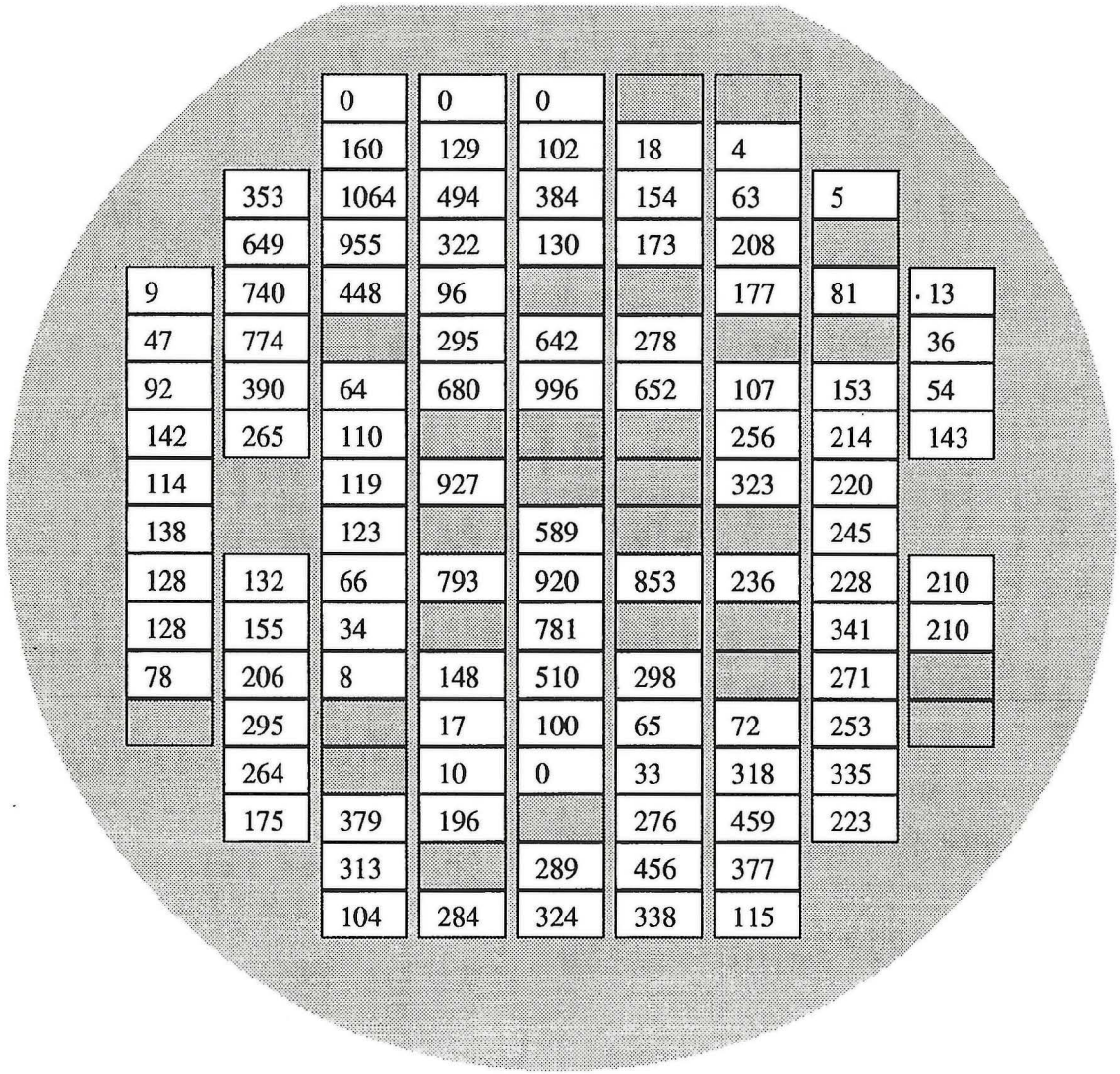


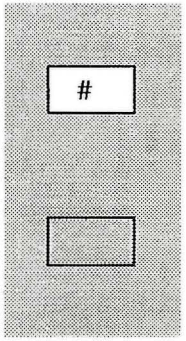
Number of bad cells in random locations

No info

Random bad cell map for wafer 72 s/n: Y21316-10-08 (not backplated)

Date: 04/09/99



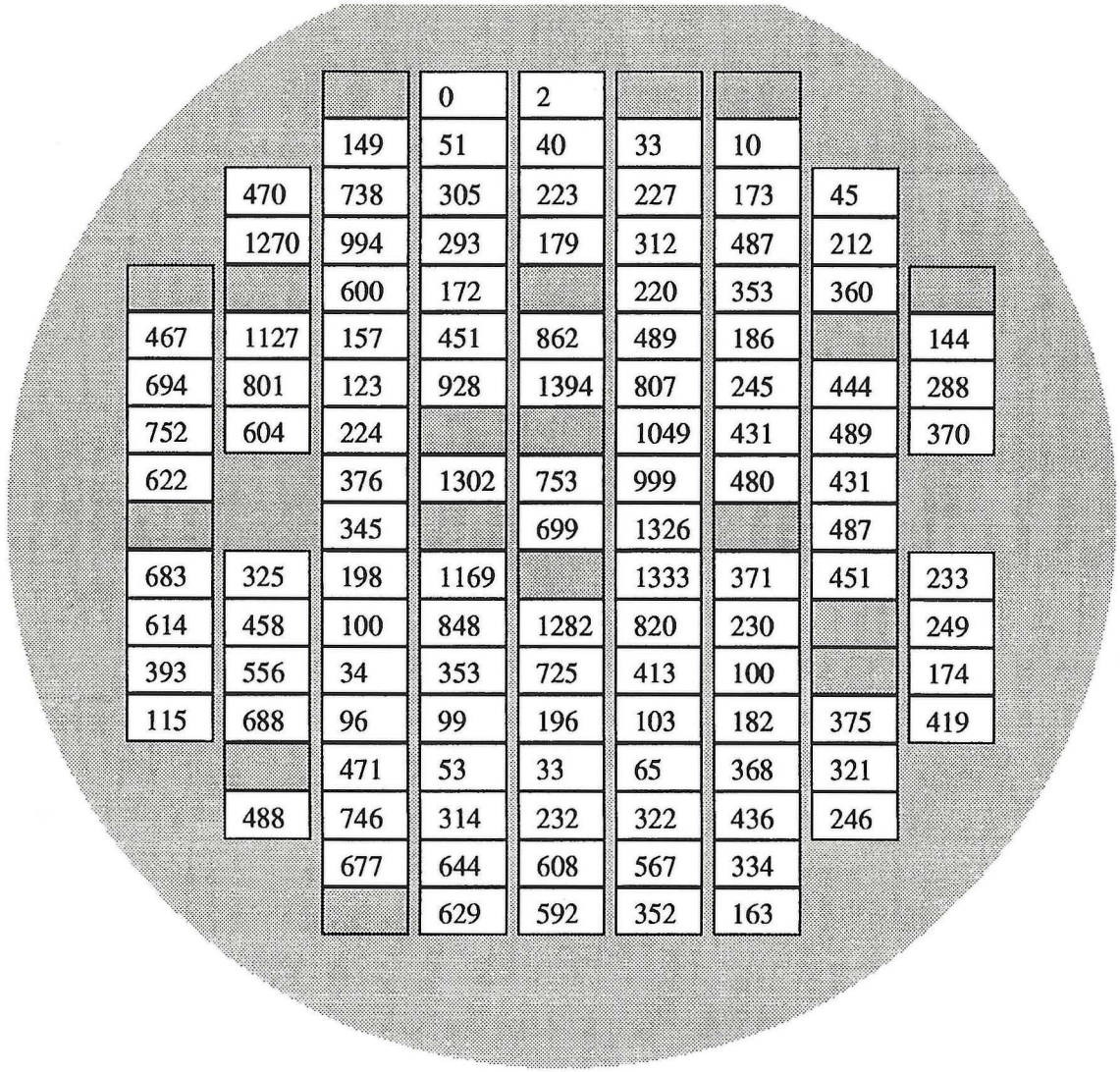


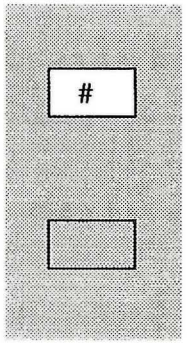
Number of bad cells in random locations

No info

Random bad cell map for wafer 146 s/n: Y21316-10-10 (not backplated)

Date: 04/14/99



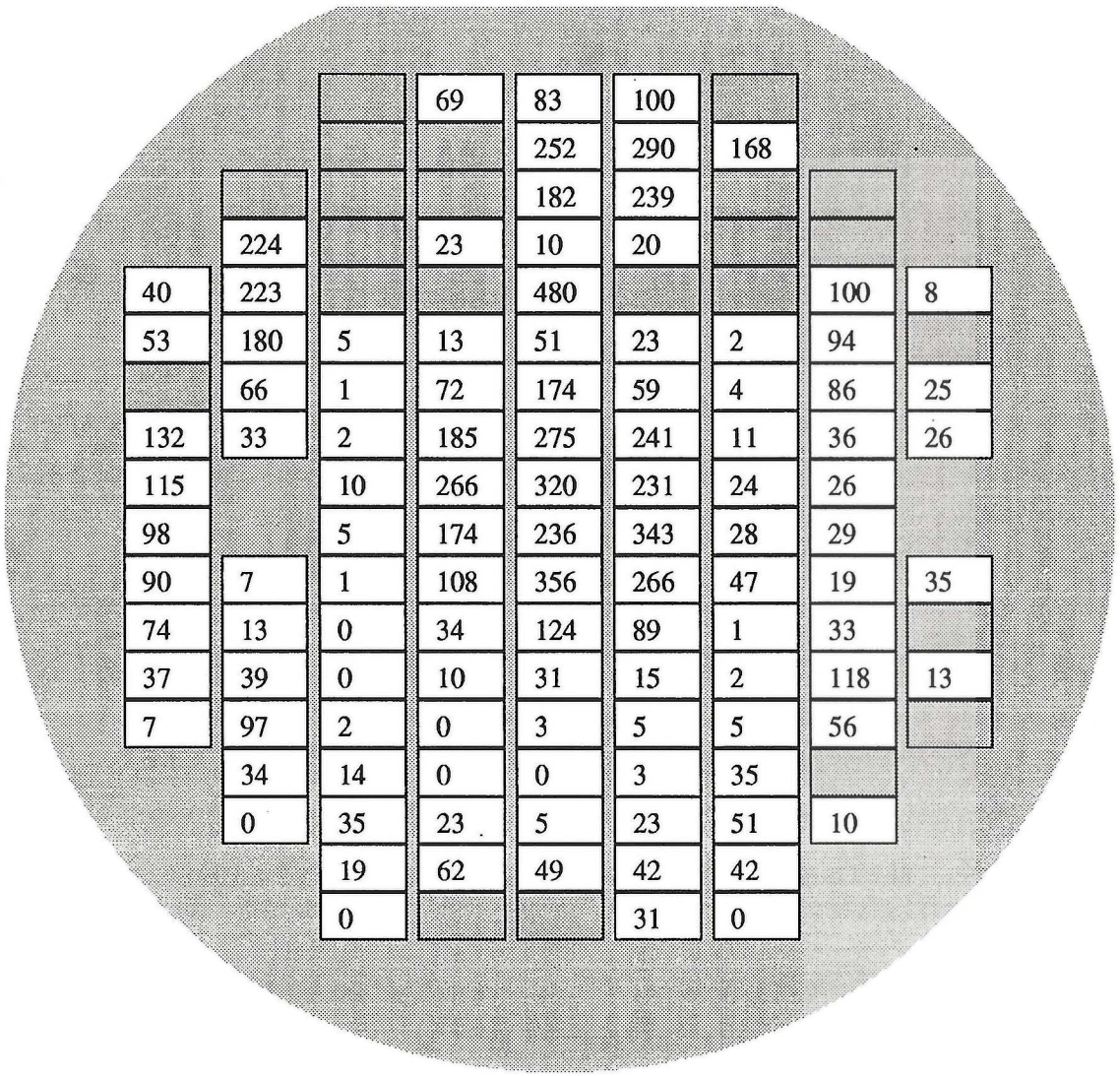


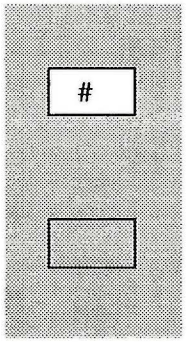
Number of bad cells in random locations

No info

Random bad cell map for wafer 145 s/n: Y21316-10-18 (not backplated)

Date: 04/13/99



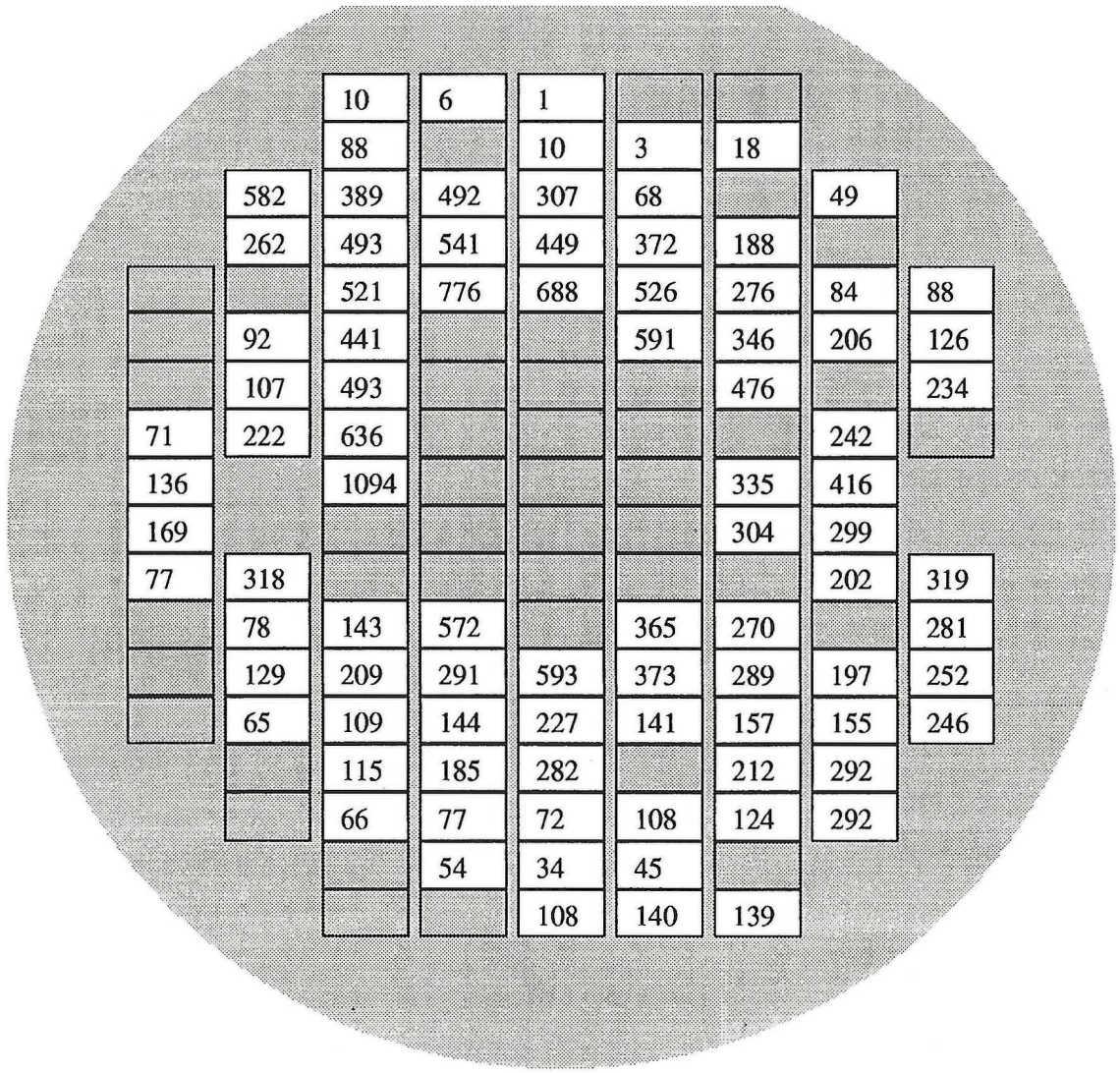


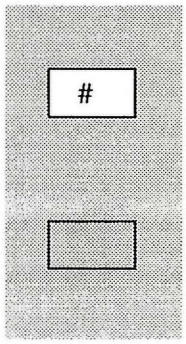
Number of bad cells in random locations

No info

Random bad cell map for wafer 81 s/n: Y21316-11-03 (not backplated)

Date: 04/09/99



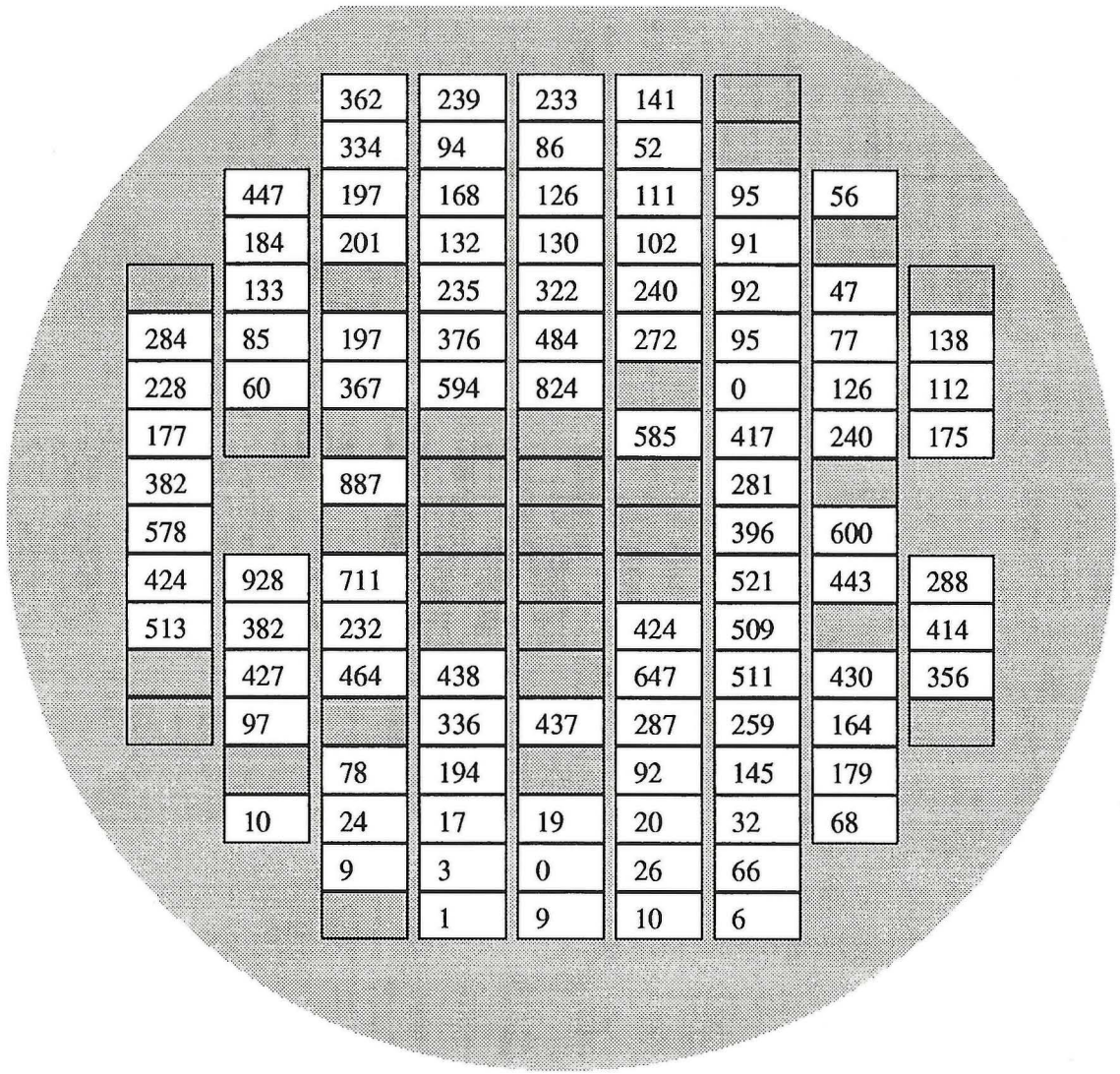


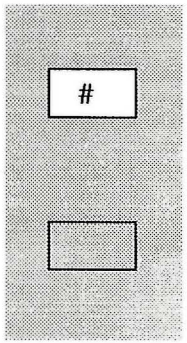
Number of bad cells in random locations

No info

Random bad cell map for wafer 144 s/n: Y21316-11-05 (not backplated)

Date: 04/09/99



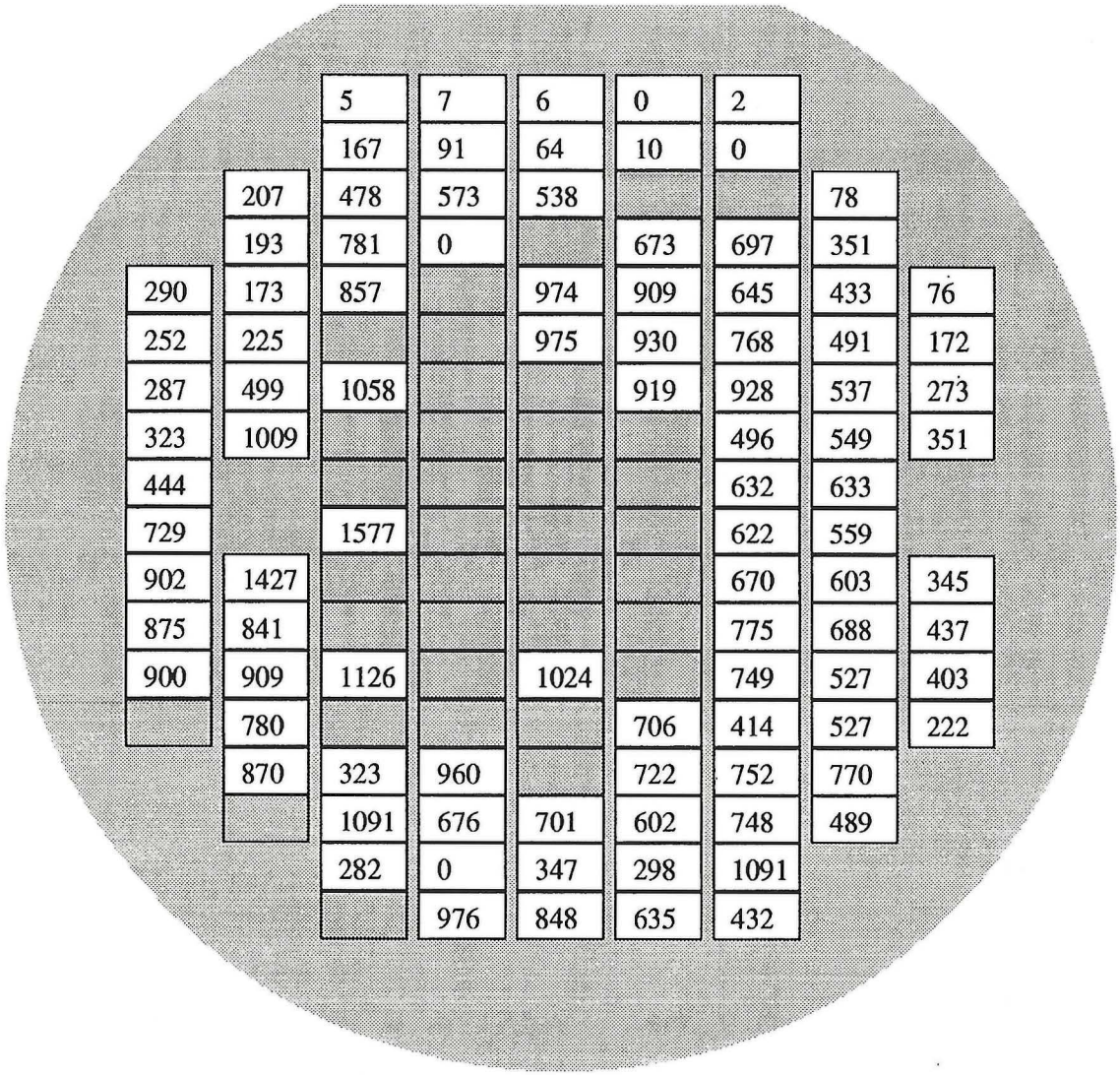


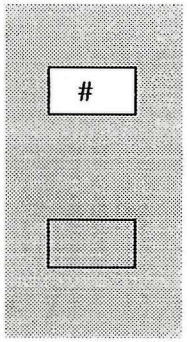
Number of bad cells in random locations

No info

Random bad cell map for wafer 138 s/n: Y21316-11-11 (not backplated)

Date: 04/09/99



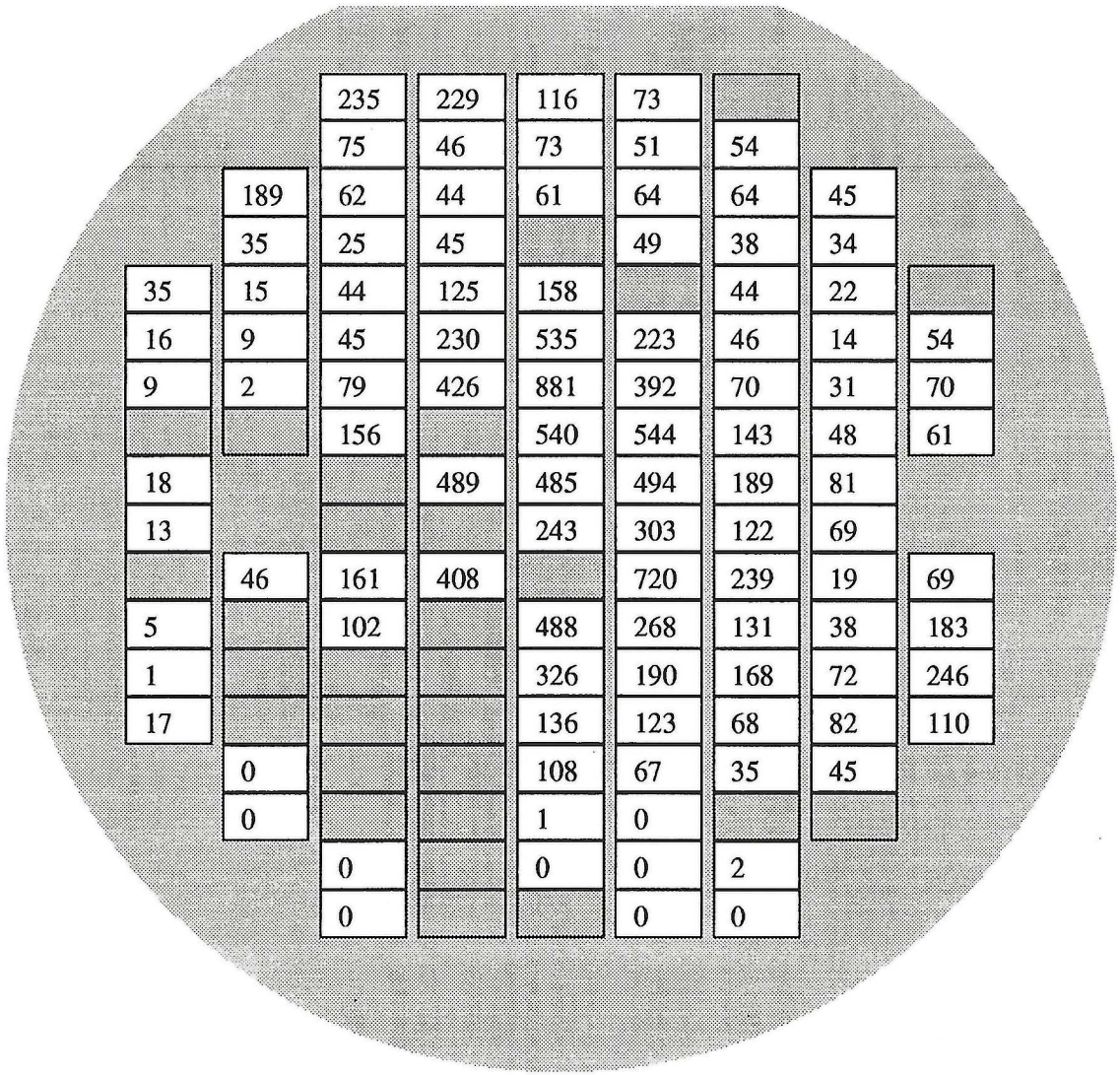


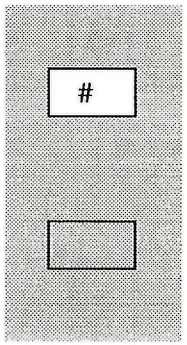
Number of bad cells in random locations

No info

Random bad cell map for wafer 83 s/n: Y21316-11-18 (not backplated)

Date: 04/09/99



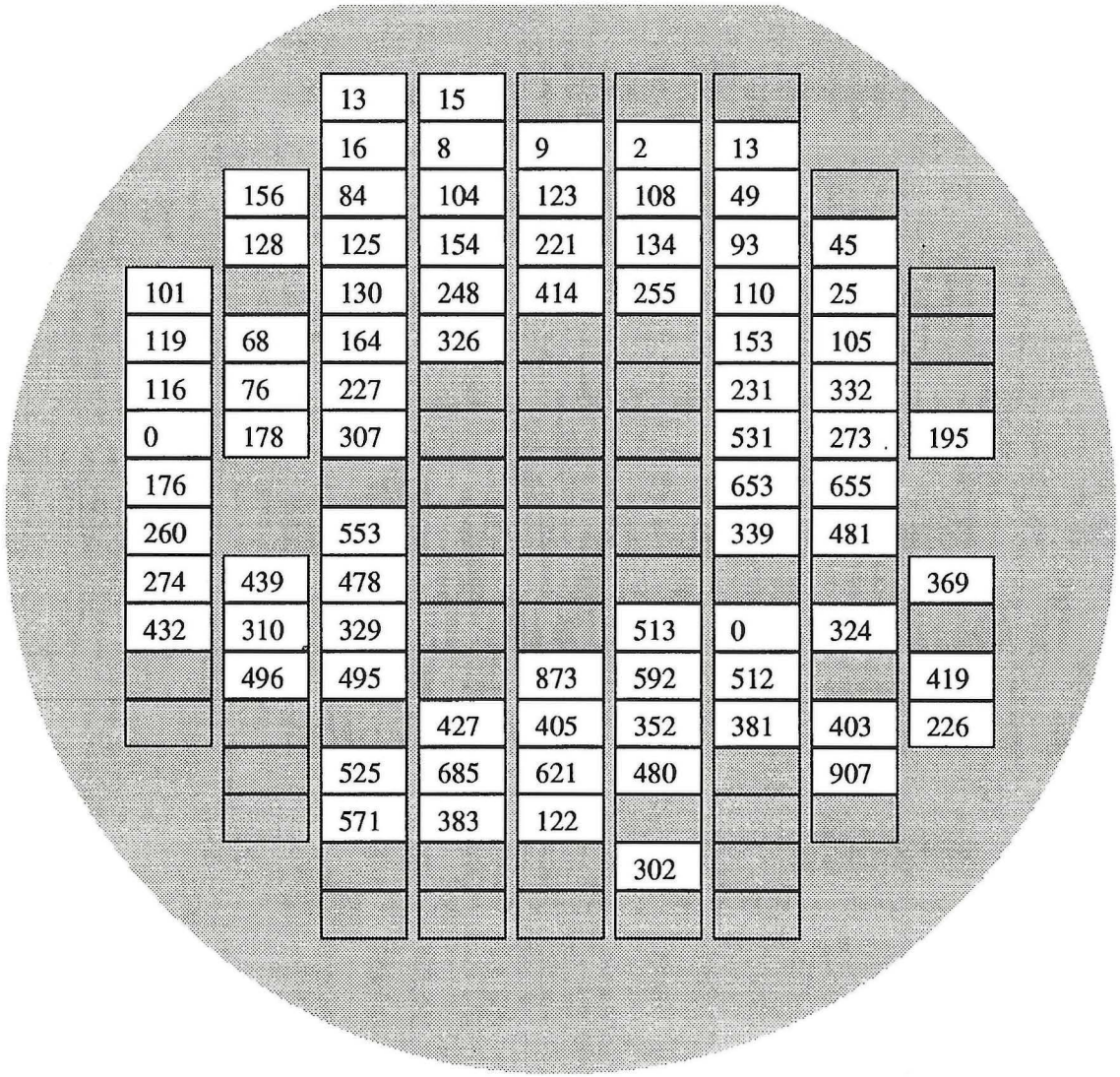


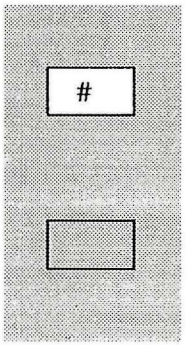
Number of bad cells in random locations

No info

Random bad cell map for wafer 69 s/n: Y21316-11-20 (not backplated)

Date: 04/09/99



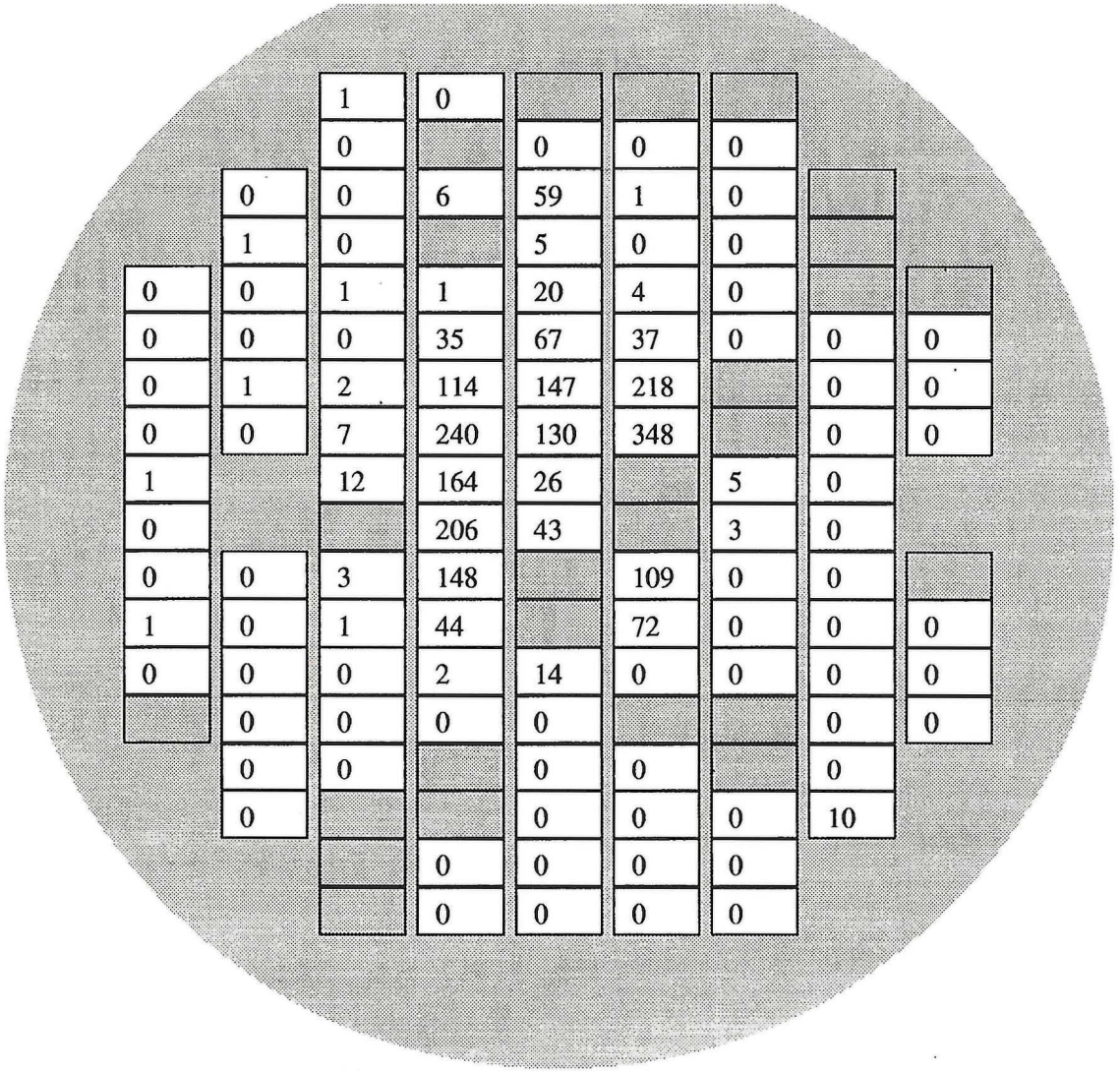


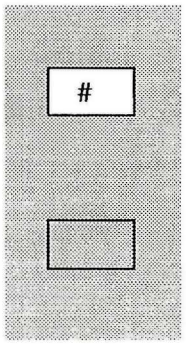
Number of bad cells in random locations

No info

Random bad cell map for wafer 76 s/n: Y21316-12-04 (not backplated)

Date: 04/09/99



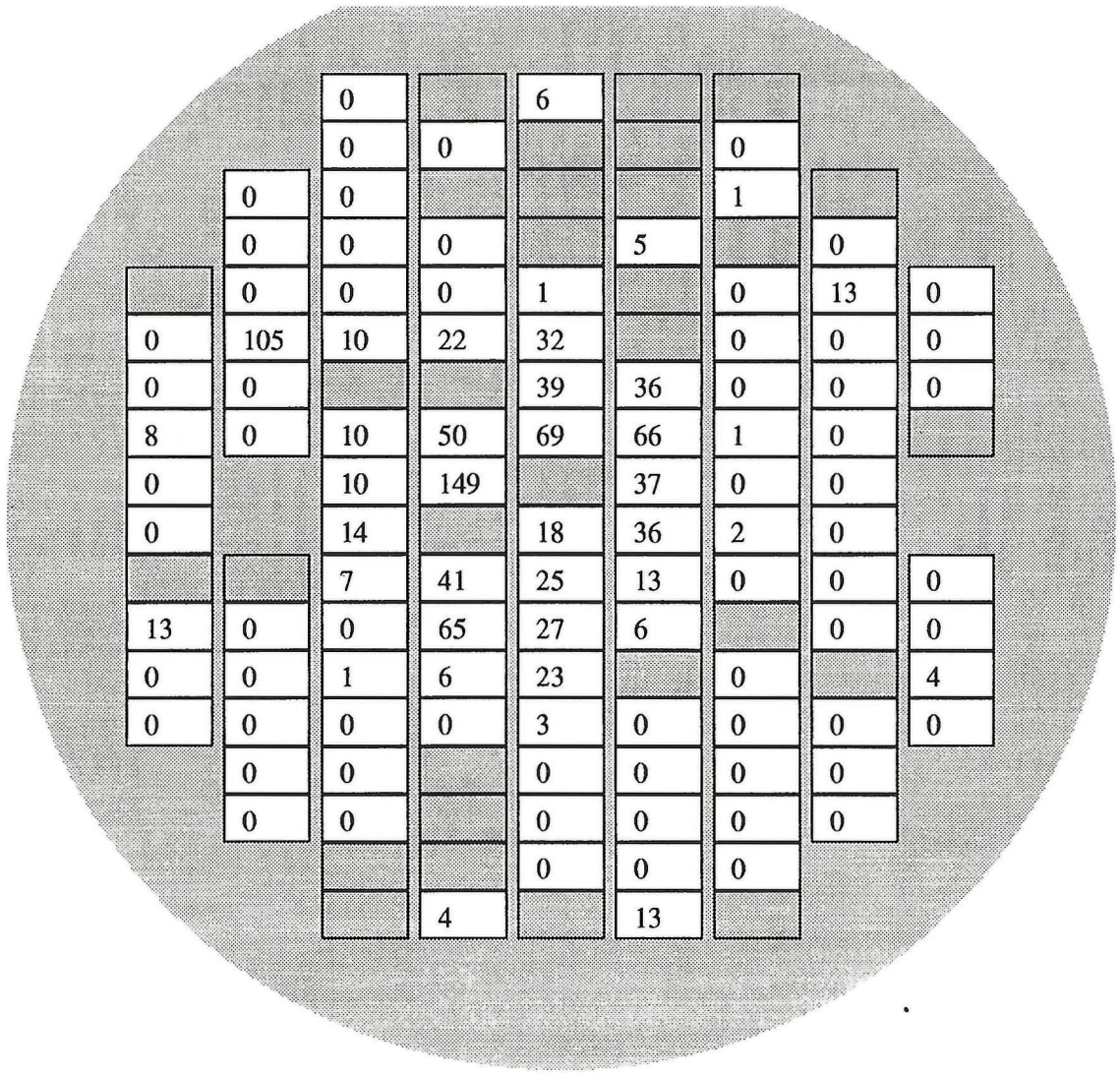


Number of bad cells in random locations

No info

Random bad cell map for wafer 82 s/n: Y21316-12-11 (not backplated)

Date: 04/09/99

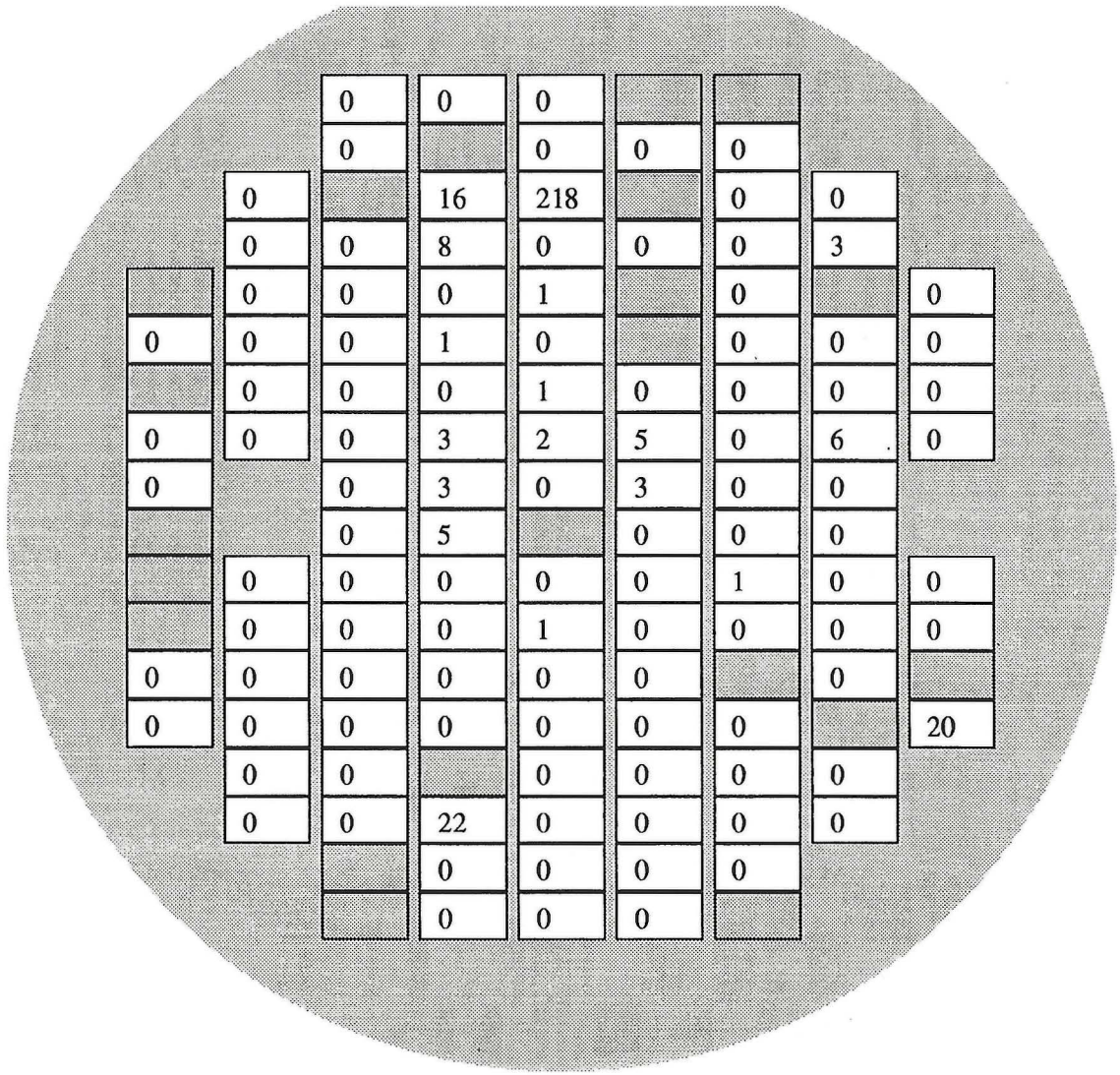


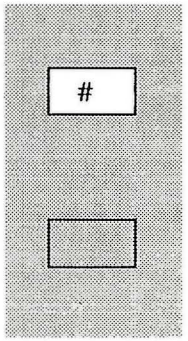
Number of bad cells in random locations

No info

Random bad cell map for wafer 137 s/n: Y21316-12-12 (not backplated)

Date: 04/09/99



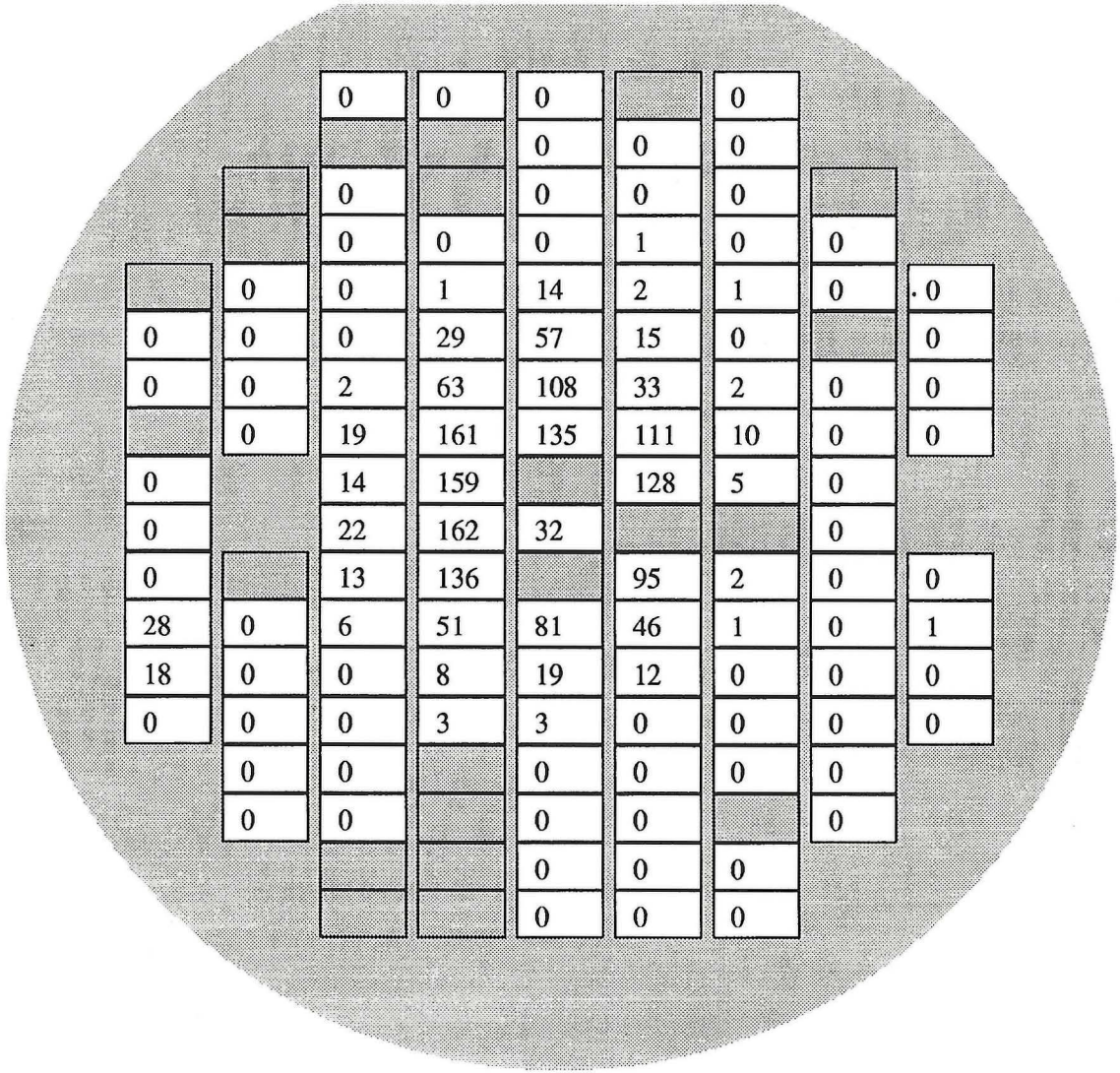


Number of bad cells in random locations

No info

Random bad cell map for wafer 80 s/n: Y21316-12-15 (not backplated)

Date: 04/09/99



APPENDIX E

Appendix E

Chip Pedestal Maps

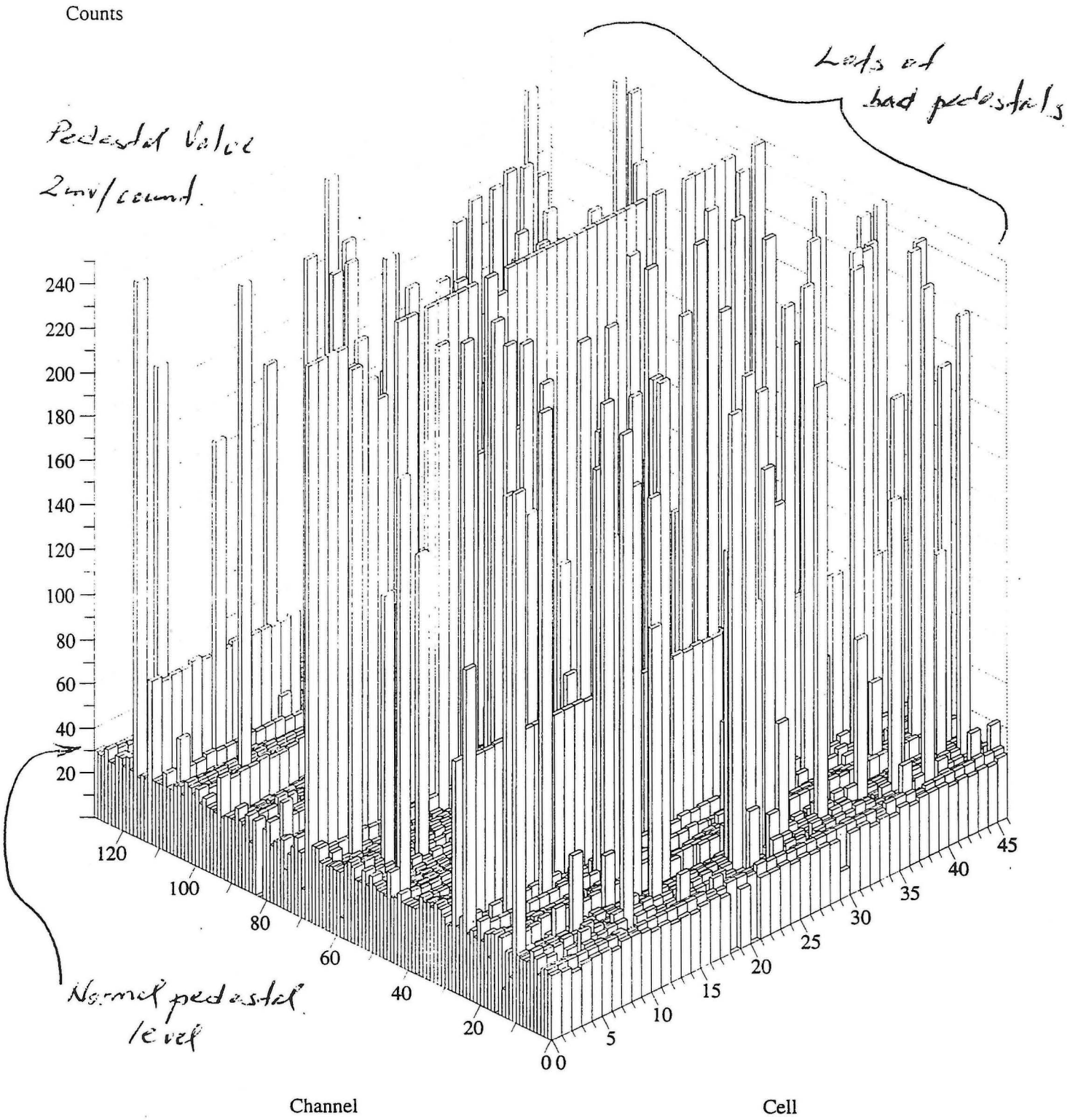
1) Good - Wafer 92 (lot 9, wafer 2), die 104, positive polarity

2) Fair - Wafer 92 (lot 9, wafer 2), die 69, positive polarity

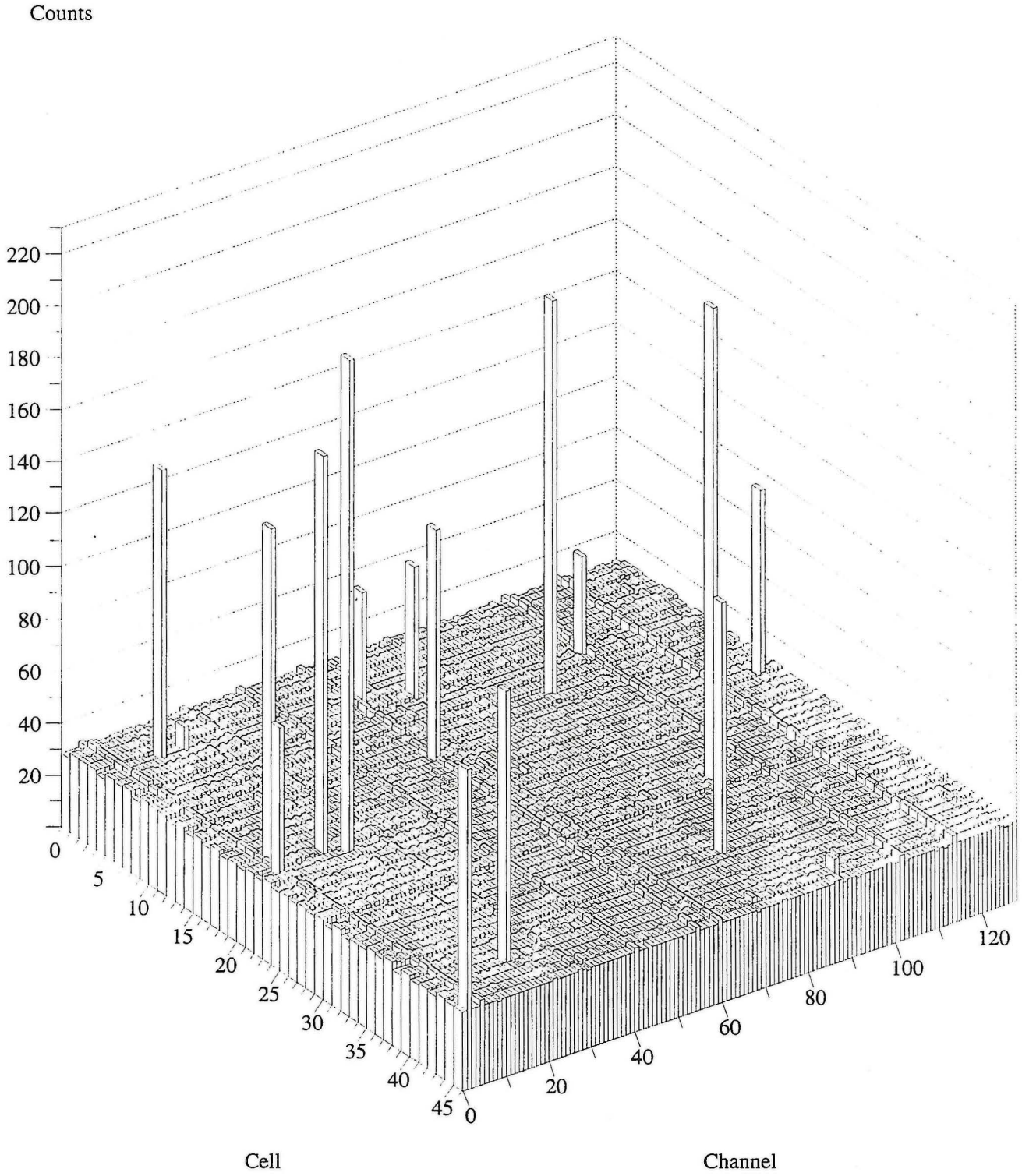
3) Fair - Wafer 92 (lot 9, wafer 2), die 69, negative polarity

4) Bad - Wafer 91 (Lot 10, wafer 1), die 38, positive polarity

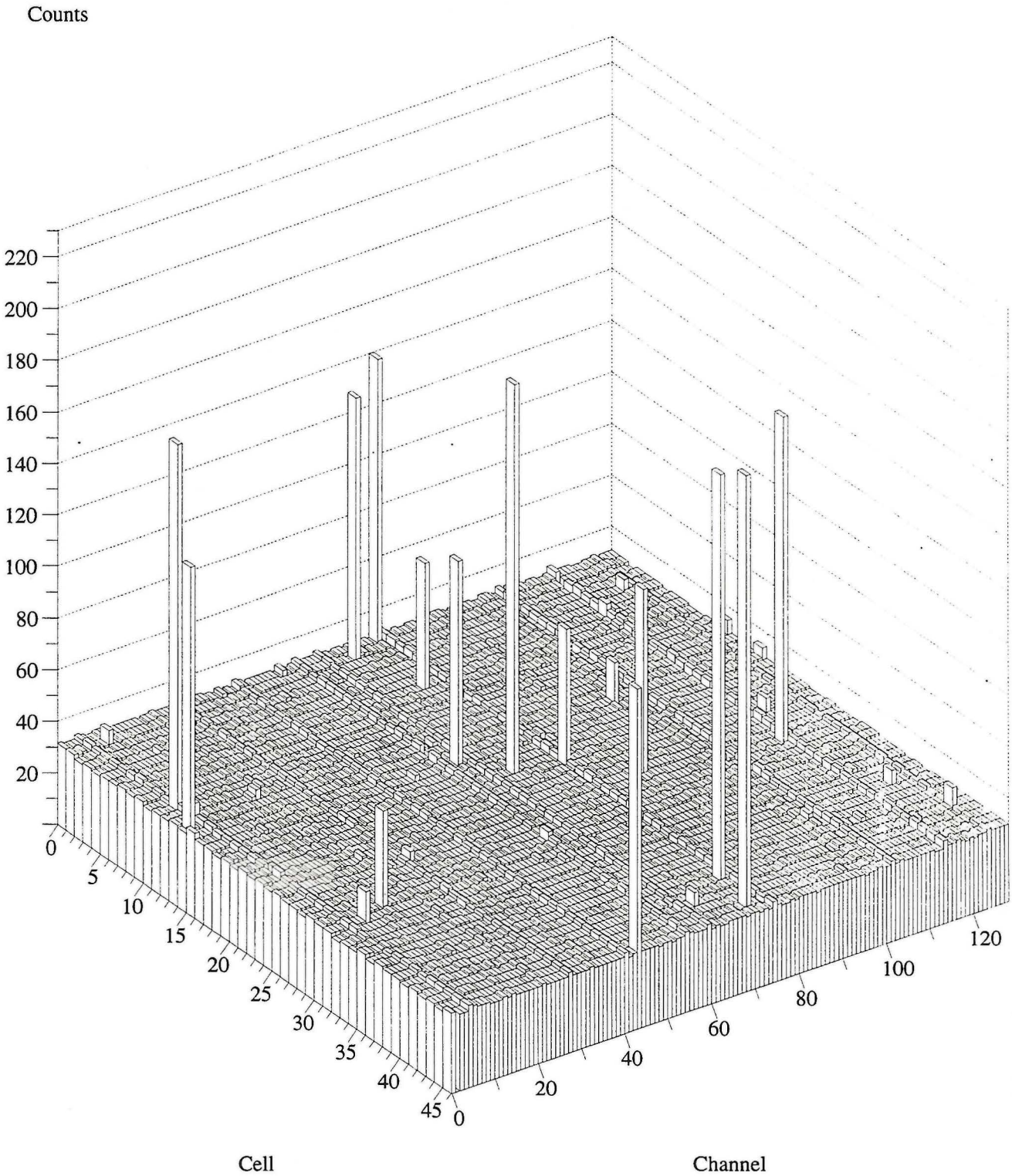
Positive polarity pedestals for die 38, wafer 91



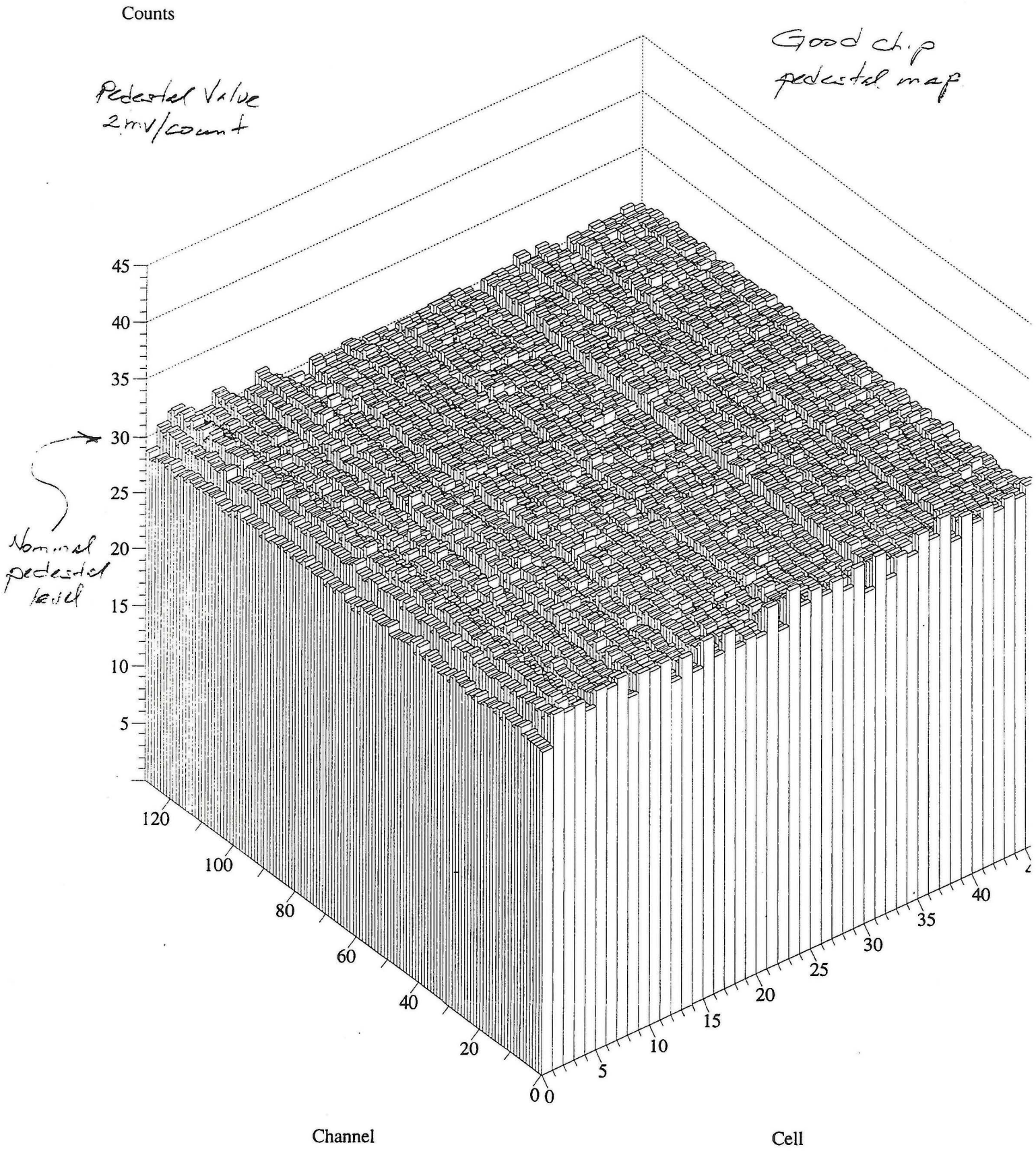
Positive polarity pedestals for die 69, wafer 92



Negative polarity pedestals for die 69, wafer 92



Positive polarity pedestals for die 104, wafer 92



APPENDIX F

Appendix F

Wafer Maps Before and After Annealing
Lot #12, Wafer #15

1) Die Quality Map before annealing

2) Die Quality Map after annealing

3) Pipeline Quality Map before annealing

4) Pipeline Quality Map after annealing

5) Types of Die Failure Map before annealing

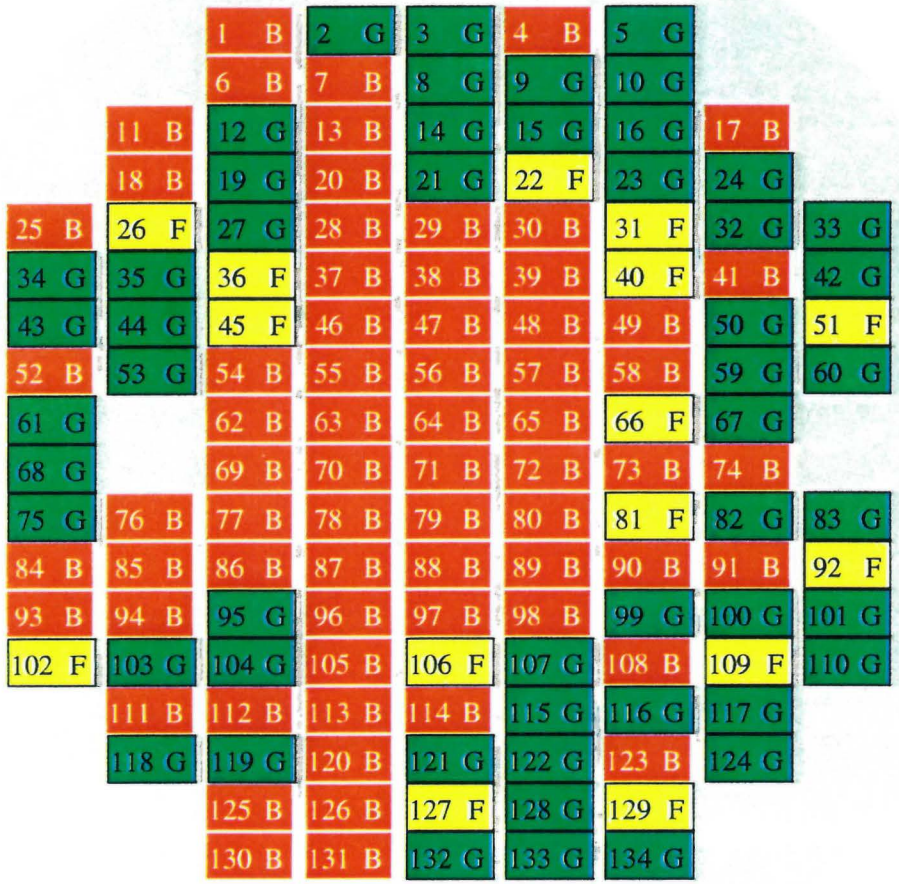
6) Types of Die Failure Map after annealing

7) Random bad Cell Map before annealing

8) Random bad Cell Map after annealing

Die quality map for wafer 80 s/n: Y21316-12-15 (not backplated)

Date: 04/01/99



B Bad die

F Fair die

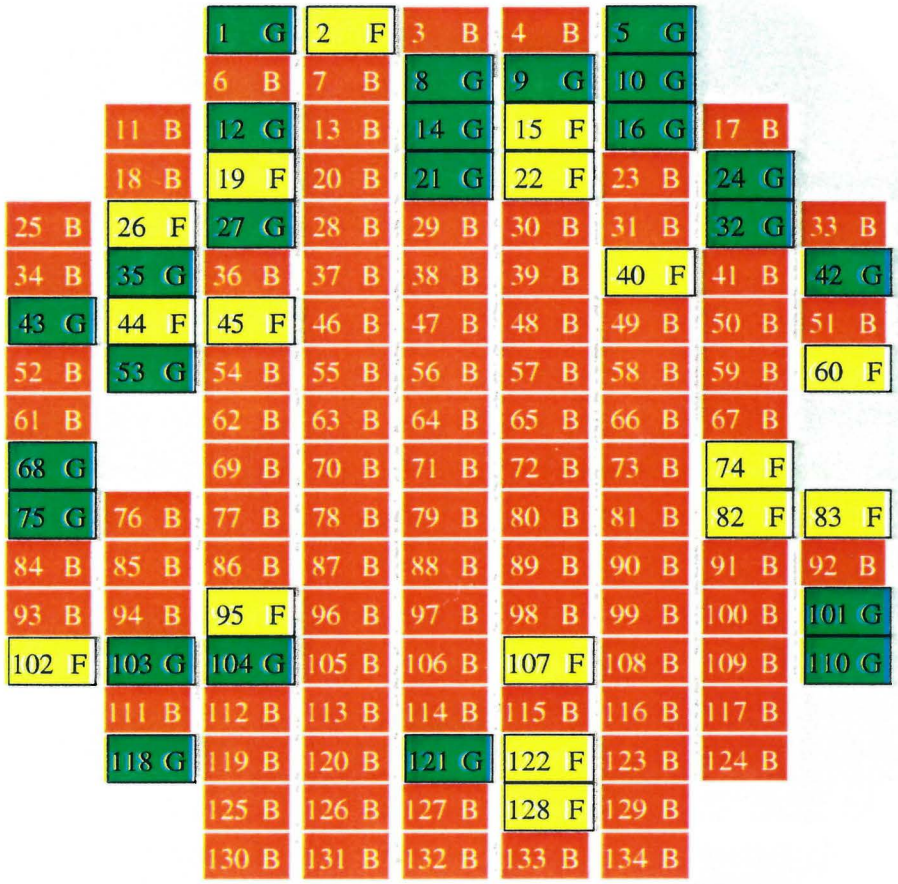
G Good die

N No info

* Manually tagged

Die quality map for wafer 80 s/n: Y21316-12-15 (annealed)

Date: 04/01/99



B Bad die

F Fair die

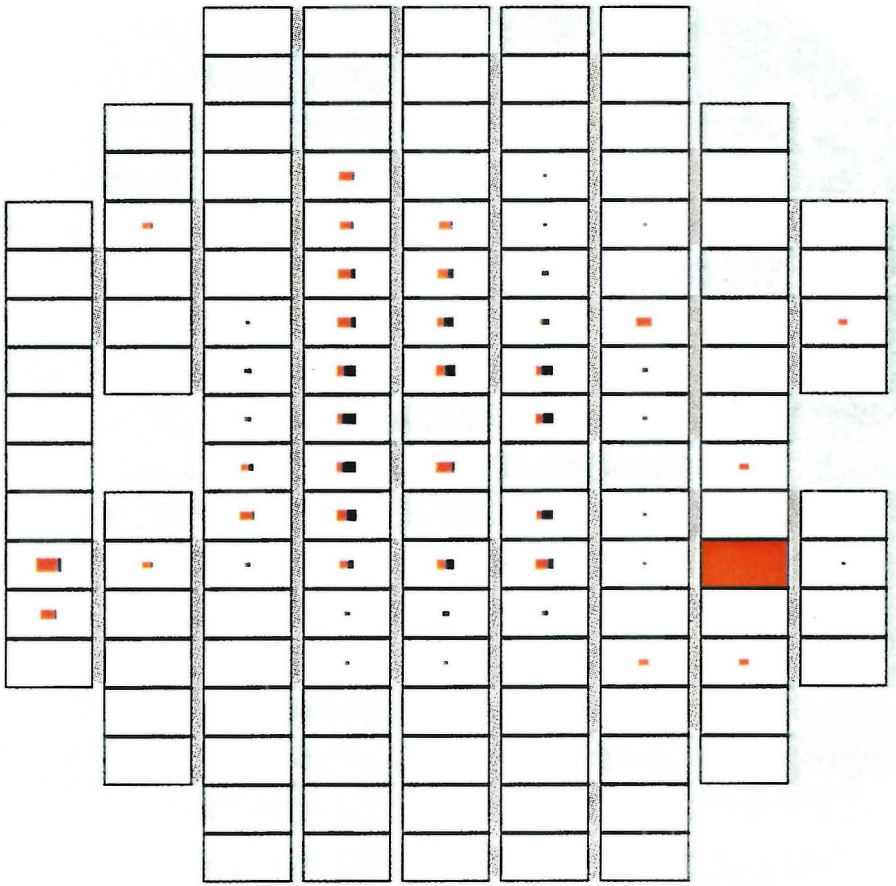
G Good die

N No info

* Manually tagged

Pipeline quality map for wafer 80 s/n: Y21316-12-15 (not backplated)

Date: 04/09/99



Cells in bad channels

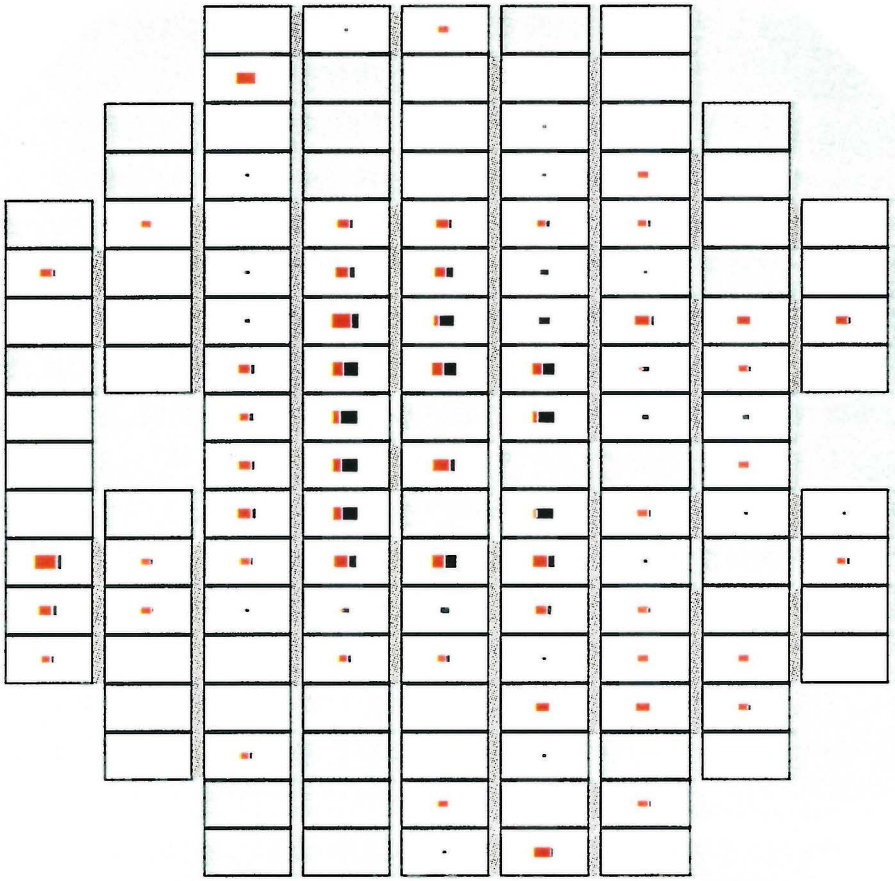
Bad cells in random locations

Good cells

No info

Capacitor quality map for wafer 80 s/n: Y21316-12-15 (annealed)

Date: 04/01/99



Caps in bad channels

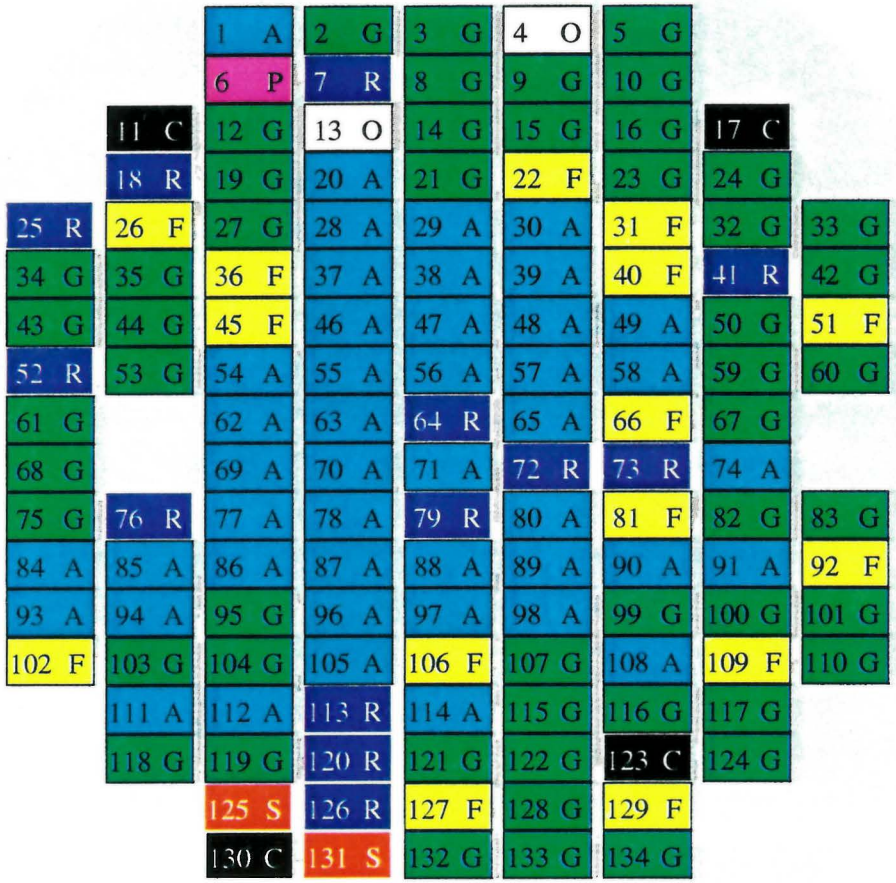
Bad caps in random locations

Good caps

No info

Types of die failures for wafer 80 s/n: Y21316-12-15 (not backplated)

Date: 04/05/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

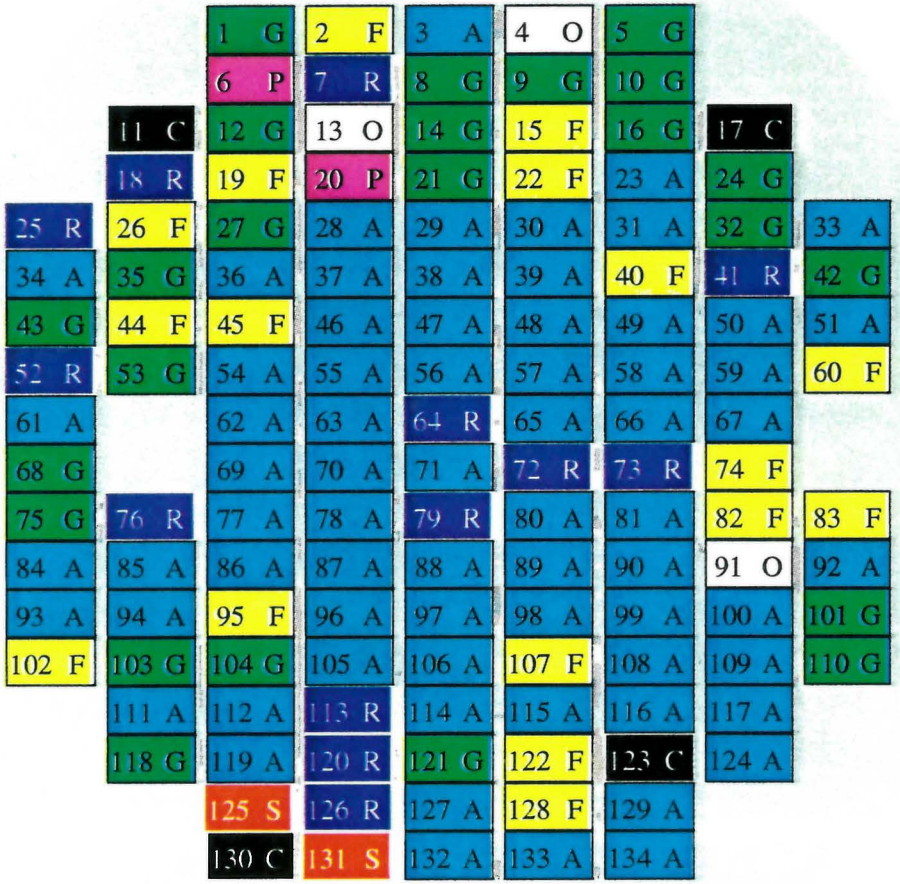
A Analog

O Operator

N No info

Types of die failures for wafer 80 s/n: Y21316-12-15 (annealed)

Date: 04/13/99



G Good dies

F Fair dies

C Currents

S Serial

R Basic readout

P Pipeline logic

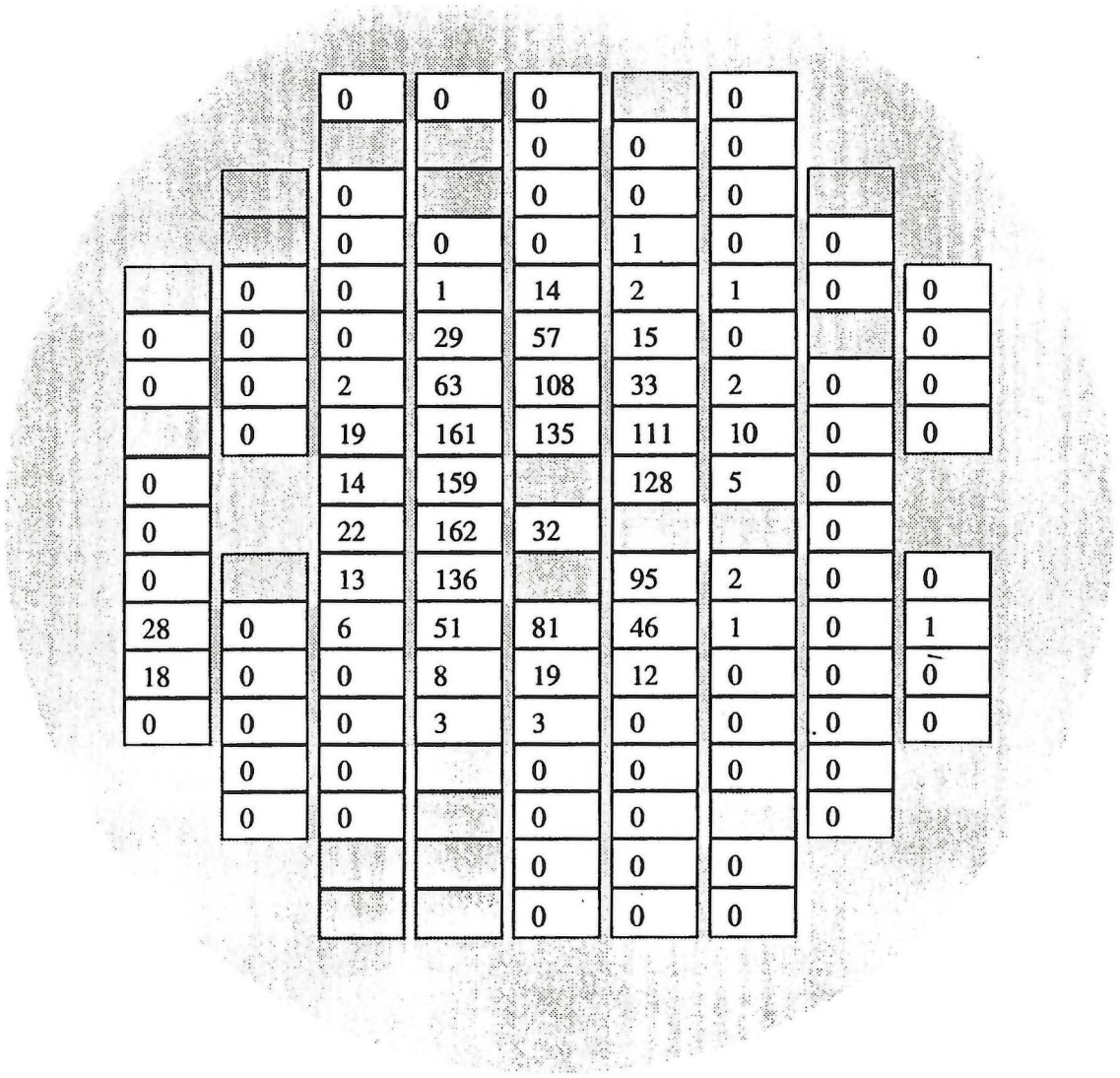
A Analog

O Operator

N No info

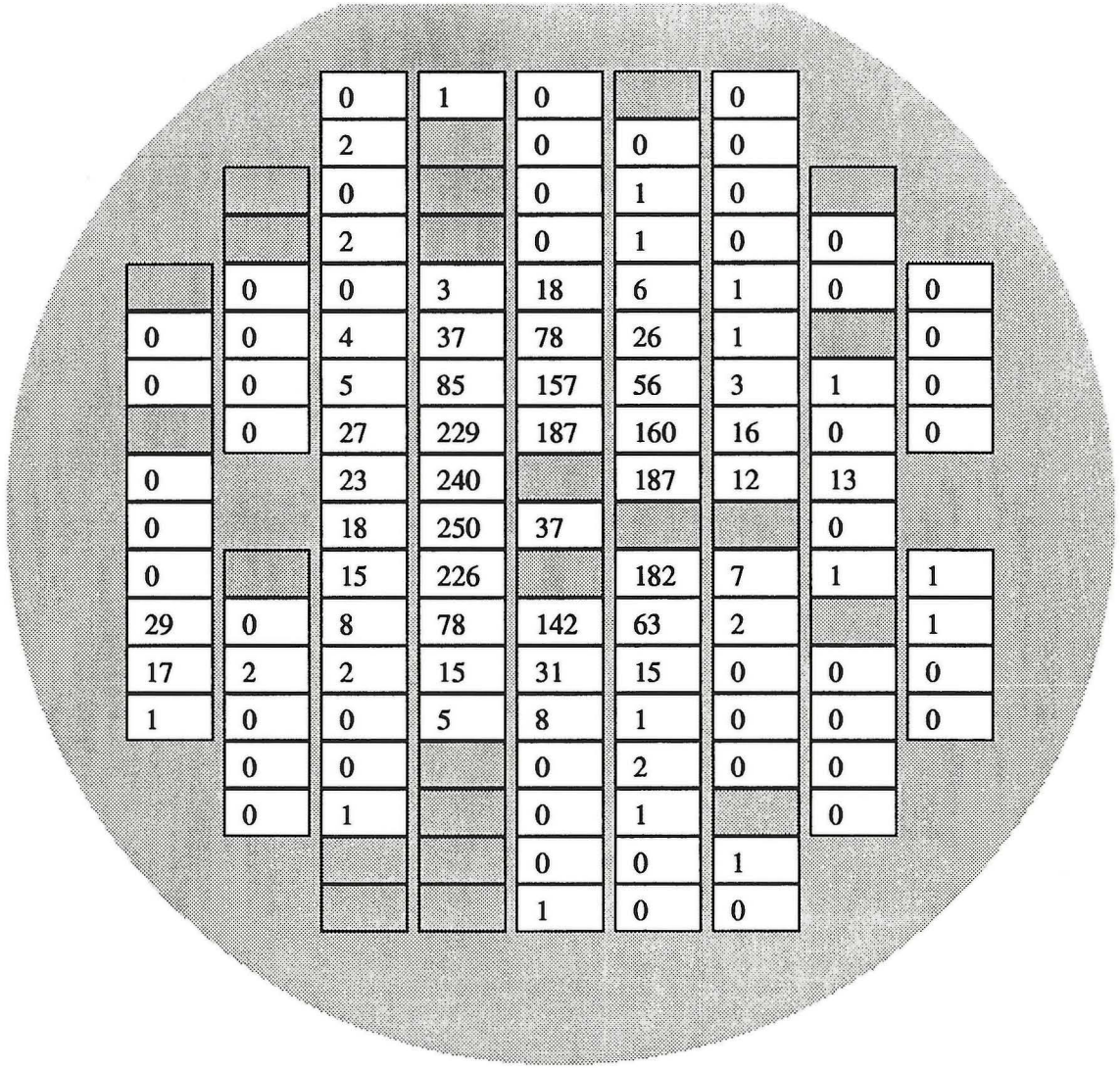
Random bad cell map for wafer 80 s/n: Y21316-12-15 (not backplated)

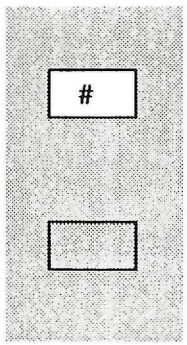
Date: 04/09/99



Random bad cell map for wafer 80 s/n: Y21316-12-15 (annealed)

Date: 04/13/99





Number of bad cells in random locations

No info