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Evaluation of FOXFET biased AC-coupled silicon strip detector prototypes for CDF SVX upgrade

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1. Introduction

Silicon microstrip detectors for high-precision charged particle position measurements have been used in nuclear and particle physics for years. The detectors have evolved from simple surface barrier strip detectors with metal strips [1] to highly complicated double-sided AC-coupled junction detectors [2]. The feature of AC-coupling the readout electrodes from the diode strips necessitates the manufacture of a separate biasing structure for the strips, which comprises a common bias line together with a means for preventing the signal from one strip from spreading to its neighbours through the bias line. The obvious solution to this is to bias the strips through individual high value (several MΩ) resistors. These resistors can be integrated on the detector wafer by depositing a layer of resistive polycrystalline silicon (polysilicon) and patterning it to form the individual resistors [3].

To circumvent the extra processing step required for polysilicon resistor processing and the rather difficult tuning of the process to obtain uniform and high enough resistance values throughout the large detector area, alternative methods for strip biasing have been devised. These include the usage of electron accumulation layer resistance for n^+- strips [4] or the usage of the phenomenon known as the punch-through effect for p^+- strips [5,6]. In this paper we present measurement results about the operation and radiation resistance of detectors with a punch-through effect based biasing structure known as a Field OXide Field-Effect Transistor (FOXFET) [7], and present a model describing the FOXFET behavior. The studied detectors were prototypes for detectors to be used in the CDF silicon vertex detector upgrade (SVX').

2. The punch-through effect

The operation of the FOXFET biasing structure is based on the punch-through effect previously reported in the context of p^+np^+ diodes for microwave applications [8]. When a voltage is applied between the p^+ electrodes in a p^+np^+ structure, the voltage is divided between the two pn junctions. Hence one of the junctions becomes forward biased and the other one reverse biased. In the beginning the voltage sharing is determined by the condition that the current flowing through both junctions be the same, which means that most of the voltage is carried by the reverse biased junction RB and only a minor fraction by the forward biased junction FB. When the depletion region produced by the RB junction meets the shallow depletion region of the FB junction, a punch-through (reach-through) is said to occur, and the current through the device starts to be dominated by the hole current thermionically emitted over the FB junction. The current flowing through the device increases exponentially as a function of voltage over the FB junction after punch-through is reached.

Fig. 1 illustrates the operation in terms of potential distribution in the device. Fig 1a depicts the potential distribution in a p^+np^+ structure at the onset of punch-through. Any further increase in the voltage reduces the shallow potential barrier at the FB junction and a large hole current can flow over the barrier. Note that in fig 1a the potential of the n-region between the p^+-contacts is floating, and is free to adjust to a value satisfying the current balance condition in the junctions. For comparison, the potential distribution of two back to back RB junctions - a geometry encountered in Si drift chambers or when punch-through between neighbouring strips in a strip detector is considered - is shown in fig 1b, where the structure is biased to full depletion with two RB junctions with different bias voltages. In this case the potential barrier for holes is so high that no punch-through current flows.

The flat-band voltage of a p^+np^+ structure is defined as the voltage where no potential barrier exists at the forward biased junction, and can be shown to correspond to the one-sided depletion voltage of the n-region [9]:

$$V_{FB} = \frac{qN_dW^2}{2\varepsilon_s} \qquad (1)$$

where q = electron charge, N_d = silicon doping (cm^{-3}) and W = width of the n-region.

Typical operation voltage of a p^+np^+ diode lies between V_{RT} and V_{FB}, in which region the relation between the voltage applied to the p^+np^+ structure and the forward biased barrier height is [9]:

$$V_{bi} - V_1 = \frac{(V_{FB}-V)^2}{4V_{FB}} \qquad (2)$$

where V_{bi} is the built-in voltage in the junction, V_1 is the forward biased barrier height and V is the voltage applied between the p^+ - electrodes.

3. The FOXFET structure

A FOXFET structure used for Si microstrip detector biasing is depicted in fig. 2, which shows a cross section of the detector in the direction of the strips. In the design a p^+ diffusion line (bias line) has been placed close (5-10μm) to the ends of the diode strips to be biased. The aluminum gate electrode of the FOXFET is on top of the field oxide between the bias line and the ends of the strips. Thus the design is a multi-source transistor, where the bias line (i.e. the drain of the transistor) and the gate are common, and each strip acts as an individual source. On the other hand, the silicon part of the FOXFET can also be thought of as a lateral p^+np^+ diode, and can in a qualitative analysis be treated analogously. In quantifying the relevant parameters describing its operation, however, the surface effects caused by the positive charge in the field oxide dominate and have to be taken into account.

In detector operation the bias line is grounded and a positive bias voltage is applied to the back of the detector. The purpose of the p^+np^+ structure is to reach the punch-through condition when the voltage difference between the strips and the bias line exceeds a maximum value defined by the geometry and bias conditions of the FOXFET. This way the strip potential is held close to the potential of the grounded bias line, and an effective bias voltage exists between the strips and the backplane. So, compared with the p^+np^+-structure described above, the FOXFET is different in the sense that instead of a floating n-region

there is a floating p^+-electrode, the potential of which settles to a value required by current balance in the junctions. A negative gate voltage can be applied to control the operation of the FOXFET. In the following we present a set of measurements made for a prototype FOXFET biased detector together with a description of a model for FOXFET operation, which explains the obtained results.

4. Measurements on FOXFET characteristics

4.1 General

The detector used in the measurements[1] is described in table 1.

Table 1. Detector description

Identifier	651 - 15 - 2
Thickness	300 μm
Resistivity	>10 kΩcm
N. of strips	384
Strip width	10 μm
Strip pitch	50 μm
Detector length	82 mm
Detector width	15 mm
FOXFET gate lgth	6 μm

The detector was mounted on a test PC board, and connections to the appropriate contacts (gate, bias line, guard ring, two DC connections to different strips) were made with ultrasonic wire bonding. Connections were done also to two readout electronics circuits type SVXD and SVXH. Contact to the back of the detector was made with conductive epoxy.

All the electrical measurements were made with a programmable multichannel source-monitor unit[2]. To avoid the effect of varying ambient humidity, the measurements were made with the detector in a dry N_2 environment.

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[1] Manufactured by Micron Semiconductor Ltd., Lancing, Sussex, England

[2] Type Hewlett Packard 4145B

4.2 Results

4.2.1 Initial conditions

We start by describing the conditions in the FOXFET before any voltages are applied. The field (gate) oxide inevitably contains positive oxide charge of different types [11], the density of which is typically 10^{11}-10^{12} cm^{-2}. This oxide charge induces an electron accumulation layer under the oxide by a simple electrostatic attraction. The excess electron density in this induced layer can be found by solving the Poisson equation in the surface region with the assumption that the space charge from donor ions can be neglected, and stating that the total amount of excess electrons should equal the oxide charge density. The resulting charge distribution is [10]:

$$\rho(x) = \frac{-qn_s}{(1 + \frac{x}{\sqrt{2}L_D})^2} \qquad (3)$$

where

n_s = charge density at the surface [electrons/cm^3]
L_D = Debye length at the surface, characterizing the spatial extent of the space charge layer:

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 n_s}} \qquad (4)$$

where

ε_s = permittivity of Si
k = Boltzmann constant
T = absolute temperature

The total charge (in electrons/cm^2) contained in the space charge layer is obtained by integrating the excess electron density:

$$Q_{tot} = \frac{1}{q}\int_0^\infty \rho(x)dx = \frac{1}{q}\int_0^\infty \frac{-qn_s}{(1+\frac{x}{\sqrt{2}L_D})^2}dx = -\sqrt{\frac{2n_s\varepsilon kT}{q^2}} \qquad (5)$$

The charge density at the surface is finally obtained as a function of oxide charge by equating $Q_{tot} = -Q_{ox}$:

$$n_s = \frac{q^2Q_{ox}^2}{2\varepsilon kT} \qquad (6)$$

Fig. 3. shows the excess electron density distribution at the Si surface for an oxide charge of 0.5 10^{12} cm^{-2} according to eqs. (3), (6). The accumulation layer in the Si extends to a depth of a few Debye lengths, in this case 10-20 nm, the Debye length being ≈ 5 nm. At charge densities within a few orders of magnitude from the bulk doping (≈0.5 10^{12} cm^{-3}) equation (3) is no more accurate, since the space charge of the ionized donors is not taken into account in its derivation. Knowing the surface charge density of the accumulation layer, we can also estimate the surface potential with respect to the undepleted bulk from:

$$V_s = \frac{kT}{q}\ln\left(\frac{n_s}{N_d}\right) \qquad (7)$$

which in this case gives V_s ≈ 0.4 V. The p^+-contacts create a depletion region around themselves through the natural built-in voltage in the pn-junction. In 10 kΩ-cm silicon, the thickness of this built-in depletion region is ≈ 45 μm, so the whole of the material except for the accumulation region under the oxide is depleted already from the beginning. The accumulation layer can be thought of as a heavily doped n-region under the oxide, which is difficult to deplete and thus increases the punch-through voltage, although this is not quite an accurate analogy.

To further illustrate the conditions in the FOXFET, fig. 4 shows a more detailed picture of the FOXFET, with dimensions of the different layers in scale with the 6 μm gate length.

4.2.2 Detector leakage current

The detector leakage current as a function of bias voltage applied to the back of the detector with different gate voltages is shown in fig. 5. The effect of gate voltage can be seen as a change in the effective bias voltage on the strips. The effective bias voltage is obtained by subtracting the strip voltage from the bias voltage. With gate voltages close to zero the strip voltage is large and the effective bias small, whereas with large negative gate voltages the strip voltage is small and the effective bias voltage close to the applied bias voltage. The actual shape of the I-V curve of the detector junctions is close to the curve measured with Vg = -20 V.

4.2.2 V_{strip} vs. V_{bias} characteristics

Fig. 6. shows the measured strip voltage as a function of bias voltage applied to the back of the detector. The input impedance of the voltage measuring instrument was $>10^{12}$ Ω, which ensures that the strip voltage was not affected by the measurement.

In the beginning the strips are essentially floating, and thus follow the bias voltage. In a simplified picture the strips are fully floating, and should follow the bias voltage exactly (with the difference of the built-in voltage in the pn-junction) until punch-through occurs, after which the strip voltage should be constant (fig. 6). The observed deviation from this behaviour can be explained with a simple current balance argument. In addition to the requirement for the currents in the FB and RB junctions in the FOXFET to be equal, also the detector leakage current shall be equal to both of these. If the strips were to follow the bias voltage exactly, there would be no leakage current in the unbiased detector, whereas there would be a leakage current flowing in the RB junction of the FOXFET carrying the whole applied bias voltage. However, there would be no source for this current flowing in the direction from strips to ground. Thus the voltage sharing between the FOXFET and detector adjusts in a way that the FOXFET and detector leakage currents are equal. This voltage sharing is, from fig. 6, linear up to a certain point

for each gate voltage, indicating that the two leakage currents have the same shape as a function of voltage, except for a proportionality constant in the voltage scale. The I-V curve of the FOXFET before punch-through can be obtained by combining the leakage current and strip voltage measurements, and by taking into account that the detector leakage current is a sum of the currents through 384 FOXFETs. These curves with different gate voltages can be seen in fig.7.

The behaviour of the FOXFET before punch-through divides into two regions. First region is the depletion of the accumulation region n-silicon, where the shape of the I-V curve resembles that of the detector. As explained before, this leads to a linear relation between bias voltage and strip voltage. After depletion, reach-through condition is approached, indicated by a clear increase in the current. The increase in the current corresponds also to the voltage when Vb/Vs is no longer constant (cf. fig. 6). Interestingly, this occurs always at the same current, approximately 35 pA, which is evidently the leakage current from the depleted region of the FOXFET. The onset of actual punch-through behaviour occurs at the end of the curves of fig. 7. When punch-through is reached, the current depends exponentially on the voltage with a fairly large proportionality constant (described below). This means that, although the voltage over the FOXFET is determined by the current balance requirement, the changes in the voltage are so small that it is reasonable to call the voltage to which the strips settle at full detector bias the punch-through voltage.

The V_{pt} for Vg=0 is approximately 11 V, which may be compared with the value 10 mV calculated for a geometry not involving a surface accumulation layer. Obviously the accumulation layer really effectively inhibits the punch-through at the surface. At more negative gate voltages V_{pt} gets smaller, as the gate voltage partly compensates the effect of the positive oxide charge in creating the electron accumulation layer. Fig. 8. shows V_{pt} as a function of gate voltage. At gate voltage Vg = -22V V_{pt} is effectively zero, which indicates that the accumulation layer has vanished and that the transistor is starting to turn on.

The effect of the gate voltage can be quantized by calculating the amount of charge at the gate capacitance at a specific voltage and subtracting that charge from the oxide charge to obtain the effective oxide charge from the point of view of silicon. That is:

$$Q_{gate} = V_{gate} * C_{gate} = V_{gate} * (\frac{\varepsilon_{ox}}{T_{ox}})$$

$$Q_{eff} = Q_{ox} - Q_{gate} \qquad (8)$$

We can also estimate the total amount of oxide charge present by noting that at gate voltage = -22V the charge on the gate equals the oxide charge. This gives an oxide charge of $\approx 5\ 10^{11}\ cm^{-2}$.

From fig. 8. we can also notice the small effect that increasing bias voltage has on the punch-through voltage, also previously observed in measurements made on floating strip potentials in strip detectors [5].

4.2.3 Current vs. voltage characteristics after punch-through, dynamic resistance

In detector operation it is essential for the user to know the I-V characteristics of the strip biasing structure to be able to predict detector behavior with, for instance, increasing leakage current or damaged strips. Also with respect to the noise in the amplifier that reads the signals from the strips the resistance of the bias structure is critical. For detectors with resistive bias elements the quantity containing all the necessary information is the resistance value of the bias resistor. For a non-linear biasing element like a FOXFET the situation is not so straightforward.

Let us first look at the general picture of current flow in a FOXFET biased detector. Once again the main principle is that in steady state the current flowing through the FOXFET must equal the leakage current of the detector. The voltage difference between the strips and the bias line is adjusted accordingly. The current flowing through the FOXFET after punch-through is based on the thermionic emission of minority carriers over the potential barrier of a forward-biased junction, and is thus expected to behave exponentially as a function of voltage over the junction [9].

In the previous section the I-V characteristics of the FOXFET before punch-through were deduced from the leakage current and strip voltage measurements. Next we try to verify the same characteristics after punch-through. This can be done in two ways: injecting a current to the FOXFET and measuring the corresponding voltage shift or applying a voltage to the FOXFET and measuring

the resulting current. The first method was chosen for two reasons. Firstly, the situation likely to occur with the detectors is a current increase in the whole detector (caused by for instance radiation damage) or in one strip, so the current injection method imitates this situation fairly well. Secondly, the voltage range in which the applied voltages should lie is very small and varies with gate voltage, so in practice it is much easier to work with the current injection method.

Fig. 9. illustrates the measurement setup during I-V measurements. The injected current was varied logarithmically from 40 pA to 400 nA, and corresponding changes in the strip voltages were observed. The strip voltage as a function of injected current for different gate voltages is depicted in fig. 10. It seems that changes in the gate voltage have little or no effect on the shape of the I-V characteristics except when the gate voltage approaches the threshold voltage, in this case at voltages exceeding -22 V.

A subject of interest in the FOXFET is the quantity known as the dynamic resistance, defined as:

$$R_d = \frac{\delta V_s}{\delta I_s} \qquad (7)$$

Fig. 11 shows the dynamic resistance as a function of injected current. The resistance is very high, over 100MΩ, at very low currents, and decreases as a function of injected current to around 1 MΩ at 400 nA. The dependence of dynamic resistance as a function of drain current is discussed in more detail in the next section. Fig. 12 shows the dependence of dynamic resistance on the gate voltage, where we observe the dynamic resistance to be relatively weakly dependent on the gate voltage at gate voltages below the threshold voltage V_T. At the threshold voltage a sharp drop in the dynamic resistance is seen, as the transistor is turned on and operates in its linear region. In the light of this measurement it seems unrealistic that the dynamic resistance of the FOXFET could actually be adjusted with the gate voltage.

In a detector biased with polysilicon resistors, the value of the bias resistor can be used in considering a multitude of operational issues such as:

- voltage drop in bias structure caused by the detector leakage current ($V_{drop} = I_{leak,strip} \times R_{bias}$)
- voltage differences between neighbouring strips with different leakage currents ($\Delta V = (I_{leak,S1} - I_{leak,S2}) \times R_{bias}$
- a current noise source at the amplifier input caused by the bias structure ($i^2_{noise} = \frac{4kT}{R_{bias}}$)
- signal spread to neighbouring strips via the bias resistance - strip to ground capacitance network ($\tau_{spread} = \frac{1}{R_{bias} C_{strip}}$)

In a FOXFET biased detector these issues are not so straightforward, so we consider them one by one.

1) Voltage drop in the bias structure with different leakage currents can be determined from the shape of the relevant V-I curve (fig. 10). At large currents the voltage drop behaves logarithmically (cf. next section) as a function of current.

2) Voltage difference between strips with different leakage currents can be determined as a difference between voltage drops evaluated as in 1).

3) The noise contribution at the amplifier input from the FOXFET is presumably different from the thermal noise in a bias resistor, and cannot be estimated as a thermal noise in a resistor with a value R_d. Since the current flowing through the FOXFET consists of charge carriers thermionically injected over a potential barrier, the current is expected to exhibit a shot noise with $i^2_{noise} = 2qI$. At gate voltages $\geq V_T$, the FOXFET can, in turn, be thought of as a resistor since the current flows through the resistive inversion layer under the oxide. This behavior should be observed as a sharp increase in the noise at $V_G \geq V_T$. The 1/f-noise typically exhibited by MOS transistors can also be thought to be suppressed, since the current flow occurs inside the bulk rather than at a surface inversion region.

4) To estimate the effective resistance to be used in signal spread estimation, the most reasonable choice is to use the value of the dynamic resistance at a typical signal current. Typical signal currents from a minimum ionizing particle in a strip detector are 100 - 200 nA during charge collection [12].

4.2.4. Analysis of I-V - curve shapes

In the following we take a closer look at how the current flowing through the FOXFET depends on the voltage between the drain and the source. According to the theory of the punch-through effect in simple p^+np^+ - junctions (section 2) the relation between the current and applied voltage V_S (for $V_{RT} < V_S < V_{FB}$) should be [9]:

$$I_S = I_O \exp\left[- \frac{q(V_{FB}-V_S)^2}{4kTV_{FB}} \right] \qquad (9)$$

where k = Boltzmann constant and T = absolute temperature. This relation is derived for an ideal slab geometry with no surface regions involved, so in the FOXFET geometry we should expect only an approximate accuracy. We have fitted our measured data to this formula keeping the I_O, V_{FB} and the coefficient in the exponent as variable parameters. Fig. 13. shows the measured points and the result of the fit for an I-V measurement with V_G = 0V. The logarithmic scale graph in fig. 13 b) shows that the fit is excellent over the whole range of 3 decades. The parameter values obtained in the fitting process are I_O = 1.1 μA, exponential coefficient = 41 1/V, and V_{FB} = 12.4 V. Of these the flatband voltage bears the clearest physical significance, and is in good agreement with observed strip voltages. Using the estimated flatband voltage we can from eq. 2 calculate an effective doping level at the region under the gate, where the punch-through occurs, and obtain $n_d \approx 2\ 10^{16}$ cm-3, which is well comparable with the charge density in fig. 3.

From eq. (9) we can also derive the expected dependency of the dynamic resistance on the strip current, which is:

$$R_d = \left(\frac{kTV_{FB}}{q\ln(I_O/I_S)} \right)^{1/2} \frac{1}{I_S} \qquad (10)$$

which to a good approximation is an 1/I - dependence. This expression is valid for strip currents below I_0, so care should be taken not to extrapolate R_d values for too high currents.

4.2.5. Strip voltage uniformity

One may expect that process originated fluctuations in parameters like gate length, gate oxide thickness and oxide charge may cause nonuniformity in the punch-through voltages for different strips. This nonuniformity may be observed as a distribution of strip voltages. A measurement was made for a small number of strips in order to ensure that the voltage fluctuations between the strips are not unacceptably high, leading to field and charge collection nonuniformities and eventual resolution degradation.

Fig. 14. shows the voltage distribution of 8 measured strips on the detector. The uniformity is good, with the standard deviation of the fluctuation in the strip voltages being less than 0.1 V; that is, all the strips are contained within ≈0.3 V in the sample, and within ≈0.5 V in a large number of strips. This voltage fluctuation is likely due to FOXFET geometry variations rather than leakage current differences between strips, because the strip currents are so low (<1 nA/strip) that for the strip current differences to cause the observed voltage fluctuations, the dynamic resistance should be several gigaohms, which is not the case.

4.2.6. Effect of ambient humidity level on the detector

Ambient humidity may effect detector operation by allowing negative charges provided by the grounded Al electrodes to redistribute on the oxide [13]. This may lead to a situation in which the negative charges on top of the oxide compensate for the positive oxide charge, and thus allow the Si-SiO_2 interface to become depleted, as depicted in fig. 15. The depletion of the surface region leads to large surface generated currents being added to the bulk leakage current.

In order to determine if a critical ambient humidity level exists, a measurement of detector leakage current as a function of humidity was made. The detector was placed in a sealed box flushed with dry nitrogen. The box was then slowly flowed with nitrogen saturated with water vapor by bubbling nitrogen through water. The bubbler and the detector were kept at the same temperature, and the flow of saturated nitrogen was kept low to avoid humidity condensing on the detector.

The detector leakage current was then monitored as a function of the humidity level. The result is shown in fig. 16. On a more accurate scale small fluctuations in leakage current could be observed already at 50% RH, but the effects become evident at humidity levels exceeding 60% RH. Approaching 90%RH the leakage current has already increased by a factor of 20, being occasionally over 1μA at 90%RH. No changes in the strip voltages were observed as a result of increased humidity. The temperature during the measurement was 18.9 ^{o}C. As a conclusion, it seems advisable to operate the detector at humidity levels under 50%RH for its most stable operation.

5. Radiation measurements

5.1. General

The detector was irradiated with ^{137}Cs 667 keV photons at the University of Pittsburgh. The dose rate delivered by the source at the detector location was 156 kR/h or 274 kR/h as measured with a calibrated air-ionisation chamber. The detector was placed in the radiation field facing the source with no material in between. The gate voltage was held at - 9V during irradiation, the electric field in the oxide being $\approx 9\ 10^4\ \frac{V}{cm}$. The cumulative radiation doses given to the detector were 10 kRad, 20 kRad, 50 kRad, 100 kRad, 500 kRad and 1 MRad. The measurements were made typically 24 hours after irradiation, during which time the detector was shipped from Pittsburgh to Fermilab. The time between irradiations was approximately 1 week, except for a 100 d interval between 100 kRad and 500 kRad irradiations.

5.2 Leakage current

The detector leakage current increased during irradiations from 87 nA to 1700 nA at 1 MRad (fig. 17). This corresponds to a damage constant of $2.7\ \frac{nA}{cm^3 kRad}$, which is in agreement with previous studies done with non-hadronic irradiation [11]. The leakage current increase is not, however, expected to be a significant phenomenon when ionization effects delivered by photon irradiation are considered.

5.3. Strip voltage characteristics

Fig. 18a shows the strip voltage as a function of gate voltage for different radiation doses up to 100 kRad. From the figure the behavior of both the punch-through voltage and the FOXFET threshold voltage (=gate voltage where V_{strip} = 0V) as a function of radiation. The punch-through voltage increases significantly with increased dose. This can be understood in the framework explained in section 4.2.1, where the oxide charge induced electron accumulation layer was the main cause for large punch-through voltages. As the radiation increases the amount of interface charge at the Si-SiO_2 interface, the electron accumulation layer gets stronger and the punch-through voltage increases. Fig. 18b depicts the strip voltage as a function of radiation dose for doses up to 1 MRad. In this figure the effect of the 100 d interval between 100 kRad and 500 kRad irradiations is clearly visible. During the interval a significant amount of annealing took place, so that the 500 kRad and even the 1 MRad curves show less voltage shifts than the 100 kRad curve before annealing. Fig. 19 shows the transistor threshold voltage as a function of radiation dose. In the beginning most of the change appears to occur already at 20 kRad, where the change is 14V. After 20 kRad the threshold voltage changes slowly at a rate of ≈25mV/kRad up to 100 kRad. The amount of oxide charge present after irradiation to 100 kRad is (according to eq.8) ≈8.4 10^{11} $\frac{1}{cm^2}$. The effect of annealing is demonstrated by the data point measured after annealing but before the irradiation to 500 kRad. Typically a saturation in oxide charge buildup is reached when oxide charge approaches the well-known theoretical limit of ≈ 3 10^{12} $\frac{1}{cm^2}$. This, however does not seem to apply in our case, so in the following we try to understand our measured results.

According to the simple theory of interface charge buildup [15] from radiation the buildup involves 1) charge generation in the oxide and transport to the interface by the electric field in the oxide, and 2) the actual buildup of trapped charge, which can last several thousands of seconds. According to this theory interface charge buildup practically does not appear if a negative gate voltage is applied during irradiation, since no positive charges are transported to the interface. The effect of charge buildup in thick oxides and under negative gate

voltages has been studied by Boesch and co-workers [16], whose results indicate that another mechanism for charge buildup during irradiation does exist, which causes charge buildup at the interface even with negative gate voltages. For irradiations with negative gate voltages, it also holds true that if charge trapping occurs also in the bulk of the oxide (which has been observed for field oxides [15]), the trapped charge starts to perturb the applied electric field when the observed flatband voltage shifts approach the voltage applied to the gate. When that occurs, the electric field at the Si-SiO_2 interface approaches zero and efficient recombination at this low field region suppresses the charge trapping. Fig. 20 illustrates the charge buildup process for a field oxide and a negative gate voltage during irradiation. Hence at low doses charge trapping occurs both at the interface and in the bulk of the oxide, resulting in a quick increase of the oxide charge and consequently punch-through and threshold voltage. When the trapped charge in the bulk of the oxide equals the charge at the gate during irradiation, electric field goes to zero first at the interface, and with increasing charge trapping the zero field recombination region extends inward to the bulk of the oxide. The creation of the zero field region should occur when the shift in the threshold voltage caused by oxide charge trapping equals the gate voltage during irradiation, which is indeed close to our experimental observation. After the electric field is zero throughout the oxide, only trapping at the interface (created by radiation interactions at the interface region [16]) continues causing the slow increase in the punch-through and threshold voltages.

The annealing process is a tunnel anneal at the Si-SiO_2 interface, where electrons from silicon tunnel to the oxide and recombine with charge trapped at or near the Si-SiO_2 interface. Thus the annealing process does not significantly reduce the amount of charge trapped in the bulk of the oxide, but only that at the interface region. This means that the electric field conditions in the oxide, which led to the saturation of the charge buildup in the oxide, do not change during annealing, although charge from the interface is removed. As a result of this, charge trapping after annealing occurs still only through radiation interactions at the interface and is therefore relatively slow.

In regular MOS transistors with thin gate oxides the space-charge and recombination effects described above do usually not occur until high doses (several MRad), but in our case the doses required are much lower because of the thick oxide.

5.4. Dynamic resistance vs. dose

Fig. 21 shows the measured dynamic resistance as a function of injected current for different radiation doses. The behavior shows the typical I_{inj}^{-1} - dependence at large currents. At low currents the resistance decreases by a factor of 4 at 1 MRad, whereas the dynamic resistance value measured at high currents (≈100 nA/strip) shows practically no dependence on dose. This is better illustrated in fig. 22 where the dynamic resistance has been plotted versus radiation dose. The effect at low currents is to a large extent explained by the increase in the leakage current at higher radiation doses. Fig. 22 shows also the expected dynamic resistance decrease calculated using the increased detector leakage current and the measured (fig. 11) dependence of dynamic resistance on current. The strip current used in the calculation is obtained by simply dividing the total leakage current of the detector by the number of strips, which may account for the small difference between measured and calculated values in fig. 22.

The threshold voltage shift depicted in fig. 19 can also be observed from the dynamic resistance curves, when the dynamic resistance is presented as a function of gate voltage for different radiation doses, figures 23a and 23b. The drop in dynamic resistance can be clearly observed at gate voltages corresponding to threshold voltages measured from the condition $V_{strip} = 0$.

5.5 Noise measurements

To observe the FOXFET behavior in terms of amplifier noise, the detector was bonded to two SVX readout circuits, one of which was the SVXD version and the other one a radiation hardened version SVXH. The results of the measurements are presented in fig. 23. Unfortunately the SVXH chip was damaged during shipping after 20 kRad, so the measurements do not extend any further. In any case, two effects are clearly visible from fig. 24. Firstly, the FOXFET threshold voltage shift can be observed as a shift of the gate voltage where the measured noise increases. The threshold voltages determined by the conditions i) Vs < 0.1V, ii) drop in the dynamic resistance or iii) increase in the noise measured with a readout chip, coincide within measurement accuracy (≈

1V). Secondly, the overall increase in the noise of the SVXD chip can also be observed, whereas no increase in the noise of the SVXH chip can be seen.

6. Conclusions

The operation and radiation resistance of a FOXFET biasing structure have been studied. The main parameters describing the properties of a FOXFET are the punch-through voltage (= the voltage drop imposed by the FOXFET to the detector bias voltage), the threshold voltage (= the voltage required on the FOXFET gate for the FOXFET transistor to turn on) and the dynamic resistance (= the slope of the I-V curve of the FOXFET). It has been found that the effect of the gate voltage is mainly that of reducing the punch-through voltage, rather than changing the dynamic resistance of the FOXFET. The change in the punch-through voltage is due to the charges on the FOXFET gate compensating the positive oxide charge in the gate oxide. The measured punch-through voltage was V_{pt} = 11V @ V_g = 0V, decreasing linearly to V_{pt} = 0V @ V_g = -22V (=$V_{threshold}$). The dynamic resistance depends fairly weakly on the gate voltage until the gate voltage reaches the threshold voltage, at which point the dynamic resistance drops dramatically. The I-V characteristics of the studied FOXFET has been found to be compatible with the theory developed for bulk p^+np^+ - structures, although FOXFET characteristics are strongly affected by the conditions at the Si-SiO_2 interface at the gate. The theory predicts a slightly modified 1/I - dependence for the dynamic resistance of a FOXFET, which has also been measured, with dynamic resistance varying between ≈80 MΩ @ I_s = <<1nA and ≈1 MΩ at I_s = 400 nA. The uniformity of the FOXFET structures on the studied detector in terms of voltage differences between strips has been found to be good, with $\sigma(V_{strip}) < 0.1$V. The ambient humidity has been found to make detector operation unstable at humidity levels exceeding 60%RH at room temperature.

The radiation effects from photon irradiation in the FOXFET have been found to be mainly due to increased oxide charge, with a strong effect at low doses on the punch-through voltage and on the threshold voltage. The dynamic resistance values have been found to remain almost constant as a function of radiation up to 1 MRad. Only changes observed in the dynamic resistance could be attributed to a radiation induced increase in the leakage current of the detector. This is expected

in the framework of the presented theory of FOXFET operation. The changes in the punch-through voltage and the threshold voltage of the FOXFET have been found to saturate with radiation doses over 10 - 20 kRad, where the measured $V_{pt} \approx 17V$ @ $V_g = 0V$, and $V_{threshold} = -37$ V after a dose of 100 kRad. A hypothesis is presented, where the large change in V_{pt} and $V_{threshold}$ at low doses is assumed to be caused by the negative voltage applied to the gate during irradiation, which inhibits charge recombination in the oxide during irradiation. We also observed a significant amount of annealing of the radiation induced oxide charge, which is assumed to be a result of a tunnel annealing process, which removes trapped positive charges from the Si-SiO_2 interface. The leakage current of the studied detector increased in an expected manner as a function of radiation, from 90 nA @ 0 kRad to ≈ 1.8 μA at 1 MRad. By measuring the noise in the detector with SVX readout circuits, the threshold voltage can be accurately determined as the gate voltage where the detector noise increases. No significant effect on the detector noise was observed when operating the FOXFET with the gate voltage below $V_{threshold}$.

We have neither from the point of view of FOXFET operation in general nor from the point of view of radiation damage found reason to operate the FOXFET at a gate voltage other than 0V.

References

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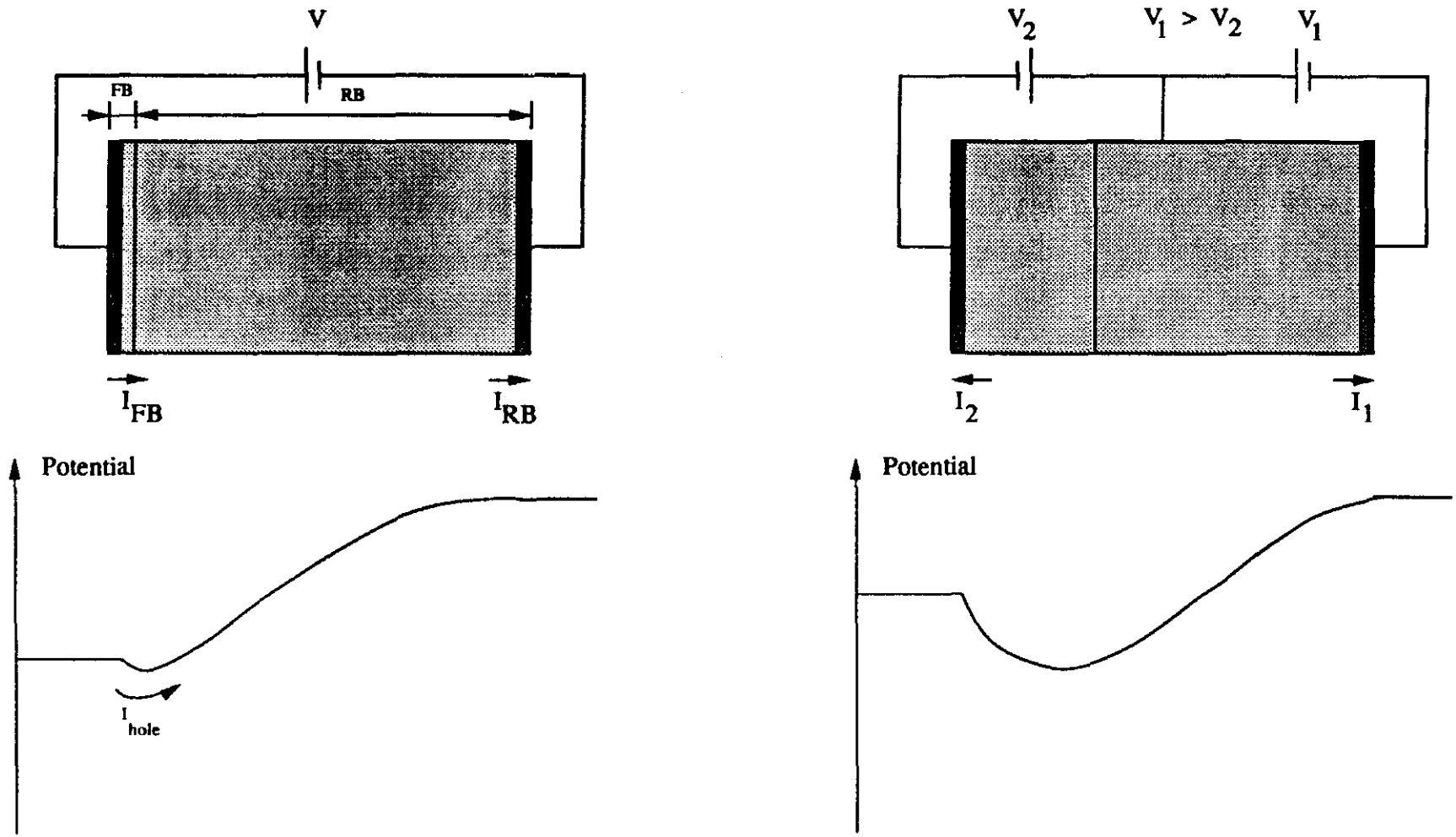


1a

1b

Figure 1

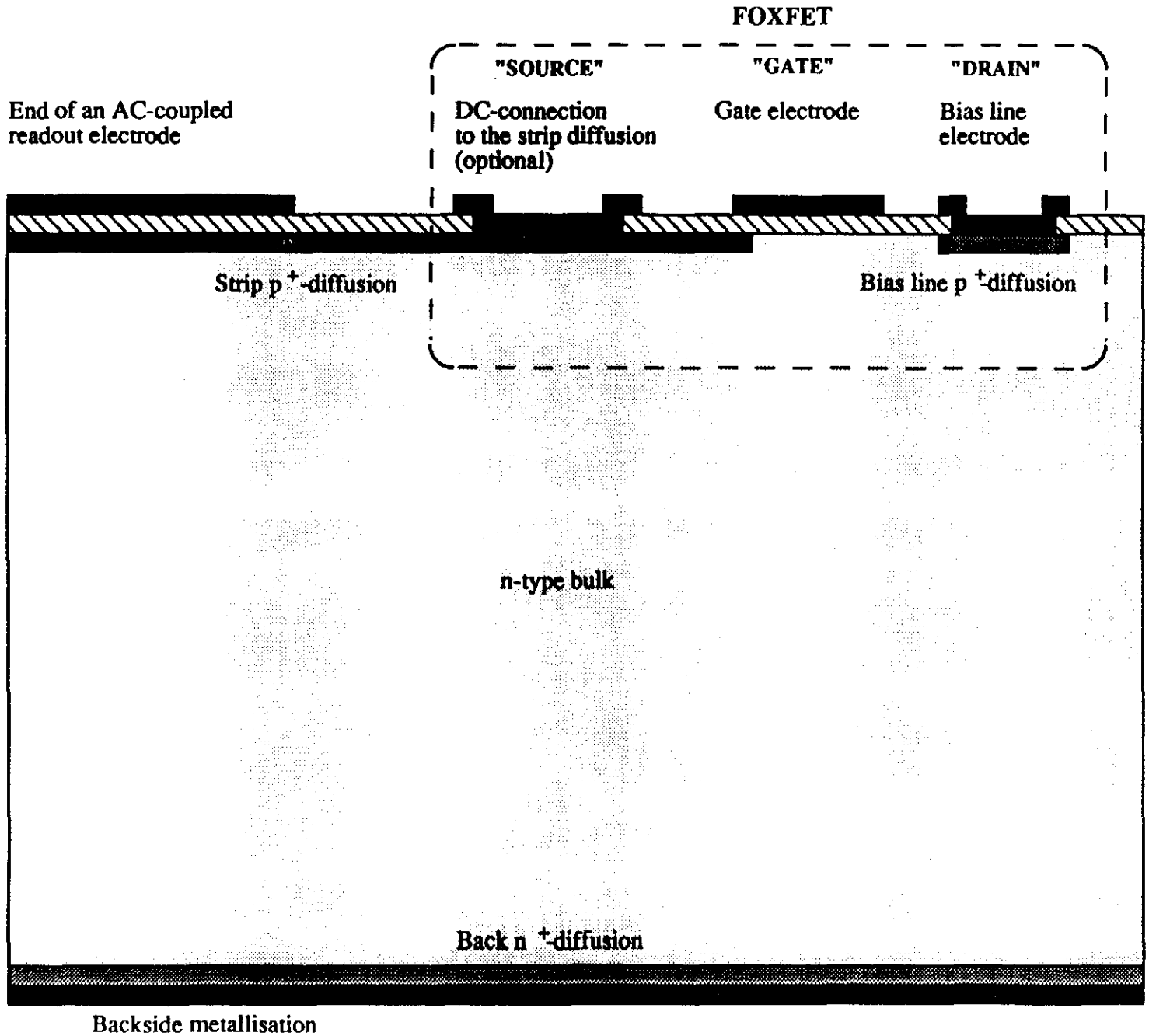

FOXFET
"SOURCE"
"GATE"
"DRAIN"
End of an AC-coupled readout electrode
DC-connection to the strip diffusion (optional)
Gate electrode
Bias line electrode
Strip p+-diffusion
Bias line p+-diffusion
n-type bulk
Back n+-diffusion
Backside metallisation

Figure 2

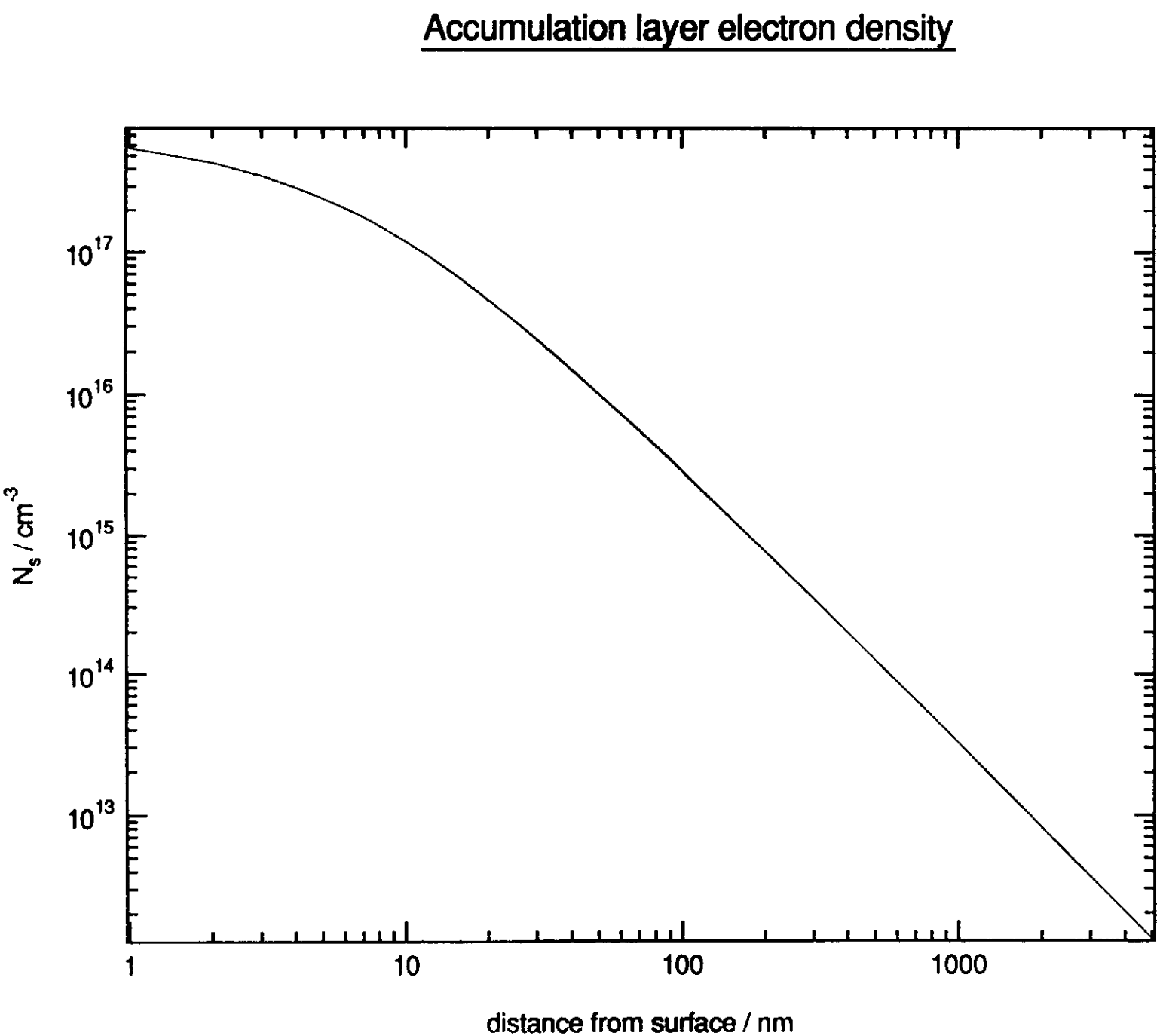

Accumulation layer electron density
10^{17}
10^{16}
10^{15}
10^{14}
10^{13}
N_s / cm^{-3}
1
10
100
1000
distance from surface / nm

Figure 3.

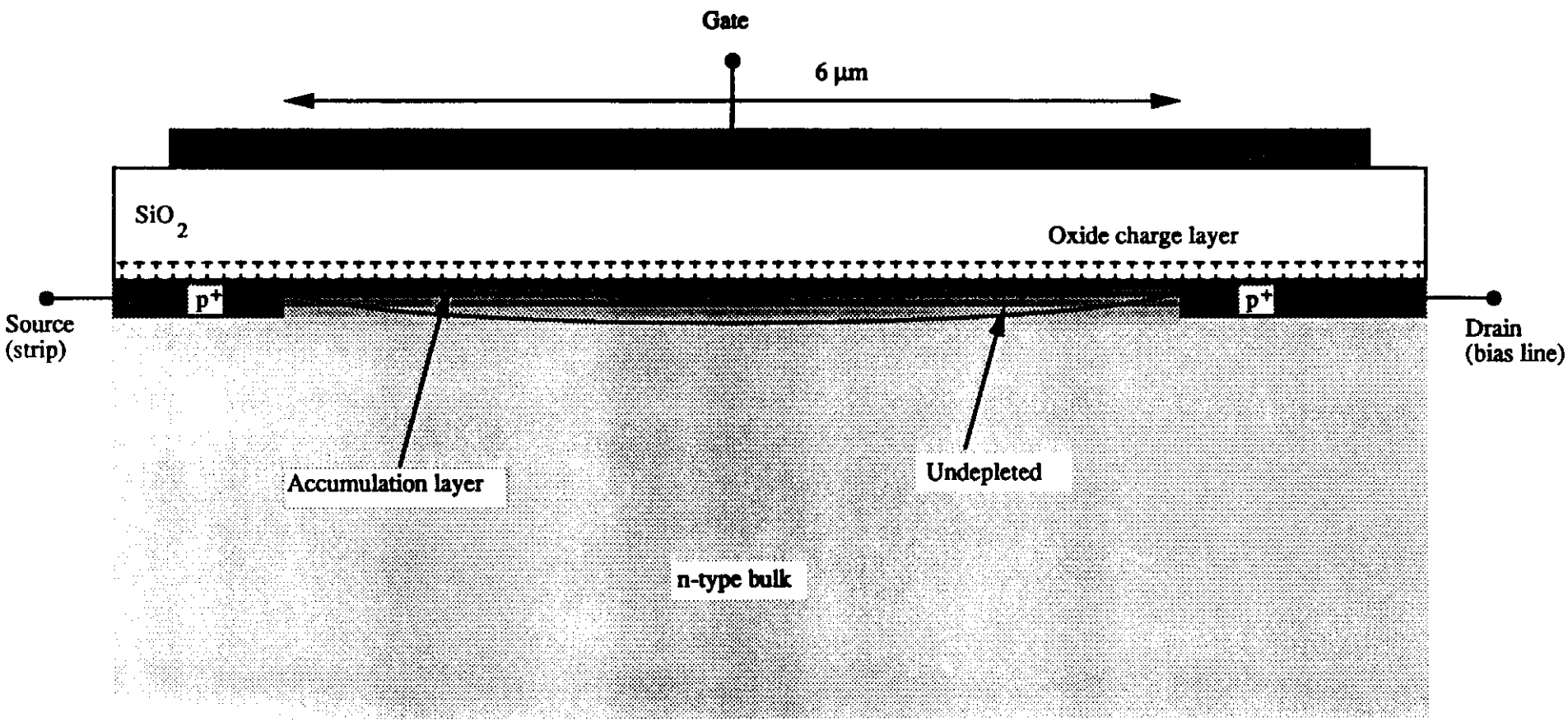

Gate
6 µm
SiO2
Oxide charge layer
p+
p+
Source
(strip)
Drain
(bias line)
Accumulation layer
Undepleted
n-type bulk

Figure 4.

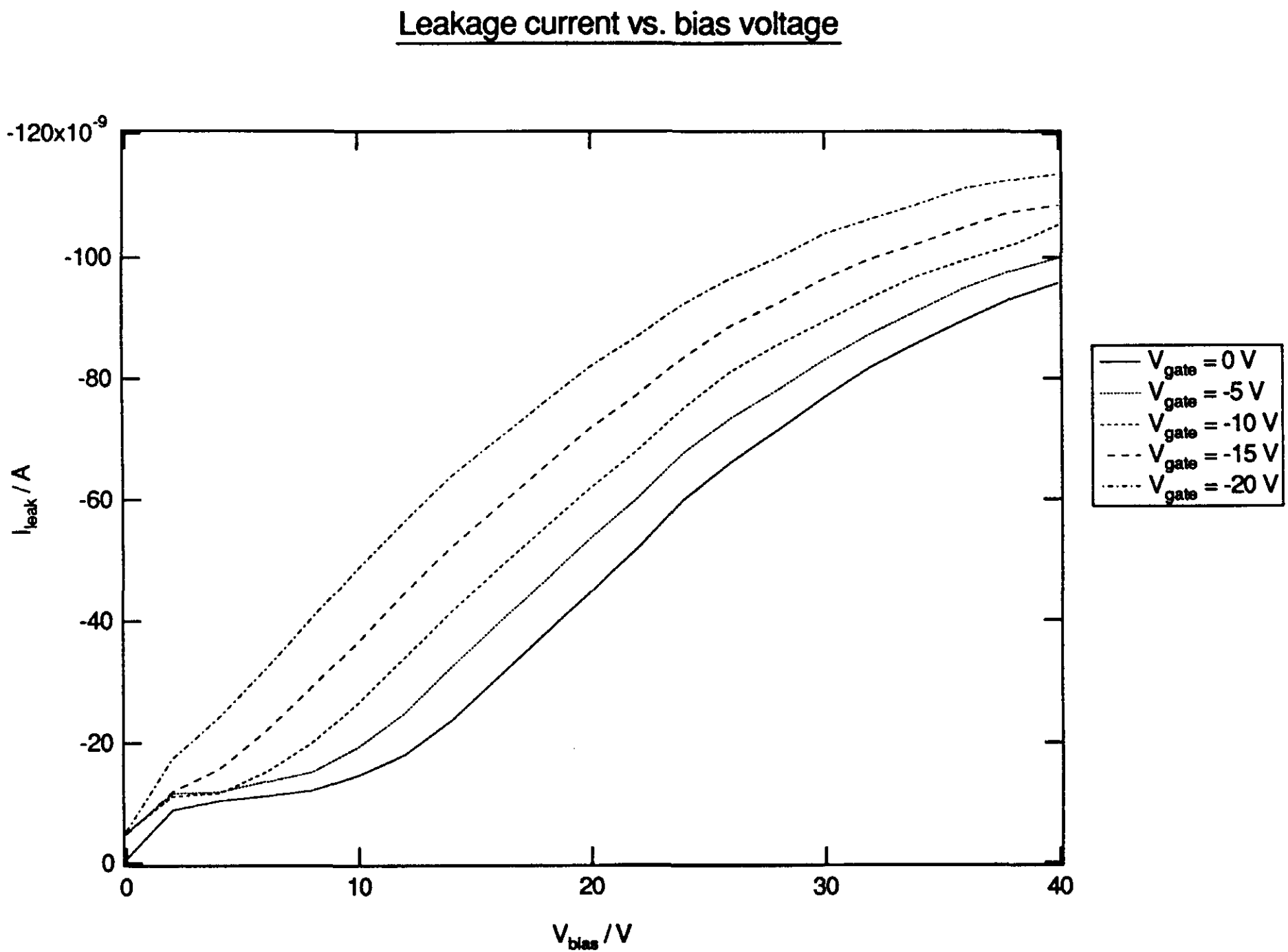

Leakage current vs. bias voltage
-120x10^-9
-100
-80
-60
-40
-20
0
I_leak / A
0
10
20
30
40
V_bias / V
V_gate = 0 V
V_gate = -5 V
V_gate = -10 V
V_gate = -15 V
V_gate = -20 V

Figure 5.

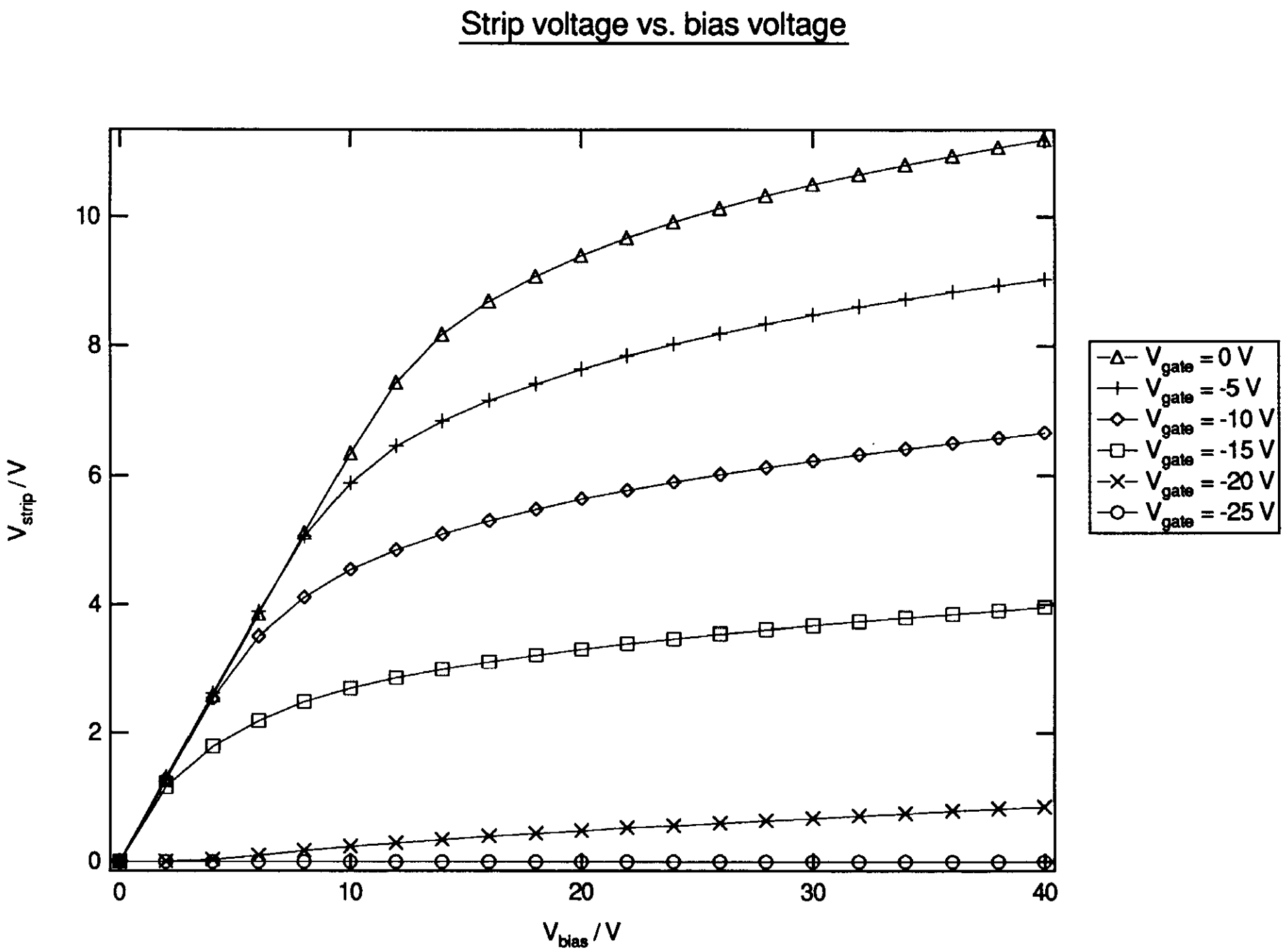

Strip voltage vs. bias voltage
V_{strip} / V
V_{bias} / V
0
2
4
6
8
10
0
10
20
30
40
V_{gate} = 0 V
V_{gate} = -5 V
V_{gate} = -10 V
V_{gate} = -15 V
V_{gate} = -20 V
V_{gate} = -25 V

Figure 6

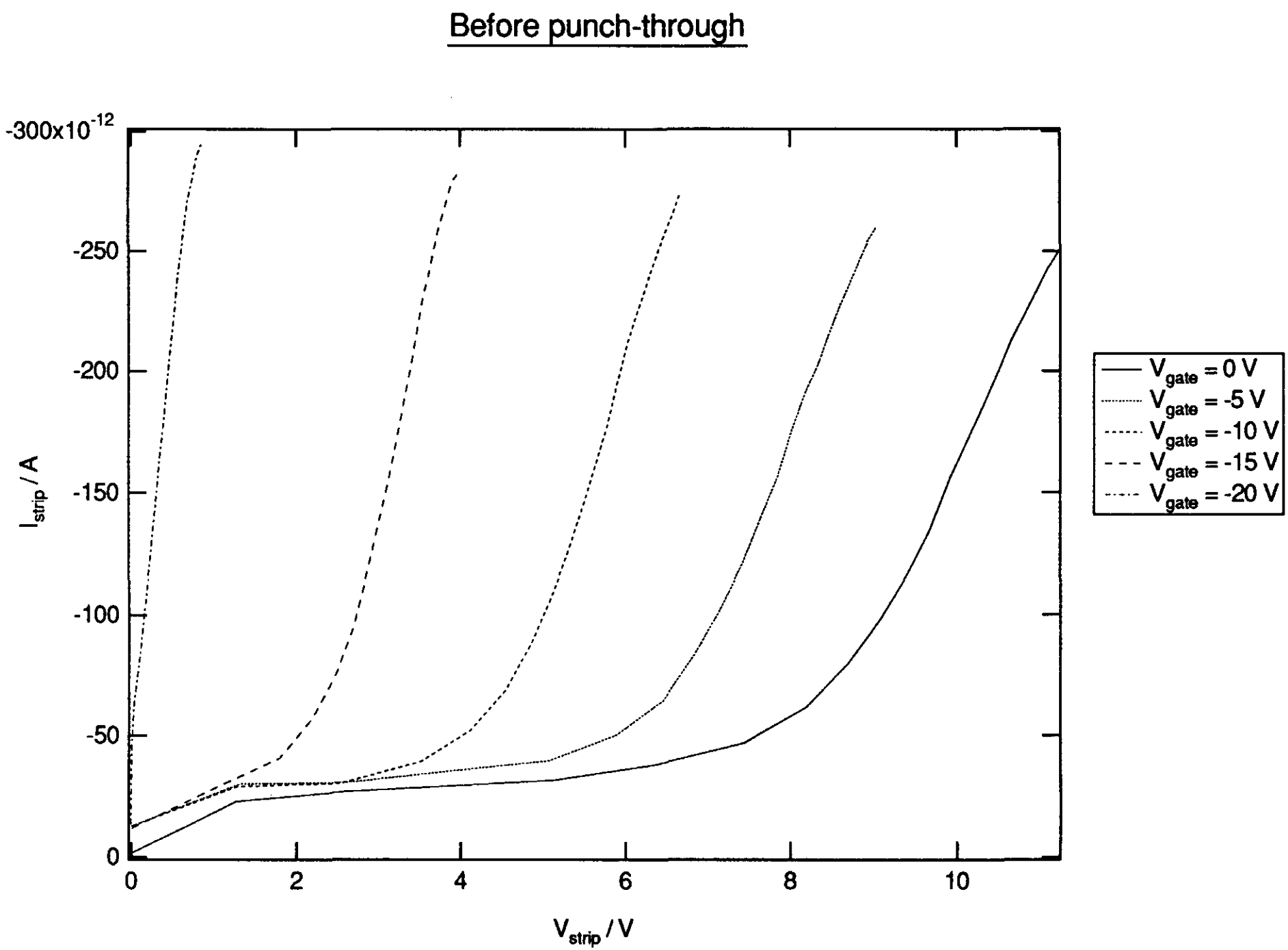

Before punch-through
-300x10^-12
-250
-200
-150
-100
-50
0
I_strip / A
0
2
4
6
8
10
V_strip / V
V_gate = 0 V
V_gate = -5 V
V_gate = -10 V
V_gate = -15 V
V_gate = -20 V

Figure 7.

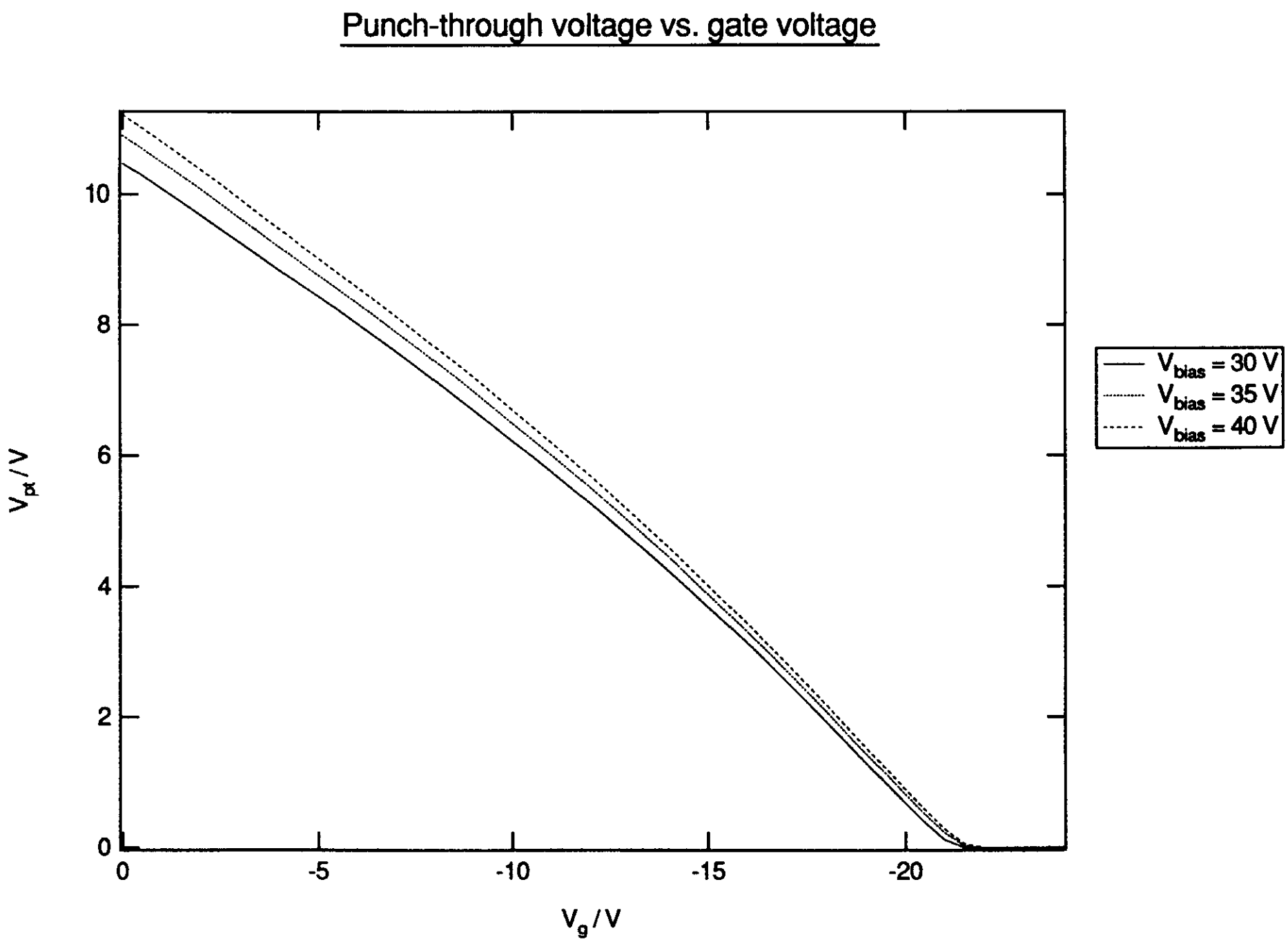

Punch-through voltage vs. gate voltage
10
8
6
4
2
0
0
-5
-10
-15
-20
V_{pt} / V
V_g / V
V_{bias} = 30 V
V_{bias} = 35 V
V_{bias} = 40 V

Figure 8.

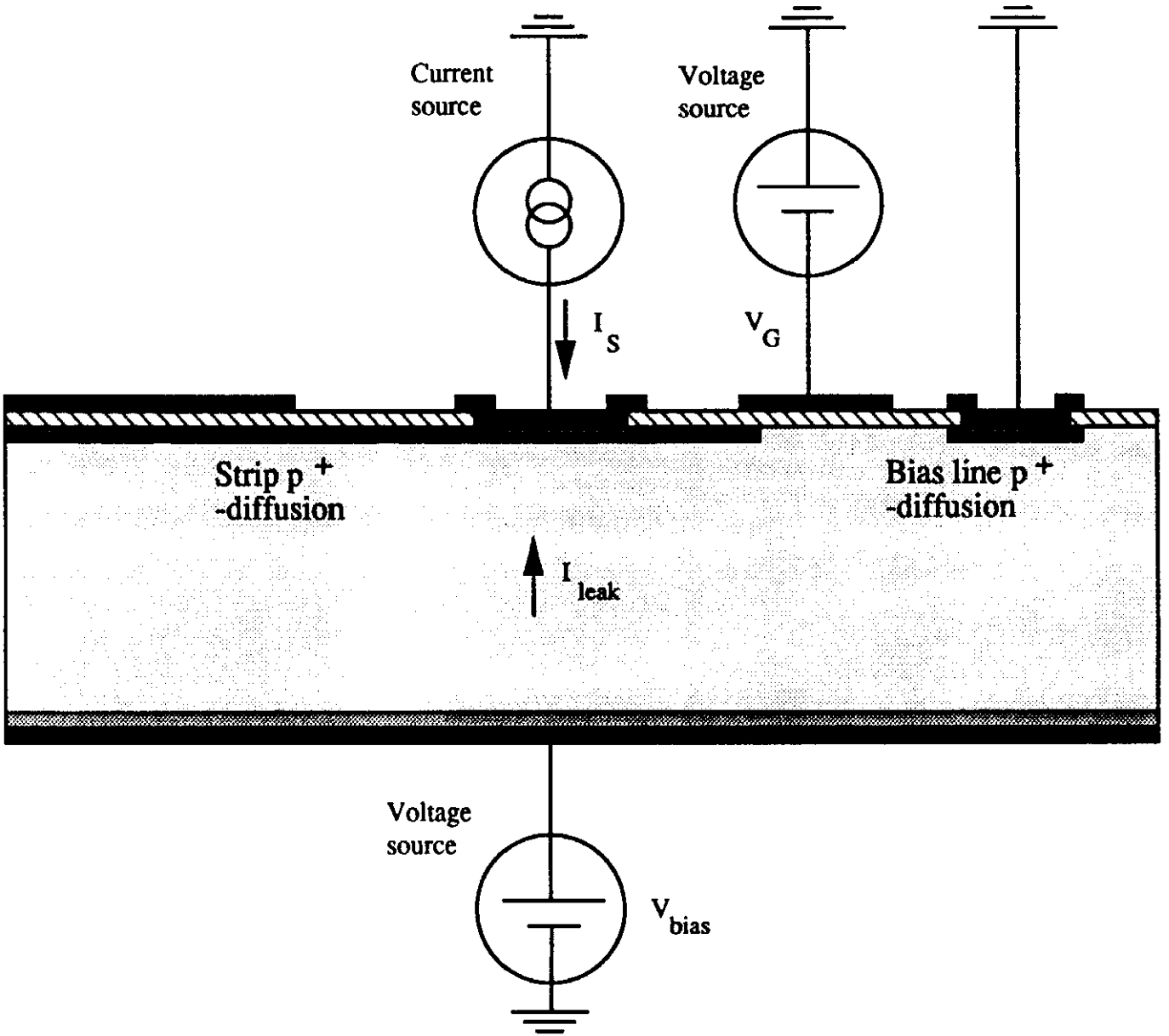

Current
source
Voltage
source
I_S
V_G
Strip p +
-diffusion
Bias line p +
-diffusion
I_{leak}
Voltage
source
V_{bias}

Figure 9.

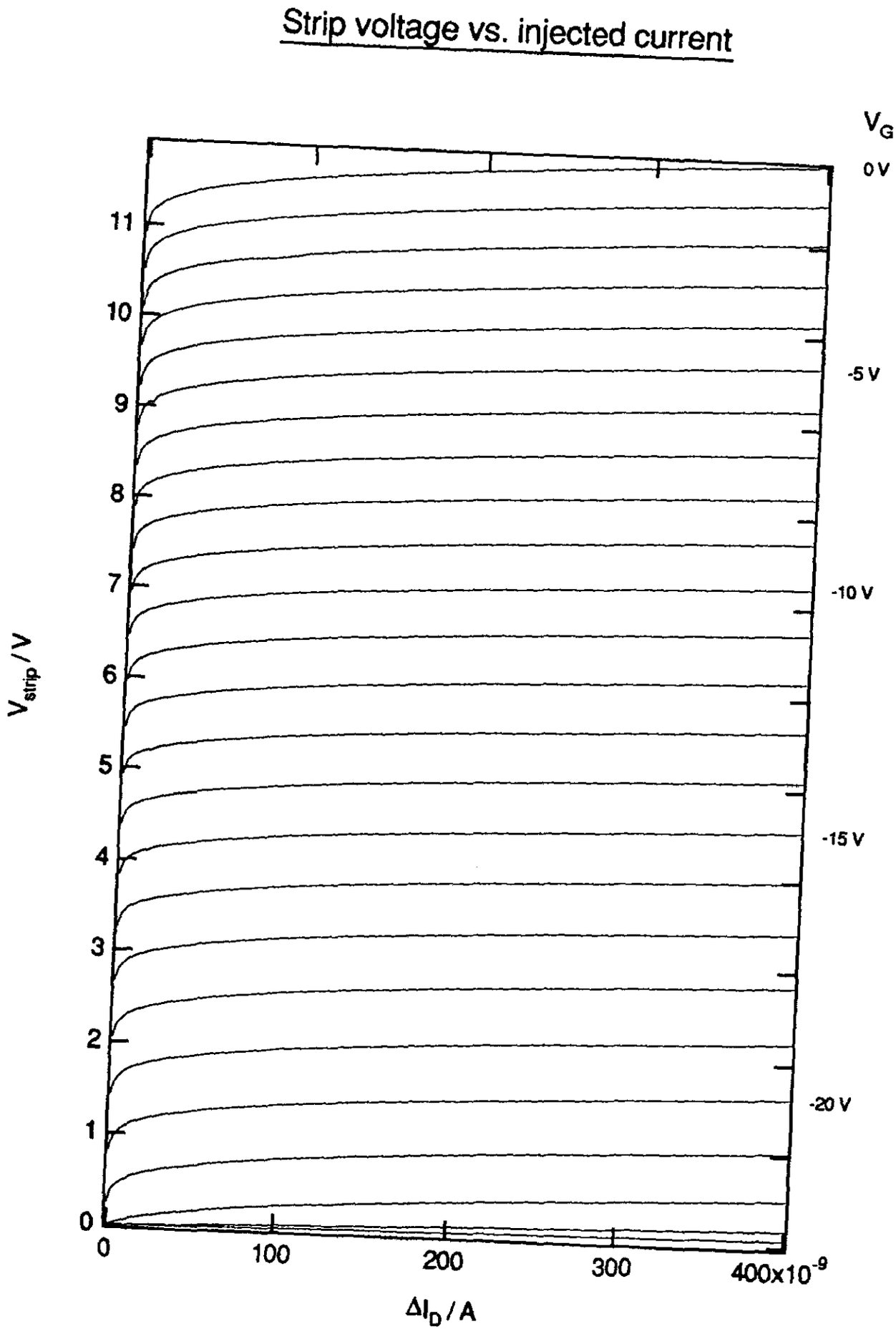

Strip voltage vs. injected current
V_G
0 V
-5 V
-10 V
-15 V
-20 V
V_{strip} / V
0
1
2
3
4
5
6
7
8
9
10
11
0
100
200
300
400x10^{-9}
ΔI_D / A

Figure 10.

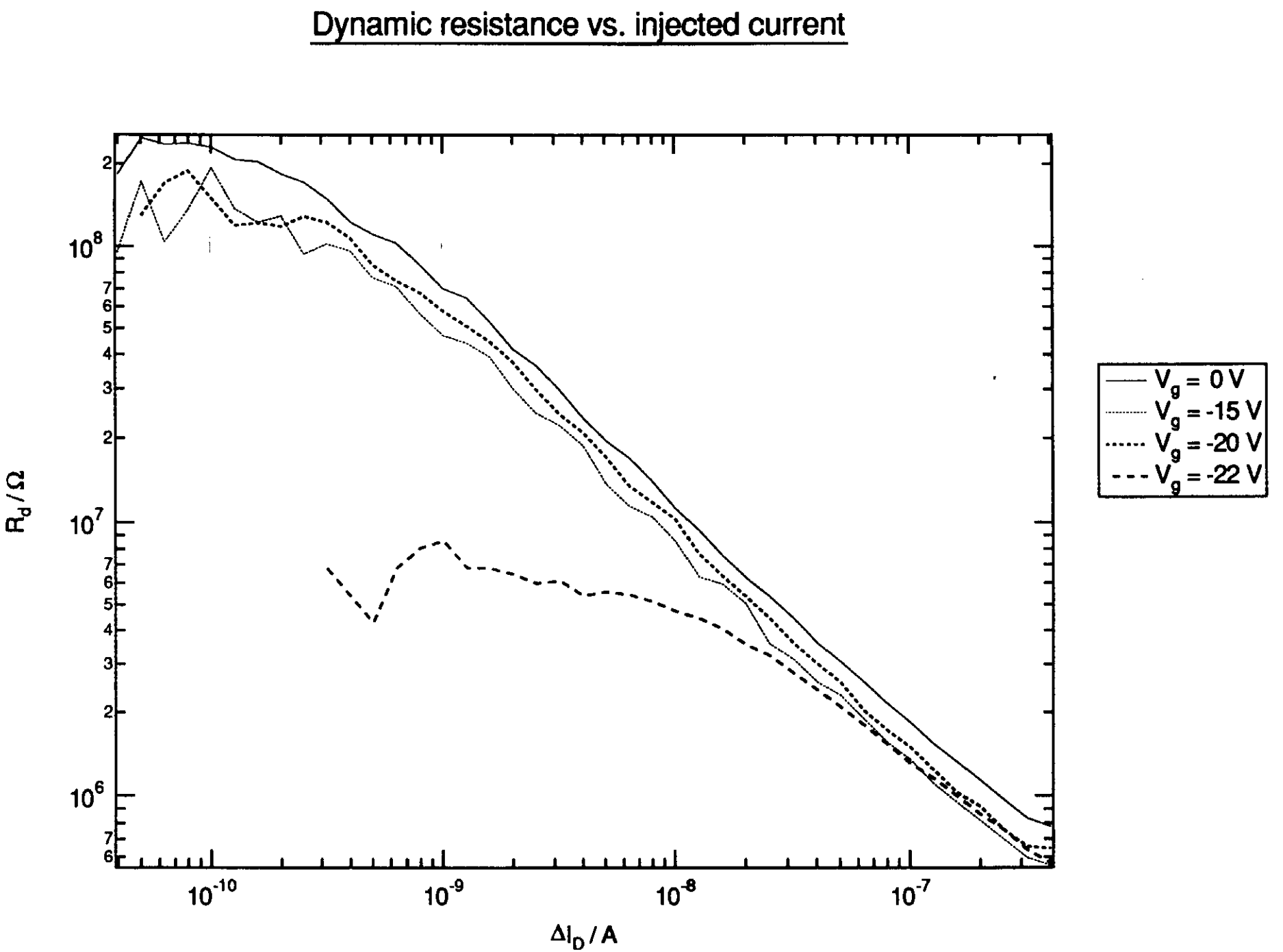

Dynamic resistance vs. injected current
R_d / Ω
10^8
10^7
10^6
10^{-10}
10^{-9}
10^{-8}
10^{-7}
$\Delta I_D / A$
$V_g = 0$ V
$V_g = -15$ V
$V_g = -20$ V
$V_g = -22$ V

Figure 11.

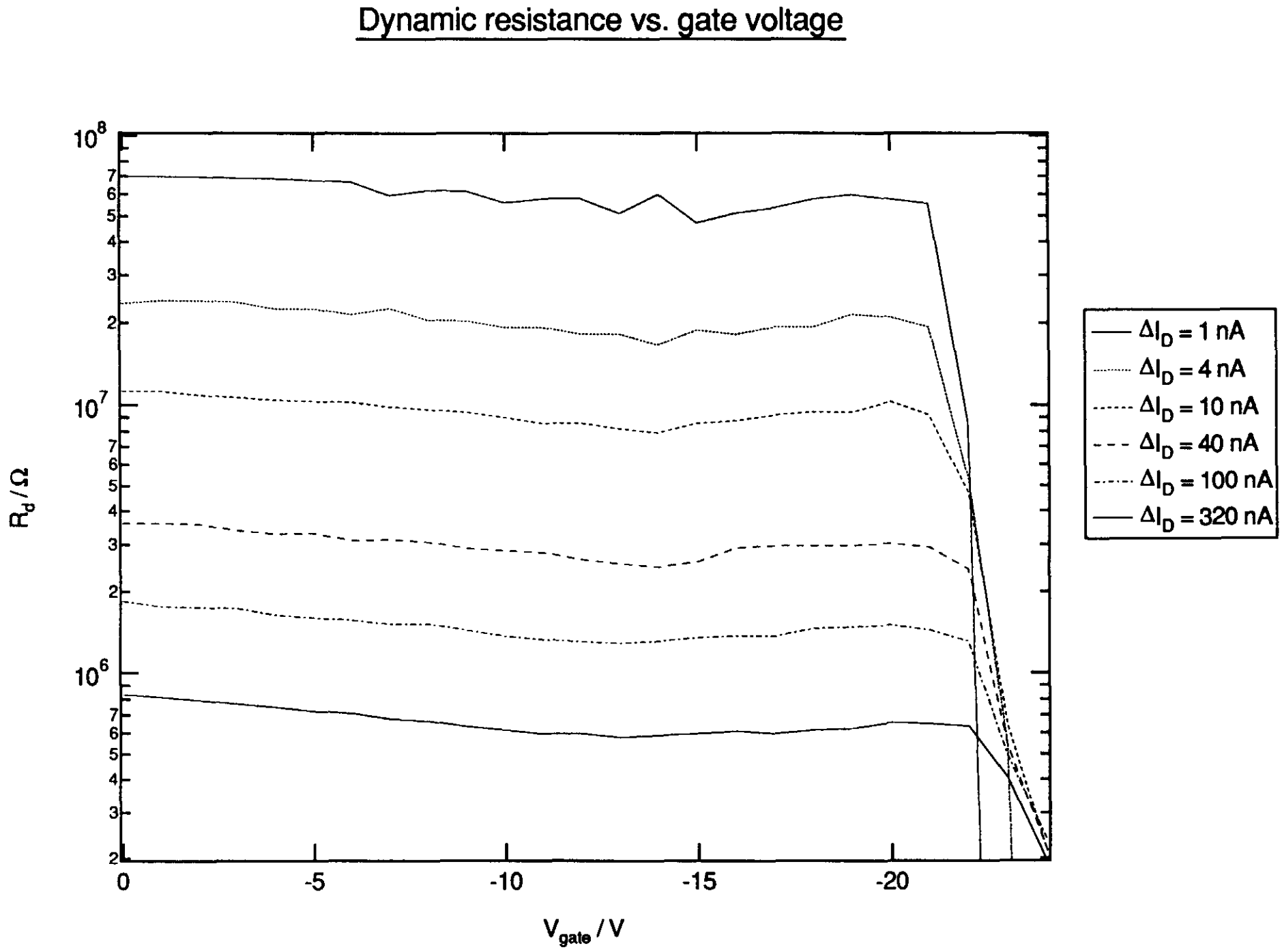
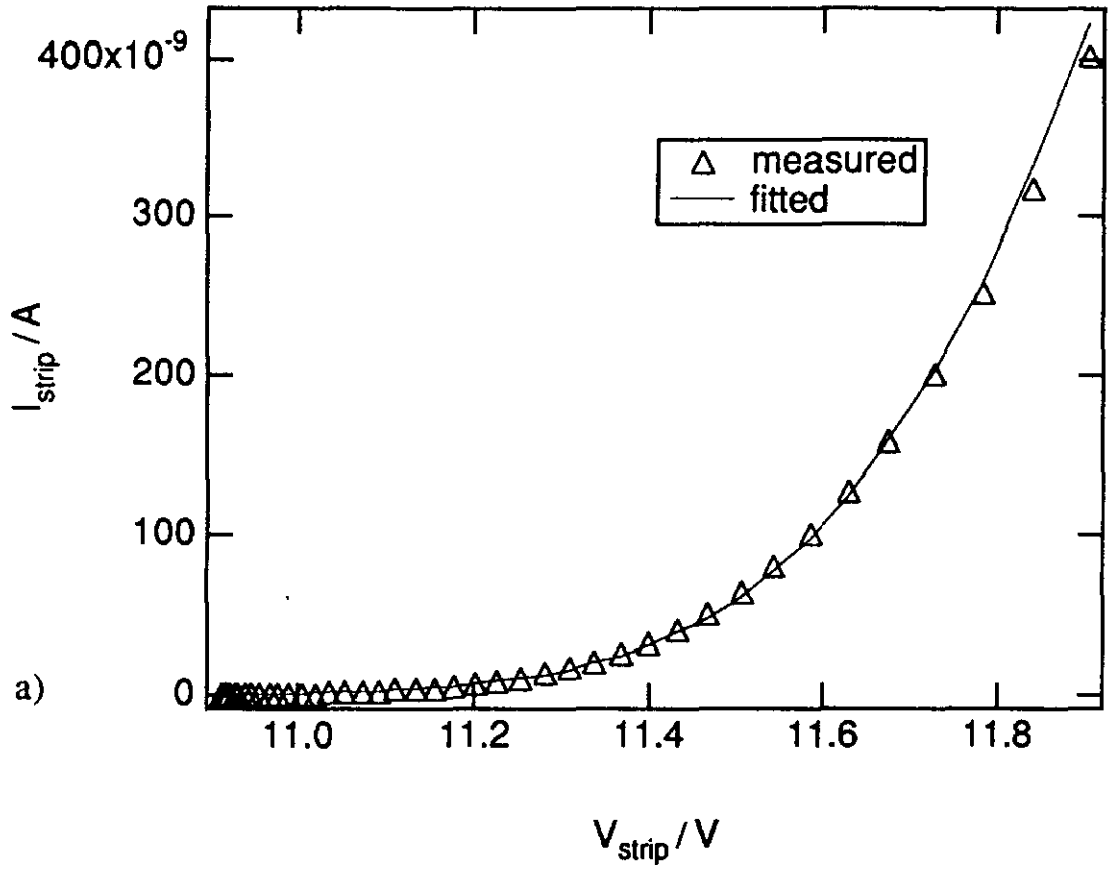


Figure 12.

FIG. 12


400x10-9
300
200
100
0
a)
Istrip / A
measured
fitted
11.0
11.2
11.4
11.6
11.8
Vstrip / V

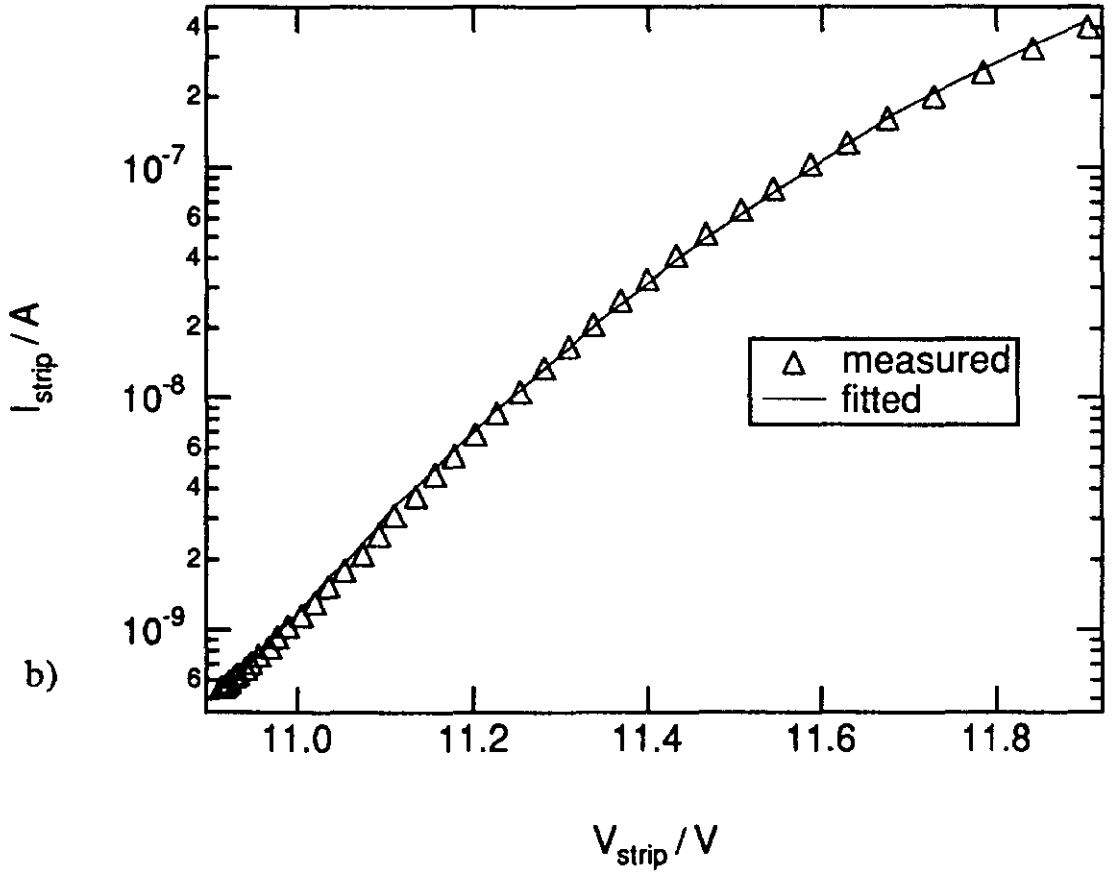

4
2
10-7
6
4
2
10-8
6
4
2
10-9
6
b)
Istrip / A
measured
fitted
11.0
11.2
11.4
11.6
11.8
Vstrip / V

Figure 13

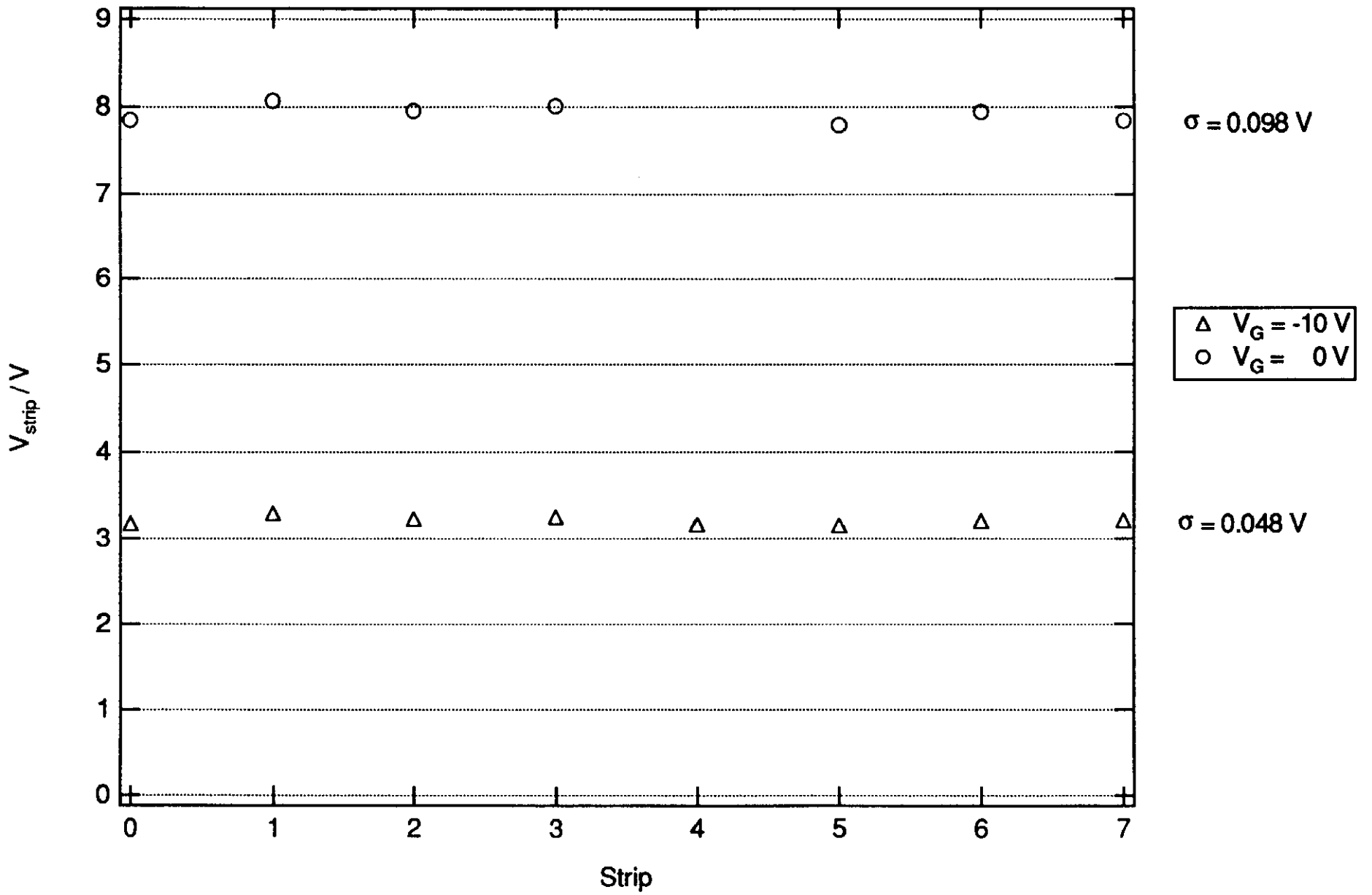

9
8
7
6
5
4
3
2
1
0
V_{strip} / V
0
1
2
3
4
5
6
7
Strip
σ = 0.098 V
σ = 0.048 V
Δ V_G = -10 V
O V_G = 0 V

Figure 14

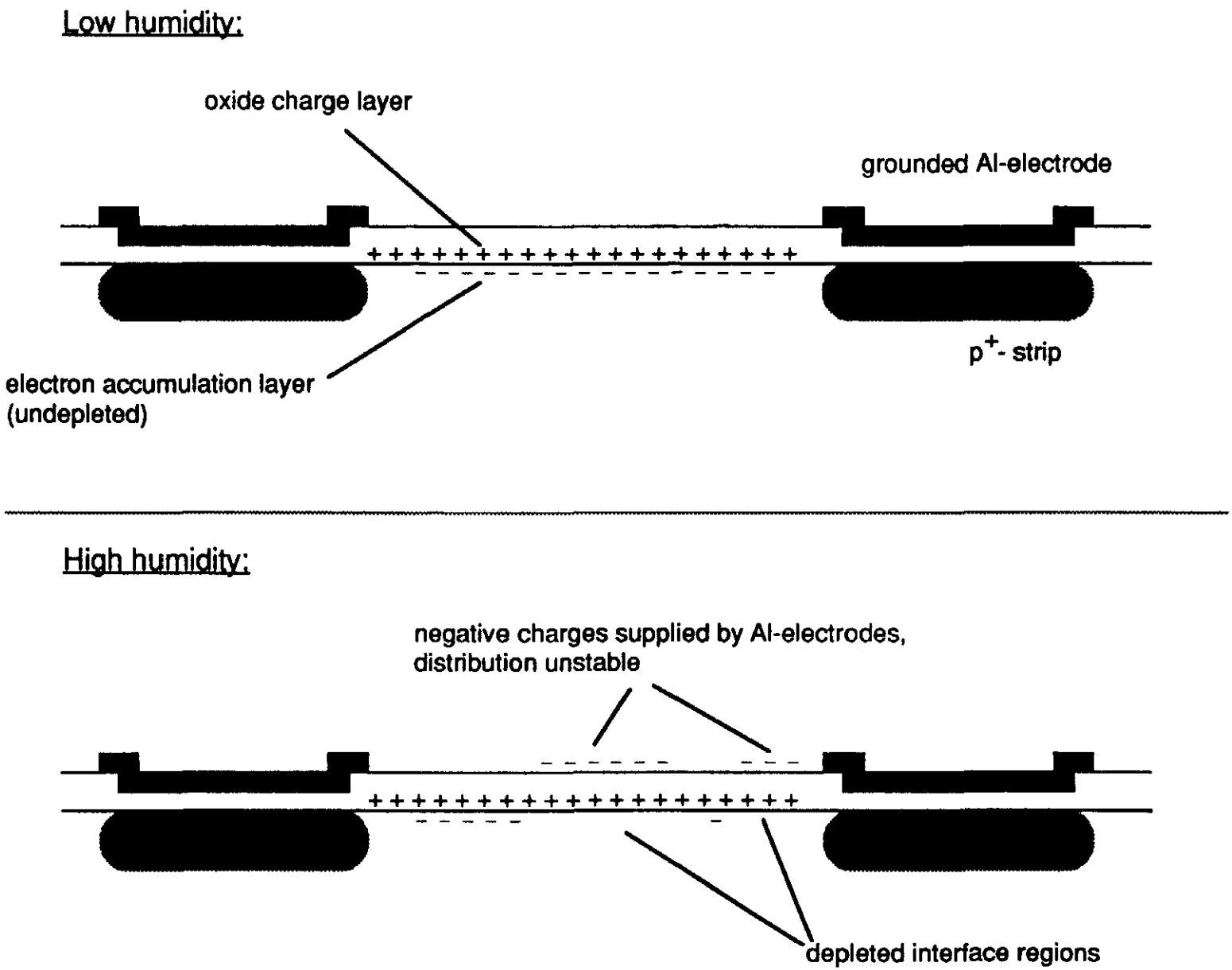

Low humidity:
oxide charge layer
grounded Al-electrode
p+- strip
electron accumulation layer
(undepleted)
High humidity:
negative charges supplied by Al-electrodes,
distribution unstable
depleted interface regions

Figure 15.

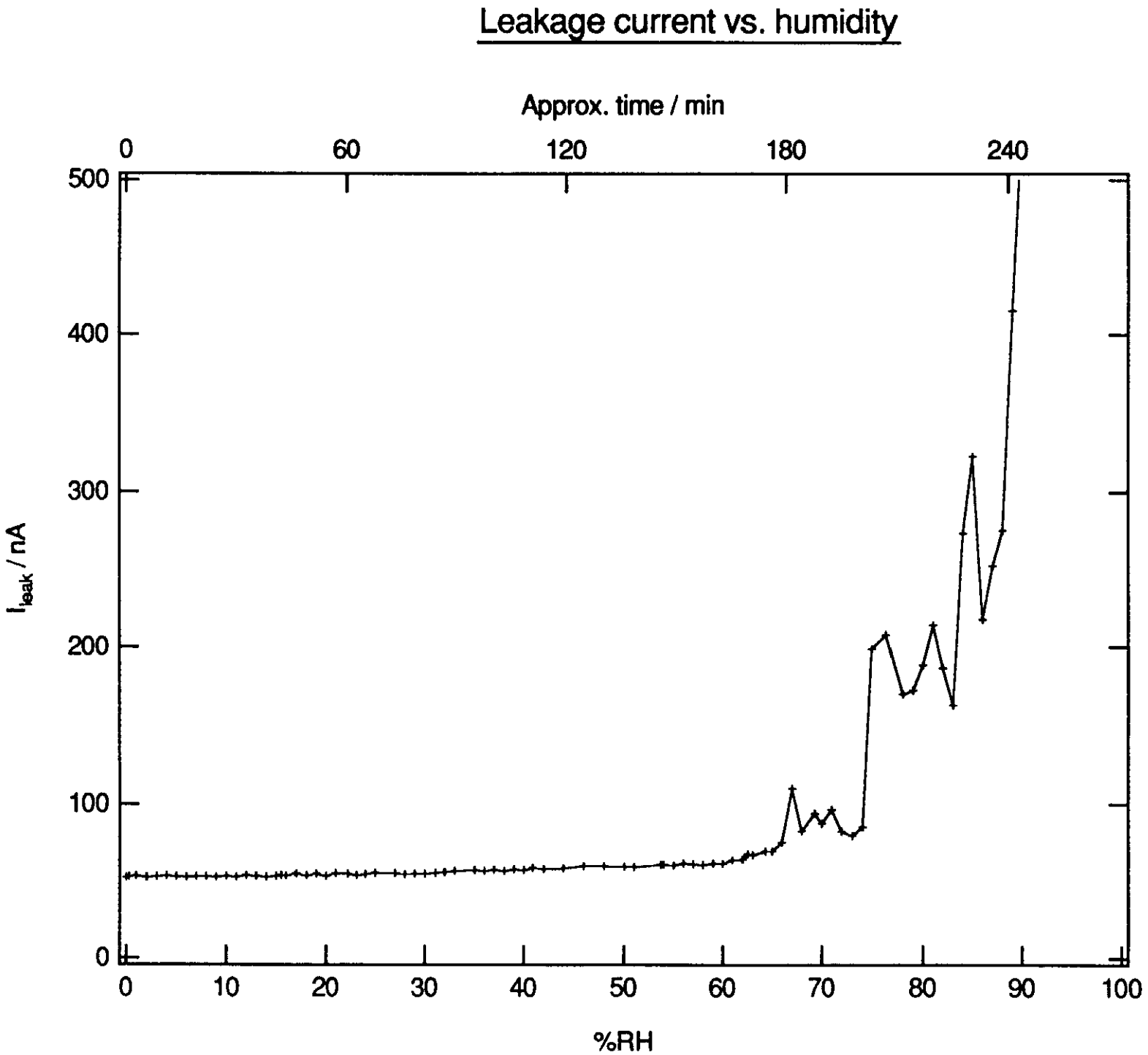

Leakage current vs. humidity
Approx. time / min
0
60
120
180
240
500
400
300
200
100
0
I_{leak} / nA
0
10
20
30
40
50
60
70
80
90
100
%RH

Figure 16

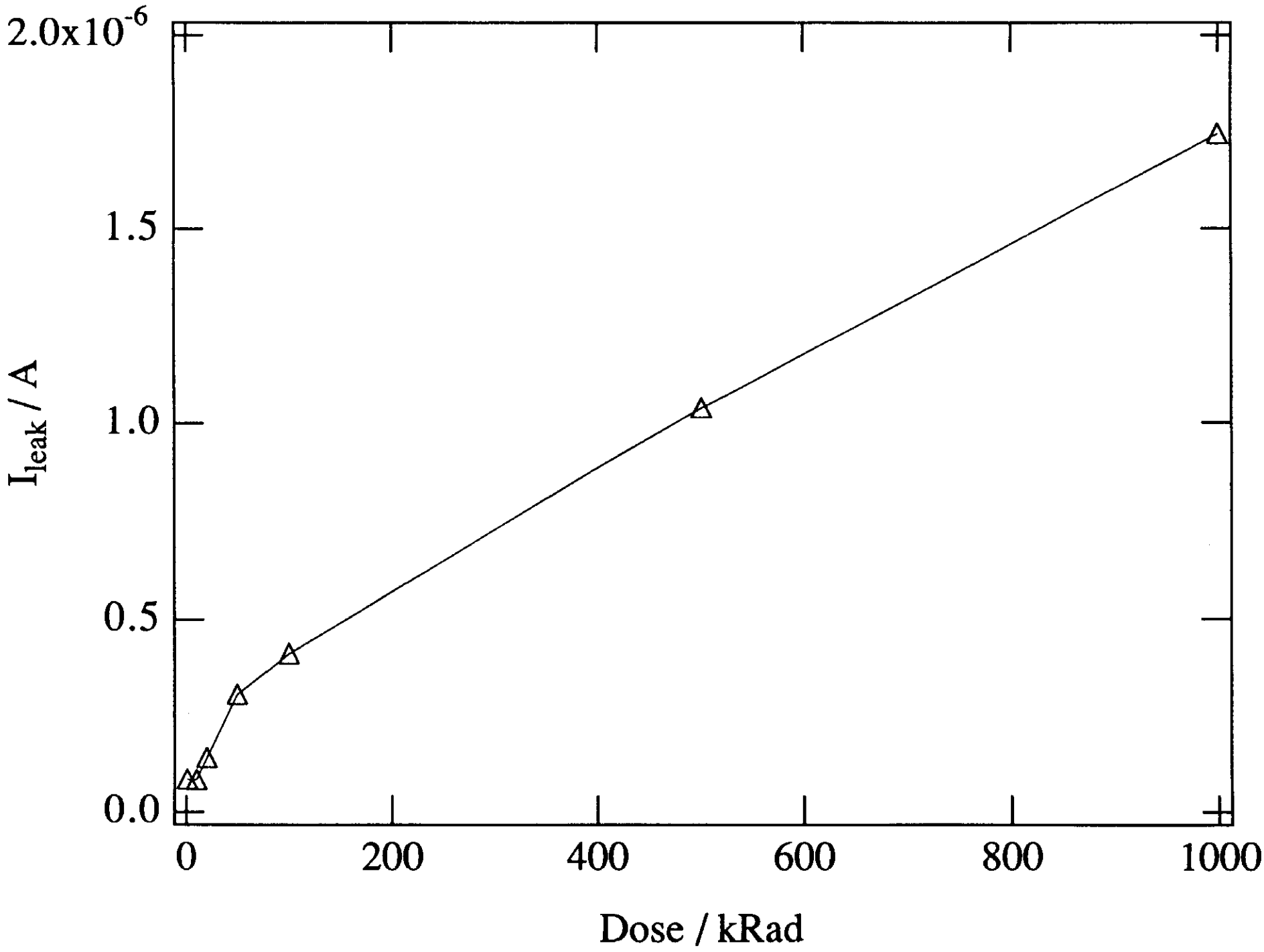


Figure 17

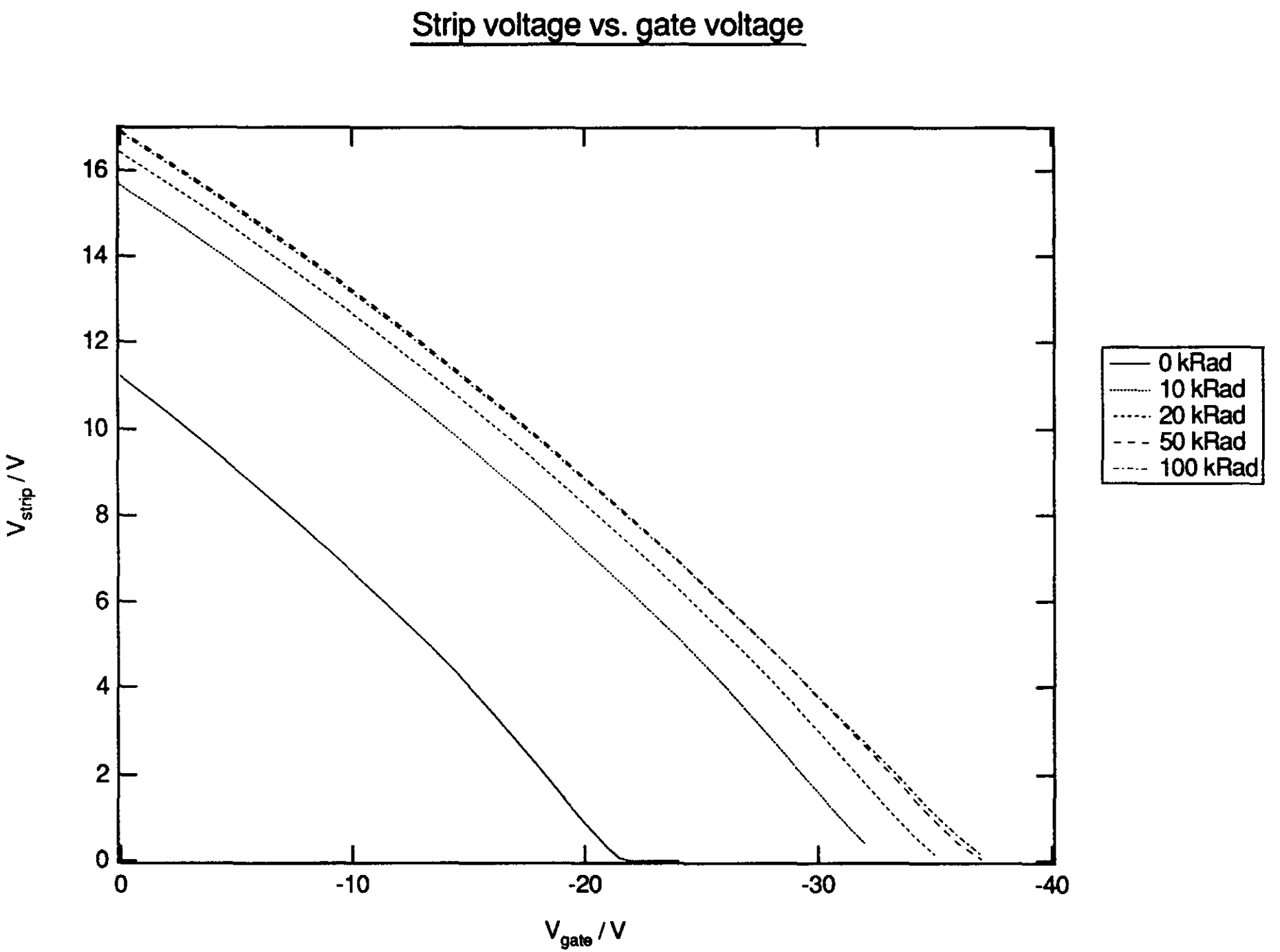

Strip voltage vs. gate voltage
16
14
12
10
8
6
4
2
0
0
-10
-20
-30
-40
V_{strip} / V
V_{gate} / V
0 kRad
10 kRad
20 kRad
50 kRad
100 kRad

Figure 18a

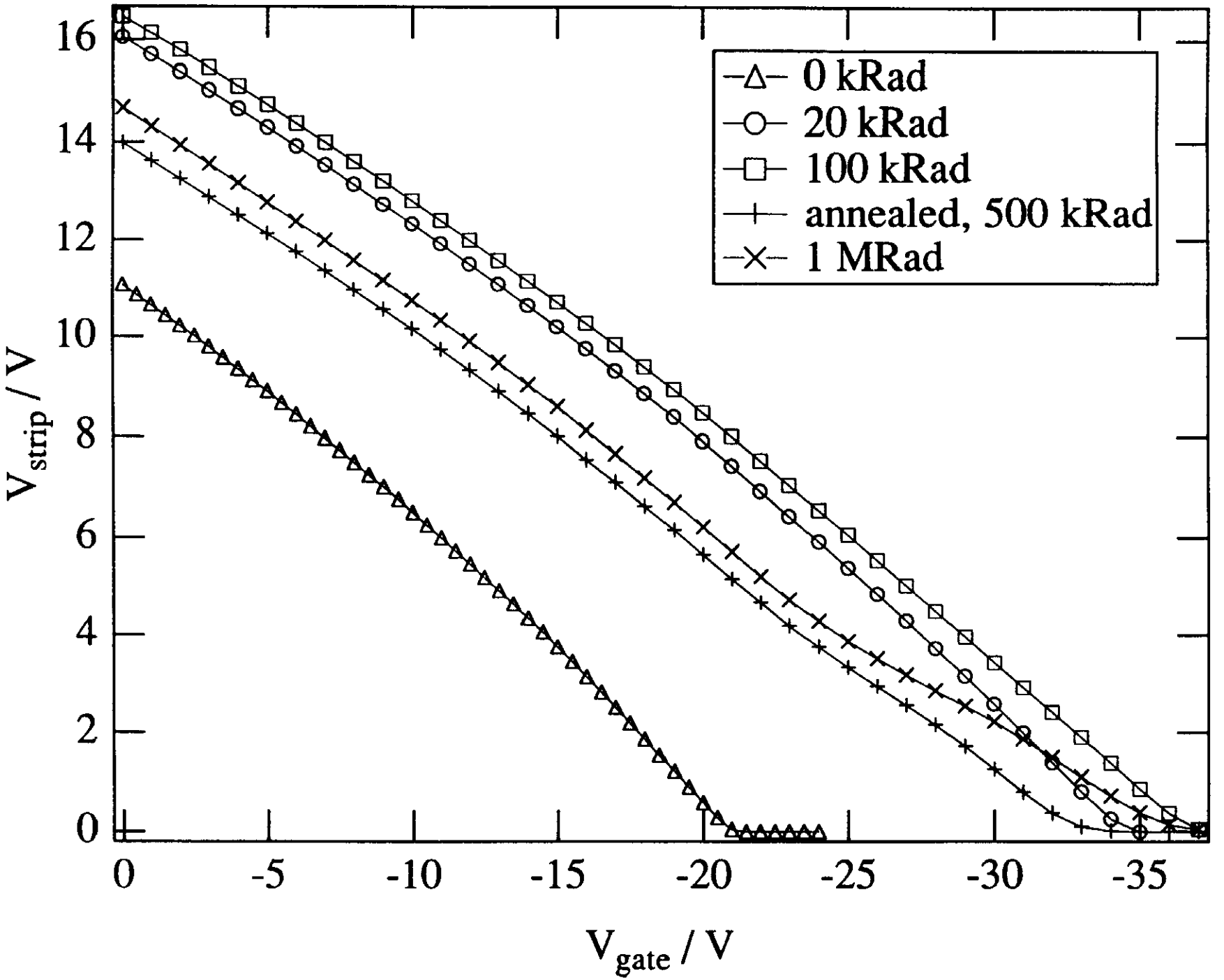

0 kRad
20 kRad
100 kRad
annealed, 500 kRad
1 MRad
16
14
12
10
8
6
4
2
0
0
-5
-10
-15
-20
-25
-30
-35
V_{strip} / V
V_{gate} / V

Figure 18b

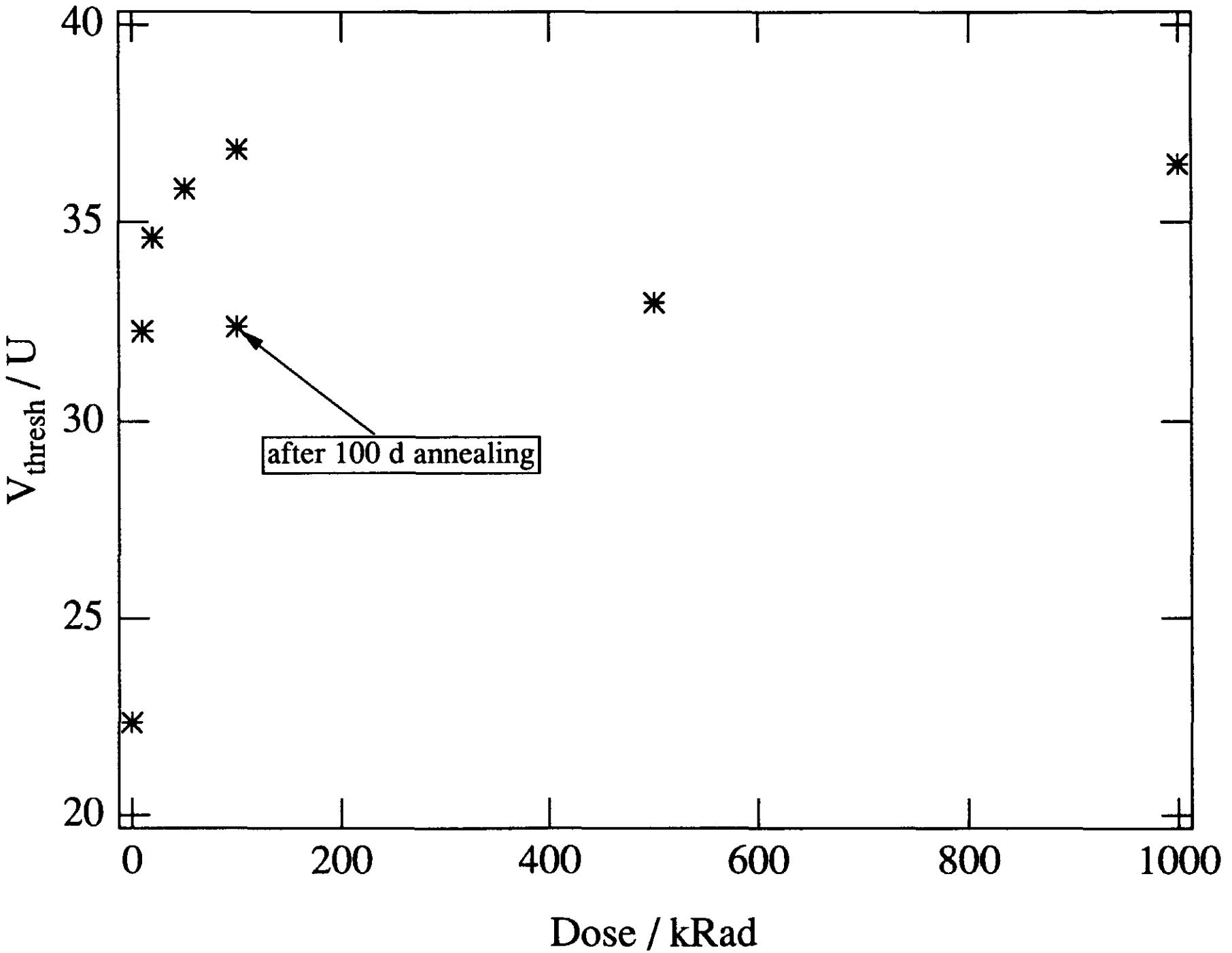

40
35
30
25
20
0
200
400
600
800
1000
V_{thresh} / U
Dose / kRad
after 100 d annealing

Figure 19

Charge trapping mechanism:

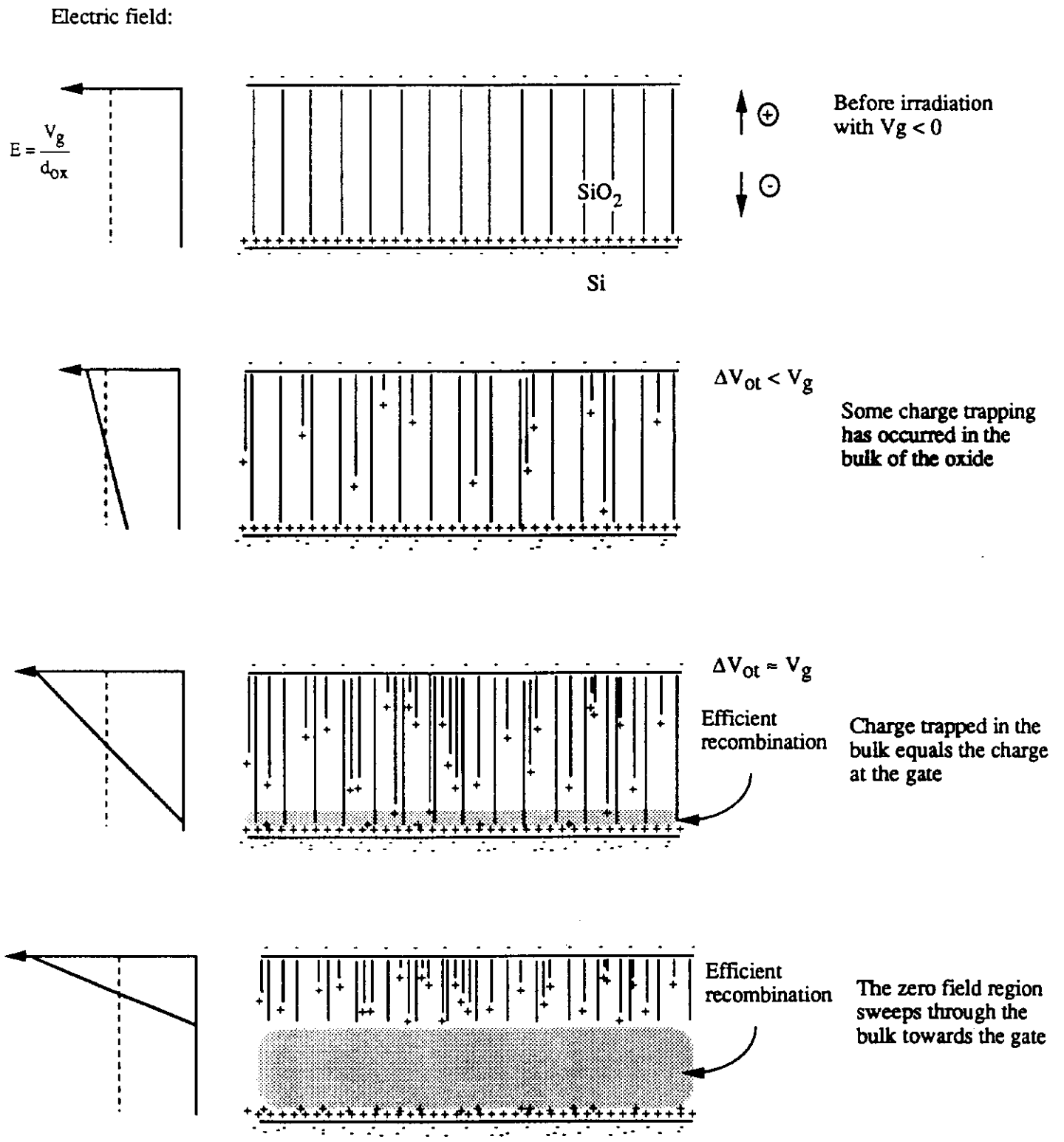


Figure 20

Dynamic resistance vs. injected current, $V_{gate} = 0$ V

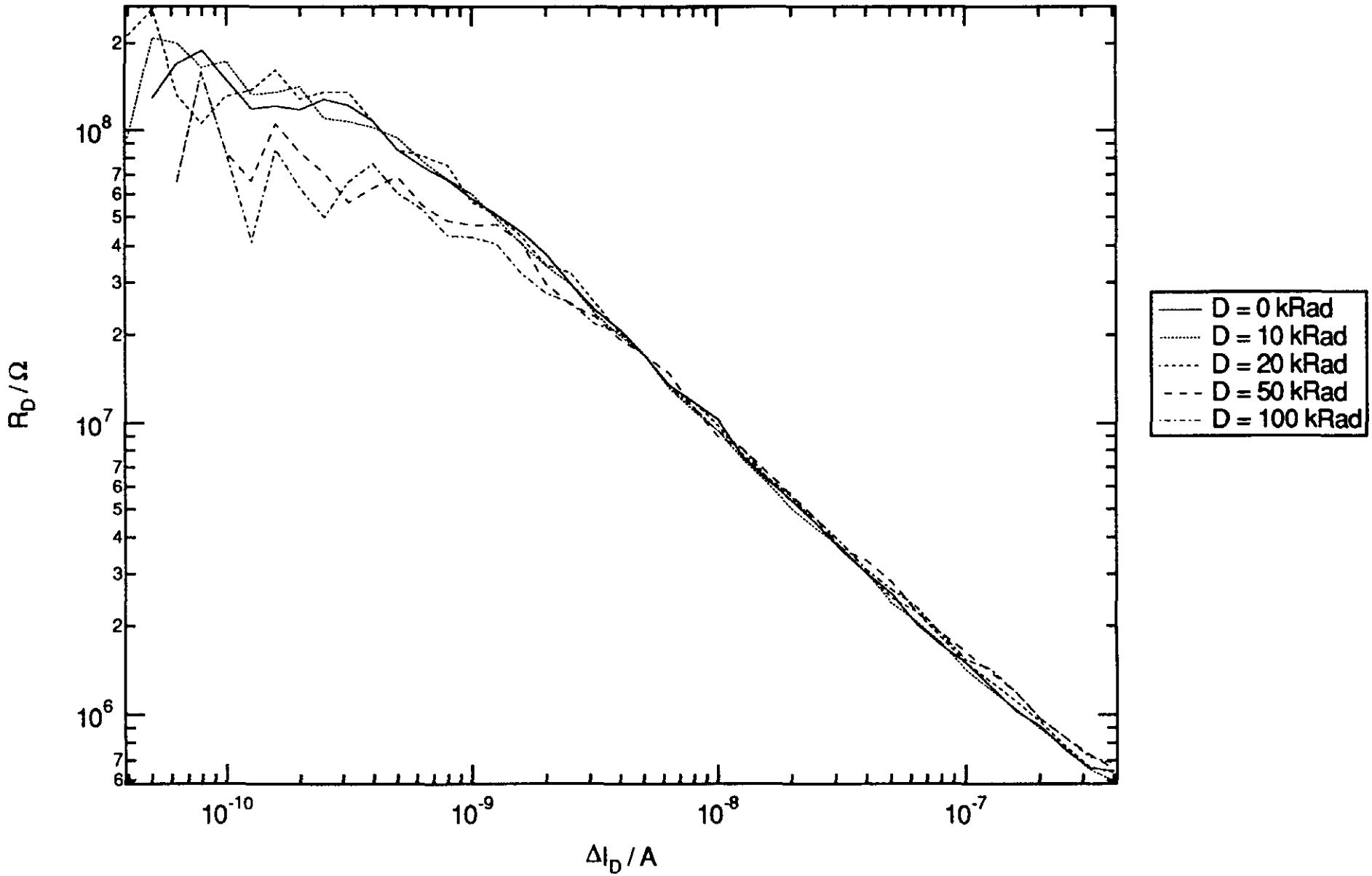


Figure 21

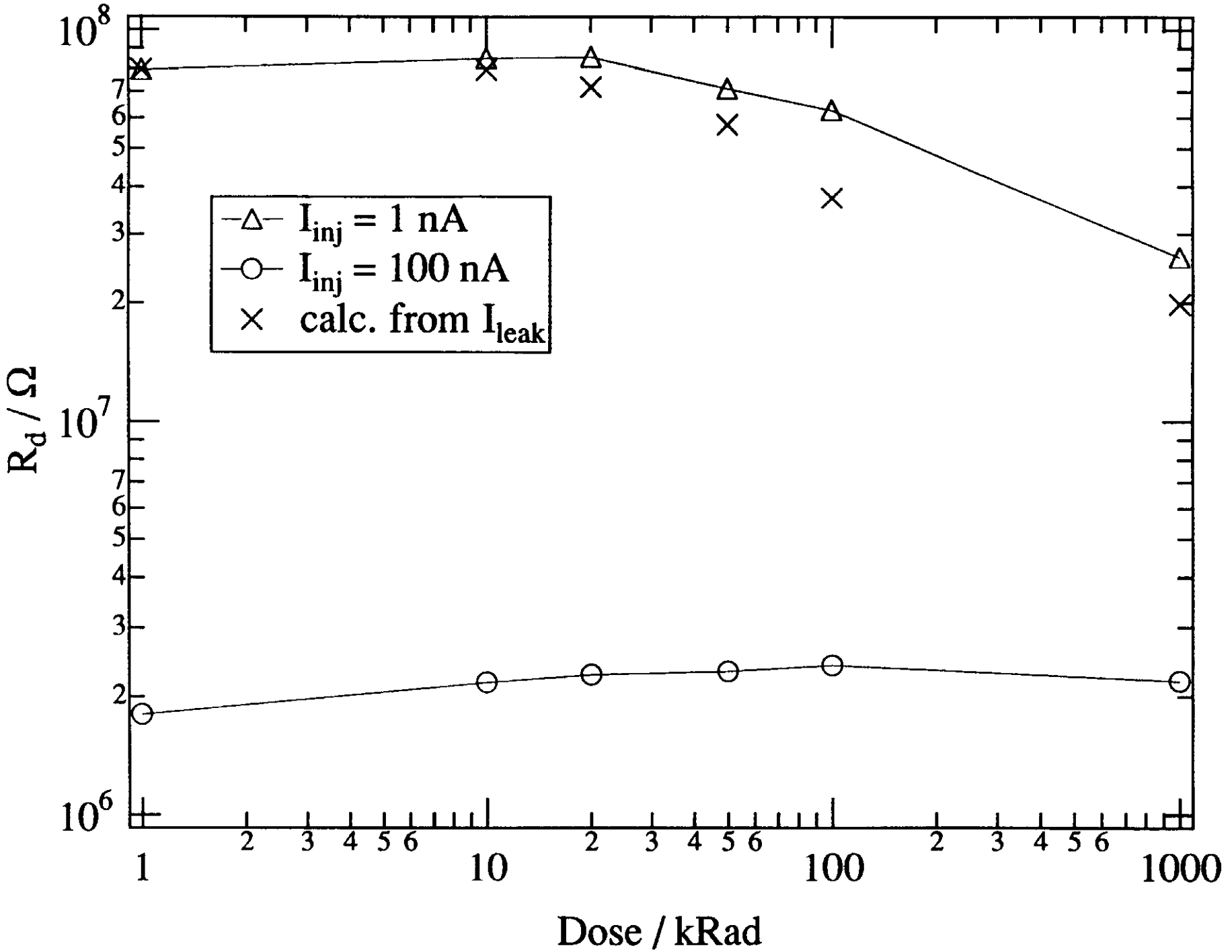

10^8
7
6
5
4
3
2
10^7
7
6
5
4
3
2
10^6
R_d / Ω
I_{inj} = 1 nA
I_{inj} = 100 nA
calc. from I_{leak}
1
2 3 4 5 6
10
2 3 4 5 6
100
2 3 4 5 6
1000
Dose / kRad

Figure 22

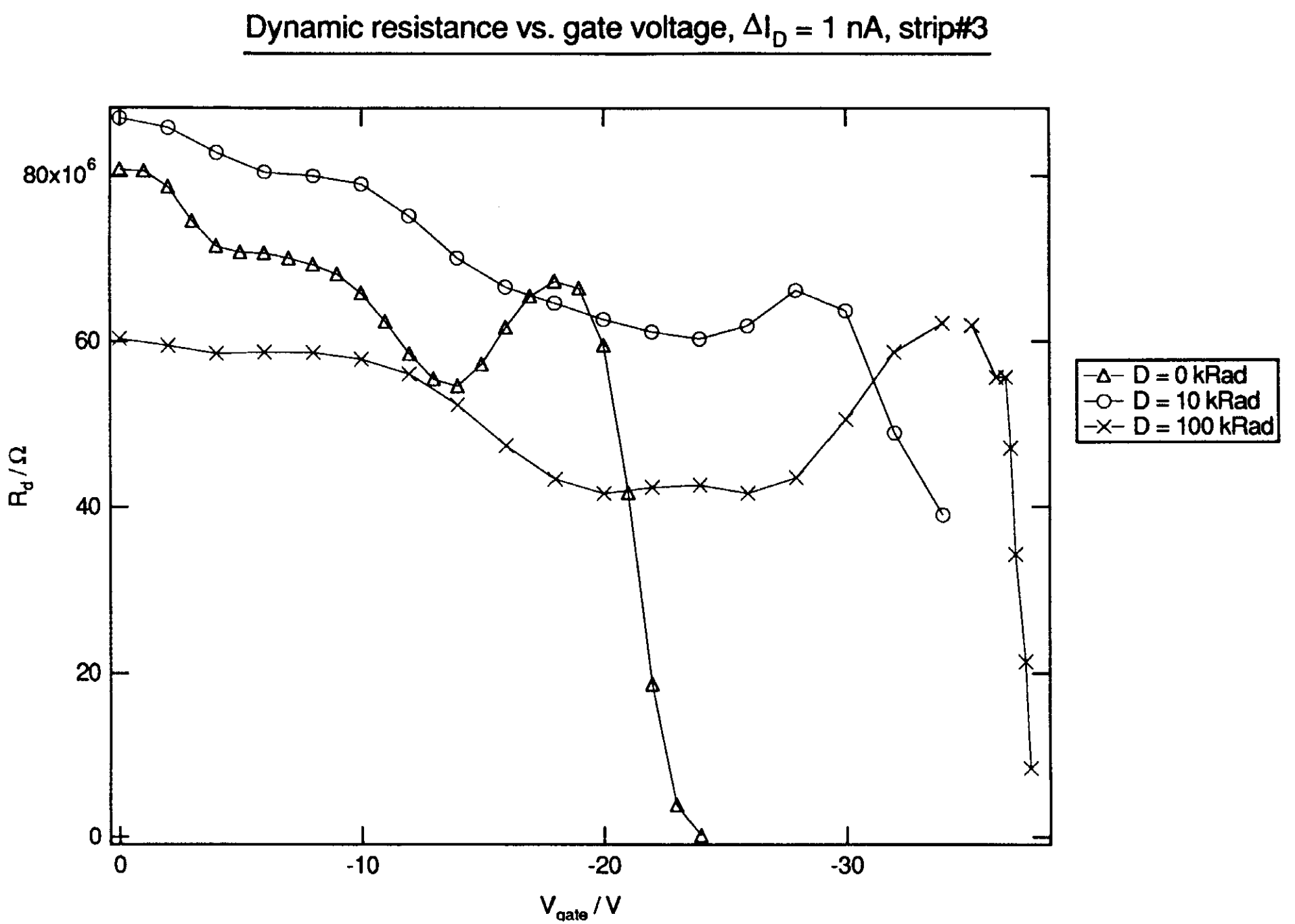

Dynamic resistance vs. gate voltage, ΔI_D = 1 nA, strip#3
80x10^6
60
40
20
0
R_d / Ω
0
-10
-20
-30
V_{gate} / V
D = 0 kRad
D = 10 kRad
D = 100 kRad

Figure 23a

Dynamic resistance vs. gate voltage, ΔI_D = 100 nA, strip#3

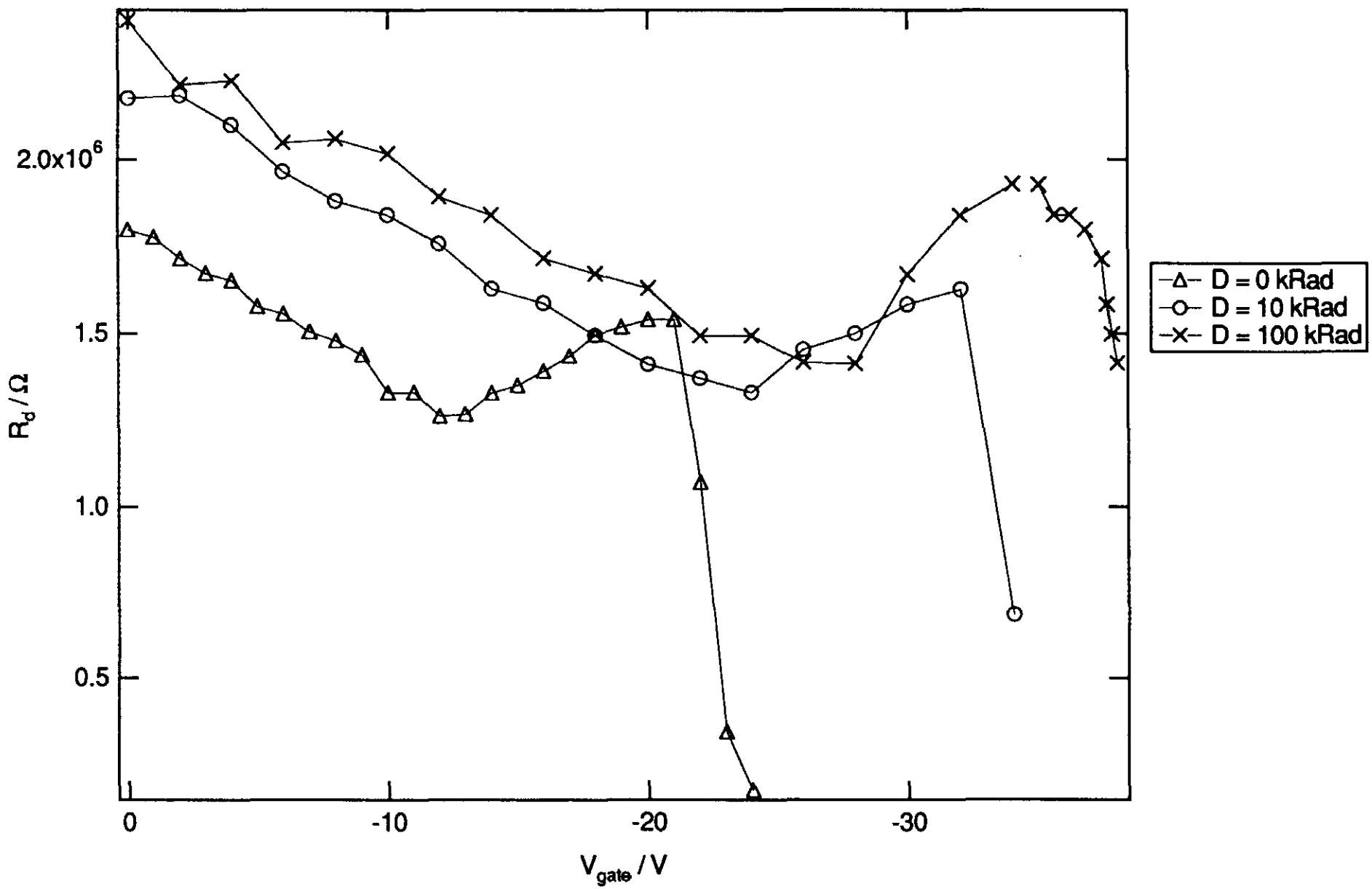


Figure 23b

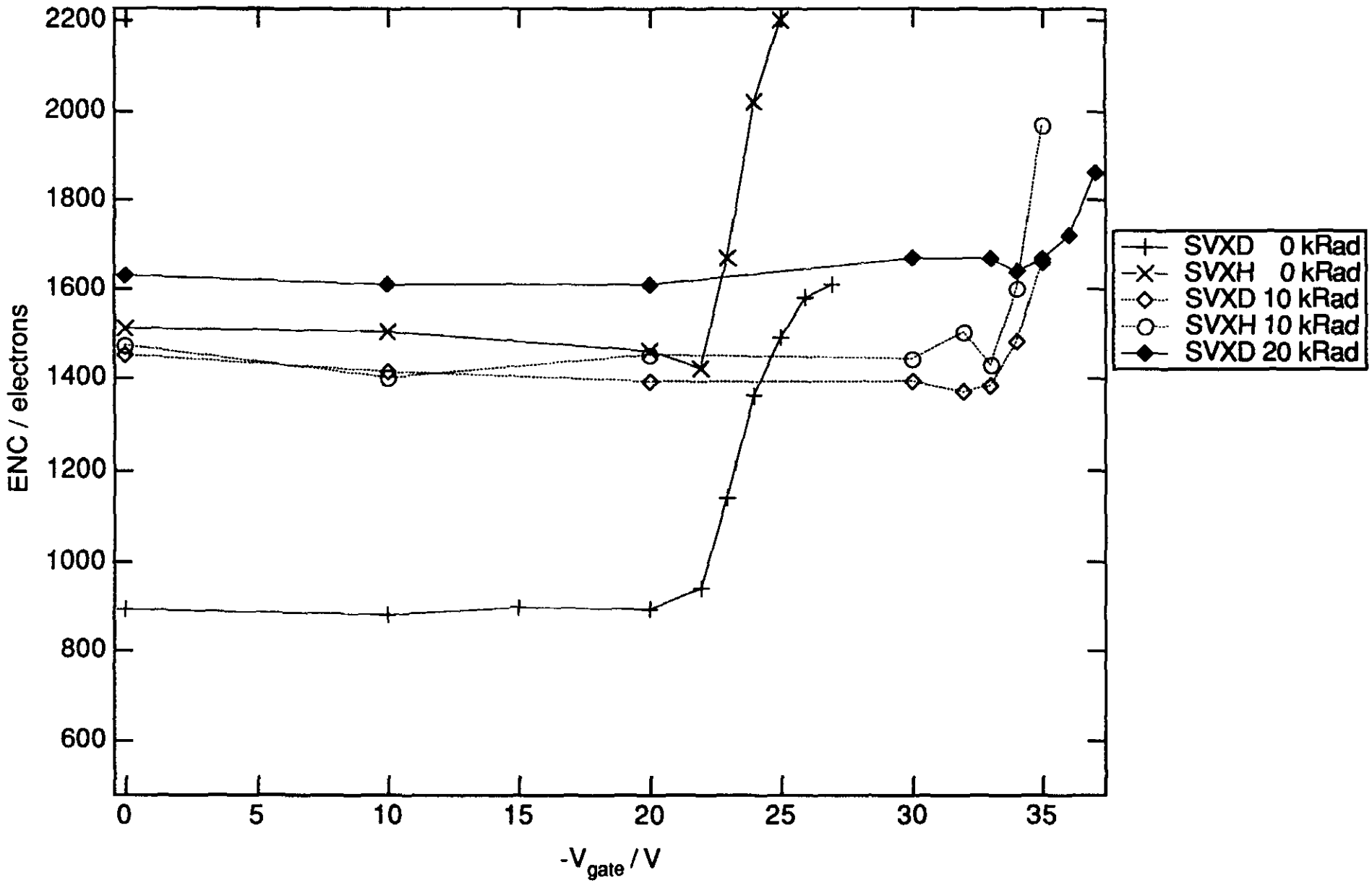

2200
2000
1800
1600
1400
1200
1000
800
600
ENC / electrons
0
5
10
15
20
25
30
35
-V_gate / V
SVXD 0 kRad
SVXH 0 kRad
SVXD 10 kRad
SVXH 10 kRad
SVXD 20 kRad

Figure 24