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An Approximate HSPICE Model for Orbit Low Noise Analog Bipolar NPN Transistors

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Vertical bipolar NPN transistors can be fabricated cheaply through MOSIS by using the Orbit 2 um Low Noise Analog CMOS process. The collector is formed from an N-well, the base from a p-base diffusion, and the emitter from an N-diffusion. However, since this is a CMOS process there is no buried layer in the collector. Therefore the collector resistance is quite large. Also, the minimum emitter size is 8 um X 8 um, which is substantially larger than many fast bipolar processes. For certain applications, though, such as common base or emitter follower amplifiers, the performance of this transistor may be quite acceptable. However, no AC SPICE model is published for this device. This paper describes a simple approximate measurement method that was used at Fermilab to formulate an HSPICE model for these transistors. This method requires only a fast pulse generator and a good digitizing oscilloscope with an active FET probe for the AC measurements. Model parameters for two transistors of different size are then given. An invaluable reference used throughout this work is the Tektronix,Inc. publication "Modeling the Bipolar Transistor," by Ian Getreu (copyright 1976).

DC Parameters

DC parameters are easily measured using an H.P. Semiconductor Parameter Analyzer. Following is a list of basic parameters and how they were measured.

BF -- Forward beta = IC/IB

VAF -- Forward Early Voltage = ΔIC/ΔVCE

IS -- Saturation current. log(IS) = Y-intercept of log(IC) vs. VBE curve

RC -- Collector series resistance. Measured by lowering VCE at a given IC until IB begins to increase. RC≈(VCE-0.2)/IC.

RB, RE -- Hard to measure individually, but RB + (1+ß)RE is easily measured from the log(IB) vs. VBE graph. Ideally, this is a straight line, but RB and RE cause curvature at higher currents. The horizontal deviation from the ideal line at a given IB is ΔVBE = IB*RB + IE*RE, thus RB + (1+ß)RE = ΔVBE/IB. For now, assume a reasonable RE and then calculate RB. Later tests can give a more accurate value for RB (and thus RE).

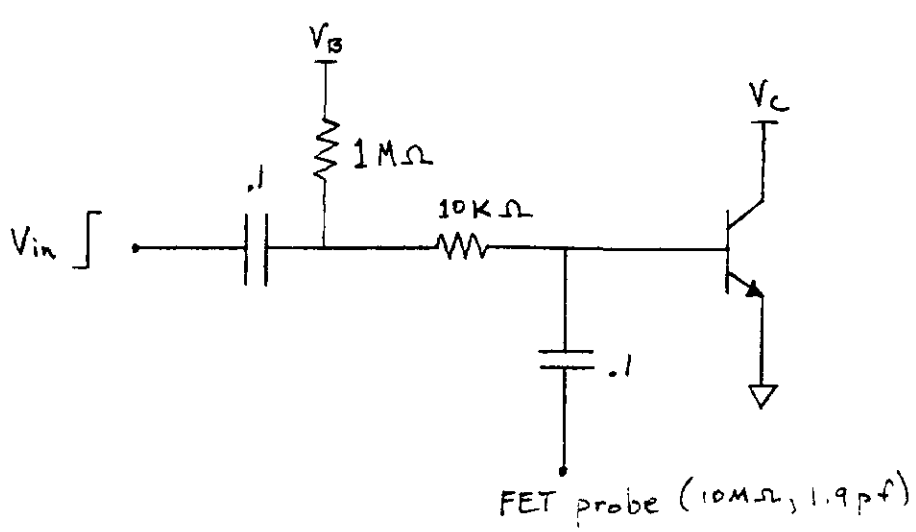
NE, ISE -- These model the low current decrease in beta. Using the log(IB) vs. VBE curve, the theoretical moderate current slope of the line is q/kT. At low currents, the slope is q/(NE*kT). The y-intercept is IS*ISE.

Junction Capacitance Parameters

To measure junction capacitances, the simple technique of applying a step voltage through a known resistance to the appropriate point and measuring the risetime is used. Parasitic minimization is very important, so an active FET probe must be used. Also, a large area transistor should be used so that junction capacitances are not swamped out by the parasitics. This transistor should be connected to the shortest possible leads if in a chip carrier. The parasitic capacitance is measured by disconnecting the bond wire at the die. This capacitance can then be subtracted from the following measurements.

Cbe, Cbc measurement

The following circuit is used to make this measurement:



To measure Cbe (base-emitter depletion capacitance) as a function of VBE, VC is set to a constant value above VB (as high as is practical) to minimize Cbc (base-collector depletion capacitance), then VB is varied and the risetime at the base measured. Once Cbe is known, VB is set to zero and VC varied to measure Cbc vs. VC (the value of Cbe and the parasitics are subtracted from the measured value).

Values of the HSPICE parameters CJE, VJE, MJE, and FC enter into the HSPICE calculation of Cbe as a function of VBE. CJE is simply the base-emitter capacitance at VBE=0. A simple method of determining the other parameters is to vary them empirically until the HSPICE calculation result matches the measured capacitance for the range of interest. HSPICE uses one of two methods to calculate the voltage dependent capacitance. It was found that the option DCAP=1 should be set to invoke the most accurate calculation for these junctions. Values for CJC, VJC, and MJC (collector-base junction parameters) can be found in a similar manner.

Ccs measurement

The collector-substrate junction capacitance is measured using the same method, but by connecting the input circuit to the collector instead of the base, and varying VC. The collector-base should be reversed biased by a constant amount (as high as is practical) in order to minimize base-collector capacitance. CJS, VJS, and MJS can then be found by using the same method as for the other junctions.

TF measurement

The forward transit time is an important speed parameter, since it determines the base-emitter diffusion capacitance under forward bias. At first, one might suppose it could be easily measured by inserting a 50 ohm resistor into the collector of the circuit used for measuring Cbe, and looking at the output risetime with a 50 ohm scope input, and thus calculate the total input capacitance. However, the presence of RB and RE affects the result, and the large collector resistance causes a substantial Miller effect. The simplest way to get an approximate value for TF, then, is to measure the output risetime for several different collector currents, and then model the circuit in HSPICE, using all the previously measured parameters, and adjust TF in the model until the simulated behavior matches the measured.

RB measurement

Since only the quantity RB + (1+ß)RE has been measured, it would be desirable to measure RB only. A simple dynamic method was derived from the fact that the input to a common base amplifier can look inductive due to the presence of RB. If a capacitor is connected from the emitter to ground, and the emitter is driven with a step current pulse, the common base output will ring, with the frequency being sensitive to the value of RB. Thus RB (and correspondingly, RE) was adjusted in the HSPICE model until the simulated response matched the observed response. This method seemed to work quite well for a small transistor (with relatively large RB), but for larger transistors care is required since the circuit becomes more sensitive to the stray inductance of the package leads.

Results

Parameters were measured for two different transistors on a test chip produced by MOSIS and designed by Dr. Vance Tyree. The layout of these is intended to be optimized for low parasitic resistance. One device is NPN1, a minimum size transistor with 8 um X 8 um emitter area. The other is NPN32, with 32 parallel minimum emitters. The junction capacitance parameters were measured only on NPN32, and were scaled for NPN1, based on the ratios of the junction areas of the two transistors. The results of all measurements are given here in the form of an HSPICE BJT model. Remember, DCAP=1 should be set in the .OPTIONS statement.

```
*Orbit minimum NPN (NPN1)
.model npn1 npn  is=6.7e-17 vaf=35 bf=141 rc=800 rb=300 re=14.7
+ne=1.46 ise=2.6 tf=60e-12 cje=.1p cjc=.1p cjs=.22p mje=.333
+vje=.75 mjc=.5 vjc=.75 mjs=.5 vjs=.75 fc=.67
```

```
*Orbit big NPN (NPN32)
.model npn32 npn  is=2e-15 vaf=35 bf=143 rc=65 rb=25 re=3 ne=1.46
+ise=2.6 tf=60e-12 cje=3.2p cjc=2.1p cjs=2.0p mje=.333 vje=.75
+mjc=.5 vjc=.75 mjs=.5 vjs=.75 fc=.67
```