



Fermilab

PA CASCODE RECORDER/DISPLAY SYSTEM DESCRIPTION AND OPERATING INSTRUCTIONS

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I. General

The Recorder/Display System is a 16-channel signal recorder used to test the cascode power amplifiers in the Booster and Main Ring rf systems. The system digitizes and records 16 analog signals (14 cathode currents, control grid current, and screen grid current) at $2\mu\text{s}$ sampling rates. These analog signals must be externally scaled to 0-10V full scale range. When a playback trigger pulse is received, the system continues to digitize the 16 analog input signals for the number of samples selected by a delay selector. Then four of the sixteen analog signals can be displayed on a standard oscilloscope for visual analysis. A trigger delay selector can be used to trigger the oscilloscope at different points on the display, allowing for visual expansion of different areas of the display.

The system also includes bar graph displays indicating levels on the 16 analog signal lines. These displays are independent of operation of the recorder/display functions and can be used to monitor DC levels of the cathode and grid currents.

The Recorder/Display System is housed in two crates. One crate contains the electronic PC boards necessary to control the system functions. All selector switches, indicators and outputs to the oscilloscope are mounted on the front panel of this crate. All input connectors are mounted on the rear panel. The other crate contains all power supplies required by the system. The planar gas discharge bar graph displays are mounted on the front panel of this crate.

Located on the rear panel of each crate are power and display connectors. The power connectors must be connected with the supplied power cable for proper system operation. The system will operate without the display cable in place, but that cable must be connected for the bar graph displays to function.

II. Operating Instructions

*CAUTION: High voltage (250 VDC) is present in both crates when the system is in operation. Be certain to disconnect power and wait at least 10 seconds before making any modifications or repairs to the system electronics.

A. Input Signals

The input signals are connected to the BNC connectors on the rear panel of the electronics crate. All ANALOG IN signals must have 0-10V full scale range. Each input provides approximately 5K Ω load impedance. Each vertical column represents a group whose four inputs can be simultaneously viewed on an oscilloscope during playback. The Group 1 Input signal is viewed on the Group 1 Output port, Group 2 Input is viewed on Group 2 Output, and so on.

The PLAYBACK TRG signal is also connected to a BNC connector on the same rear panel. This signal must have a negative-true TTL-compatible level. Minimum pulse width is 50 nS. The input provides one TTL gate load.

The DISPLAY and POWER connectors on the rear panel of each crate must be connected using the cables provided. The POWER connector must be in place for the system to operate. The DISPLAY connector must be in place for the bar graph displays to operate.

B. Output Signals

The output signals to an oscilloscope are located on the front panel of the electronics crate. These are the OUT 1-4, POS INT, TRG, and NEG INT BNC connectors. The Group OUT 1-4 signals are the analog output signals to the vertical inputs of an oscilloscope (or scopes). The TRG signal is the external trigger for the scope. POS INT and NEG INT are the Z axis intensity modulation inputs for the scope. For scopes with negative blanking, POS INT is used; for scopes with positive blanking, NEG INT is used.

To obtain a display, an oscilloscope with capability of displaying four analog inputs (or two dual-trace scopes) must be used. Group OUT 1-4 are connected to the four vertical inputs. TRG is connected to the external trigger. The appropriate INT output is applied to the Z axis input. The oscilloscope settings should be as follows:

Vertical Mode: chopped
Vertical Sensitivity: 5V/div
Horizontal Sweep: 1ms/div
Trigger Source: External
Trigger Mode: Normal
Trigger Coupling: AC
Trigger Slope: Positive
Trigger Level: Approx. 2.0V

These settings cause the entire batch of data recorded (1024 words, or about 2mS time period) to be displayed during the playback mode. The vertical sensitivity can be varied, and the horizontal sweep speed, X10 magnifier, and DISPLAY DELAY SELECTOR can be used to more accurately display the data.

C. System Operation

When the appropriate input and output connections are made, power can be applied to the system. When the power switch is turned on, the RECORD LED should light, indicating that the system is in the record mode. The bar graphs should light, with the bars extending to a length representing the input signal of the corresponding channel. Each bar graph contains 100 segments, so each segment represents a 1% increment of that channel's full scale range.

When a PLAYBACK TRG pulse is received, the system continues to digitize and store the 16 analog inputs for the number of counts indicated by the RECORD DELAY COUNT switch (each count is a 2 μ S time period; the total information stored in memory represents 1024 counts). After this delay, the RECORD LED extinguishes and the DISPLAY LED lights, indicating that the system is in the playback mode. The analog input signals indicated by the OUTPUT selector switch are displayed on the scope. The OUTPUT switch can be changed during the playback mode to view the other signals.

Normally, the DISPLAY DELAY COUNT switch is set to "0" to view the signals as they occurred. However, the oscilloscope trigger can be delayed with respect to the beginning of the analog signal by the number of counts indicated. This has the effect of moving a certain portion of the signals closer to the beginning of the trace so that it can be expanded and viewed more carefully. The DISPLAY DELAY COUNT switch can be changed during the playback mode.

When the DISPLAY DELAY COUNT switch is not set to "0," the signal appearing at the beginning of the trace is not the first event which occurred in "real time." In order to view the beginning of "real time," the START MARKER switch can be turned on. This causes an intensified marker to appear on the analog signals at the start of "real time."

To return to the record mode, the DISPLAY RESET button is depressed. This terminates the oscilloscope display and returns the system to the record mode.

III. Block Diagram Description (Refer to Fig. 1 - block diagram)

The Recorder/Display System contains seven printed circuit cards: one Recorder Control, one Display Control, one Bar Graph Driver and four Quad Recorders. The functional arrangement of these circuit boards is shown in the system block diagram.

Each Quad Recorder board converts four analog input signals to digital information, stores the data in memory, multiplexes the four channels to one (depending on the position of the OUTPUT switch), and converts that information back to analog for display. Thus, for each position of the OUTPUT switch, one of four channels is selected on each of the four Group OUTPUT Quad Recorder boards and displayed.

The Recorder Control board contains the necessary control and timing signals required by the Quad Recorders for digitization and data storage. It also generates timing and control signals to access data for display and contains the circuitry required to implement the PLAYBACK DELAY and OUTPUT Group selectors.

The Display Control board contains circuitry required to display the stored data on an oscilloscope. It also provides the DISPLAY DELAY option and generates the START MARKER.

The Bar Graph Driver board provides the signals required to drive the gas discharge bar graph displays. This board is designed to operate with Burroughs self-scanning displays.

IV. Circuit Description

Refer to the following schematic drawings for the Recorder/Display System circuit description:

1. Quad Recorder - 0333.00-ED-63443
2. Recorder Control - 0333.00-ED-63442
3. Display Control - 0333.00-ED-63449
4. Bar Graph Driver - 0333.00-ED-63446

A. Record Mode

At power-on, a POWER-ON CKT (U14 pin 10) on the Recorder Control sets the DECADE CTR to a count of 9 preventing it from clocking during the START-UP and RESET pulse, and resets the PLAYBACK FF, READ FF, R/W FF and PLAYBACK DELAY CTR.

When START-UP and RESET goes low, the latch ENBL FF on the Recorder Control is set, and the DECADE CTR is allowed to advance, starting the record mode. \overline{WE} enables the write cycle on the 1Kx8 RAM's (U9-U12) on the Quad Recorders, and $\overline{LATCH ENBL}$ enables the outputs of the tri-state latches (U5-U8).

The RECORDER CLOCK is divided by two to form a symmetrical 5 MHz clock, which is applied to the DECADE CTR. Gate U9 pin 6 provides a negative-going pulse each time the DECADE CTR reaches a count of 9, disabling gate U11, and generating DATA CLK and ADDR CLK (see Fig. 2 - Record Mode Timing Diagram). The CONVERT PULSES produced by this gate arrangement are applied to all ADC's on the Quad Recorders, causing them to digitize the analog voltage presented on V_{in} (refer to the Burr-Brown data book for detailed description of operation of the ADC82KG with external clock). An external clock is used in order to obtain faster conversion time than would be obtained with the internal clock. At the leading edge of the ninth EXT CLK pulse, conversion is complete and data is ready at the ADC outputs. The leading edge of DATA CLK then loads the data into the tri-state latches on the Quad Recorders. The leading edge of ADDR CLK advances on ADDRESS COUNTER on the Display Control board. This counter provides the memory address inputs for the 8K RAM's on the Quad Recorders.

At the trailing edge of DATA CLK and ADDR CLK, a WRITE PULSE monostable generates a \overline{CE} pulse, which is applied to all 8K RAM's, causing data stored in the tri-state latches to be loaded into the memory locations pointed to by the ADDRESS COUNTER. This process repeats indefinitely in the record mode. Analog signals at V_{in} are digitized and stored into memory. When the ADDRESS COUNTER overflows, new data is written over old data in memory.

The functions of the tri-state latches on the Quad Recorder are twofold: they provide the necessary tri-state interface to the memory I/O lines, and they allow use of slower (less power-consuming) memories. From the timing diagram, it can be seen that data is not loaded into memory until the next A/D conversion process has begun. The timing sequence generated by the Recorder Control ensures that the write cycle timing parameters of the 8108-5CD memories are met. The Recorder Control also provides accurate 2 μ S sampling periods for the digitization process.

During the record mode, the U11-6 OUTPUT pulses are applied to U21 pin 9, a retriggerable monostable which causes the RECORD LED to be continuously lit.

B. Playback Mode

When a PLAYBACK TRG pulse is received by the Recorder Control, the PLAYBACK FF is set, causing monostable U15 to load the digits selected by the RECORD DELAY selector (RD66-RD898) into PLAYBACK DELAY CTR. At each trailing edge of DATA CLK, the PLAYBACK DELAY CTR is advanced one count, until overflow occurs (U8 pin 6 goes high) setting the READ FF. Overflow will occur when the number of pulses received by the PLAYBACK DELAY CTR equals the number selected by the RECORD DELAY switch. This also generated RECORD STOP, which causes the contents of the ADDRESS COUNTER to be loaded into a 10-BIT REGISTER on the Display Control. This register is used for oscilloscope trigger generation during the playback mode.

When the READ FF sets, U9 pin 12 disables ADDR CLK, preventing the ADDRESS COUNTER on the Display Control from advancing on DATA CLK edges. The READ FF also triggers monostable U22 pin 12, which resets the LATCH ENBL FF, removing LATCH ENBL, which disables the outputs of the tri-state latches on the Quad Records. After the 2 μ S pulse at U22 pin 12, the R/W FF is set, removing WE, which disables the write cycle of the 8K RAM's and enables their output drivers, preparing for a read cycle. The 2 μ S delay between the LATCH ENBL and WE transitions ensures that at no time are the outputs of both the memories and the tri-state latches enabled at the same time - this prevents possible destruction of their output drivers.

When the R/W FF is set, the READ CLOCK is enabled (U13 pin 4 held the READ CLOCK disabled during the record mode in order to prevent additional ADDR CLK

pulses). The READ CLOCK and its associated monostables generate timing pulses as shown in Fig. 2 - Playback Mode Timing Diagram. At each positive edge of ADDR CLK, the ADDRESS COUNTER is advanced one count, allowing access of a new data word from memory. The \overline{CE} pulse, generated by the READ PULSE monostables, accesses the word from memory. Each word, as it is placed onto the memory I/O lines, is applied to the inputs of the 4-to-1 multiplexers (U13-U16) on the Quad Recorders. The OUTPUT SELECT switch selects one of the four inputs (decoded by gates on the Recorder Control) and applies the data word to the DAC on the Quad Recorders. The DAC (U17) converts the data to an analog voltage and applies it to the selected channel of an external scope. When the DISPLAY PULSE monostable on the Recorder Control generates its pulse, NEG INTENSIFY and POS INTENSIFY pulses are generated, allowing the analog information to be visible on the scope. The READ CLOCK, \overline{CE} , DISPLAY PULSE, and ADDR CLK signals repeat indefinitely as shown in the timing diagram. With each READ CLOCK cycle, a new word is accessed from memory, converted, and displayed on the scope, while level changes are blanked out.

The oscilloscope trigger pulse is generated by circuitry on the Display Control. A binary number corresponding to the position of the DISPLAY DELAY switch (DD64-DD896) is added to the outputs of the 10-BIT REGISTER in a binary ADDER (U6-U7). This result is then compared to the contents of the ADDRESS COUNTER, which is advancing at each ADDR CLK pulse. When the two are equal, that is, when the ADDRESS COUNTER reaches a count of the memory location of the final word recorded plus a delay count, the A=B output of the COMPARATOR (U8-U10) goes high, triggering the GAP WIDTH monostable, which, in turn, triggers a second monostable, generating TRG, which triggers the oscilloscope. The RETRACE signal is used on the Recorder Control to hold the READ CLOCK reset, preventing the ADDRESS COUNTER from advancing while the scope retraces and prepares for a new trigger. A TRG pulse is generated for each 1024 counts of the ADDRESS COUNTER, always occurring at the same memory location. If the DISPLAY DELAY selector is set at "0," the output of the ADDER is simply the contents of the 10-BIT REGISTER, so the TRG pulse occurs at the last word recorded. Note that when LATCH ENBL is low, the RETRACE and TRG signals are inhibited. This turns off the scope display during the record mode.

Another COMPARATOR (U11-U13) compares the outputs of the ADDRESS COUNTER

and 10-BIT REGISTER. The A=B output of this comparator goes high when they are equal, that is, at the memory location of the last word recorded. The comparator triggers monostable U15, which generates MARKER and $\overline{\text{MARKER}}$. These signals are used on the Recorder Control to provide additional intensity modulation on the scope, causing a bright dot to appear on the trace, indicating the start of "real time." The marker can be switched off by the START MARKER switch, which grounds the CLR pin of U15, inhibiting MARKER and $\overline{\text{MARKER}}$.

During the playback mode, the READ CLOCK output is used to trigger monostable U21 pin 1. This retrIGGERABLE monostable causes the PLAYBACK LED to light continuously. The U11-6 pulses applied to U12 pin 9 during the record mode are inhibited by U11 pin 5, causing the RECORD LED to extinguish during the playback mode.

To return to the record mode, the DISPLAY RESET button is depressed, resetting the PLAYBACK FF on the Recorder Control. This triggers monostable U18 at pin 1, setting the DECADE COUNTER to a count of 9, which readies it for start of a digitization process. At the end of this pulse, U18 pin 9 is triggered, resetting the READ FF. This triggers monostable U22 at pin 1, which clears the R/W FF, causing $\overline{\text{WE}}$ to disable the output drivers of the RAM's on the Quad Recorders and enable their write cycles. After the 2 μ S pulse at U22 pin 13, the LATCH ENBL FF is set, enabling the outputs of the tri-state latches. Again, this delay ensures the protection of the memory and tri-state latch output drivers.

C. Bar Graph Driver

The Bar Graph Driver is designed to provide the necessary signals to drive Burroughs self-scan gas discharge bar graph displays. For details on theory of operation and use, refer to the Burroughs BG16101-2 data sheet and Bulletin number BG101B Applications Notes.

The bar graph displays operate on the glow-transfer principle. The bar driver applies anode current to a keep-alive segment, which is continually glowing. The ionization voltage of the adjacent reset segment is thereby lowered. The anodes of all 100 segments and the reset segment of each bar graph are connected, and every third cathode of each bar graph are connected.

To start a scan, the anode voltage of a bar graph is raised, and a ground is applied to the reset cathode ($\emptyset R$ CATHODE), ionizing the reset segment, which causes it to glow. This lowers the ionization voltage of the next segment. A $\emptyset 1$ CATHODE pulse ionizes that segment, lowering the ionization voltage of the next segment. A $\emptyset 2$ CATHODE pulse ionizes that segment. This process continues, with alternating $\emptyset 1$, $\emptyset 2$ and $\emptyset 3$ CATHODE pulses causing the glow to be transferred up the bar graph. The Signetics NE580 provides the necessary cathode pulses to implement this process.

The length of the bar graph is determined by the ANALOG IN VOLTAGE. The NE580 produces a staircase ramp wave (pin 9) which reaches maximum value (2.5V) when 100 $\emptyset 1$ - $\emptyset 3$ CATHODE pulses have been produced. This implies that the 100 element bar graph has maximum height when ANALOG IN/4 voltage is 2.5V, or ANALOG IN = 10V. If ANALOG IN voltage is less than 10V, a comparator turns on the anode driver transistor, lowering the anode voltage such that the bar graph segments can no longer ionize (the comparators for channels 1 and 2 are located on the NE580). Thus, segments are ionized until the RAMP voltage is greater than the ANALOG IN/4 voltage; then the anode voltage is lowered and glow is no longer transferred. After 100 cathode pulses, the NE580 generates a $\emptyset R$ CATHODE pulse, allowing another scan to begin. An external timing capacitor sets the scan rate to 70 Hz, producing a flicker-free display.

V. Calibration Procedures

The following procedures are suggested for periodic calibration of the Recorder/Display System.

A. Quad Recorder

One adjustment is required on the Quad Recorder boards. The REF ADJ potentiometer for the DAC (U17) should be adjusted such that REF IN voltage (U17 pin 14) is $5.000V \pm 1mV$.

B. Bar Graph Driver

One adjustment is required on the Bar Graph Driver board. The VREF pot for the NE580 should be adjusted such that VREF (U6 pin 7) is $2.5 \pm 0.01V$.

C. Recorder Control

Display pulse timing and scope intensity have adjustment capability. VR8 must be set such that output frequency of the READ CLOCK (U5 pin 3) is 100 KHz. VR1 should be set such that the READ PULSE (U16 pin 13) is 9.0 μ S wide. VR2 should be set such that U17 pin 5 is a 3.0 μ S pulse. VR3 should be set such that the DISPLAY PULSE (U17 pin 13) is a 5.6 μ S pulse.

VR4 and VR5 control the intensity of the signal and marker dots, respectively, for positive blanking scopes. VR6 and VR7 perform the same functions for negative blanking scopes. These adjustments are best made by visual inspection of the scope trace.

D. Display Control

No adjustments are required on the Display Control board.

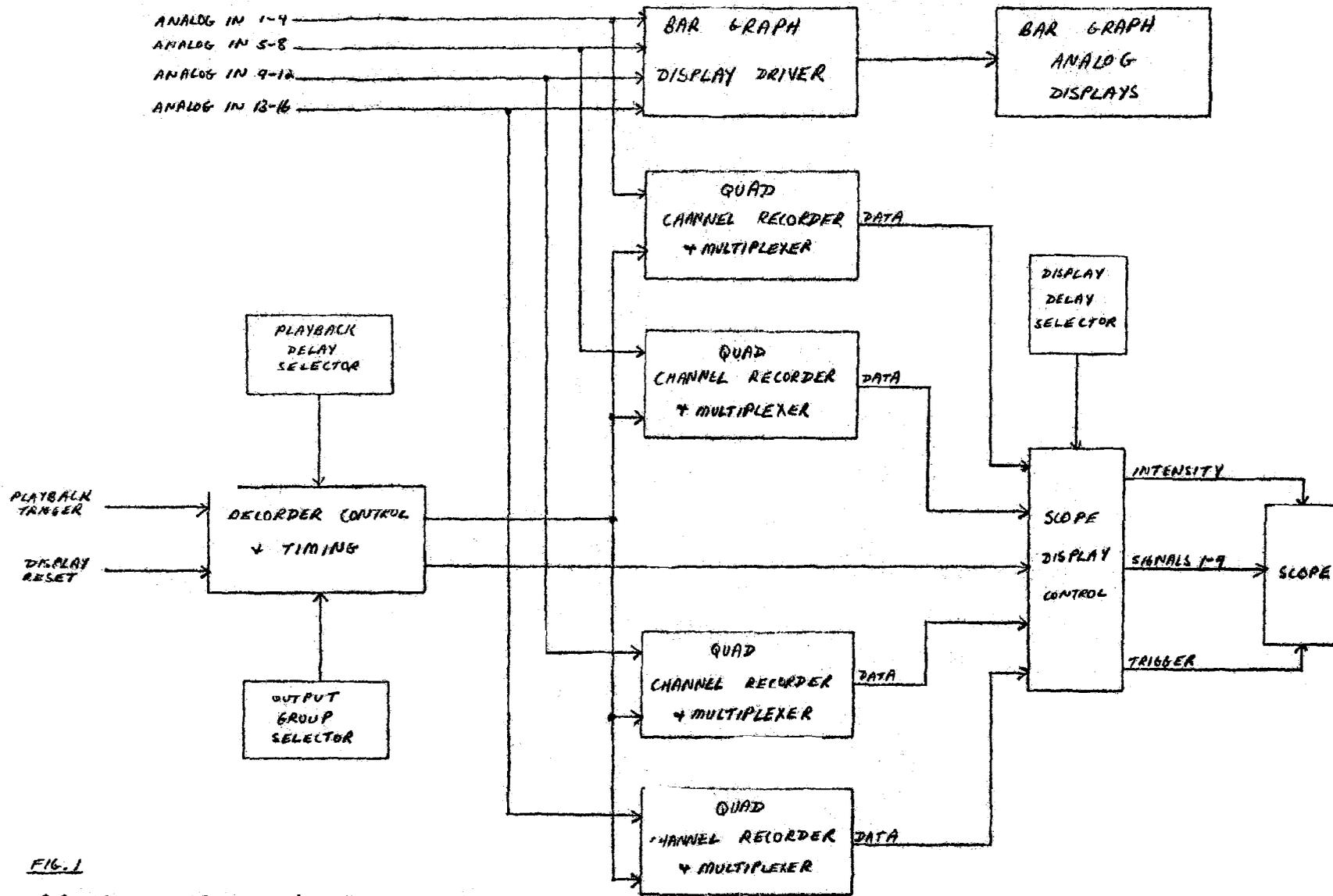
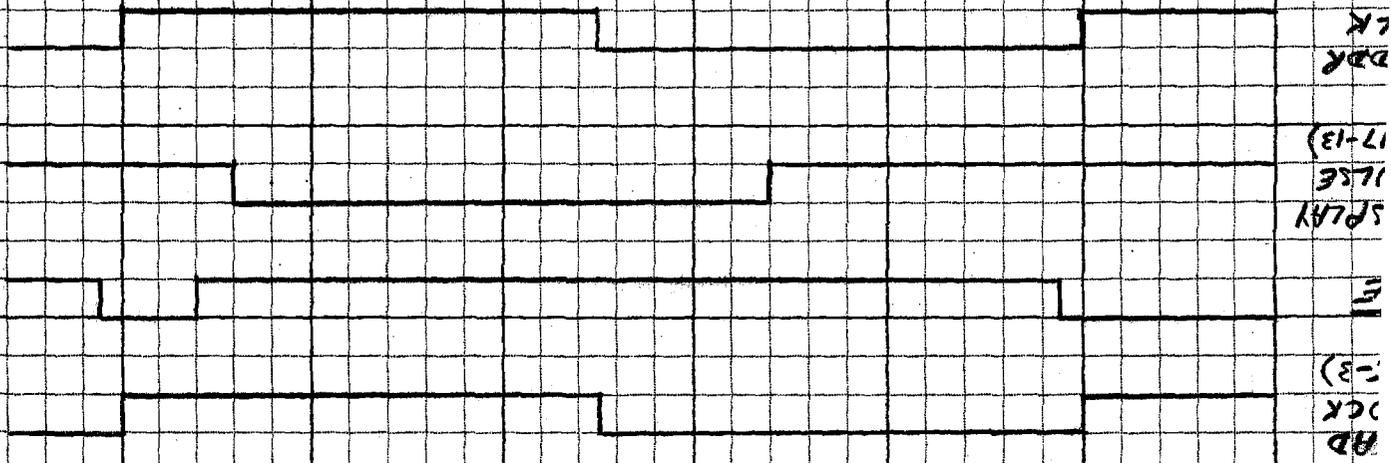


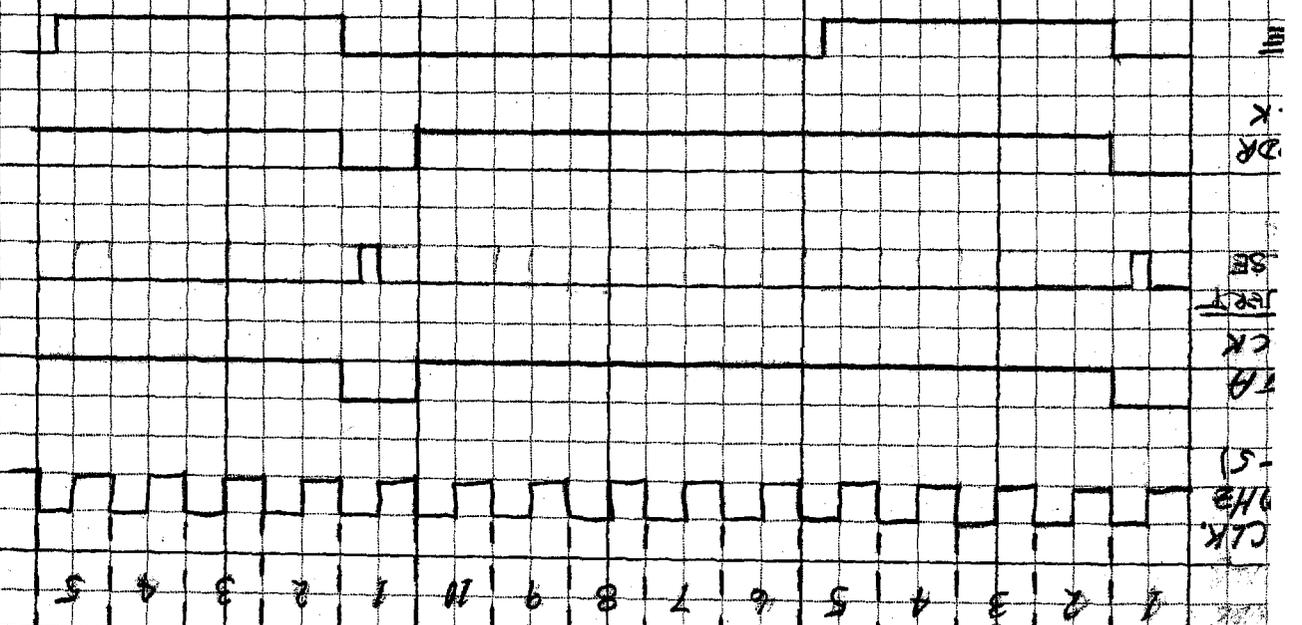
FIG. 1

P.A. CASCODE RECORDER / DISPLAY SYSTEM
BLOCK DIAGRAM

FIG. 2 - RECORDER/DISPLAY SYSTEM TIMING DIAGRAMS

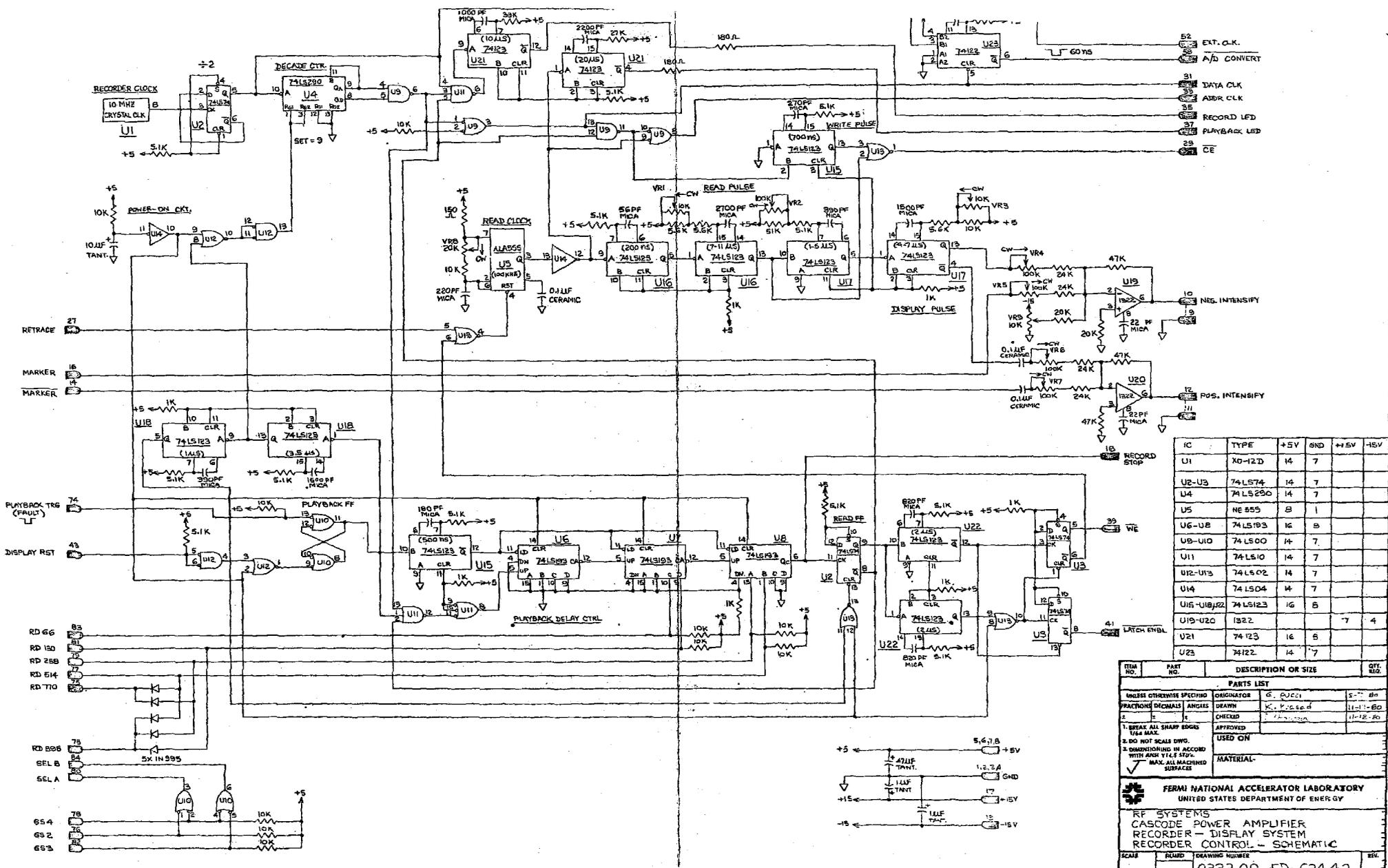


PLAYBACK MODE (400ns/div)



RECORD MODE (100ns/div)

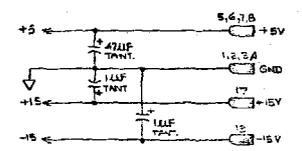
1 2 3 4 5 6 7 8 9 10 1 2 3 4 5



- 52 EXT. CLK.
- 53 A/D CONVERT
- 31 DATA CLK
- 32 ADDR. CLK
- 35 RECORD LED
- 37 PLAYBACK LED
- 29 CE

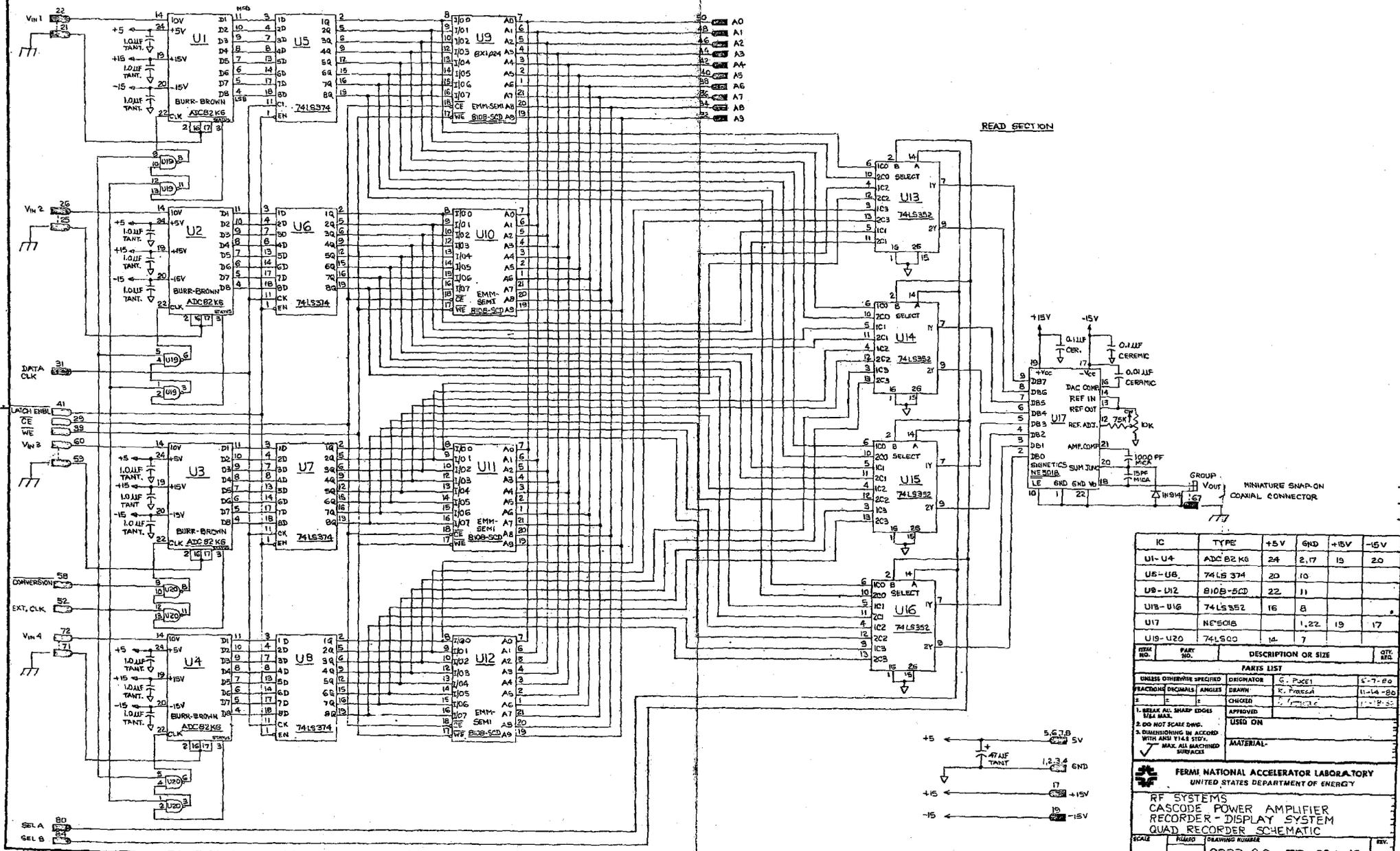
IC	TYPE	+5V	GND	+5V	-5V
U1	X0-12D	14	7		
U2-U3	74LS74	14	7		
U4	74LS290	14	7		
U5	NE 555	8	1		
U6-U8	74LS193	16	8		
U9-U10	74LS00	14	7		
U11	74LS10	14	7		
U12-U13	74LS02	14	7		
U14	74LS04	14	7		
U15-U18/22	74LS123	16	8		
U19-U20	1522			7	4
U21	74123	16	8		
U23	74122	14	7		

ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY.	REQ.
PARTS LIST				
UNLESS OTHERWISE SPECIFIED		ORIGINATOR	G. GUCCI	5-78
FRACTIONAL DECIMALS	ANGLES	DRAWN	K. P. S. S. S.	11-1-80
1		CHECKED		11-12-80
1. BREAK ALL SHARP EDGES VISA MAX.		APPROVED		
2. DO NOT SCALE DWG.		USED ON		
3. DIMENSIONING IN ACCORD WITH ASME Y14.5M-80.		MATERIAL		
FERMIL NATIONAL ACCELERATOR LABORATORY				
UNITED STATES DEPARTMENT OF ENERGY				
RF SYSTEMS CASCADE POWER AMPLIFIER RECORDER - DISPLAY SYSTEM RECORDER CONTROL - SCHEMATIC				
SCALE	PLUMED	DRAWING NUMBER	REV.	
		0333.00-ED-634 42		



WRITE SECTION

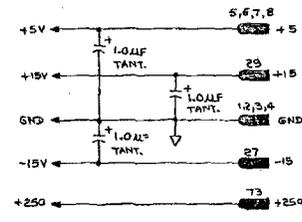
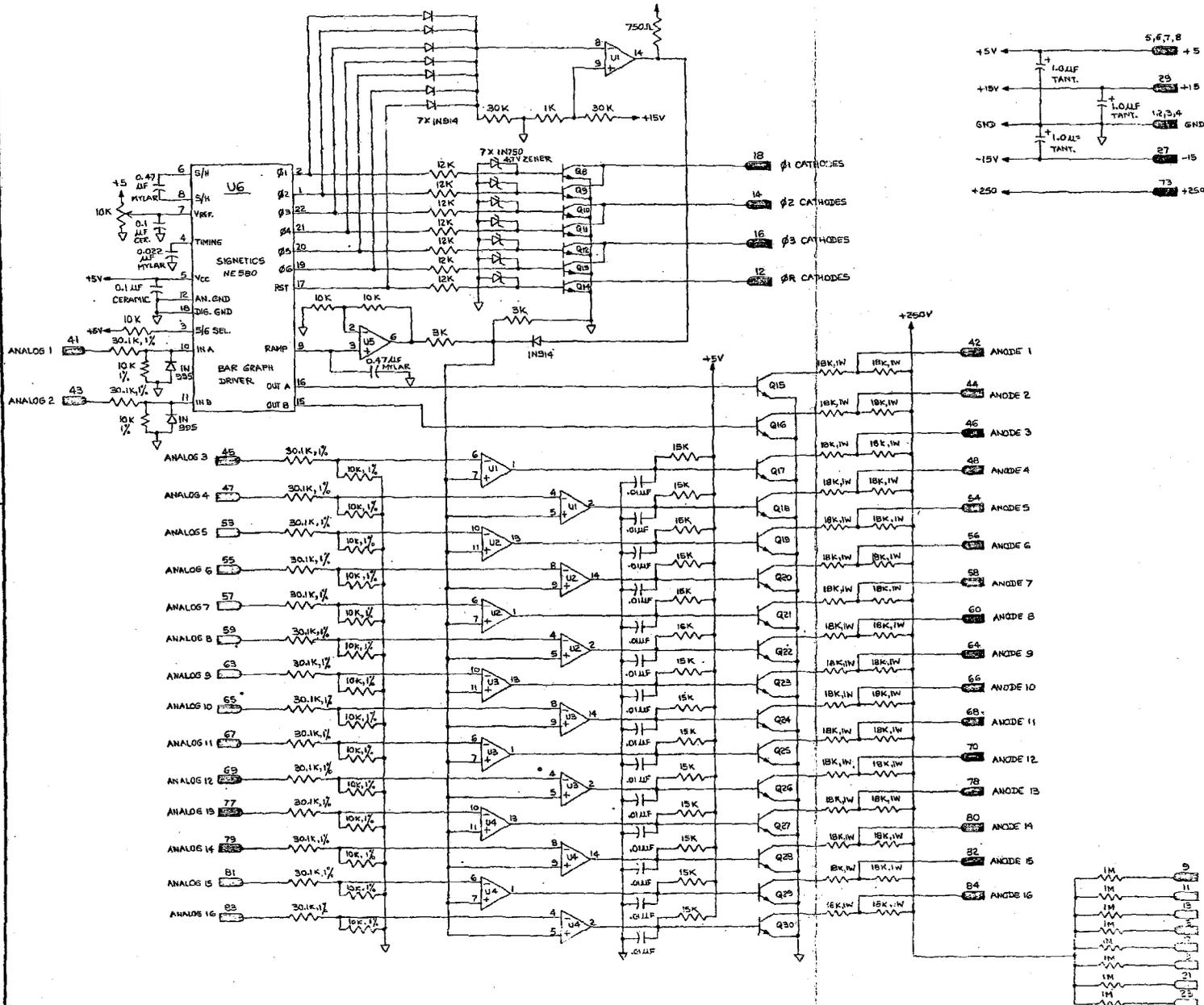
READ SECTION



IC	TYPE	+5V	GND	+15V	-15V
U1-U4	ADC 82 K6	24	2,17	15	20
U5-U8, U9-U12	74LS 374	20	10		
U13-U16	74LS 352	16	8		
U17	NE5016		1,22	19	17
U18-U20	74LS 50	14	7		

ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY.	REV.
PARTS LIST				
UNLESS OTHERWISE SPECIFIED		DRAWN BY	S. PACEI	5-7-80
FRACTIONAL DIMENSIONS		DESIGNED BY	R. FORTZA	11-14-80
1		CHECKED BY		11-18-80
1. BREAK ALL SHARP EDGES 3/16" MAX.		APPROVED BY		
2. DO NOT SCALE DIMS.		USED ON		
3. DIMENSIONING IN ACCORD WITH ANSI Y14.5 STD.		MATERIAL		
4. MAKE ALL MACHINED SURFACES				

FERMI NATIONAL ACCELERATOR LABORATORY
 UNITED STATES DEPARTMENT OF ENERGY
RF SYSTEMS
CASCADE POWER AMPLIFIER
RECORDER-DISPLAY SYSTEM
QUAD RECORDER SCHEMATIC
 SCALE: _____ FILLED: _____ DRAWING NUMBER: _____ REV: _____
0333.00-ED-634-43



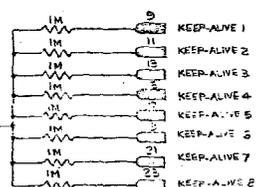
IC	TYPE	+5V	GND	+15V	-15V
U1-U4	LM339		12	3	
U5	741		7	4	
U6	NE 580	5	12, 18		

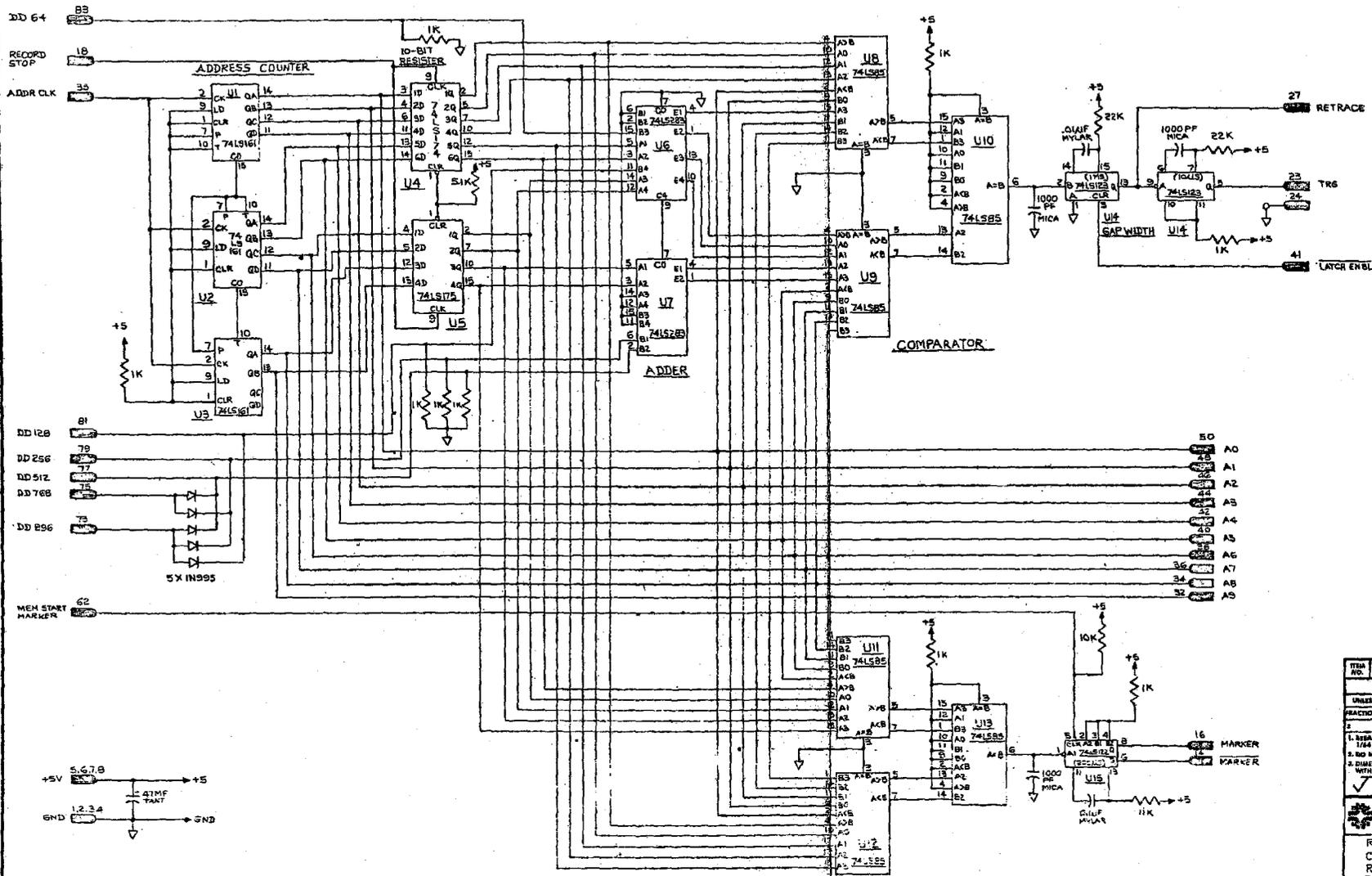
ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY. REQ.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED	ORIGINATOR	QTY. REQ.	
FRACTIONS DECIMAL	ANGLES	DRAWN	1-7-80
1. BREAK ALL SHARP EDGES 1/64 MAX.	CHECKED		1-7-80
2. DO NOT SCALE DWG.	APPROVED		1-7-80
3. DIMENSIONS IN ACCORD WITH ANSI Y14.5 STD.	USED ON		
✓ MAX. ALL MACHINED SURFACES	MATERIAL:		

FERMI NATIONAL ACCELERATOR LABORATORY
 UNITED STATES DEPARTMENT OF ENERGY

RF SYSTEMS
 CASCADE POWER AMPLIFIER
 RECORDER-DISPLAY SYSTEM
 BAR GRAPH DRIVER

SCALE: FILMED DRAWING NUMBER: **0333.00-ED-63446** REV.





IC	TYPE	+5V	GND
U1-U3	74LS161	16	8
U4	74LS174	16	8
U5	74LS175	16	8
U6-U7	74LS283	16	8
U8-U13	74LS85	16	8
U14	74LS123	16	8
U15	74LS122	14	7

ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED	ORIGINATOR	D. P. JOE	5-7-80
REACTIONS DIMENSIONS	ANGLE	K. F. REAS	11-11-80
1	CHECKED		
2	APPROVED		
1. BREAK ALL SHARP EDGES 1/16" MAX.			
2. NO NOT SCALE DIMS.			
3. DIMENSIONING IN ACCORD WITH ASMT. & STD. MAX. ALL MACHINED SURFACES			
MATERIAL			
FERMILAB FERMILAB NATIONAL ACCELERATOR LABORATORY UNITED STATES DEPARTMENT OF ENERGY			
RF SYSTEMS CASCADE POWER AMPLIFIER RECORDER - DISPLAY SYSTEM DISPLAY CONTROL SCHEMATIC			
SCALE	PLotted	DRAWING NUMBER	REV.
		0233.00-ED-23449	

