Fermilab

TM-835
2822.000

MESON SUPERCONDUCTING MAGNET ENERGY DUMP SYSTEM

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INTRODUCTION

This paper describes an energy dump system for use with superconducting magnets when used as external beam line components.

PROBLEM

Previous energy dump schemes needed an inductance which continuously passed the magnet current of up to 4500 amperes. In addition the dump resistor could only be placed on the power supply side of the reversing switch. This reversing switch requirement is necessary to beam line magnet systems.

SOLUTION

The described dump system, shown in Figure I, overcomes both of these problems. An air core inductor is used and because it passes current only for the few seconds of a dump, a 1/4" copper rod conductor is sufficient. The circuit is such that the dump resistor can be placed on the magnet side of the reversing switch and thereby protect the magnet if a faulty switch opens with current flowing.

CIRCUIT OPERATION

During operation of the superconducting magnet, the state of the system is shown in Figure II. The magnet current flows from power supply (+), through the magnet (s), through SCR_r, and back to power supply (-). The current through the dump resistor is zero as the voltage across the magnet is zero. C_d is discharged, and C_c is charged with 550^V (V_{cc})

When SCR_c is fired, this charge will reverse bias SCR_r for the required 250μ sec so that it will turn off reliably and force the magnet current through the dump resistor R_d. The purpose of C_d is to limit the $dv/_{dt}$ that SCR_r sees as the current is diverted through R_d. L_d limits the current through R_d during the reverse bias of SRC_r. The short and long term waveforms are shown in Figure IX.

DETAILED ANALYSIS

Figure III shows our system model and its state before the dump sequence starts. The power supply is driving current through the magnet via the run SCR's (SRC_r). A closer look (figure I) shows six (6) SCR's in parallel, each with sharing resistors. C_c is charged with a voltage V_{cc}, C_d is discharged, and $i_{cl}= 0$ in the commutation loop. Also, note that $i_d= 0$ in L_d (dump inductance) and R_d (dump resistor) as the voltage across the superconducting magnet = 0^V.

The dump is initiated when the gate pulses are removed from SCR_r and SCR_c is fired. Figure IV shows the model used to study the commutation loop current buildup. Initially i_m is flowing thru SCR_r . Then with a slope of $(V_{cc} - V_{cd}) \div L_c$, i_{cl} increases to i_m . L_c is included in the loop to prevent abrupt changes in i_{cl} ($\frac{di}{dt}$ <100A/μs). At first $V_{cd} = 0$, but as i_{cl} continues to flow V_{cc} decreases as V_{cd} increases with the polarity shown in Figure IV. When $i_{cl} = i_m$, SCR becomes reversed baised and another model must be considered.

Figure VII is a graphical display of loop current and capacitor voltage for different values of loop inductance and capacitance. With a commutation voltage of 550^V, an L_c = 8μh limits $\frac{di}{dt}$ thru SCR_c to 69 amps/μs. This is 69% of the maximum condition to achieve long industrial life ($\geq$ 20 years).

Figure V is the model used to analyze the system for SCR_r reversed biased. The analysis is straighfoward if the magnet is modeled as a current source with $i = i_m$. This is valid for times that are small compared to L_m/R_d.

Figure IX shows the voltages and currents of interest that are generated by the model when the actual component values are used. At the instant SCR_r becomes reversed biased, the voltage across it jumps to a maximum and then decays as a function of the capacitance and the magnet current. As C_c discharges, C_d charges and SCR_r becomes forward biased. If the reverse bias period was more than 250μ sec it won't conduct. The C_d charges up and the current through the dump resistor increases to its maximum value of i_m. Note that this happens in 5 m sec which is relatively small compared to the magnet-dump resistor time constant (.675 sec).

Figure VIII shows the effect that varying the capacitance will have on the time of reverse bias for SCR_r. To guarantee commutation, this time must be in excess of 250μs. Hence, for i_m = 4500 amp, L_c = 8μh, C_c = 16,000μf, and C_d = 6400μf the duration of the reverse bias will be a conservative 383μ sec.

The simple model shown in Figure VI is adequate for a long term study on the dump voltage as all other system time constants are relatively short. Figure IX shows this dump voltage

EXPERIMENTAL RESULTS

The picutres in Figure X of the SCR_r and R_d voltages during a dump sequence shows a good approximation to Figure IX and its calculated waveforms.

The table below demonstrates that the predicted values of ΔT_{rb} (reverse bias) are longer than the measured ones.

I Magnet	ΔT (calculated)	ΔT (measured)
2000 A	750 μs	720 μs
2500 A	650 μs	600 μs
3000 A	560 μs	500 μs
3500 A	500 μs	440 μs

The top picture also shows an overshoot when the SCR is reverse biased. This can be explained by i_{c1} increasing to more then $i_m(0)$ due to the charge carriers that must be swept out of the junctions of SCR_r during the process of reversing the bias.

Figure XI shows pictures of the dump voltage with and without a magnet quench. Note the fast decay of the quench photo as compared to a non-quench. This is due to the increasing resistance in the magnet as the quench propagates.

The author received a great deal of assistance in this project from:

John Dinkel explained the operation of the original dump scheme and was a source of parts to get the project off to a fast start.

Paul Czarapata helped with his knowledge of programming the PDP-10 for the analysis of the system.

Terrance O'Brien made the greatest contribution by building and debugging the system.

And in addition many other people at the Meson Lab, Energy Doubler and Accelerator.

<u>References</u>: (For the detailed analysis)

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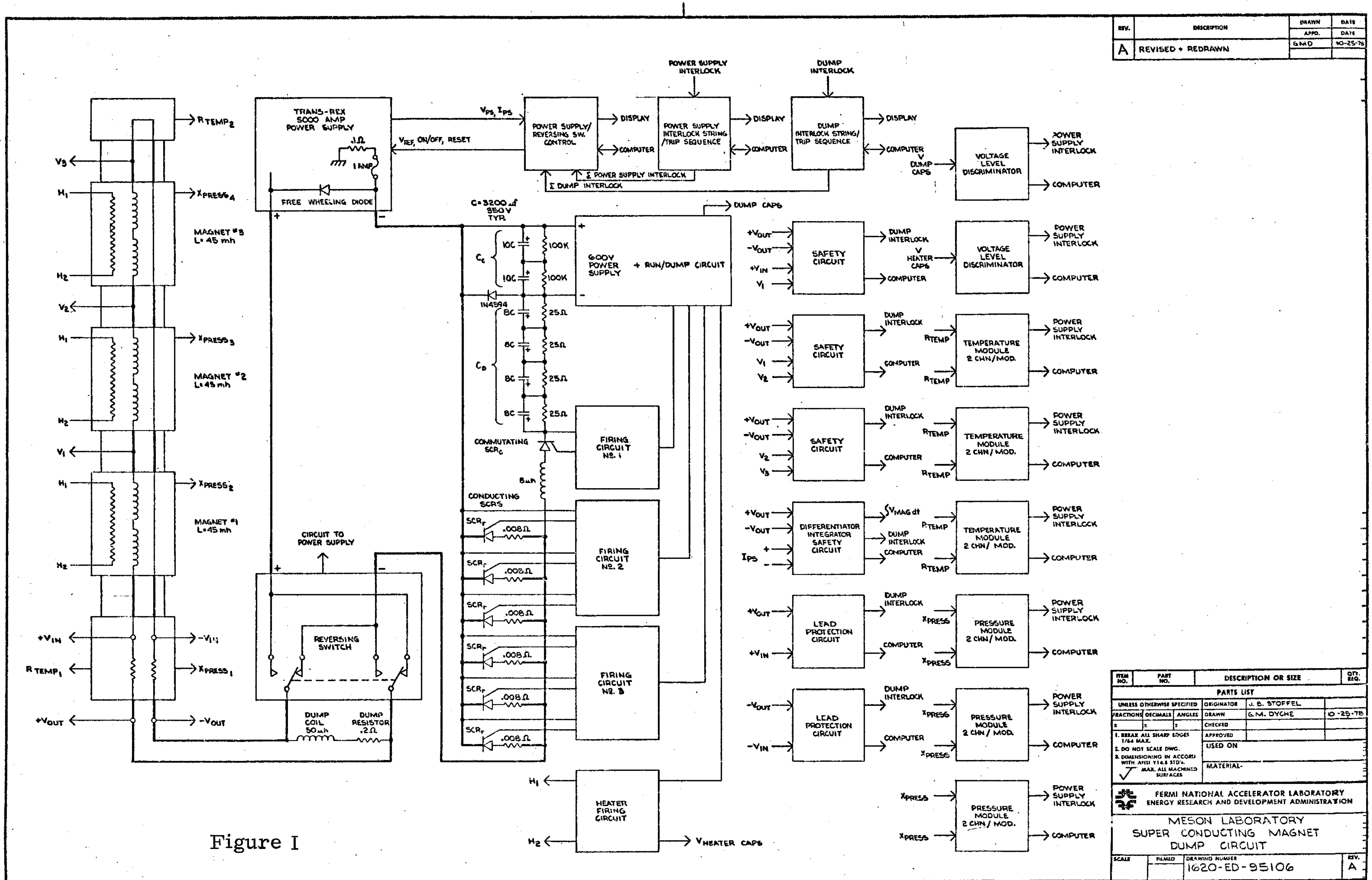

REV. | DESCRIPTION | DRAWN | DATE | APPD. | DATE
A | REVISED + REDRAWN | GMD | 10-25-78
TRANS-REX 5000 AMP POWER SUPPLY
.1Ω
1 AMP
FREE WHEELING DIODE
V_{PS}, I_{PS}
V_{REF}, ON/OFF, RESET
POWER SUPPLY INTERLOCK
DUMP INTERLOCK
POWER SUPPLY/ REVERSING SW. CONTROL
POWER SUPPLY INTERLOCK STRING /TRIP SEQUENCE
DUMP INTERLOCK STRING/ TRIP SEQUENCE
DISPLAY
COMPUTER
Σ POWER SUPPLY INTERLOCK
Σ DUMP INTERLOCK
R_{TEMP_2}
V_3
H_1
H_2
X_{PRESS_4}
MAGNET #3 L= 45 mh
V_2
X_{PRESS_3}
MAGNET #2 L=45 mh
V_1
X_{PRESS_2}
MAGNET #1 L=45 mh
$+V_{IN}$
$-V_{IN}$
R_{TEMP_1}
X_{PRESS_1}
$+V_{OUT}$
$-V_{OUT}$
CIRCUIT TO POWER SUPPLY
REVERSING SWITCH
DUMP COIL 50 μh
DUMP RESISTOR .2Ω
C=3200 μf 350V TYP.
C_c
10C
100K
1N4594
8C
25Ω
C_D
600V POWER SUPPLY + RUN/DUMP CIRCUIT
DUMP CAPS
COMMUTATING SCR_C
8μh
CONDUCTING SCRS
SCR_F
.008Ω
FIRING CIRCUIT No. 1
FIRING CIRCUIT No. 2
FIRING CIRCUIT No. 3
HEATER FIRING CIRCUIT
$V_{HEATER\ CAPS}$
V DUMP CAPS
V HEATER CAPS
VOLTAGE LEVEL DISCRIMINATOR
POWER SUPPLY INTERLOCK
SAFETY CIRCUIT
DIFFERENTIATOR INTEGRATOR SAFETY CIRCUIT
$\int V_{MAG}\,dt$
I_{PS}
LEAD PROTECTION CIRCUIT
R_{TEMP}
TEMPERATURE MODULE 2 CHN/MOD.
X_{PRESS}
PRESSURE MODULE 2 CHN/MOD.
ITEM NO. | PART NO. | DESCRIPTION OR SIZE | QTY. REQ.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
ORIGINATOR J. B. STOFFEL
DRAWN G.M. DYCHE 10-25-78
CHECKED
APPROVED
USED ON
MATERIAL
FRACTIONS DECIMALS ANGLES
1. BREAK ALL SHARP EDGES 1/64 MAX.
2. DO NOT SCALE DWG.
3. DIMENSIONING IN ACCORD WITH ANSI Y14.5 STD's.
MAX. ALL MACHINED SURFACES
FERMI NATIONAL ACCELERATOR LABORATORY
ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
MESON LABORATORY
SUPER CONDUCTING MAGNET
DUMP CIRCUIT
SCALE | FILMED | DRAWING NUMBER 1620-ED-95106 | REV. A

Figure I

SIMPLIFIED SYSTEM OVERVIEW

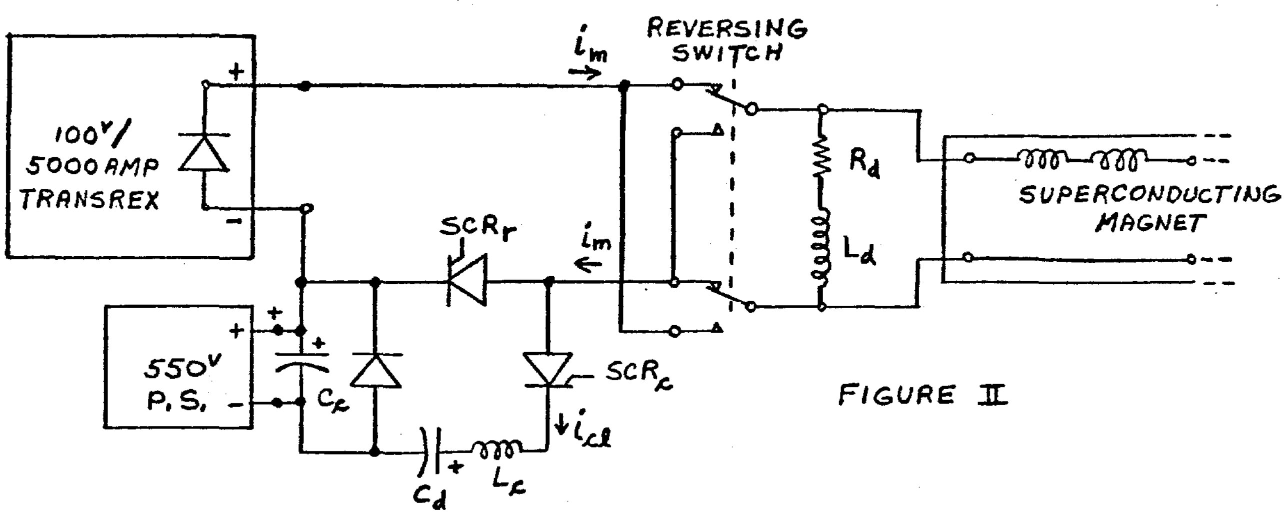

FIGURE II

R_d = DUMP RESISTOR

L_d = DUMP INDUCTANCE

C_c = COMMUTATION CAP.

i_m = MAGNET CURRENT

i_{cl} = COMMUTATION LOOP CURRENT

C_d = DUMP CAPACITOR

SCR_c = COMMUTATION SCR

SCR_r = CONDUCTION SCR

L_c = COMMUTATION INDUCTANCE

CONDUCTION MODEL

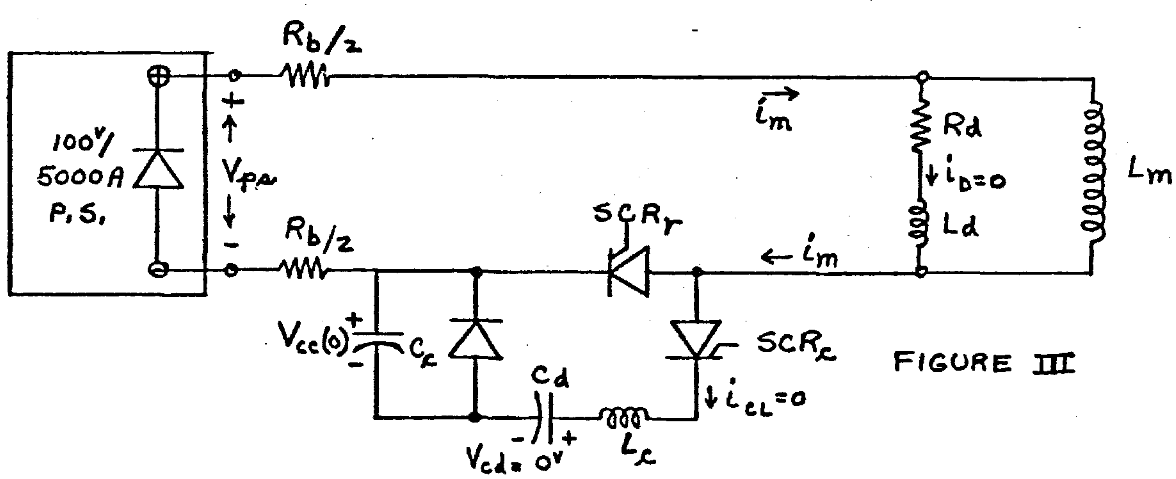

FIGURE III

L_m = MAGNET INDUCTANCE

R_b = BUSS RESISTANCE

i_d = CURRENT THRU R_d

V_{ps} = POWER SUPPLY VOLTAGE

$V_{cc}(0)$ = INITIAL VOLTAGE ON C_c

$V_{cd} = 0^V$

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SUBJECT: FIGURE IV

NAME | DATE | REVISION DATE

COMMUTATION LOOP CURRENT BUILDUP MODEL

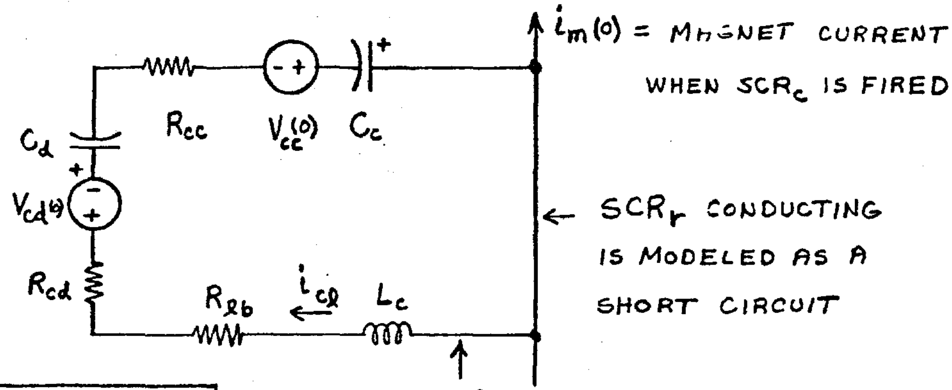

FIGURE IV

R_{cc} = RESISTANCE OF C_c R_{cd} = RESISTANCE OF C_d

R_{lb} = RESISTANCE OF LOOP BUSS

$V_{cc}(0)$ = INITIAL VOLTAGE ON C_c $V_{cd}(0)$ = INITIAL VOLTAGE ON C_d

FOR THE CURRENT BUILDUP MODEL:

$$i_{cl}(t) = \frac{(V_{cc}(0) - V_{cd}(0))}{\omega L_c} e^{-\alpha t} \sin \omega t$$

$$v_{cc}(t) = V_{cc}(0) - \frac{(V_{cc}(0) - V_{cd}(0))}{C_c\, \omega} \sqrt{\frac{L_c}{C}} \sin(\omega t + \beta) - L_c C$$

$$v_{cd}(t) = V_{cd}(0) + \frac{(V_{cc}(0) - V_{cd}(0))}{C_d\, \omega} \sqrt{\frac{L_c}{C}} \sin(\omega t + \beta) + LC$$

WHERE $C = \frac{C_c \times C_d}{C_c + C_d}$ $R = R_{cc} + R_{cd} + R_{lb}$

$\alpha = \frac{R}{2L_c}$ $\omega = \left(\frac{1}{L_c C} - \frac{R^2}{4L_c^2}\right)^{1/2}$ $\beta = \tan^{-1}\frac{\omega}{\alpha} - \pi$

AS THE UNDERDAMPED CASE $\left(\frac{1}{LC} > \frac{R^2}{4L^2}\right)$ IS THE ONE OF PRACTICAL INTEREST

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SUBJECT: FIGURES V AND VI

NAME

DATE | REVISION DATE

SCR_R REVERSED BIASED MODEL

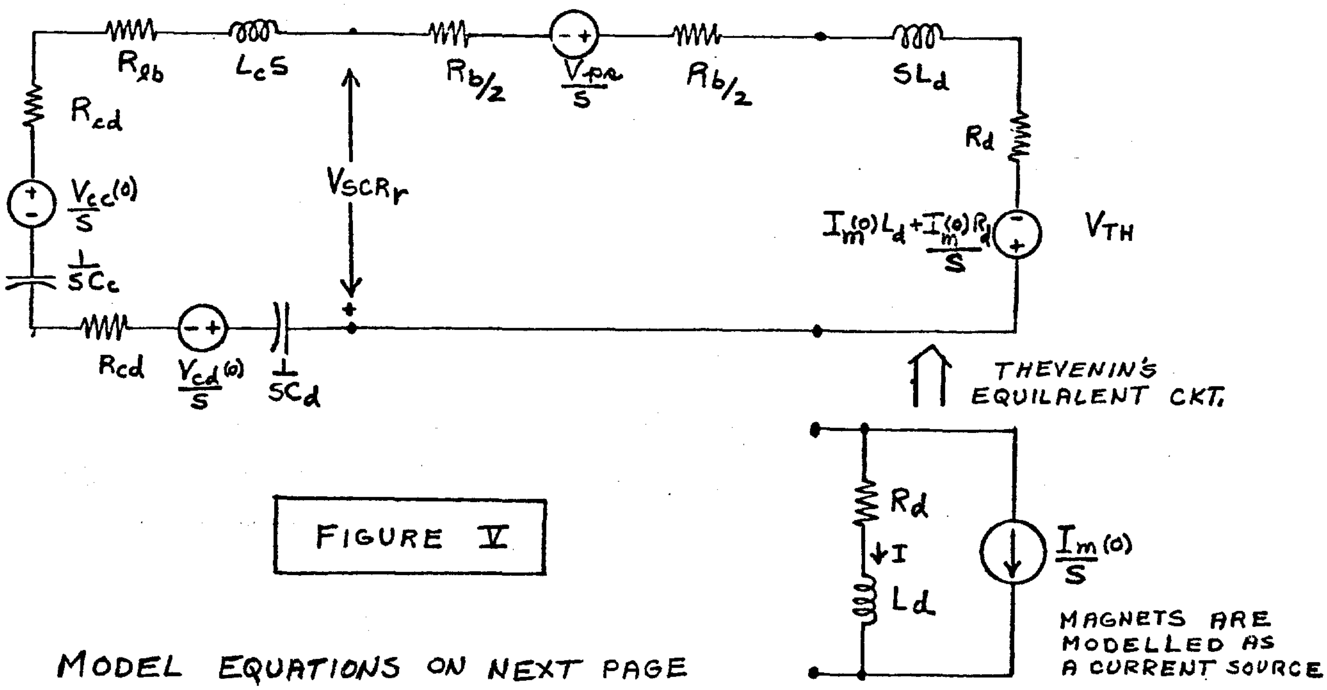

FIGURE V

MODEL EQUATIONS ON NEXT PAGE

LONG TERM DUMP MODEL

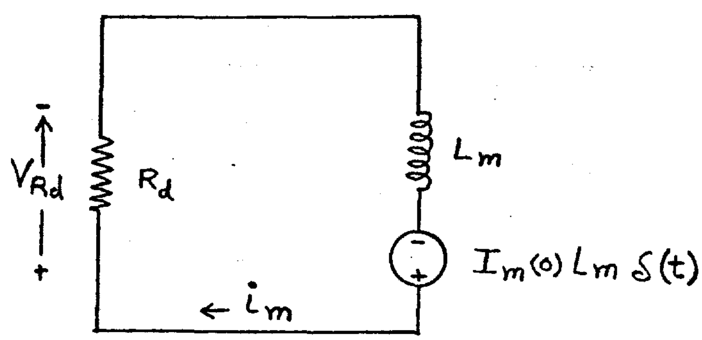

FIGURE VI

$$i_m(t) = I_m(0)\, e^{-t\frac{R_d}{L_d}}$$

$$V_{R_d}(t) = R_d\, i_m(t)$$

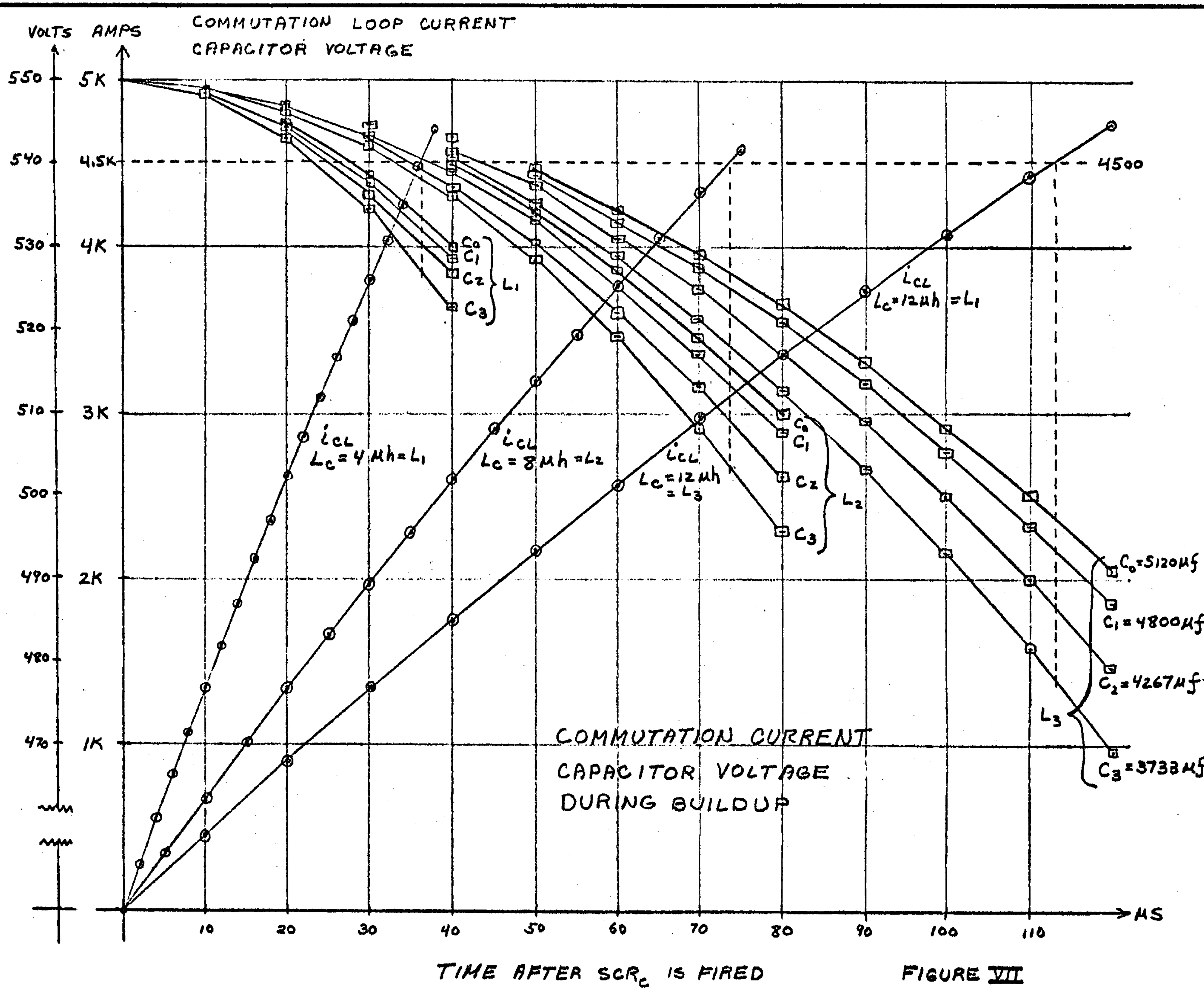

FIGURE VII

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FIGURE VII

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SUBJECT: FIGURE VIII

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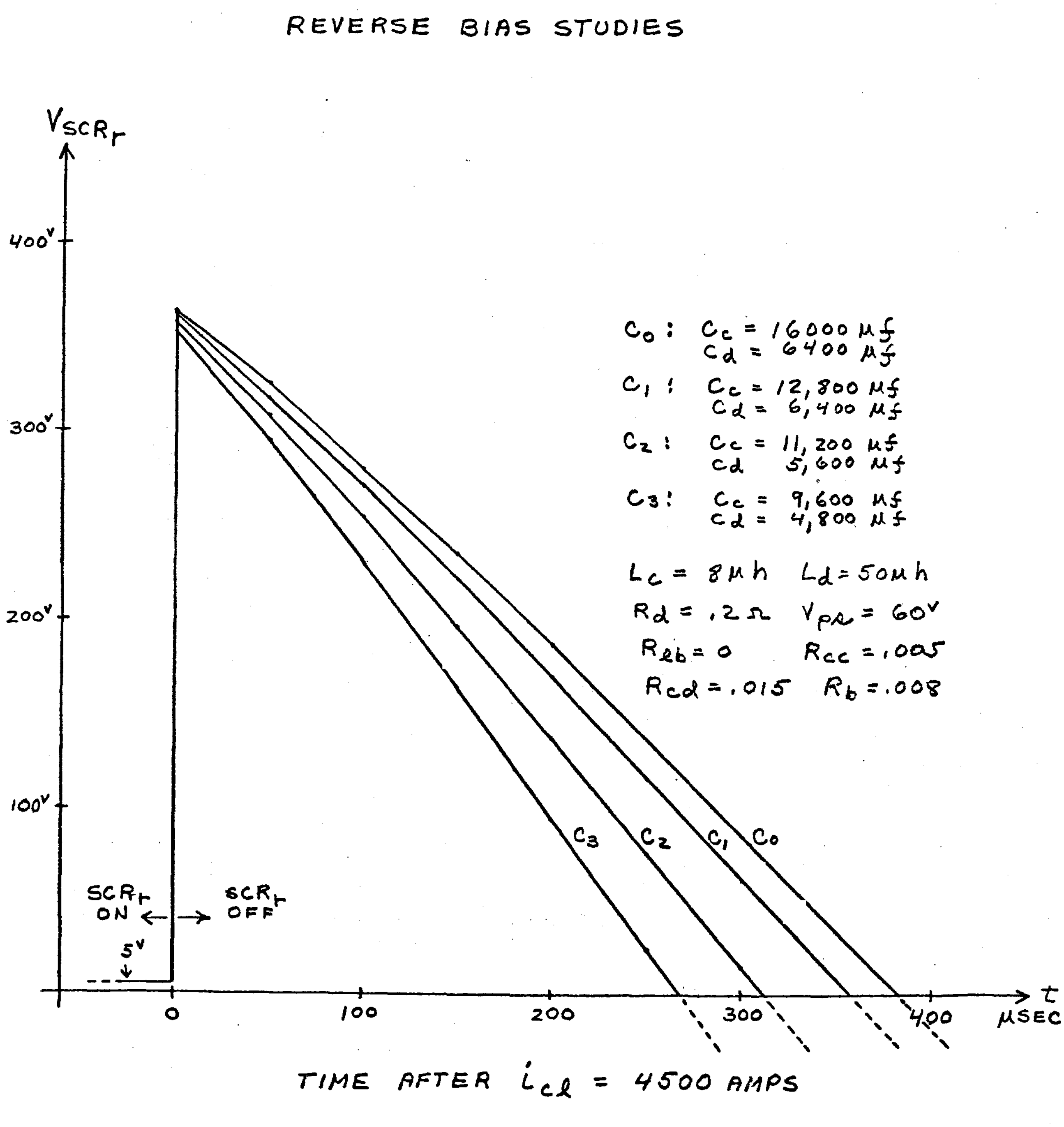

FIGURE VIII

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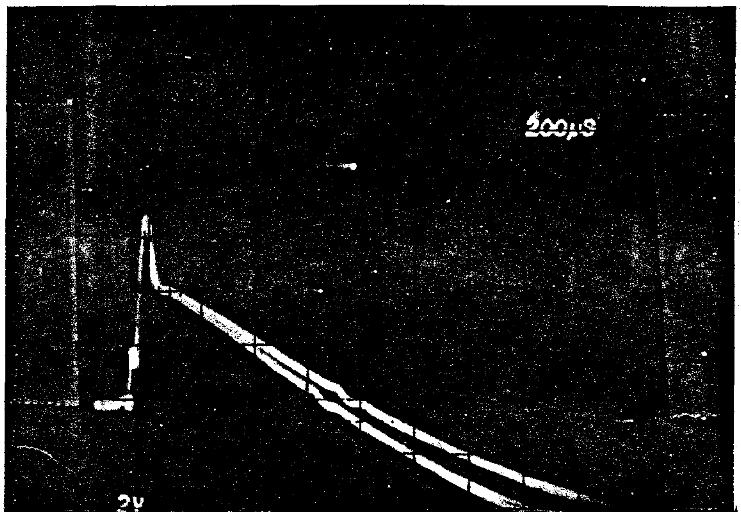
SUBJECT	NAME	
FIGURE X		
	DATE	REVISION DATE



8-8-78 3000A

UPPER $I_m(0)$ = 2000 AMPS

LOWER $I_m(0)$ = 2500 AMPS

V_{SCR_r} (REV BIAS) 200V/DIV

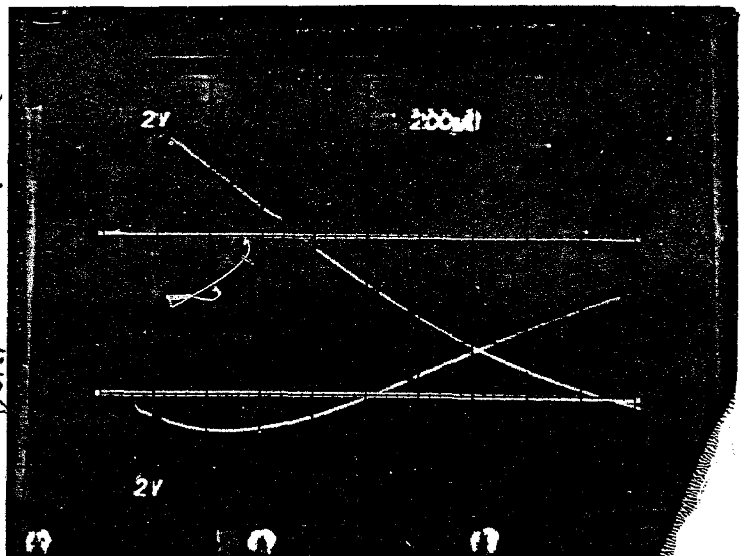
→ 200µS/DIV

$\Delta T(RB) = 720\ \mu S$ @ $I_m(0) = 2000\ A$

$\Delta T(RB) = 600\ \mu S$ @ $I_m(0) = 2500\ A$

VSCR

VDUMP



8-8-78 3450

V_{SCR_r} 200V/DIV

→ 200µS/DIV

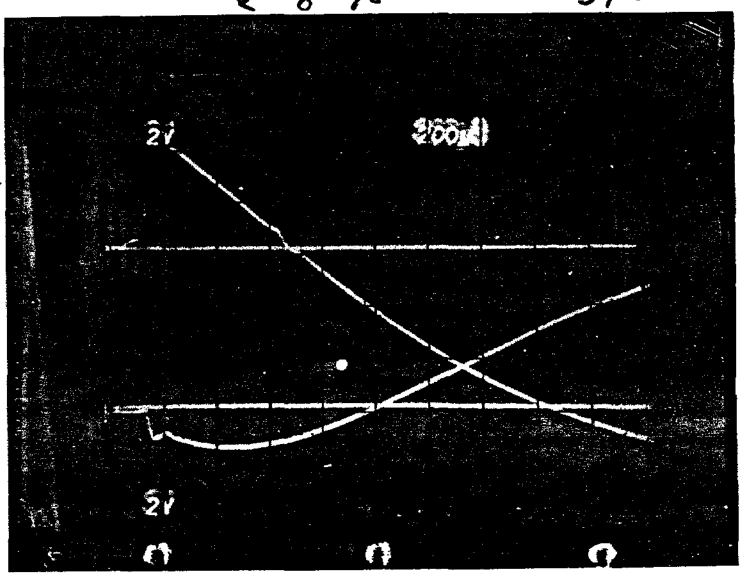
V_{Rd} 200V/DIV

→ 200µS/DIV

$\Delta T(RB) = 500\ \mu S$ @ $I_m = 3000\ A$

VSCR

VDUMP



QUENCH

V_{SCR_r} 200V/DIV

→ 200µS/DIV

V_{Rd} 200V/DIV

→ 200µS/DIV

$\Delta T(RB) = 440\ \mu S$ @ 3500A

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SUBJECT: FIGURE XI

NAME

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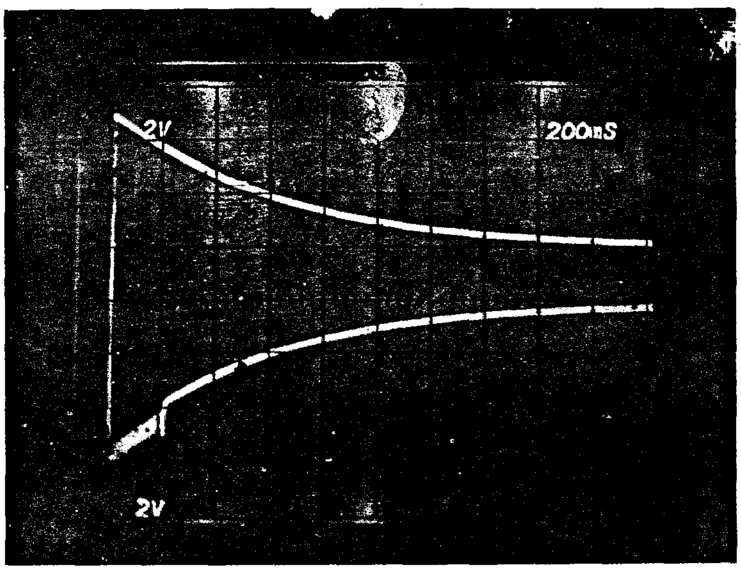
MAGNET NOT QUENCHED

6/30/78

$I_m(0) = 2000$ A



V_{Rd} (200V/DIV)

200 ms/DIV

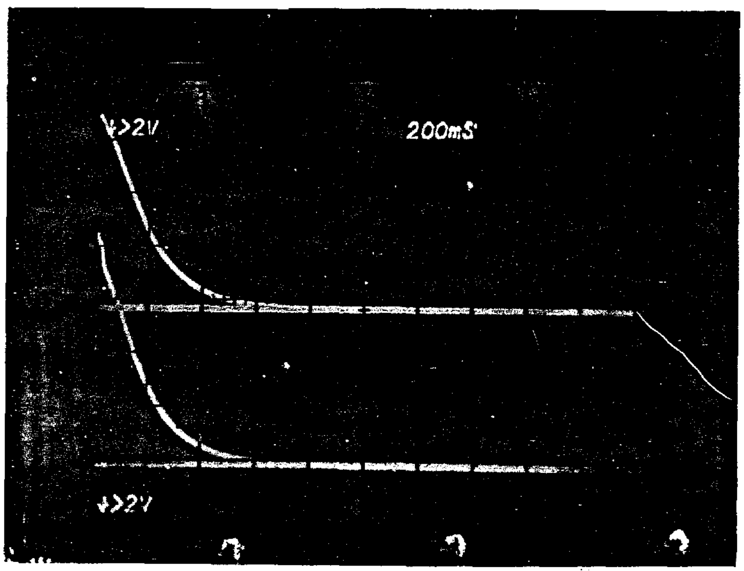
200 ms/DIV

V_{SCR_r} (FORWARD BIAS) (200V/DIV)

MAGNET QUECHED

$I_m(0) = 3500$ A

10/25/78



V_{Rd} (200V/DIV)

200 ms/DIV

V_{SCR_r} (200V/DIV)

200 ms/DIV