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NOTES ON DRIFT CHAMBER TIME DIGITIZER MEETING

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Drift chambers have become powerful detectors for high energy physics experiments since they were experimented[1] with in 1968. Rapid development of sophisticated integrated circuits with costs within reach has made these chambers very practical detectors.

Spatial accuracies better than $\sigma = 100\mu m$ have been obtained from drift chambers at CERN[2], Fermilab[3], and LBL[4]. Drift chambers are easy to construct and operate relative to multiwire proportional wire chambers (MWPC) of the same area. Generally drift chamber systems cost less than MWPC's including electronics, and provide far better spatial accuracies.

Readout systems for drift chambers have been constructed by various laboratories for specific drift spaces and accuracies. Very few systems have been utilized by experiments. At present, drift chamber electronics is mainly in the developmental stage. For measuring drift times, digital, analog and a mixture of both techniques have been experimented with.

A meeting was held at the Fermilab on February 12, 1975 to talk about the existing systems and the systems in the developmental stage. At the meeting, some important design parameters, timing accuracies, double track resolutions, total drift times, event processing times, abort times, track multiplicities, etc.,

were discussed. Discussions on these subjects were started at a meeting at LBL last May and further carried out at the Fermilab workshop[7]. We found that there has been considerable progress on the drift time digitizers since May, 1974.

At this meeting, there were few talks on experiments utilizing drift chamber systems. J. Lach (Fermilab) described the Charged Hyperon Experiment, E-97 which is planned to run at the Meson Laboratory sometime in 1975. The experiment requires 20 drift chambers of 40 x 60 cm^2 area with 1 cm drift spacing and spatial accuracies of σ = 100μm.

B. Sadoulet (LBL) talked about LBL-SLAC proposal on the $e^+e^- \rightarrow$ Hadrons experiment at SPEAR. He pointed out that some progress was made in making a few prototype drift chambers. This experiment requires cylindrical drift chambers of 1 m in diameter operating in 10-12 kG magnetic fields. They hope to obtain 100μm accuracy across 1 cm drift space. Strip or printed circuit delay lines may be used for obtaining a longitudinal coordinate with 1 cm spatial accuracy.

Another cylindrical drift chamber e^+e^- experiment is being prepared by B. Richter's group. These chambers are going to provide a momentum resolution of $\frac{\Delta P}{P} \sim 1\%$ and will replace the present spark chambers. D. L. Hartill informed us that a prototype chamber with electronics is being tested. The time digitizer provides better than 0.5 nsec accuracy with a full range of 100 nsec. The drift times are stored in shift registers and then are serially read out.

L. Sulak (Harvard) presented some data from the BNL neutrino experiment (neutral current search) using their 4 x 4 m^2 area

drift chambers. A total of 24 chambers with 5 cm drift space and 5 cm gap are used for the experiment. Deviation, $\sigma \leq 0.45$ mm was measured from straight line fit to six planes under the experimental running condition with geometric optimization. Event rate is one per 20 machine cycles in the average. Background μ's are used to calibrate the whole system.

R. Thun (University of Michigan) described the Charmed Particle Search Experiment, E-357 at Fermilab. The experiment requires a total number of 372 sense wires for 32 drift chambers. All coordinates are measured with pairs of drift chambers shifted by half a cell spacing to eliminate left-right ambiguities. Three different cell sizes are used, with 0.4, 0.6, and 1.2 inch drift spaces. Sense wire pulses are amplified and discriminated with a LRS LD 603 hybrid chip located on the chamber box. The input has a threshold of 0.5 mV across 100Ω. Signals are transmitted through ~300 nsec of RG-58 cables to LRS 2228 time-to-digital converters. All TDC's have a common start. A prototype module containing four chambers has been built and tested using 90% Argon and 10% CH_4. Spatial accuracy of $\sigma = 0.20$ mm was obtained with a narrow beam of 10^5 particles per second per cell.

In the following, we will briefly discuss accuracy requirements in drift time measurements, some problems in detecting multiple tracks from a single drift chamber cell, and we will summarize some important features of the readout systems which were presented at this meeting.

Let us consider the following simplified block diagram (Fig. 1). This diagram is chosen to make some remarks which may be relevant to drift chamber readout systems.

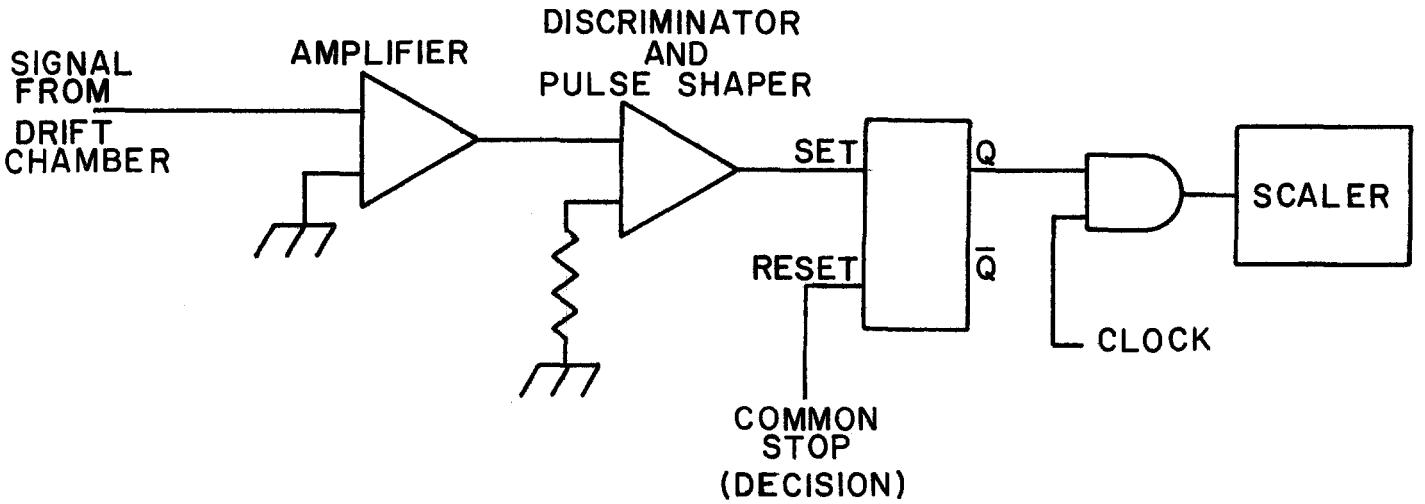
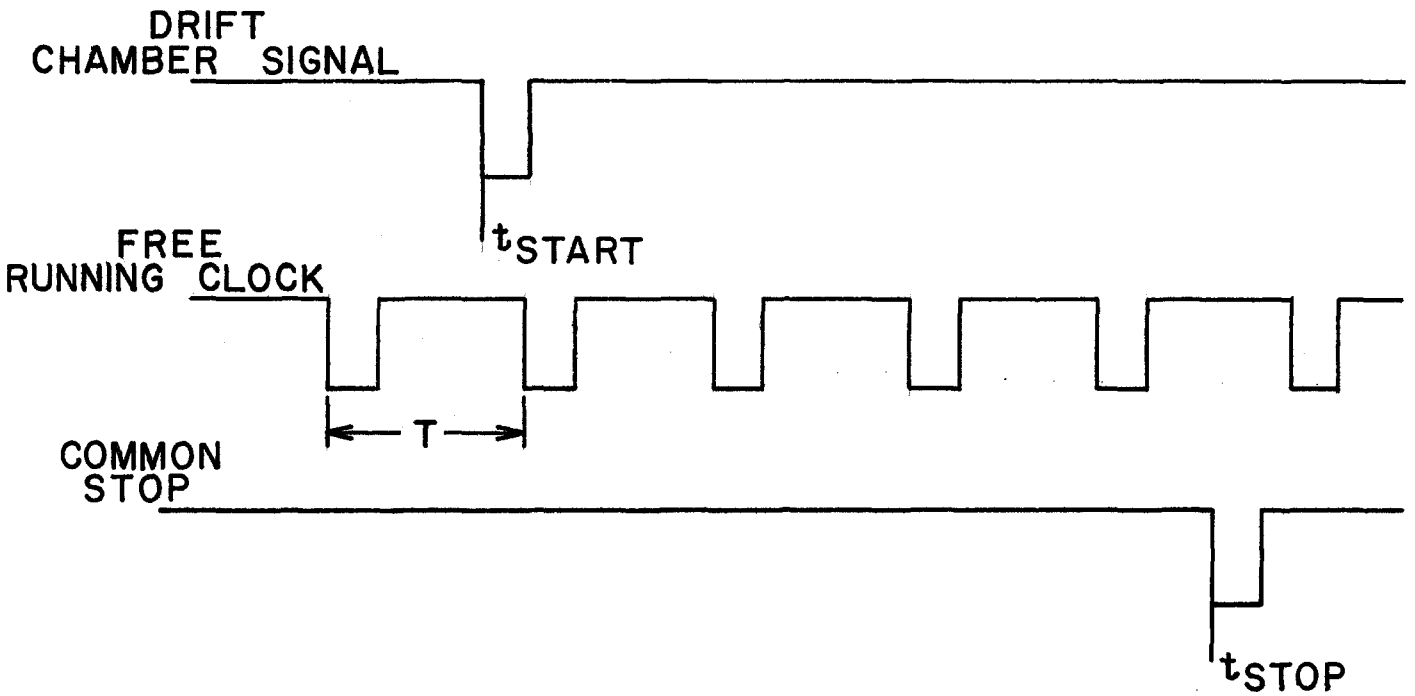


Figure 1

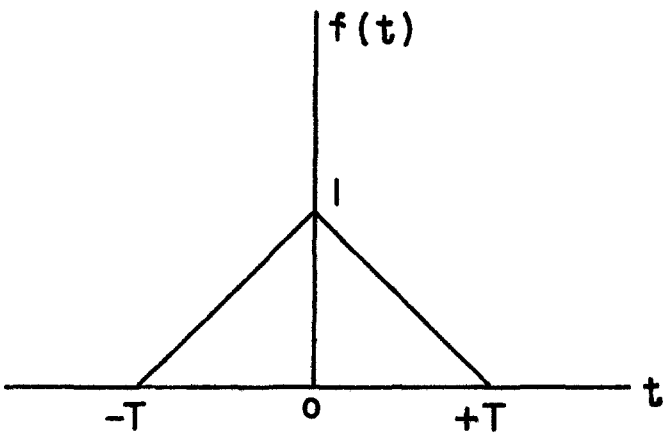
Pulses resulting from charged particle tracks are amplified and shaped by an amplifier-discriminator circuit attached to every signal wire. The amplifier-discriminator circuit should be selected to minimize time slewing due to finite drift chamber rise time and pulse height. This time jitter can be minimized by having fast rising large pulses from drift chambers and fast switching discriminators (four to 8 nsec pulse rise times and a minimum pulse height of 2-4 mV across 300Ω are achievable.)

Assume that a pulse from the drift chamber sets the flip-flop and the clock pulses are counted by the scaler until the delayed common reference pulse from the scintillator resets the flip-flop. In most cases it is advantageous to start the drift time measurement with the drift chamber signal and have a common stop. This minimizes the dead time and cable length for every sense wire. We would like to measure this time with a timing

accuracy of $\sigma \leq 2$ nsec. Let us look at the timing diagram given in Fig. 2. Consider that the clock period is T.



The maximum error in measuring $t_{sT} - t_{sP}$ is 2T. The error distribution function, f(t) is given by a triangle as shown in Fig. 3.



Thus the f(t) = 1-t.

The second moment (variance) of this error function can be written as follows,

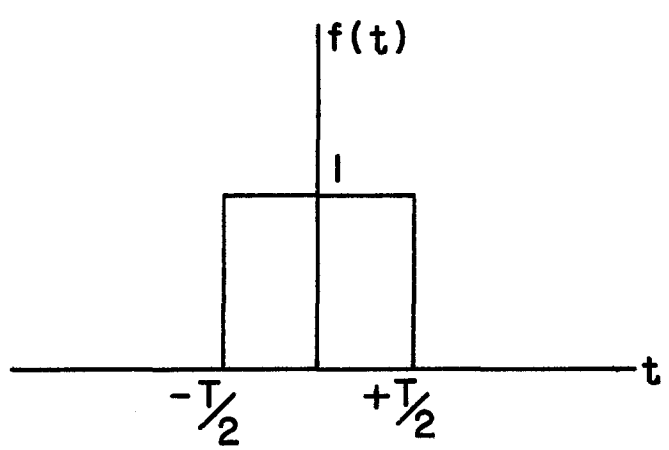
$$\sigma^2 = \frac{\int_{-T}^{T} t^2(1-t)\ dt}{\int_{-T}^{T} (1-t)\ dt}$$

For simplicity take T = 1 nsec. Then the integral yields a standard deviation of,

$$\sigma = \frac{1}{\sqrt{6}}$$

For T = 4 nsec, σ = 1.6 nsec. This corresponds to 75μm spatial error with an electron drift rate of 200 nsec/cm.

Now let us consider measuring the time between the last clock pulse and the common stop, t_{sP} very accurately. Since this measurement is common to all channels, the cost of our readout system will not be effected much (a commercial time to digital converter of 200 psec accuracy costs less than $200). Then the error distribution function becomes a square function, as shown in Fig. 4.



The second moment of this function for T = 1 nsec yields,

$$\sigma = \frac{1}{\sqrt{12}}$$

For the same example T = 4 nsec, σ = 1.2 nsec corresponds to spatial error of 60μm due to the electronics for a drift rate of 200 nsec/cm.

Assume a drift chamber accuracy of 100μm, then the total accuracy is,

$$\sigma_{Tot} = \sqrt{100^2 + 60^2}$$

The standard deviation for the whole system is σ_{Tot} = 115μm. From the logic given above, we conclude that if we measure common start or stop time (reference time) with high accuracy in principal we may not need clock periods less than T = 4 nsec with a purely digital system. This would imply that about a maximum error of 2% is acceptable in measuring drift times with an analog system for obtaining 100μm spatial accuracies.

Many experimental groups have been concerned about detecting multitracks from single sense wire consequently multitrack resolution. We would like to make some comments about this concern. We keep discriminator levels low to reduce time slewing (time over threshold). As a result of this the discriminator may fire more than once due to noise pulses on the input signal from the sense wire. We work with large electric fields to reach saturated drift velocities (complete saturation may not really exist). A consequence of this is that after-pulses may occur after the primary pulse due to long penetrating photons producing secondary

electrons. A way to prevent false tracks produced by noise pulses or after-pulses is to provide dead times of about 100 nsec with the discriminators. A result of this is that the two track resolution becomes worse than 5 mm. Thus, for high flux high multiplicity experiments, we will recommend the following:

a. Construct drift chambers of moderately small drift spacing. Chambers with 1 cm drift spacing appear to be ideal.

b. Stagger two chambers with 1 cm drift spacings. This arrangement not only resolves left-right ambiguity, it provides two track resolutions better than 5 mm. The maximum drift time is about 200 nsec with 1 cm drift spacing. This is a reasonably short time for most experiments. Cost of the readout system providing σ of 2 nsec timing accuracy is about a factor of four times less expensive compared with electronics for proportional wire chambers of 2 mm wire spacing.

c. Accept one event per wire.

In the following tables we outline the features of the drift chamber hardware discussed at this meeting as well as a few other systems known to us. Design details of the final systems may differ from the descriptions here since most are still in design or early construction. These tables are an attempt to provide a format for comparison of the different systems. Where items are not directly comparable or where exact information was not available entries are marked * to indicate they are estimates.

SYSTEM: CERN, H. Verweij

INPUT: MECL, 50 OHM

DIGITIZER: Digital Plus Delay Line Latch Vernier

TRIGGER: Common Stop, Automatic Reset on Overflow

TIME RESOLUTION: 2 ns

DOUBLE TRACK RESOLUTION: PER WIRE 3 ns*
PER MODULE 3 ns*

RUNDOWN OR PROCESSING TIME: None

ABORT TIME: None

FULL SCALE TIME: 512 ns

STABILITY: Clock

DIGITIZERS: 4 SHARED BY: 8 WIRES:

OUTPUT BUFFER: One EVENTS:

OUTPUT FORMAT: 8 Bits Hit Wire + 6 Bits Time + 4 Bits Vernier

PACKAGING: 8 WIRES IN: 2-W CAMAC

LOGIC: MECL III, MECL 10,000

POWER PER WIRE: 3 Watts*

PARTS COST PER WIRE: $100.00*

In this scheme wire signals are clipped to 3 ns width and OR'ed together to form the start signal (Fig. 5). The first signal through the OR sets the start flip-flop for the first digitizer (Fig. 6). A four bit register with a two ns delay between each input records the time between setting the start flip-flop and the first clock pulse. Succeeding clock Pulses are counted in a 125 MHz scaler until a derandomized

common stop. Setting the start flip-flop also loads a one bit per wire register, suitably timed, which is associated with the first digitizer. The first start flip-flop enables the AND gate at the input to the start flip-flop for the second digitizer. Since the input wire signals are clipped to 3 ns, which roughly matches the propagation delay through the first flip-flop, a signal pulse will activate only the first digitizer. If two wires have closely spaced pulses which may even overlap, the next digitizer will be enabled and the time suitably recorded.

Editorial Comment

This system is capable of the fastest double pulse resolution on the same wire of any of the other systems discussed here. This may be a disadvantage since after-pulsing on one wire could use up all the digitizers and block good information on another wire. Further, it is not clear that the system can ever be timed perfectly so that when signals arrive at close spacing on two different wires they may be recorded in more than one register. It would then be difficult (depending on the hit combination) to tell which wire should be associated with a digitizer. At worst this would result in reduced accuracy on a small fraction of the hits though it does require consideration in the analysis program.

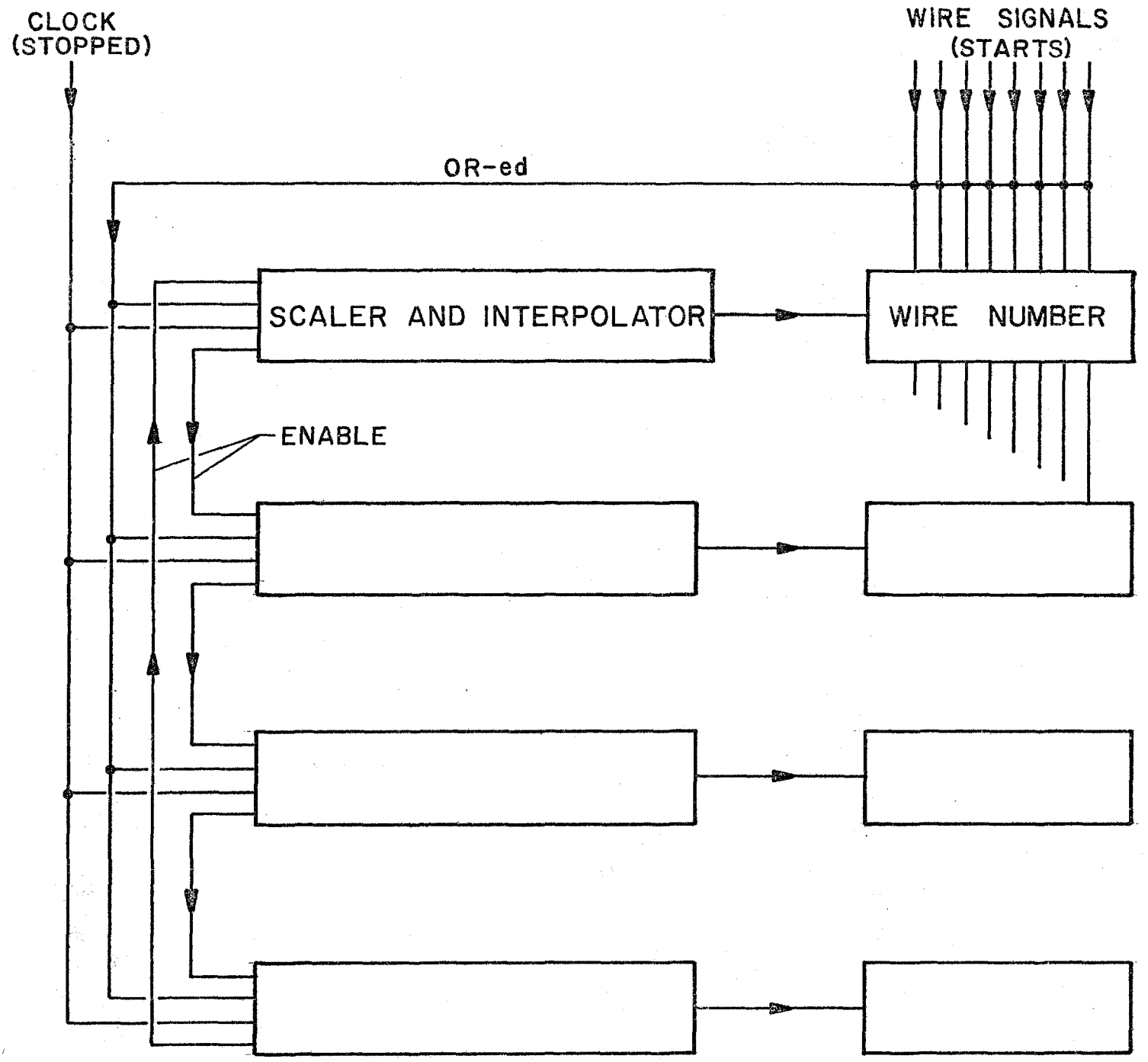
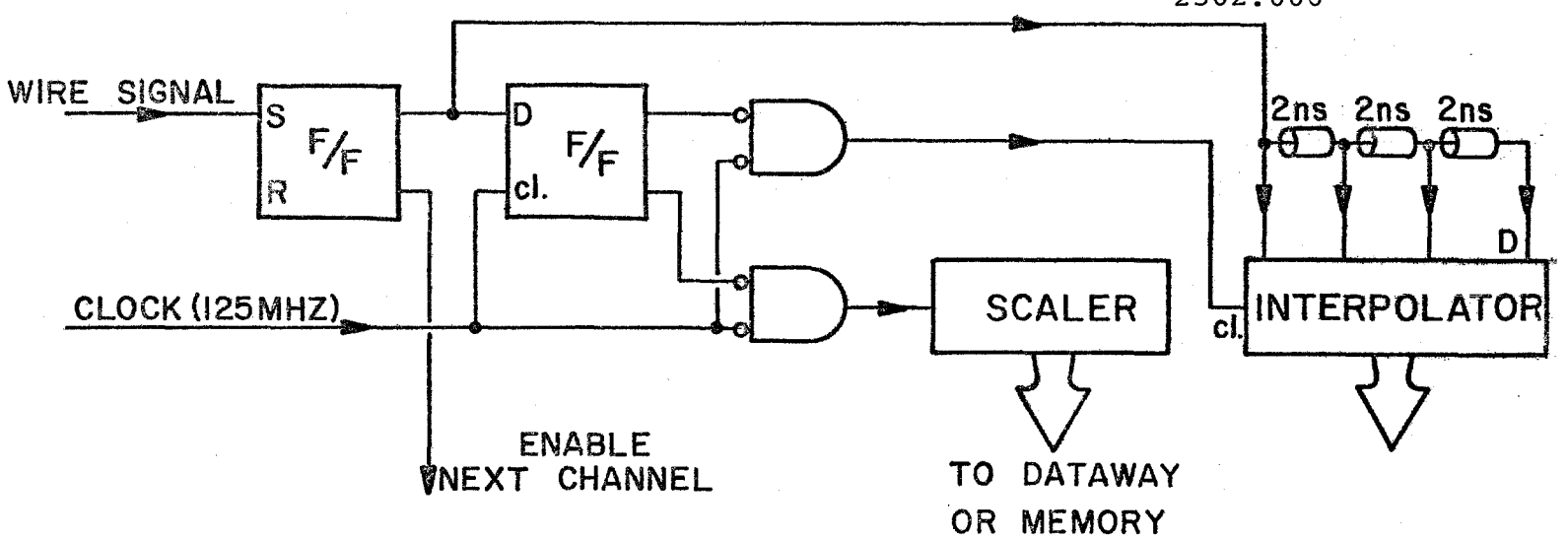
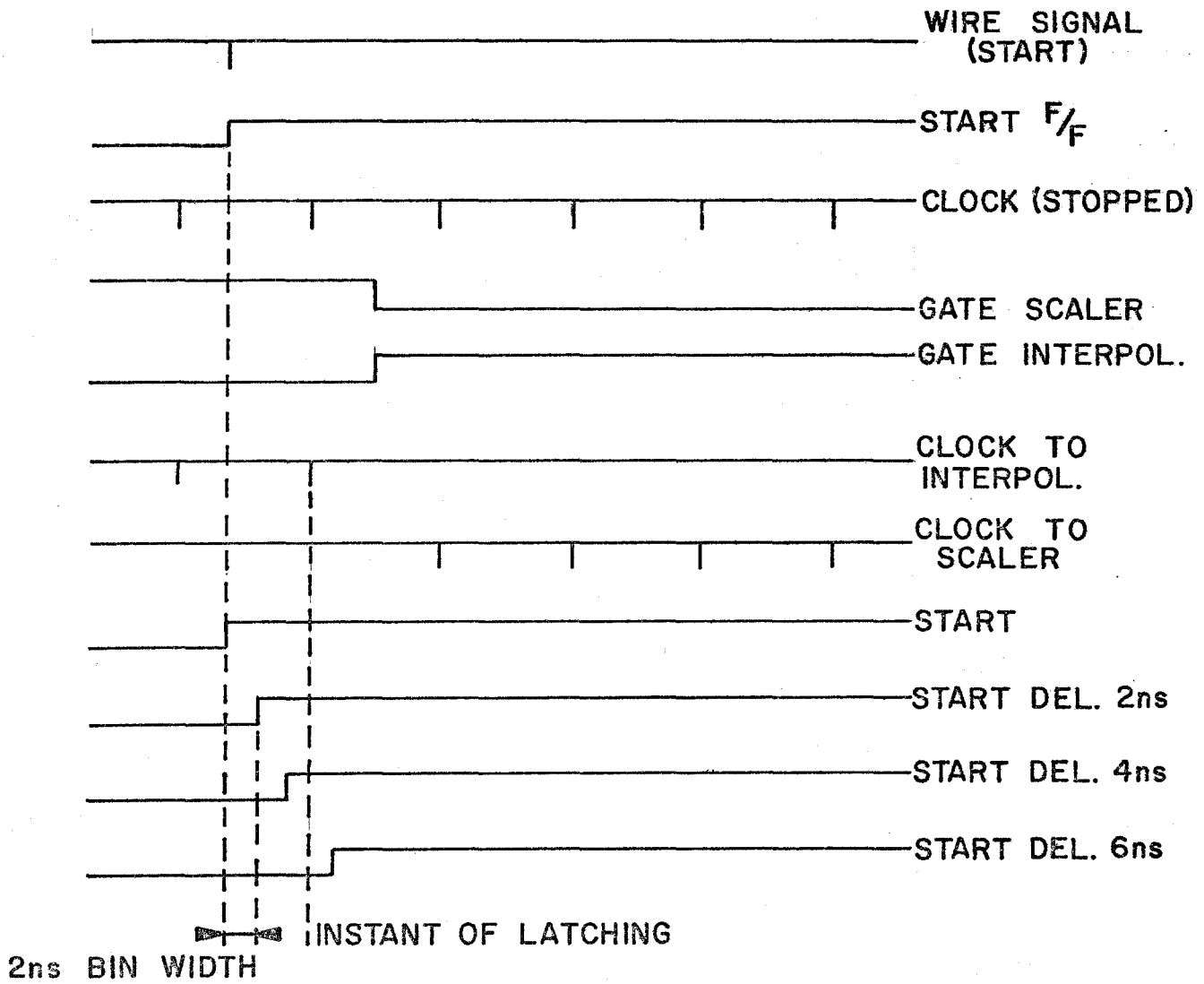


FIG. 5 FUNCTIONAL BLOCK DIAGRAM OF SHARING OR DIGITRON ARRANGEMENT


WIRE SIGNAL
S
F/F
R
D
F/F
cl.
2ns
2ns
2ns
D
CLOCK (125MHZ)
SCALER
cl.
INTERPOLATOR
ENABLE
NEXT CHANNEL
TO DATAWAY
OR MEMORY


WIRE SIGNAL
(START)
START F/F
CLOCK (STOPPED)
GATE SCALER
GATE INTERPOL.
CLOCK TO
INTERPOL.
CLOCK TO
SCALER
START
START DEL. 2ns
START DEL. 4ns
START DEL. 6ns
INSTANT OF LATCHING
2ns BIN WIDTH

SYSTEM: Columbia, W. Sippach

INPUT: MECL

DIGITIZER: Digital + Delay Line Latch Vernier

TRIGGER: Common Stop

TIME RESOLUTION: 1.6 ns

DOUBLE TRACK RESOLUTION: PER WIRE 25 ns
PER MODULE 1.6 ns

RUNDOWN OR PROCESSING TIME: None

ABORT TIME: None

FULL SCALE TIME: 1.6 Microseconds minimum (See Text)

STABILITY: Clock

DIGITIZERS: 16 SHARED BY: 8 WIRES:

OUTPUT BUFFER: 16 HITS

OUTPUT FORMAT: 6 Bit Counter + 6 Bit Vernier for Each Wire

PACKAGING: 8 WIRES IN: 1-W CAMAC-Special Bus

LOGIC: MECL 10,000

POWER PER WIRE: 5 Watts*

PARTS COST PER WIRE: $40.00

MISC: 250 8 Wire Modules Under Construction

This system (Fig. 7), contains a six bit interpolation register and a hit flip-flop for each of eight wires. When an incoming wire pulse sets its associated flip-flop the contents of the interpolation clock(s) are stored in a six bit latch. At the next major clock cycle (25 ns) the 8 bit flip-flop states, the contents of the 8 six bit interpolation registers, and the contents of a six bit major clock counter are all stored in a 16 word circulating buffer. Each time a

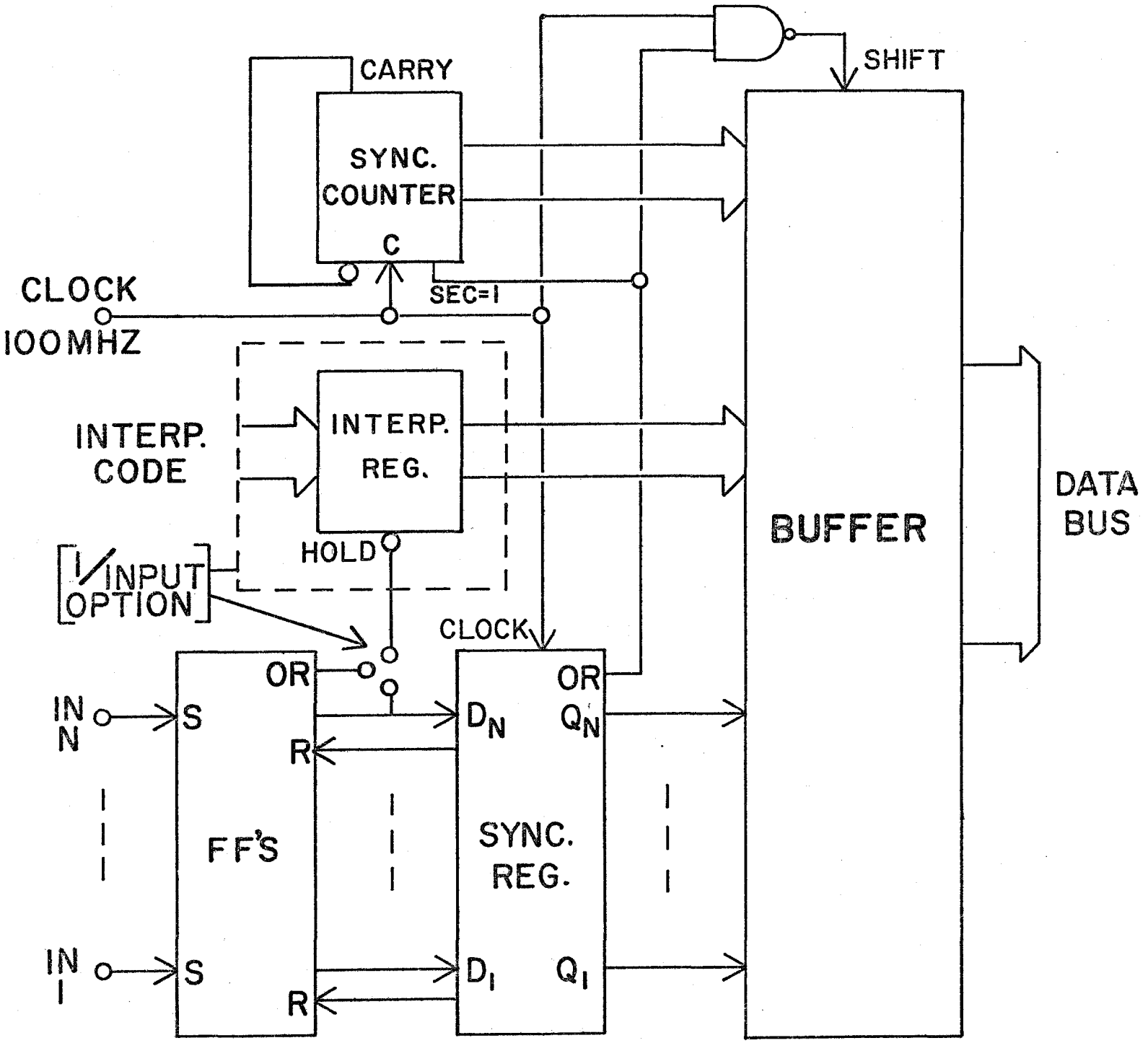

CARRY
SYNC.
COUNTER
C
SHIFT
CLOCK
100MHZ
SEC=1
INTERP.
CODE
INTERP.
REG.
HOLD
1/INPUT
OPTION
BUFFER
DATA
BUS
CLOCK
OR
IN
N
S
R
FF'S
OR
D_N
Q_N
SYNC.
REG.
IN
I
S
R
D_I
Q_I

Fig. 7

storage cycle takes place, the major clock counter is reset. Thus the system records the interval between pulse arrivals A stop tag bit allows read out of only the active channels.

Editorial Comment

This system solves the problem of accurately recording closely spaced hits on different wires since each wire has its own vernier latch. This requires a large, fast memory since sixty odd bits are recorded for each event. The resulting power consumption and parts cost are the highest of any system discussed here. Still the system appears to be very powerful, and would seem to be capable of recording accurately any possible hit combination.

SYSTEM: FERMILAB, C. Kerns

INPUT: ECL

DIGITIZER: Digital

TRIGGER: Common Start

TIME RESOLUTION: 10 ns

DOUBLE TRACK RESOLUTION: PER WIRE None
PER MODULE None

RUNDOWN OR PROCESSING TIME: None

ABORT TIME: None

FULL SCALE TIME: 320 ns

STABILITY: Clock

DIGITIZERS: 1 SHARED BY: 1 WIRES

OUTPUT BUFFER: 1 EVENTS

OUTPUT FORMAT: 5 Bit Time 6 Bit Address

PACKAGING: 16 WIRES IN: PC Board - CAMAC I.F.

LOGIC: ECL/TTL

POWER PER WIRE: Not Known

PARTS COST PER WIRE: $13.00/Wire

MISC: A 48 Wire Prototype System has Been Built.

A common start, originating from coincident phototubes, simultaneously resets the flip-flops associated with each channel and permits all scalers to count the clock pulses (Fig. 8). As various wires receive valid (during the acceptance window time) bits, the associated channel flip-flop is set, stopping and holding the count in that channel's scaler. The priority encoder (9318) now receives a logic "1" from each channel wire flip-flop which has received a bit. The 9318 encodes its inputs as a binary number on a priority basis, displaying only that binary number which holds the highest priority. This binary number is now used (recorded) as the address of a particular channel as well as being converted back to decimal via the 74154 chip. The output of the 74154 enables one scaler at a time to be multiplexed onto the data lines for storage in a FIFO Memory. As each scaler number and its associated binary address is stored, a "send next word" pulse is returned and routed to the correct flip-flop (the previously read one) to reset it. This action allows the 9318 priority to "read" the next address and put its scaler data in memory.

This sequence continues on until all wire addresses which contain valid data are read out and recorded in memory.

Editorial Comment

This is a straight forward 100 MHz clock counter system. ECL and TTL are mixed to conserve power and to reduce cost. A priority encoder read out scheme quickly selects only the wires having hits for read out and the selected data is buffered in a FIFO memory to preserve read out speed. This system was

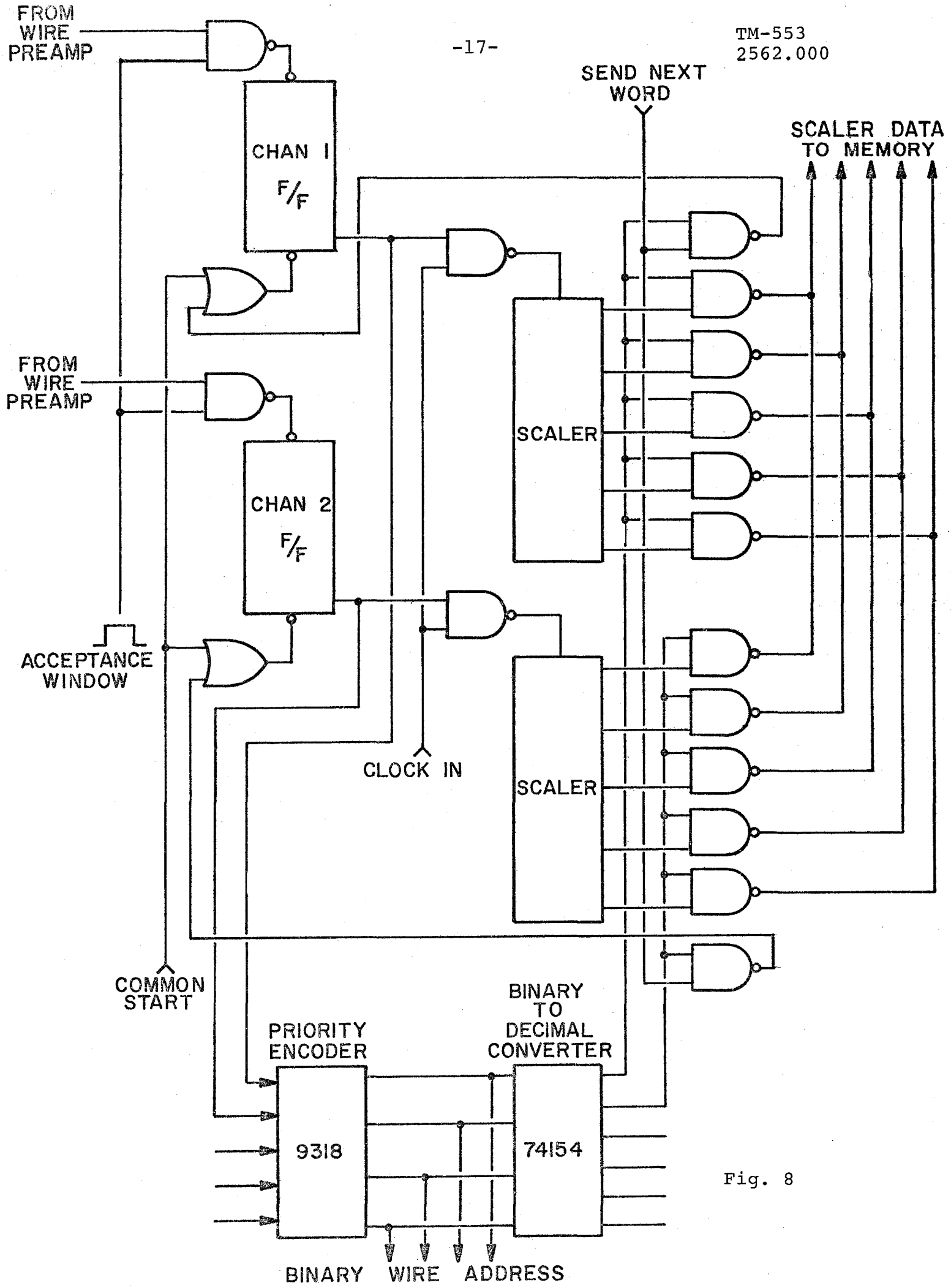

FROM WIRE PREAMP
CHAN 1 F/F
SEND NEXT WORD
SCALER DATA TO MEMORY
FROM WIRE PREAMP
SCALER
CHAN 2 F/F
ACCEPTANCE WINDOW
CLOCK IN
SCALER
COMMON START
BINARY TO DECIMAL CONVERTER
PRIORITY ENCODER
9318
74154
BINARY WIRE ADDRESS

Fig. 8

built as a prototype for evaluation. A 200 MHz equivalent system is being developed.

SYSTEM: HARVARD, C. Rubbia, H. Weedon

INPUT: Standard MWPC Pre-amp and Delay One-shot

DIGITIZER: Time Stretcher X15

TRIGGER: Common Start (But Uses Electronic Delay in Each Line to Provide Effective Common Stop Operation)

TIME RESOLUTION: 5 ns

DOUBLE TRACK RESOLUTION: PER WIRE None
Per Module

RUNDOWN OR PROCESSING TIME: 20 μs

ABORT TIME: Up to 20 μs

FULL SCALE TIME: 2.5 μs

STABILITY: 50-100 ps/°C

DIGITIZERS: 1 SHARED BY 1 WIRE

OUTPUT BUFFER: 6 EVENTS

OUTPUT FORMAT: 8 Bit Serial to 120 Wire CAMAC Controller

PACKAGING: 12 Digitizers on a card. WIRES IN: Large PC Card Mounted on Chamber

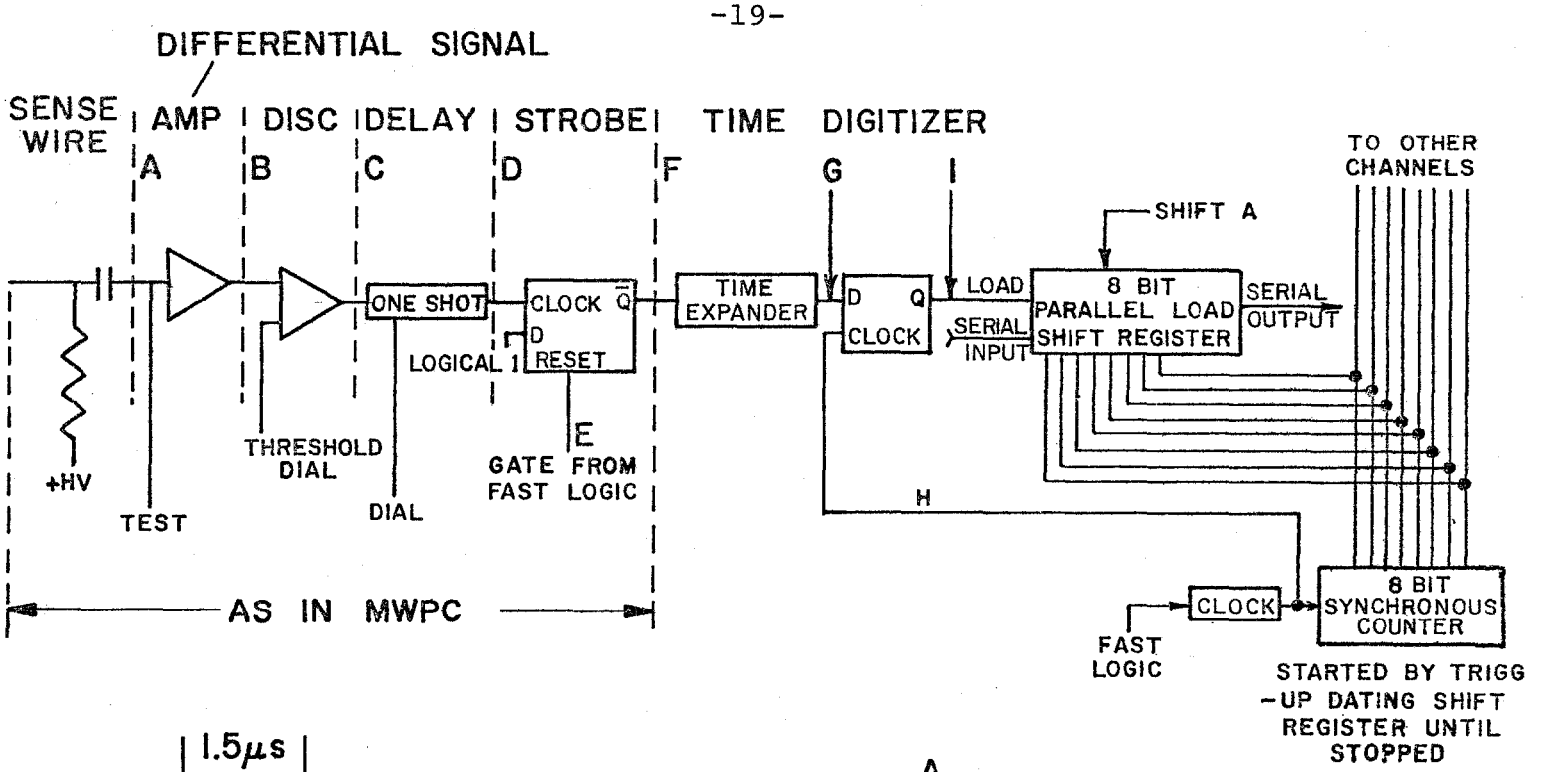
LOGIC: TTL

POWER PER WIRE: 400 mA

PARTS COST PER WIRE: $15.00

MISC: Built in Calibration, 1000 Wire System Operating for Long Time.

Incoming pulses (Fig. 9) are amplified by a conventional proportional wire chamber circuit. A 700 ns one shot delay provides time for trigger decision logic. When a logic gate is generated, the time between the end of the 700 ns delay and the end of the trigger pulse is a measure of the drift time. This is stretched by 15/1 and the end is used to gate a clock into an eight bit shift register. Since this clock is started by the decision logic the shift register contains a measure of the drift time. The shift register contents are clocked into a 40 bit circulating buffer so that six events can be accumulated


DIFFERENTIAL SIGNAL
SENSE WIRE
AMP
DISC
DELAY
STROBE
TIME DIGITIZER
A
B
C
D
F
G
I
TO OTHER CHANNELS
SHIFT A
ONE SHOT
CLOCK
Q̄
D
RESET
LOGICAL 1
TIME EXPANDER
D
Q
CLOCK
LOAD
SERIAL INPUT
8 BIT PARALLEL LOAD SHIFT REGISTER
SERIAL OUTPUT
+HV
TEST
THRESHOLD DIAL
DIAL
E
GATE FROM FAST LOGIC
H
AS IN MWPC
CLOCK
8 BIT SYNCHRONOUS COUNTER
FAST LOGIC
STARTED BY TRIGG -UP DATING SHIFT REGISTER UNTIL STOPPED

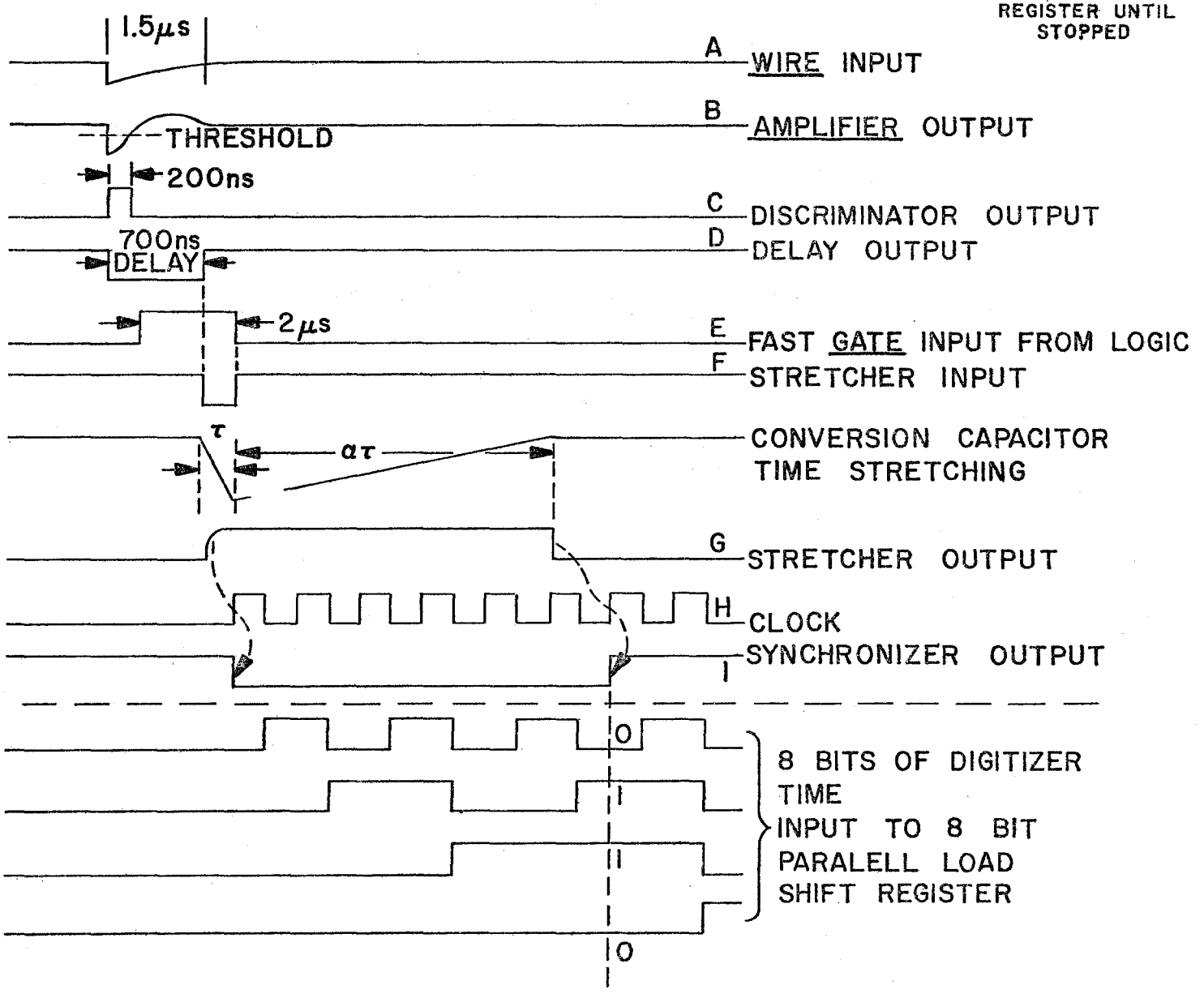

1.5μs
A
WIRE INPUT
B
AMPLIFIER OUTPUT
THRESHOLD
200ns
C
DISCRIMINATOR OUTPUT
700ns DELAY
D
DELAY OUTPUT
2μs
E
FAST GATE INPUT FROM LOGIC
F
STRETCHER INPUT
τ
ατ
CONVERSION CAPACITOR TIME STRETCHING
G
STRETCHER OUTPUT
H
CLOCK
SYNCHRONIZER OUTPUT
I
O
I
I
O
8 BITS OF DIGITIZER TIME INPUT TO 8 BIT PARALELL LOAD SHIFT REGISTER

Fig. 9

before read out is necessary.

Most electronics is located on large printed circuit boards which easily fit on one edge of the 12' x 12' chambers. One CAMAC read out module is used for each 120 wires with a very small number of interconnecting wires required due to the serial read out scheme.

Editorial Comment

This is one of the largest operating system known to us in size - 12' x 12' of chambers, in number of wires - approximately 1000 and in operating time at least 6 months. It is difficult to conceive of operating this experiment by any other technique. A MWPC system would require of the order of 10^5 wires for equal resolution. It is difficult to imagine either building such chambers or getting all the electronics working at once. Magnetostrictive chambers might be used but it is the author's opinion that drift chambers are already at a higher level of development and appear to require less "black magic" for successful operation.

This is a very impressive system for an early application of a new technique. While we do not wish to detract from the achievement of the Harvard group, this system would seem to prove the assertion that drift chambers are easier to build than previous large volume, high resolution detectors.

SYSTEM: LECROY Model 2770

INPUT: Differential, 100Ω, ECL

DIGITIZER: Time Stretcher, Approximately 10/1

TRIGGER: Common Stop

TIME RESOLUTION: 4 ns Optional 2 ns

DOUBLE TRACK RESOLUTION: PER WIRE 40 ns Recovery
PER MODULE

RUNDOWN OR PROCESSING TIME: Approximately 15 μs

ABORT TIME: 40 ns

FULL SCALE TIME: 1 μs Optional 500 ns

STABILITY: Not Known

DIGITIZERS: 1 SHARED BY: 1 WIRES:

OUTPUT BUFFER: 32 FIFO HITS

OUTPUT FORMAT: 8 Bit Time, 7 Bit Wire Address

PACKAGING: 96 WIRES IN: 2 W - CAMAC

LOGIC: Not Known

POWER PER WIRE: 0.19 W*

PARTS COST PER WIRE: Commercial System $50.00/wire

MISC: Front end routing box allows one wire to drive four digitizer channels.

The LECROY System is advertised to achieve very high packing density (96 channels in a 2 W CAMAC) while operating at the lowest power level of any of the systems described here. The time stretcher circuitry resets with each incoming pulse until a stop pulse is received. Laser trimming of the hybrid time stretchers is expected to minimize calibration between channels.

SYSTEM: LBL, F. Kirsten

INPUT: Not Defined

DIGITIZER:

TRIGGER: Common Stop

TIME RESOLUTION: Not Specified

DOUBLE TRACK RESOLUTION: PER WIRE
PER MODULE

RUNDOWN OR PROCESSING TIME:

ABORT TIME:

FULL SCALE TIME:

STABILITY:

DIGITIZERS: SHARED BY: WIRES:

OUTPUT BUFFER: EVENTS:

OUTPUT FORMAT:

PACKAGING: WIRES IN:

LOGIC:

POWER PER WIRE:

PARTS COST PER WIRE:

Misc: See Following LBL Design Proposal

The following is a description supplied by F. Kirsten:

"Recently, several experiments have been proposed by LBL experimenters which involve the digitization of fairly large numbers (hundreds or thousands) of channels of analog information. The analog quantities can be categorized as: time intervals, amplitudes and static levels. Time intervals arise with scintillator time-of-flight telescopes, delayline readout of

MWPCs or drift chambers, and drift times in drift chambers. Amplitudes are, for example, the volt-second content of a pulse delivered by a dE/dx counter or a calorimeter. Static sources include the multitudinous phototube power supply voltages, magnet currents, etc.

We decided, therefore, to extend our original charter, which was to design drift chamber electronics, to a more general aim--i.e., to see if all the above-mentioned sources could be accommodiated by a single, multipurpose system. The block diagram (Fig. 10) shows one way in which this might be accomplished. On the left are various analog converters which are adapted from a more or less common design to the various applications. These are all attached to a digitizing system. The example in the block is a single scaler with scratch pad memory. The block also shows a stacked comparator interface between the analog converters and the memory. The converters all present a level to their comparator. The common ramp is attached to the other input of all comparators. The memory is pulsed when the amplitude of the ramp equals the static level from the converter. The ramp can be made to be non-linear if desired, to compensate for non-linearities in drift time, or to provide a logarithmic conversion.

Work on this sort of system has been started."

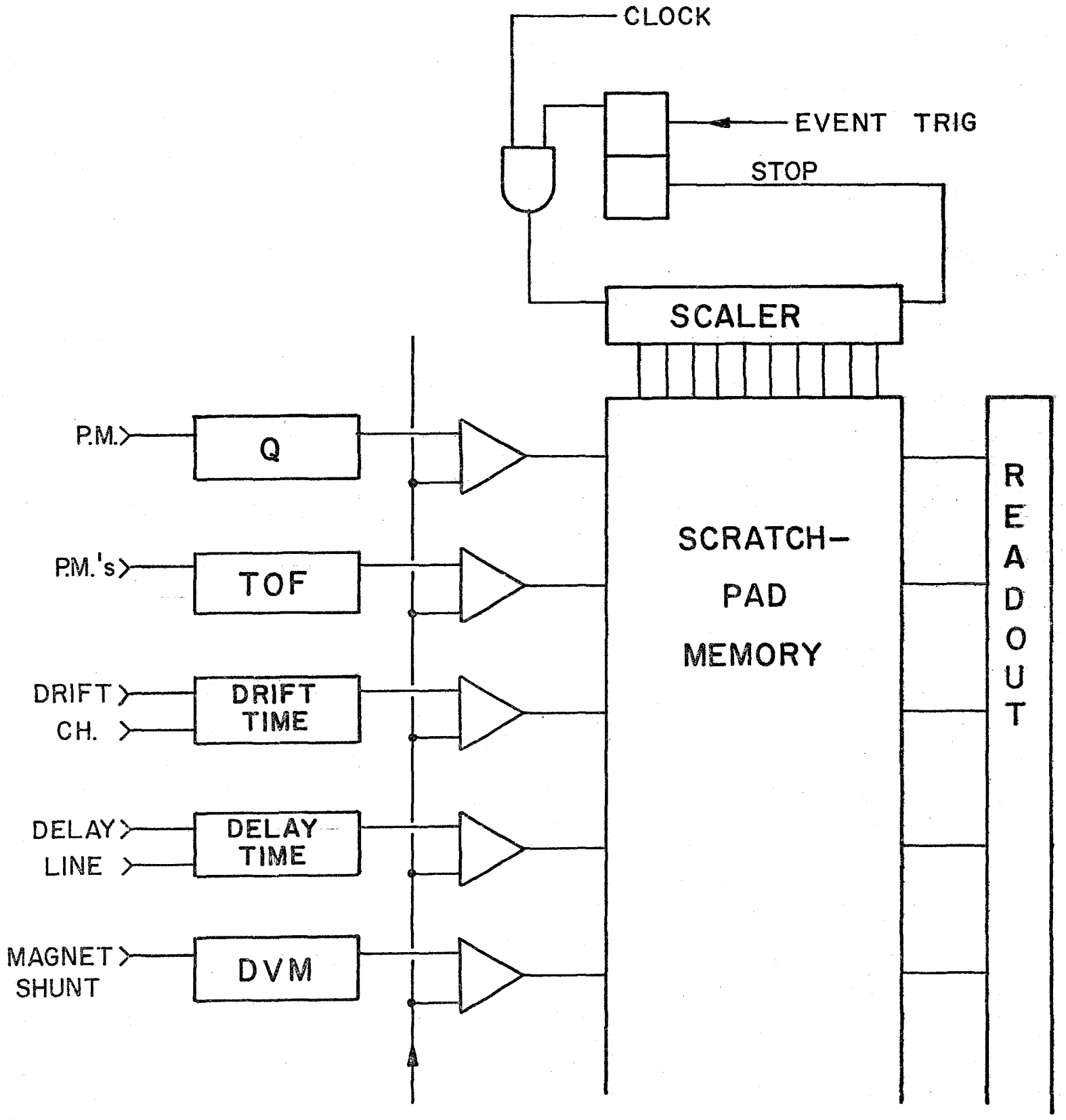

CLOCK
EVENT TRIG
STOP
SCALER
P.M.
Q
P.M.'s
TOF
DRIFT
CH.
DRIFT TIME
DELAY
LINE
DELAY TIME
MAGNET
SHUNT
DVM
SCRATCH-
PAD
MEMORY
READOUT

Fig. 10

SYSTEM: UCSD - T. Burnett, W. Vernon

INPUT: Differential with Left - Right Detection

DIGITIZER: Digital with X500 Vernier Stretcher

TRIGGER: Common Start

TIME RESOLUTION: 0.5 ns

DOUBLE TRACK RESOLUTION: PER WIRE None
PER MODULE

RUNDOWN OR PROCESSING TIME: Approximately 40 μsec

ABORT TIME: Short and FET Circuit Discharges Time Stretcher

FULL SCALE TIME: 1.6 μsec

STABILITY: Not Known

DIGITIZERS: 1 SHARED BY: 1 WIRES:

OUTPUT BUFFER One EVENTS:

OUTPUT FORMAT: 5 Bits Clock, 7 Bits Vernier, 1 Right - Left
3 Channel Number

PACKAGING: 8 WIRES IN: 1 W-CAMAC

LOGIC: TTL

POWER PER WIRE: 1.7 W

PARTS COST PER WIRE: $10.00

This system uses a pair of sense wires and a fast differential comparator to solve the left-right ambiguity (Fig. 11). A 20 MHz clock is started by the event trigger and is distributed to the wire digitizers. When the signal arrives from the chamber, the contents of the fast clock (5 Bits) are stored in a shift register. The chamber signal also starts a time stretcher circuit which is stopped by the next fast clock pulse. Delays in the time stretcher result in a

UCSD DRIFT CHAMBER DIGITIZER BLOCK DIAGRAM

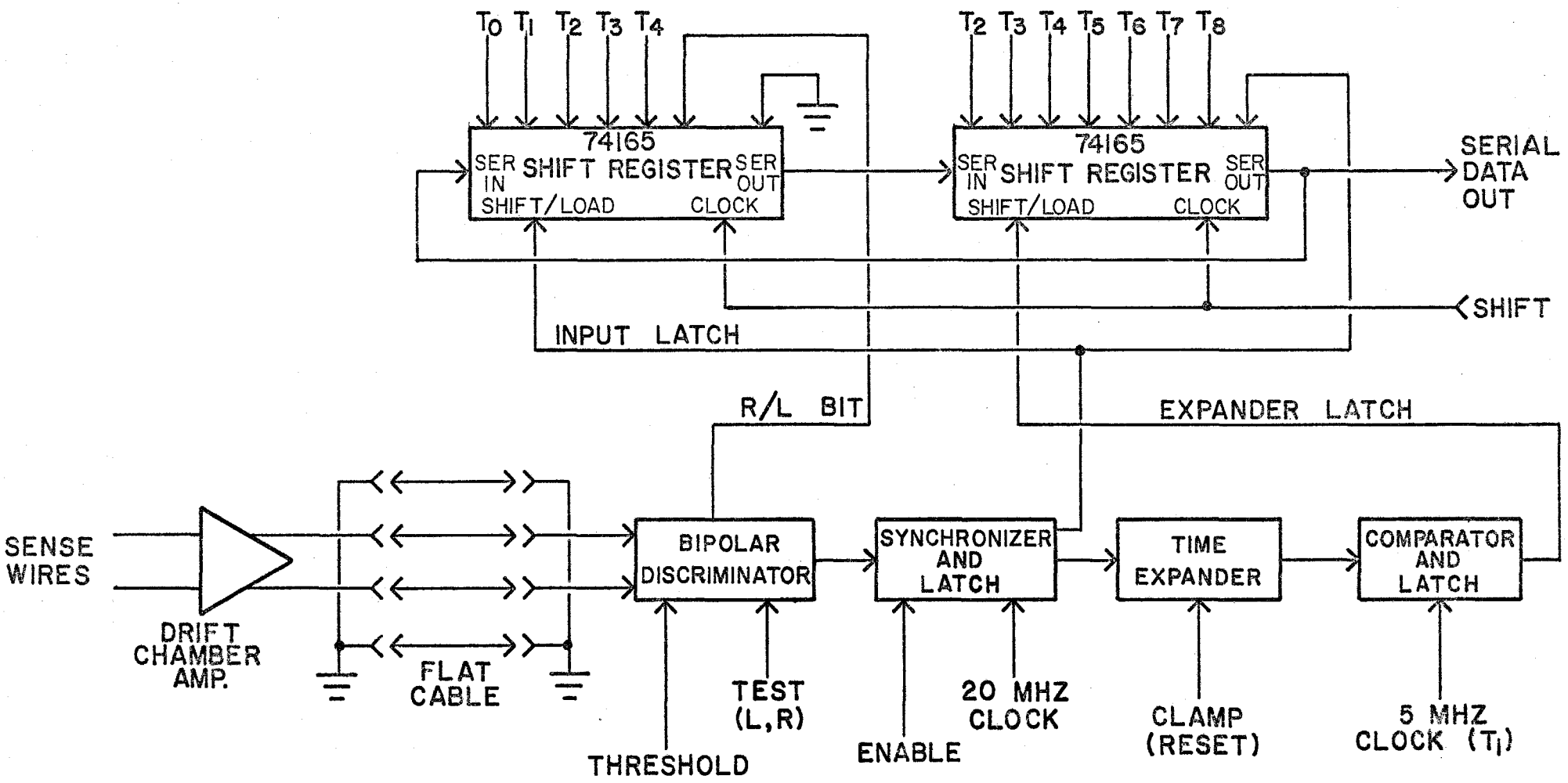


Fig. 11

minimum stretched signal. This is compensated by not starting the slow stretcher clock until the time (17 μs) which corresponds to the simultaneous arrival of fast clock and wire signals. When the time stretcher expires the slow clock contents are stored in a seven bit shift register. The result is a 7 bit vernier measurement of the chamber arrival time with respect to the fast clock.

The two shift registers, along with bits indicating L/R and hit can now be read out serially via a private CAMAC data bus.

By using more range in the stretcher than time between fast clock pulses, possible ambiguities at the end points are eliminated at the expense of different scale factors for the two clocks.

Editorial Comment

This system maintains the linearity of a clock system while achieving the high resolution possible with a time stretcher.

The previous outlines cover the principal features of some drift chamber systems that have been built or are under construction. There are a number of fundamental and practical problems associated with drift chamber system construction. Each of these systems emphasizes some features at the expense of others so there does not appear to be a best system. Some of the important features we see are:

Triggering

Multiple Tracks

Timing Accuracy.

Triggering

It is difficult to provide an event trigger ahead of the arrival of signals from the drift chamber without excessive delay cables in each signal line since event trigger logic takes some time. Harvard solves this problem by the conventional low cost proportional chamber scheme of having a 700 ns one shot delay in each signal wire. Clocks are started at the end of this delay if an event trigger is present and stopped at the end of the event trigger. While technically a common start system this has much in common with a common stop system in that electronic delays in each signal line allow ample trigger decision making time.

Columbia solves the trigger problem in a completely general way. The input is operated wide open with the arrival of each chamber signal recording the time interval since the arrival of the previous pulses or the time from the last pulse to the stop pulse. If the interval overflows the counter the event is flagged. At the stop time a circulating buffer contains the last 16 intervals. With this scheme it is possible to take an indefinitely long time to decide on an event trigger since it is only necessary that the event is still in the buffer when the decision is made. With this scheme the trigger logic could be several events behind and good events could still be separated from background.

LeCroy uses a simple scheme to provide common stop triggering. This is a one digitizer per wire system where each input pulse restarts the time measurement. It is thus only necessary to generate a stop pulse before the arrival of

any pulse from a following event.

Multiple Tracks

A number of systems have been built with a single digitizer per wire. It should be pointed out that since drift chamber systems are usually operated with two chambers staggered 1/2 cell width to solve the left - right ambiguity that this also allows detection of two tracks in the same half cell. Since two track resolution in a single cell is limited to about 2.5 mm it would not help very much to add multiple digitizers per wire if full cell spacing is of the order of one cm. Thus, for high rate applications where separation of events due to drift time becomes a problem, small cells with one digitizer per wire may be the best solution.

LeCroy has a simple solution where multiple tracks per wire are required. A routing box ahead of a group of digitizers connects successive wire pulses to four digitizers. Since the minimum pulse spacing on a single wire is of the order of 50 ns, and since the routing box deals with well shaped pulses, it is not a difficult box to build. In spite of requiring a number of digitizers for each wire, this solution may be more economical in the total system because of its simplicity.

It appears to be attractive to have m digitizers share n wires. The most economical solution would be a module where n was the total number of chamber wires and m was the maximum expected number of tracks. The CERN module has 8 wires sharing 4 digitizers. If successive wire pulses are to be routed to different digitizers there is a problem in that it is difficult

to switch digitizers to the same time resolution that time measurements are made on a single wire. Since time measurements are typically made to 2 ns, this requires switching digitizers in 2 ns if there is to be no loss of accuracy for pulses arriving on two different wires within 2 ns. There is a further problem in pile up at the OR gate that is used to detect that a pulse has arrived on one of the wires. Even if the pulses are clipped to a very narrow width, it is possible for pulses from different wires to arrive in delays equal to their width and thus appear as one pulse to the logic. CERN approaches these problems by clipping the input pulses to 3 ns, using MECL III front end decision logic, and by switching digitizers after a few gate delays in the case of pile up. Still the digitizer switching time would appear to be slower than the 2 ns time measurement of this system.

In shared digitizer schemes, it is necessary to have a latch for each digitizer for each wire. Since digitizers must be switched quickly to solve the different wire arrival time problem, these latches must set up very quickly. As a result switching digitizer schemes tend to be built from fast ECL logic and to draw high power.

Columbia has solved the near simultaneous arrival time problem by using a separate vernier delay line latch for each wire. At 25 ns major clock periods all latches and a slow clock are gated into a buffer memory if any latches have been set. This scheme preserves timing accuracy on all incoming pulses but requires a 6 bit fast latch and 6 bits of fast buffer memory for each wire and a buffer memory word 6 bits times the

number of wires plus clock and control bits in width.

Timing Accuracy

The simplest schemes directly count fast clocks. These systems usually consume high power since ECL is most often used. In principle the counters could shift to lower power TTL after a few stages but in practice designers tend to stick to one type of logic, probably due to the difficulty of reading out mixed systems. If more accuracy is needed, the basic clock can be delayed by a series of delay lines to produce a multi-phase clock. Loading a latch with the states of the phases at start time as done by Columbia and CERN, allows 2 ns time resolution with 10K ECL.

For greater accuracy than 2 ns, digital systems become rapidly very expensive and delay line vernier systems become difficult to adjust. Time stretching, as implemented by Harvard, is an old technique and is capable of much higher accuracy than that required by drift chambers. Time stretching can easily be made stable enough but does require individual calibration. Further, time stretching means that many times the measured time interval is required before the answer is available. This is quite acceptable for low event rate experiments as that designed by Harvard, but faster recovery is often needed.

LeCroy solves this problem by resetting the timing circuit with each incoming pulse. The circuit then stretches the time between the last incoming pulse and the stop pulse, moving the recovery time into computer interrupt time where more time is available. UCSD mixes a time stretcher with

direct counting. With this technique time is stretched between the start pulse and the first slow clock pulse. The total time is this stretched time plus the number of slow clock pulses until stop time. Unless the stop time is related to the event (i.e., the machine RF could be used as the slow clock), a second stretcher is needed to locate the stop pulse in relation to the slow clock, but this need be done only once for all digitizers. The advantage of this scheme is that the vernier stretcher does not need high accuracy compared to stretching the complete interval so that it can be built without requiring special calibration or individual adjustment. Further, the run down time for the vernier stretcher is a small fraction of the time required for a full stretcher scheme.

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