national accelerator laboratory

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A DIGITAL ONE-SHOT MULTIVIBRATOR

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This circuit can "recover" and start to deliver another precisely timed output pulse in 20 ns. The width of the output pulse is programmed by a 12 bit binary word, doubling for each increment in an adjacent place value of the word except the last place value. The minimum output pulse width is 42 ns for this 12 bit circuit but would be shorter for a 6 bit version. The maximum output pulse width is 83 μs. The input pulse width must be about 23 ns shorter than the programmed output pulse width or multiples of this programmed width will be produced with "glitches" whenever the input pulse width is near an exact multiple of the programmed output width. Table 1 indicates the approximate output widths as a function of the 12 bit binary word.

The circuit, as indicated in Figure 1, uses a fast control RS flip flop to gate on an oscillator composed of a closed inverter chain and also enables two cascaded "rate multiplier" counters whenever an input pulse occurs. After the counters have accumulated half the programmed count their output pulse resets the control flip flop which disables the oscillator and the counters - setting them to zero in the process. The output pulse and its complement are taken directly from the fast flip flop.

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The heart of this circuit is the SN 7497N "rate multiplier" counter. Figure 2 is a timing diagram which indicates how this IC chip works with the connections of this circuit. Note that the first output pulse of these counters (which is used to reset the control flip flop) comes after a half period of the programmed period and following outputs are spaced a full period apart if only one of the place positions of the 12 bit binary program word has a one in it. If more than one of the place positions of the program word have ones in them, the output is simply the logical or of the corresponding single one cases. These multiple one cases result in missing pulses if the counters are allowed to run continuously. Note also that the output pulse comes after the positive clock pulse falls and lasts until the next clock pulse comes along.

The actual circuit wiring is indicated in Figure 3. Of course only one "rate multiplier" IC chip would be necessary to demonstrate this circuit thus making it a three IC chip unit. The oscillator frequency of the SN 7400 chip was about 24 MHz implying an average propigation delay per gate of 7 ns. For an 8.0% increase in the 5 V supply voltage the frequency increased 6.1%. The nominal frequency could have been reduced and made adjustable as shown in Figure 3 by the addition of a variable capacitor across one of the oscillator gates. Also, the latest output of this 3-phase oscillator was chosen as the

clock in order to allow a maximum set up time in the "rate multiplier" counters. An earlier phase might reduce the minimum output pulse width width obtainable.

Finally, Figure 4 is a timing diagram which shows what is going on in the circuit for a given set of input conditions. This circuit has an extremely fast "recover time" (or conversely a very high-duty cycle) and, if the 5 volt supply voltage is well regulated, an output pulse width of no observable jitter even when the counters are accumulating 2,047 clock pulses (86 μsec) per output pulse.

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TABLE 1

PROGRAM INPUT TO RATE MULTIPLIER	APROXIMATE OUTPUT PULSE WIDTH-μs	NUMBER OF COUNTS ACCUMULATED
$A_2=B_2=C_2=D_2=E_2=F_2=A_1=B_1=C_1=D_1=E_1=F_1=0$	∞	∞
$A_2=1;\ B_2=C_2=D_2=E_2=F_2=A_1=B_1=C_1=D_1=E_1=F_1=0$	86.0	2047
$B_2=1;\ C_2=D_2=E_2=F_2=A_1=B_1=C_1=D_1=E_1=F_1=0;\ A_2=\Phi$	43.0	1023
$C_2=1;\ D_2=E_2=F_2=A_1=B_1=C_1=D_1=E_1=F_1=0;\ A_2=B_2=\Phi$	21.6	511
$D_2=1;\ E_2=F_2=A_1=B_1=C_1=D_1=E_1=F_1=0;\ A_2=B_2=C_2=\Phi$	10.5	255
$E_2=1;\ F_2=A_1=B_1=C_1=D_1=E_1=F_1=0;\ A_2=B_2=C_2=D_2=\Phi$	5.40	127
$F_2=1;\ A_1=B_1=C_1=D_1=E_1=F_1=0;\ A_2=B_2=C_2=D_2=E_2=\Phi$	2.70	63
$A_1=1;\ B_1=C_1=D_1=E_1=F_1=0;\ A_2=B_2=C_2=D_2=E_2=F_2=\Phi$	1.36	31
$B_1=1;\ C_1=D_1=E_1=F_1=0;\ A_2=B_2=C_2=D_2=E_2=F_2=A_1=\Phi$	0.680	15
$C_1=1;\ D_1=E_1=F_1=0;\ A_2=B_2=C_2=D_2=E_2=F_2=A_1=B_1=\Phi$	0.330	7
$D_1=1;\ E_1=F_1=0;\ A_2=B_2=C_2=D_2=E_2=F_2=A_1=B_1=C_1=\Phi$	0.160	3
$E_1=1;\ F_1=0;\ A_2=B_2=C_2=D_2=E_2=F_2=A_1=B_1=C_1=D_1=\Phi$	0.078	1
$F_1=1;\ A_2=B_2=C_2=D_2=E_2=F_2=A_1=B_1=C_1=D_1=E_1=\Phi$	0.042	0

WHERE: Φ = DON'T CARE

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FIG. 1

DIGITAL ONE-SHOT BLOCK DIAGRAM

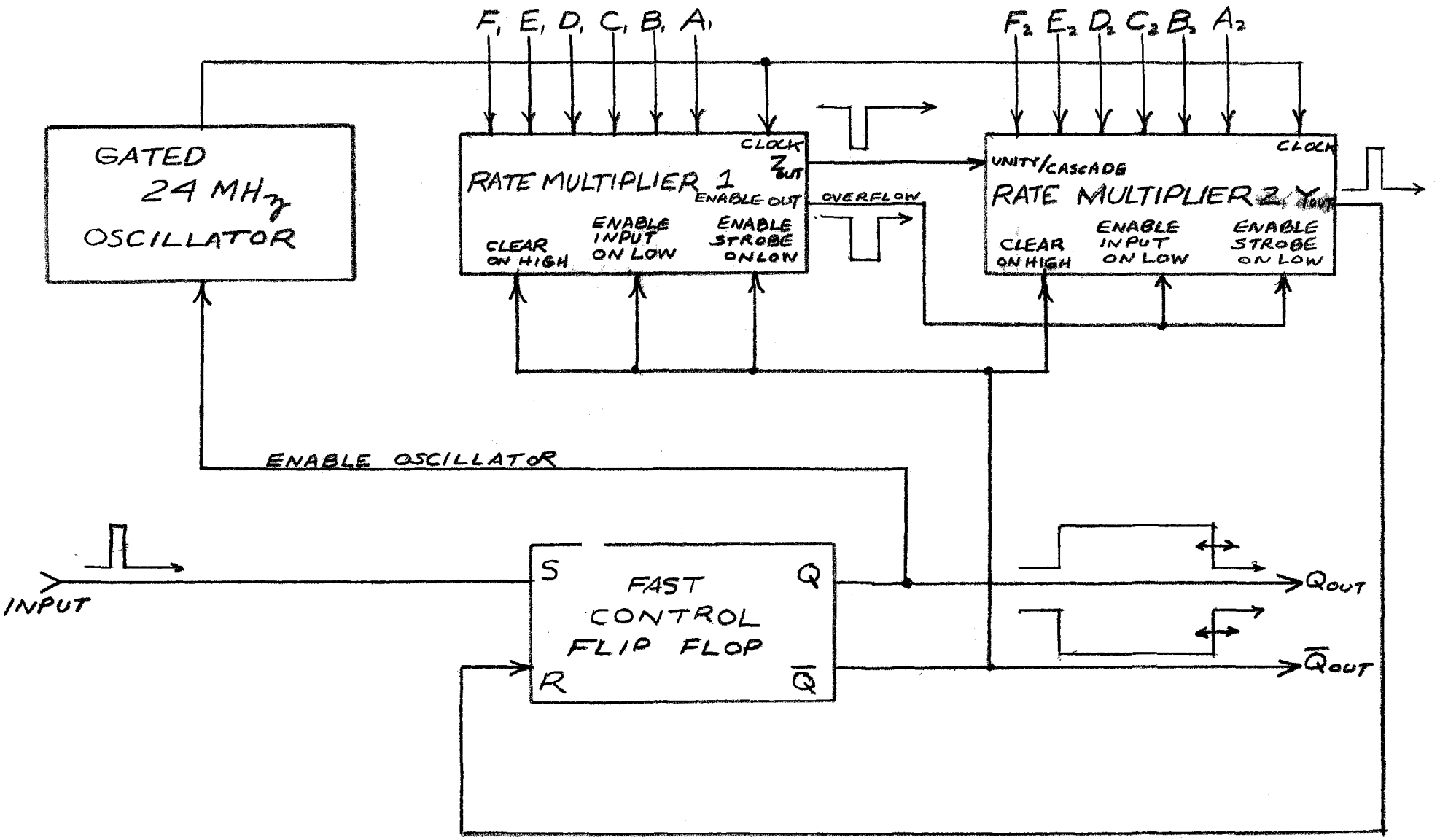

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FIG. 2

TIMING DIAGRAM OF THE SN7497 RATE MULTIPLIER

ALL INPUTS (A, B ETC) NOT SPECIFIED ARE ZERO

$Z_{OUT} = \overline{Y_{OUT}}$

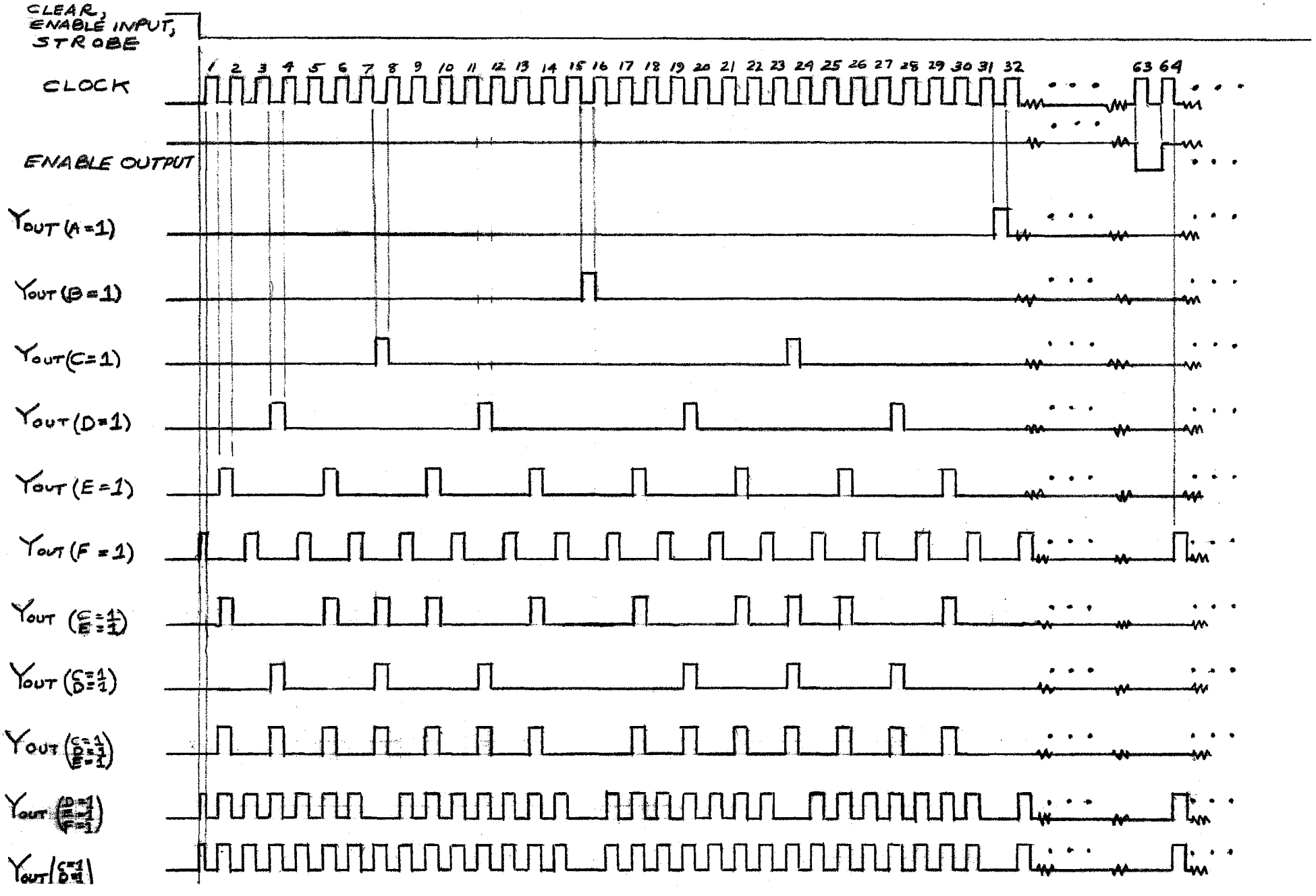

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FIG. 3

DIGITAL ONE-SHOT CIRCUIT DIAGRAM

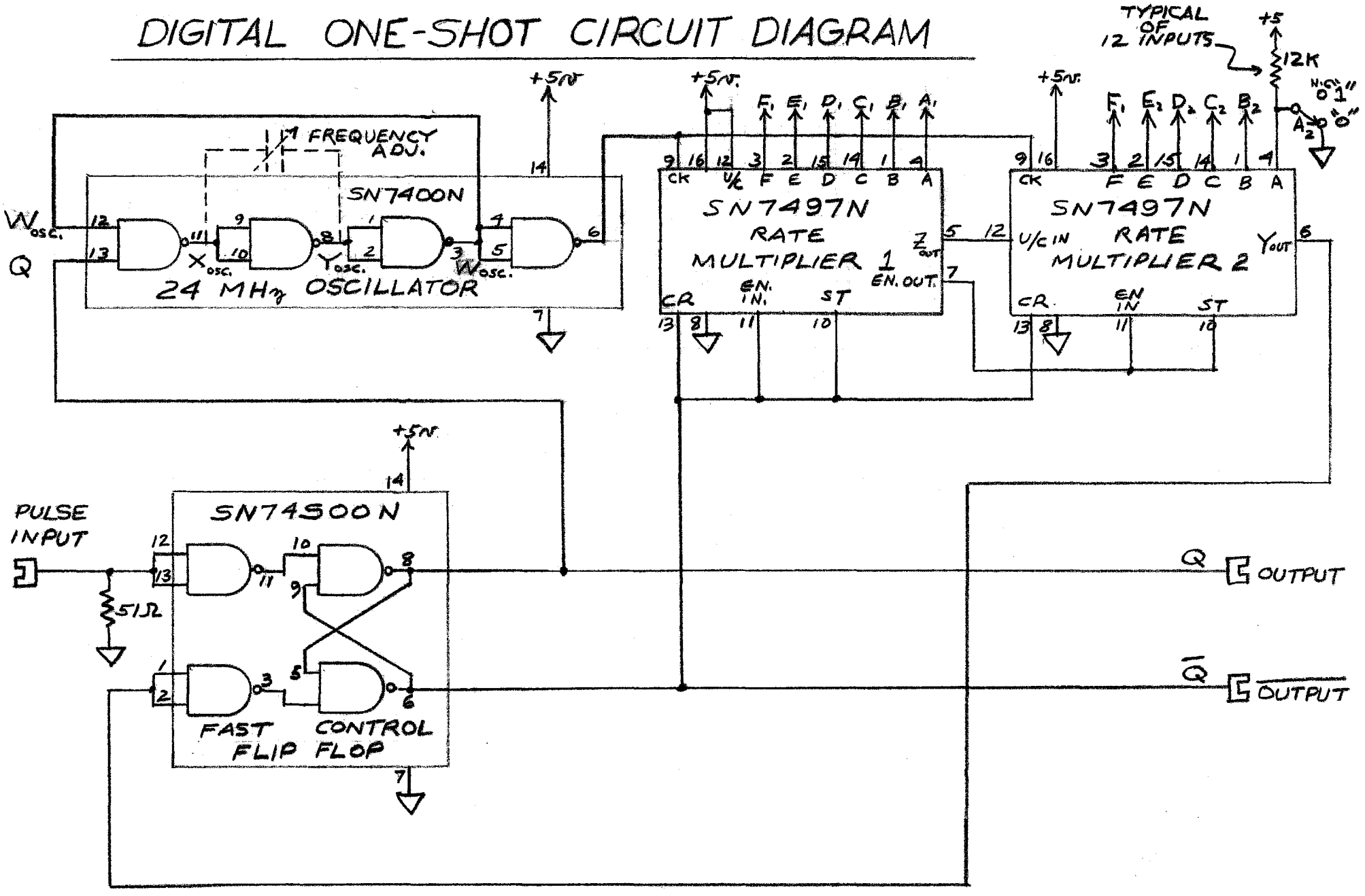

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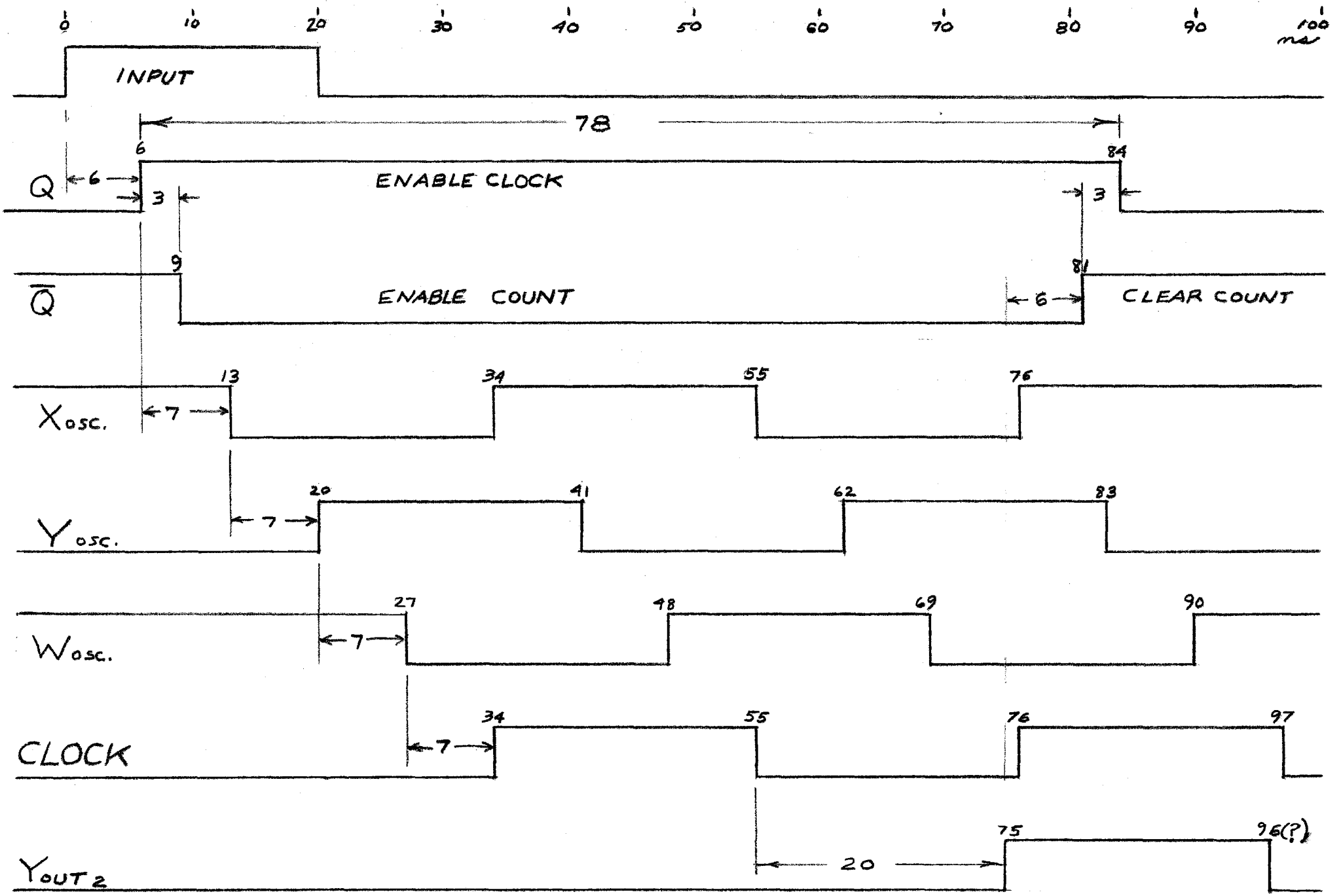
FIG. 4

ONE-SHOT TIMING DIAGRAM FOR THE CASE: $F_1 = 0$, $E_1 = 1$ (IDEALIZED)



BASED ON 3ms PROPIGATION DELAY IN SN7400N AND 7ms DELAY IN SN7400N