Fermi National Accelerator Laboratory

FN-544

Memory Lookup Unit (MLU)

Thomas Regan
Fermi National Accelerator Laboratory
P.O. Box 500
Batavia, Illinois 60510

June 7, 1990

Operated by Universities Research Association Inc. under contract with the United States Department of Energy

Memory Lookup Unit (MLU)

At the request of experiment E-760, the Physics Department designed and constructed a single width MLU Camac module which accepts ECLine and compatible signals and provides four NIM signals as outputs.

The central feature of this module consists of four P4C187-10PC 64K by 1 bit static CMOS RAMs, designed by Performance Semiconductor Corporation, which form a fast look up table. In this configuration the total delay through the P4C187 is less than 12 ns. With the associated line receivers and level translators the total propagation delay through the module is under 25 ns, typically 20 ns (depending on time jitter between inputs). One output, a buffered copy of the input, is also available in ECLine format.

The ECL input, from LeCroy discriminators in E-760, is strobed into ECL latches which drive the address lines of the RAMs. A delayed version of the strobe then gates the output of the RAMs which is converted to NIM and sent to the output LEMO fittings.

The RAM chips are initially written with 64K, four bit data words from Camac using the block transfer (Q) mode. This data can be read back into Camac, again using the block transfer mode, for checking data integrity.

While the number of memory chips for this experiment was chosen to be four, it could be expanded fairly easily however a different type of output connector would have to be used as front panel space is at a premium.

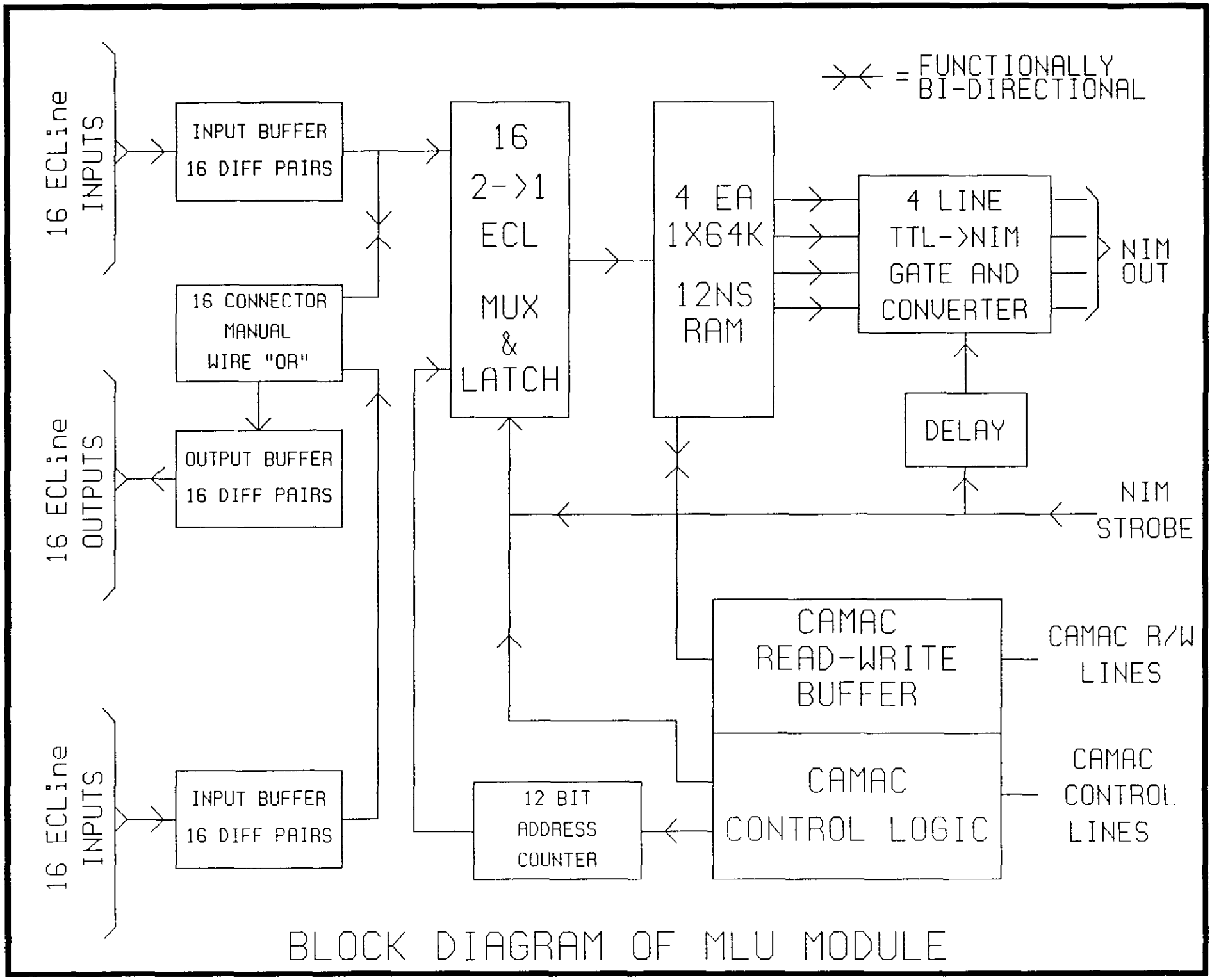
Camac commands:

N.F16.A0	Writes into memories 64K four bit words using block transfer mode.
N.F2.A0	Reads from memories 64K four bit words using block transfer mode.
N.F9	Resets address counter.

Data transfers are controlled by the Q response.

A block diagram of this module is shown. The complete schematic is available from the author.

I'd like to thank Mr. Robert Jones for his invaluable help and suggestions in the prototype phase of this project.



BLOCK DIAGRAM OF MLU MODULE