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DIGITAL SCATTERING ANGLE PREPROCESSORS

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ABSTRACT

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I. Introduction

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I. Introduction

Recently an Albany-Dubna-Fermilab-Lehigh-UCLA collaboration has been engaged in several experiments to study channeling at very high energy.[1] Particle channeling occurs when a charged particle traverses a single crystal in a direction near one of the crystal axes or planes.[2] If the particle is traveling within or slightly outside of a critical angle defined relative to the crystal axis direction its behavior in the material is drastically altered. The critical angle at 100 GeV/c is 68 microradians and goes as $1/\sqrt{p}$ where p is the beam momentum. Characteristically the energy loss is reduced by nearly a factor of two while little "multiple scattering" occurs. Experiments are often carried out with hyperpure germanium single crystals operated as intrinsic charge detectors to measure the energy loss.

Depending on the beam divergence, a large fraction of particles incident on a crystal will exhibit channeling effects. Since some of these effects are quite complicated, it is desirable to obtain many events for high statistics. For that reason, sorting the events as a function of the scattering angle considerably enriches the event statistics within a certain scattering angle range.

It is possible to consider sorting on scattering angles at several points in the event processing sequence. A preprocessor can be incorporated that analyzes the event and accepts or rejects it depending on the size of the scattering angle before it is fed to the on-line computer. A second possibility is to make a computation with the on-line computer and, on the basis of that computation, decide whether or not to store the event on disc. Finally the event can be tested using the off-line analysis program. Which technique is chosen depends on a number of factors to be discussed later. This article describes two digital preprocessors useful for the first possibility.

The experiments we are involved in employ high spatial resolution drift chambers to measure the incoming and outgoing directions of the particles.[3] Figure 1 shows a schematic of the apparatus. The system we used had been designed and operated to measure the kaon form factor by a Dubna, Fermilab, Notre Dame, Pittsburgh, UCLA collaboration. Indeed it was in operation for this purpose up to one week before our initial channeling experiment started. The fast adaptation of the

form factor equipment and programs constituted a major constraint on our approach to the first channeling experiment.

The drift chambers in the kaon form factor apparatus had a 2.1 cm spacing between the sense and potential wires and a module (4-plane) spatial resolution on the order of 90 microns. The angular resolutions for various angles measured by the system are complicated, but are on the order of tens of microradians.

The first of the experiments was carried out in the M1 beam of the Fermilab Meson Laboratory. Characterically that beam had an angular divergence of ± 400 microradians at 100 GeV/c in the experiment.

It is quite easy to operate the M1 beam line so that the beam diameter is on the order of 2 cm. Thus, while each of the modules had about ten collection wires, nearly all of the beam flux could be made to fall between one sense and one potential wire. In this mode M1 could easily yield a million particles per pulse above 250 GeV/c, spread out over a beam spill of one second.

The drift chamber output signals were fed into Ortec TD 811 time-to-digital converters to digitize the position information. These TDC's were then read into a HP2100 computer, via a CAMAC system, and from there on to a disc. Between accelerator pulses the disc content was read to magnetic tape. The read time to disc depended on the number of TDC's that had to be read out. In our initial operation we planned to adapt the k meson form factor software with as little modification

as possible. That experiment required about 3 millisceonds to read an event to disc with approximately 0.4 milliseconds minimum plus five microseconds per word read. A heroic reprogramming effort was able to reduce that time appreciably, mostly by reducing the length of the TDC list read. Based on the three millisecond number substantially less than three hundred events could be read per beam spill. This is in contrast to the fact that a million particles could go through the crystal and on the order of ten thousand events could be processed through the drift-chamber system in each accelerator pulse. Thus, if only a small fraction of the events lay within some useful scattering angle region there was significant utility in making a pre-processor that could determine the scattering angle and make a decision whether or not to store the event. The two designs discussed here evolved from that requirement. One of them was built and used in the experiment.

Several auxiliary constraints affected our designs and the ultimate choice of which system was built. We had no technical support and less than six months available for construction. This meant that all of the construction and debugging had to be done by physicists not very familiar with integrated circuits, but even less familiar with bit slice technology. At the same time there was no real chance for access to the drift chamber-computer system prior to the channeling experiment. This mediated for a choice of an integrated circuit preprocessor rather than the more elegant bit slice approach.

II. Preprocessor Logic

As noted earlier, the M1 beam could be operated so that most of the particles entered the system in a region between a single sense wire and a single potential wire. The angular acceptance for this region in the downstream module was ± 600 microradians. The projected rms multiple scattering angle for a 100-GeV/c particle in a 2 cm thick germanium crystal is 140 microradians, the axial critical angle for channeling is 68 microradians, and the beam divergence was on the order of 400 microradians. Thus most of the scattered particles detected in the third module were easily contained in the restricted region between one sense wire and a potential wire. Based on this, the preprocessor system was designed to operate with only six sense wires, that is one for each of 3x and 3y coordinates. This resulted in a major simplification since it made it unnecessary to construct a coordinate from several wires. No special provision was made for two or more tracks passing through the system within the firing gate, so that such events could give rise to incorrect scattering angle calculations. However, multi track rejection circuits were incorporated in the logic to diminish multiple track events.

Drift chambers naturally read out projected angles. Rather than processing the scattering angle we decided to analyze the x and y projected scattering angles and require each of them to lie within some range. This increases the sample of accepted events by about a third

but radically simplifies the design. The off-line computer can then be used to make a final cut if necessary.

Obviously a scattering angle preprocessor can operate to accept events either inside or outside some scattering angle region. In the comments that follow we will speak of accepting events inside a certain scattering angle region.

To satisfy the criteria for an event the following relations must be satisfied:

$$|\theta_{xo} - \theta_{xi}| < \theta_{xc} \tag{1}$$

and

$$|\theta_{yo} - \theta_{yi}| < \theta_{yc} , \tag{2}$$

where θ_{xo} is the outgoing projected angle in the x direction, the subscript i refers to an incident angle, and θ_{xc} is the projected scattering angle cut.

An incident projected angle is given by

$$\theta_i = \frac{x_2 - x_1}{L_{12}} \tag{3}$$

while an outgoing projected angle is given by

$$\theta_o = \frac{x_3 - x_2}{L_{23}} \tag{4}$$

where the scattering point in the crystal is assumed to lie near the second plane. Here the coordinate x_i is

$$x_i = s_i + u_i \tag{5}$$

where

x_i = coordinate from some virtual axis (not necessarily the beam or crystal axis)

s_i = distance from the virtual axis to the sense wire

u_i = coordinate inside the drift chamber, that is the coordinate relative to some sense wire

The coordinate inside the drift chamber is given by

$$u_i = v_i t_i , \tag{6}$$

where t_i is the drift time for the drift chamber and v_i is the drift velocity. In practice the drift time is given in terms of the TDC count so that

$$t_i = n_i/k_i , \tag{7}$$

where n_i is the TDC conversion output and k_i is the TDC conversion coefficient. Substituting (7) into (6) gives

$$u_i = \frac{v_i}{k_i} n_i . \tag{8}$$

We assume that the drift velocity is the same for each drift chamber.

The algorith that must be solved then becomes

$$\left| \frac{L_{23}}{k_1 M} n_1 - \frac{n_2}{k_2} + \frac{L_{12} n_3}{k_3 M} + \frac{1}{v} \left(\frac{L_{23}}{M} s_1 - s_2 + \frac{L_{12}}{M} s_3 \right) \right| < \frac{L_{12} L_{23}}{Mv} \theta_c , \tag{9}$$

where $M = L_{12} + L_{23}$.

This form may be shortened to

$$| A_x n_{x_1} - B_x n_{x_2} + C_x n_{x_3} + D_x | < Z_x \tag{10}$$

for the x coordinates and

$$| A_y n_{y_1} - B_y n_{y_2} + C_y n_{y_3} + D_y | < Z_y , \tag{11}$$

where the coefficients are given by

$$A = \frac{L_{23}}{M k_1} \tag{12}$$

$$B = \frac{1}{k_2} \tag{13}$$

$$C = \frac{L_{12}}{M k_3} \tag{14}$$

$$D = \frac{1}{v}\left(\frac{L_{23}}{M} s_1 - s_2 + \frac{L_{12} s_3}{M}\right) \tag{15}$$

$$Z = \frac{L_{12} L_{23}}{Mv} \theta . \tag{16}$$

Normally D and Z are determined empirically by adjusting the system parameters in operation to obtain the desired cut region. Note also that these can all be divided by a multiplier so that at least one constant, for example B, can be set equal to one. In the Fermilab experiment L_{12} = 30 m and L_{23} = 18 m so that the normalized coefficients were A = 0.712, B = 1.0, and C = 0.286.

There are several possible ways to solve these algorithms. In the past these usually have been adapted to proportional chambers. Some of the approaches include:

a. Analog method.[4] All of these operations can be performed by analog circuits. Coefficients can be preset with helipots by establishing proper reference levels. This method is relatively simple and fast but can suffer from stability problems with time and temperature.

b. Specially chosen geometry.[5] By careful choice of L_{12} and L_{23} the coefficients can be adjusted to simple whole numbers. This can result in substantial simplification of the circuits. Since we were employing an existing apparatus this was not easily possible.

c. Introduce multipliers as digital variable. By operating on these numbers one can then solve the algorith to within some precision determined by the least count of the arithmetic unit. Guzik and Basiladze[6] have an earlier solution in this form adapted to proportional planes.

d. We note that another arithmetic preprocessor, M7, intended principally for vee events, was under development at Fermilab at the time.[7] This system is more powerful than the designs we evolved but had not yet come into operation. Yet another system,[8] based in part on table lookup operations, has now been developed. That system could also find application to this problem.

In part we have followed the approach noted under c. above. In one example the logic system was built out of integrated circuits with the arithmetic operations incorporated into the hardware and the coefficients determined by modifying the TDC conversion coefficients.

In the other design, new microprocessor microslice technology with stored software was used in the design for the arithmetic operations. Both designs are presented. However, the integrated circuit design was built because of the short development time available before the experiment.

III. Microslice Preprocessor

A fast microprocessor, such as the AM 2900 bit slice family developed by Advanced Micro Devices, Inc.[9] has several advantages for this type of application. On one hand it offers flexibility of programming and at the same time, the system is high speed with a 100 nsec cycle time.

The basic operations to be performed by the microprocessor are addition, subtraction, multiplication, absolute value calculation and two's complement conversion. Comparison can be done by subtraction and sign analysis. The most critical operation is multiplication. The multiplicand is an eleven-bit number taken from the TDC's. The multipliers are the calculated and normalized coefficient (A, B, C). For at least 1 % coefficient accuracy these numbers should be 8 bits long. Thus, overall the effective arithmetic register length should be 19 bits plus a sign bit or 20 bits in all. Multiplication may be done very rapidly using a separate multiplying IC array. However, considering the 60 μsec TDC dead-time the eight times slower shift-and-add method is good enough. A separate multiplying IC array would greatly increase the cost of the device.

The microprocessor block diagram is shown in Figure 2. In this design all algorithm solutions are performed as one macrocommand which consists of several microsteps. The microword consists of 24 bits divided into two fields: a control field and an ALU (Arithmetic Logic Unit) microinstruction or operand field. When not used as an ALU microinstruction, the second field serves as an 8-bit address for the next branched microstep or the operand for entering coefficients A, B, C and constants D, Z. An additional register (ACCUMULATOR) is necessary because the ALU may not be used while the operand is entered. This register is also used during the multiplication process. This solution was chosen for microword length economy.

In this design, data from the CAMAC dataway is loaded into the microprocessor 200 nsec after entering an NAF command to the CAMACOUT register. A full 1 μsec CAMAC cycle is not necessary because data appear on the dataway approximately 200 nsec after the NAF command is set. A microprocessor module may be inserted into any CAMAC slot. The disadvantage of this method is that decoded N-address lines must be added to the crate by backplane soldering to the slot position holding TDC's or a special A-2 type controller must be used.

The microprocessor is started by applying a START pulse to the front panel in this design. At that moment, a microprogram address is forced in. This address contains the first instruction of the

algorithm. If a particle in at least one plane was scattered more than a given θ_o angle, a CLEAR pulse is produced to reset the experiment electronics back to a waiting mode for the next event. If the cut criterion is satisfied, then the LOOK-AT-ME signal is sent to the CAMAC controller and the normal readout process begins. Simultaneously a HALT signal closes the microprocessor access to the CAMAC dataway.

Maximum one plane analysis time is estimated to be about 10 μsec with this design and depends on the form of the coefficients A, B, C.

A microprogram memory, a RAM 93L422 by Fairchild was specified in the design. It's access time is 45 nsec.

Loading of the microprogram could be performed by a computer using CAMAC or from a CAMAC module front panel. One microword (24 bits) loading must be done in two steps. The first step is to load the control field and indicate the microword address, while the second step loads the operand field under the address given during the previous operation.

IV. Discrete Integrated Circuit Preprocessor

In the discrete integrated circuit preprocessor the coefficients A, B, C in equations (10) and (11) can be set equal to one if the TDC conversion coefficients k_i are properly chosen. This conversion change can be easily implemented on commercial CAMAC TDC units. For that reason this system was designed around a CAMAC format. An entire CAMAC crate was assigned to the operation. A control

unit occupied the normal slot 25 control position while the arithmetic unit occupied slots 23 and 24. These units were coupled together by an additional non-standard cable in addition to the normal CAMAC back plane bus. An Ortec TD 811 TDC unit with modified conversion coefficients occupied one of the remaining empty slots.

With the k_i properly set the algorithms become

$$\left| n'_{x_1} - n'_{x_2} + n'_{x_2} + D_x \right| < Z_x \qquad (17)$$

$$\left| n'_{y_1} - n'_{y_2} + n'_{y_3} + D_y \right| < Z_y \qquad (18)$$

(primes are used to indicate that the TDC values come from units that have modified conversion coefficients).

The eleven-bit numbers n'_i from the CAMAC TDC's are contained in a CAMAC module under the sub-addresses A(0) to A(5). The constants D_x, D_y and Z_x, Z_y are each 13- and 10-bit words respectively read in from front panel switches. The maximum device word length is also 13 bits.

The event calculation is divided into eight steps synchronized by eight clock pulses. The steps are:

Step	Accumulator Content
1. $A(0) + D_x \rightarrow A_c$	$n'_{x_1} + D_x$
2. $-A(1) + A_c \rightarrow A_c$	$-n'_{x_2} + (n'_{x_1} + D_x)$
3. $A(2) + A_c \rightarrow A_c$	$n'_{x_3} + (-n'_{x_2} + n'_{x_1} + D_x)$
4. Compare A_c to Z_x (half decision)	$\left\| n'_{x_1} - n'_{x_2} + n'_{x_3} + D_x \right\| \geq Z_x$

5.	$A(3) + D_y \rightarrow A_c$	$n'_{y_1} + D_y$
6.	$-A(4) + A_c \rightarrow A_c$	$-n'_{y_2} + (n'_{y_1} + D_y)$
7.	$A(5) + A_c \rightarrow A_c$	$n'_{y_3} + (-n'_{y_2} + n'_{y_1} + D_y)$
8.	Compare A_c to Z_y (full decision)	$\lvert n'_{y_1} - n'_{y_2} + n'_{y_3} + D_y \rvert \geq Z_y$

Here A (0) through A(5) are the inputs from the coordinate TDC's while A_c is the accumulator.

The block diagram of the arithmetic part of the device is shown in Figure 3. The schematic of the arithmetic portion is shown in Figure 4. Each operation step consists of two phases: in the first phase incoming information is processed resulting in an intermediate operand. In the second phase this intermediate result is stored in a register, usually the accumulator, by the falling edge of the timing signal. Arithmetic operations are performed by a full adder composed of four IC SN7483 four-bit adders. One side of the adder is supplied by the CAMAC dataway carrying the coordinate information. The other side is fed by either the accumulator or the content of the D_x or D_y constant switches. The appropriate choice is governed by a series of SN 74135 multiplexor chips. For simplicity one's compliment arithmetic was used and negation was performed by using SN 7486 exclusive or gates. This results in no significant loss of accuracy. The absolute value operation is performed by sign analysis. When a negative value is detected the whole number is inverted. The comparison is

made using SN 7485 magnitude comparators. The output from this comparison serves as the decision for the combined algorithms (17) and (18).

The control board (Figure 5) synchronizes the proper order of arithmetic operations and issues all necessary commands to the system. Because the TDC's have a relatively long (60 μsec) conversion time a special deadtime arrangement is required (Figure 6). The falling edge of the TD CONVERT signal begins a calculation cycle. The INIT pulse opens the BUSY flip-flop and starts the step shift register. The BUSY flip-flop also initiates a 1 μsec cycle multivibrator. During the first step a "1" is clocked in the serial input of the register. The "1" passes one parallel position each step and at the last or eighth step closes the BUSY flip-flop, which in turn disables all action of the device. During the second phase of the fourth step the decision from an X plane is stored in the half decision flip-flop, and at the end of the eighth step the full decision 200 nsec wide pulse is generated in the case when the algorithm criteria are satisfied. CAMAC N and A commands are formed by combining shift pulses (Figure 7). No CAMAC function is generated because only an F (0) read function is required. This is already established on the CAMAC dataway. In the case when the device is inserted into a master slot no N address coding is necessary. However, when a standard controller must be used either a type A-2 controller or backplane N lines are required. After cycle completion the clear C command and an S2 pulse are generated.

Note that this approach requires the arithmetic be performed sequentially, that is in a clocked mode.

V. Operation and Observations

In the course of the channeling experiment at Fermilab two factors entered that decreased the need for the preprocessor. Clever programming substantially cut the read time to the disc. At the same time it was found that the absolute counting rate in the germanium single crystal has to be held to the order of ten thousand counts per second to preserve the energy resolution. It is quite likely that this situation could have been improved substantially if a more sophisticated linear electronic system had been developed or beam clipping improved. Characteristically this limitation resulted in several hundred computer triggers per second without employing a preprocessor. Based on this limitation we nearly always operated the preprocessor to add a tagging bit to the event data.

Figure 8 shows a two-dimensional display of projected scattering angles for 35 GeV positive particles with the preprocessor tagging bit on. Note that the preprocessor selects a square in this space. Figure 9 shows the y distribution of scattering angles for the same energy near the preprocessor cut. The system resolution for the preprocessor is such that tagged events drop from 90% to 10% in 19 microradians. The edge resolution of the system is consonant with system resolution due to TDC resolution and drift plane spatial resolution.

In operation the system was easy to adjust by directly observing the effect of the cut on the on-line scattering angle distribution. The D constants, incorporating the effects of the offset coordinates S_i, were used to bracket the direction of the crystal axis.

Acknowledgments

We would like to thank the other members of the Albany-Dubna-Fermilab-Lehigh-UCLA collaboration for their assistance. D. Stork and J. Kubic of UCLA were particularly helpful in exploring how the various system times affected processor design considerations.

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LIST OF FIGURE CAPTIONS

Fig. 1. Schematic layout for the channeling apparatus · DC I, II, III are drift chamber modules each having 4x and 4y readout planes.

Fig. 2. Block diagram of the preprocessor based on microslice technology.

Fig. 3. Block diagram of arithmetic portion of the discrete version.

Fig. 4. Schematic of arithmetic portion of the discrete version.

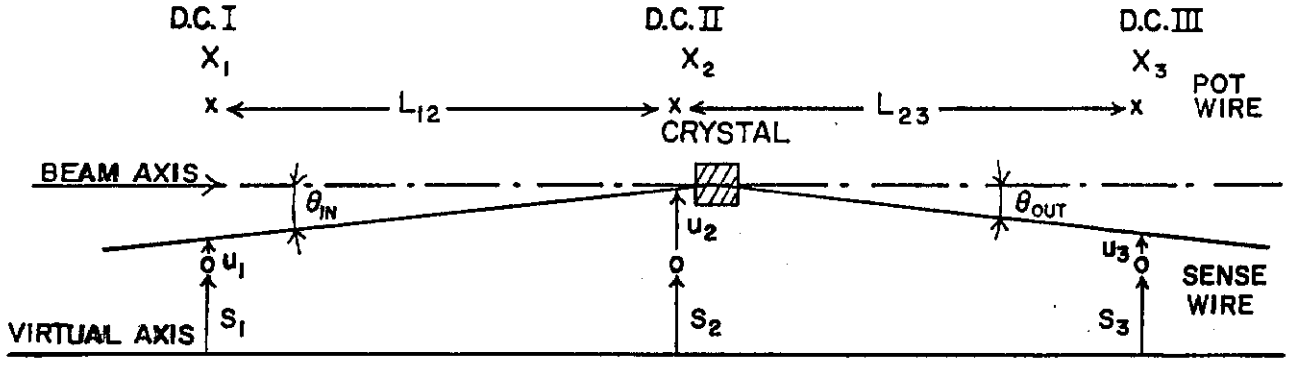
Fig. 5. Block diagram of control circuit of the discrete version.

Fig. 6. Timing diagram of the discrete syst m.

Fig. 7. Time relations of the control and CAMAC pulses for the discrete system.

Fig. 8. Two dimensional table of the projected scattering angles for a 35 GeV run with the discrete preprocessor in operation. θ_x angles read across; θ_y angles down. Angles are in microradians.

Fig. 9. Projected scattering angle distribution in y direction near the preprocessor cut. The 2σ band is twice the rms projected scattering angle resolution of the system.



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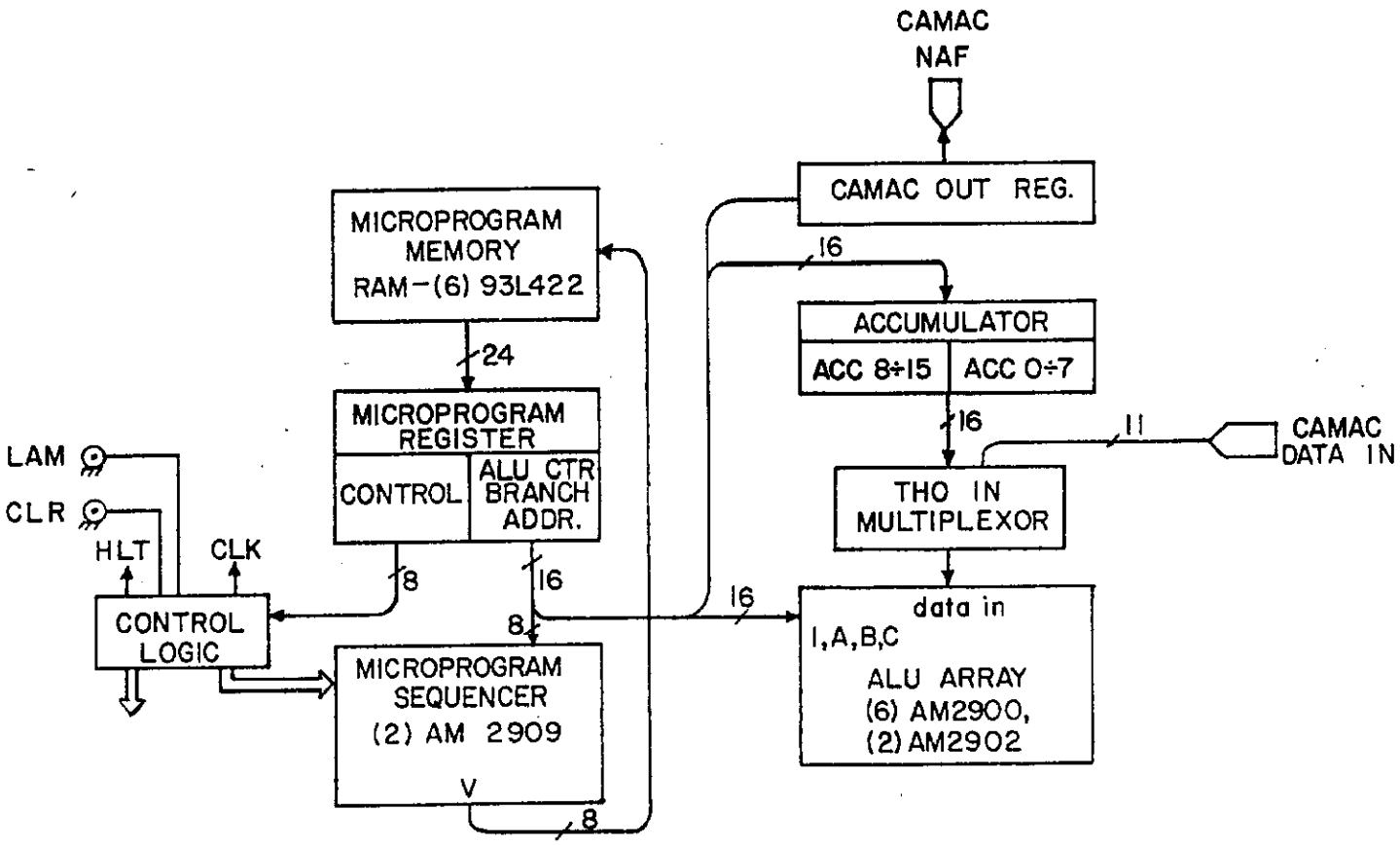

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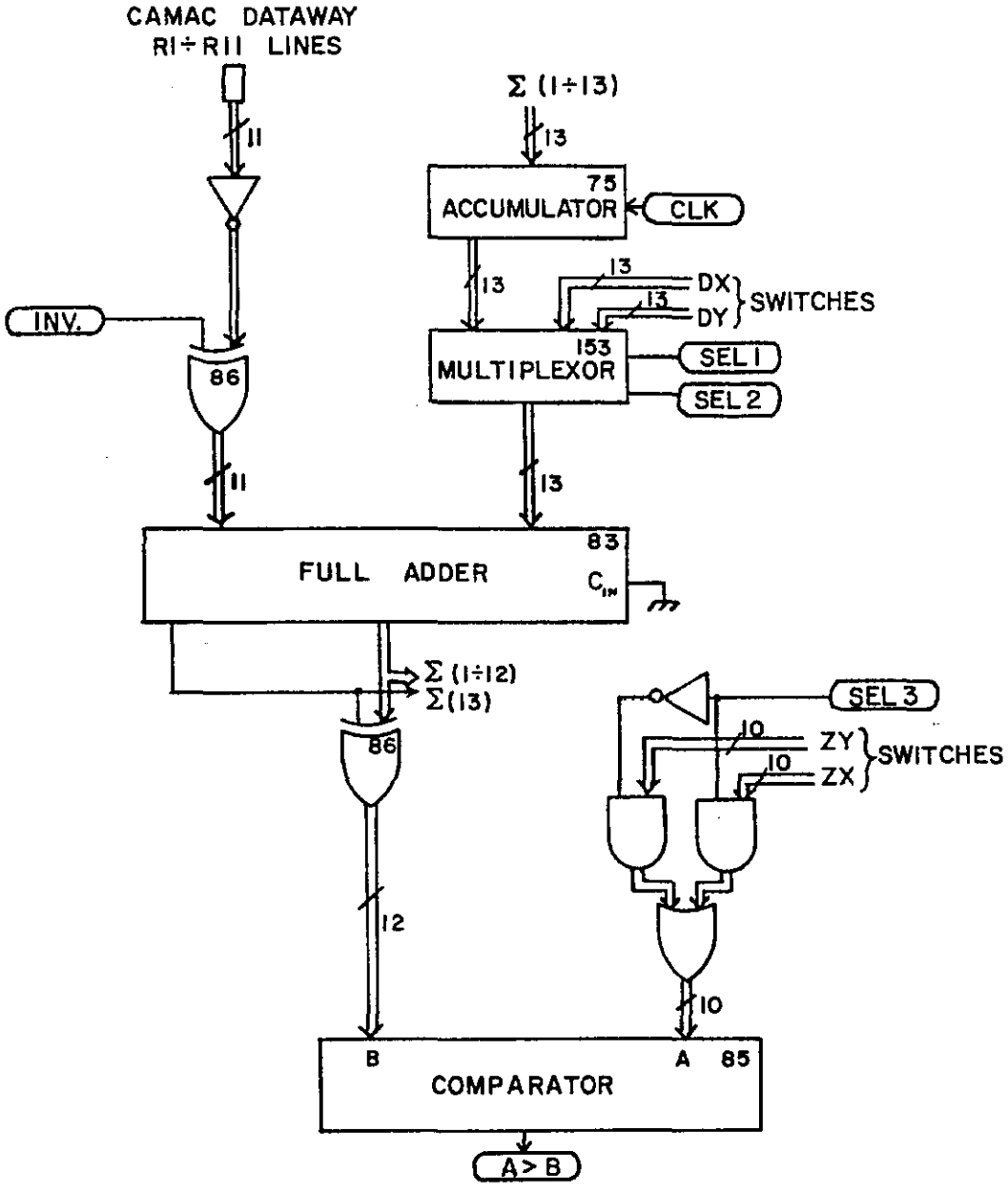

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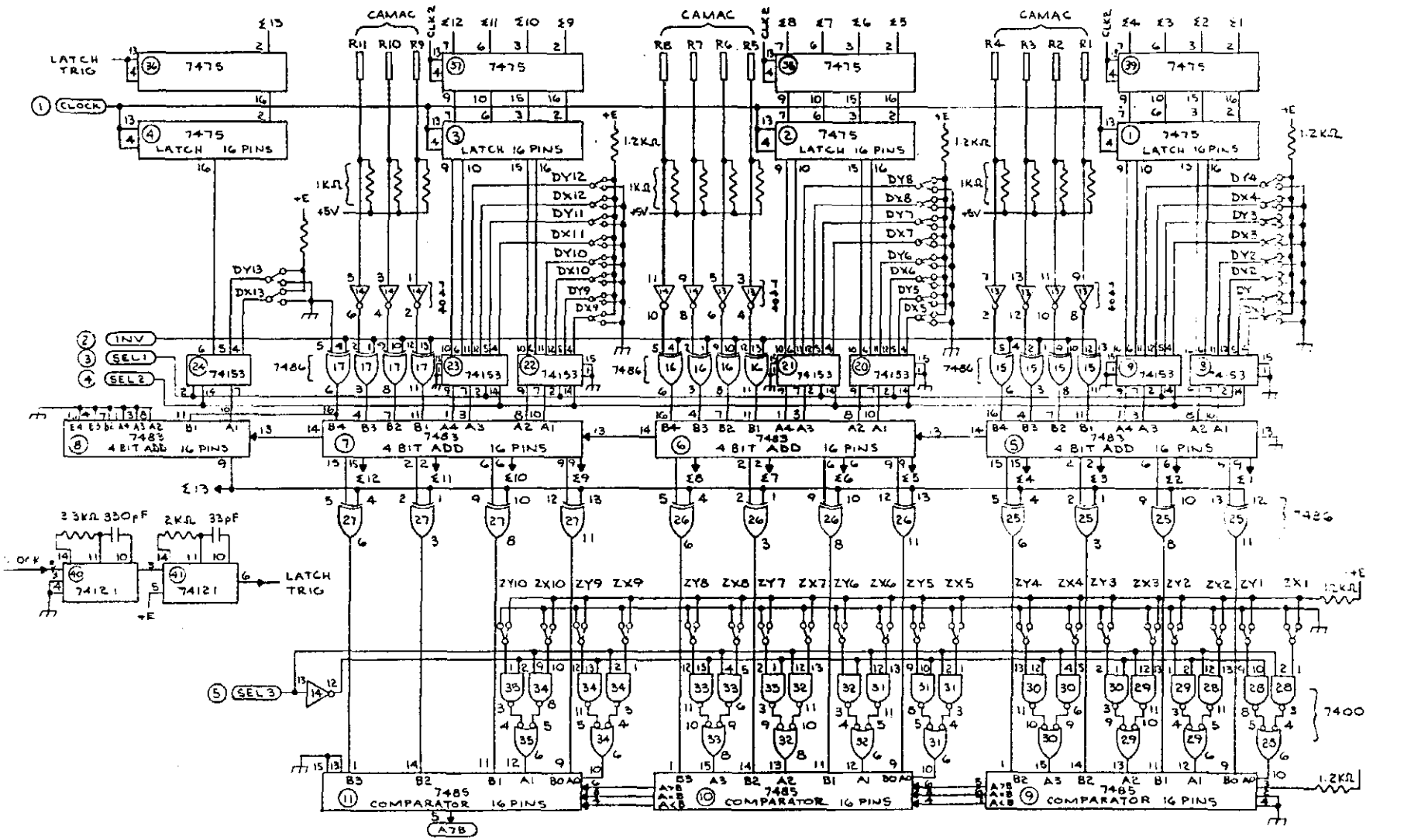


ARITHMETIC BOARD

Fig. 4. Schematic of arithmetic portion of the discrete version.

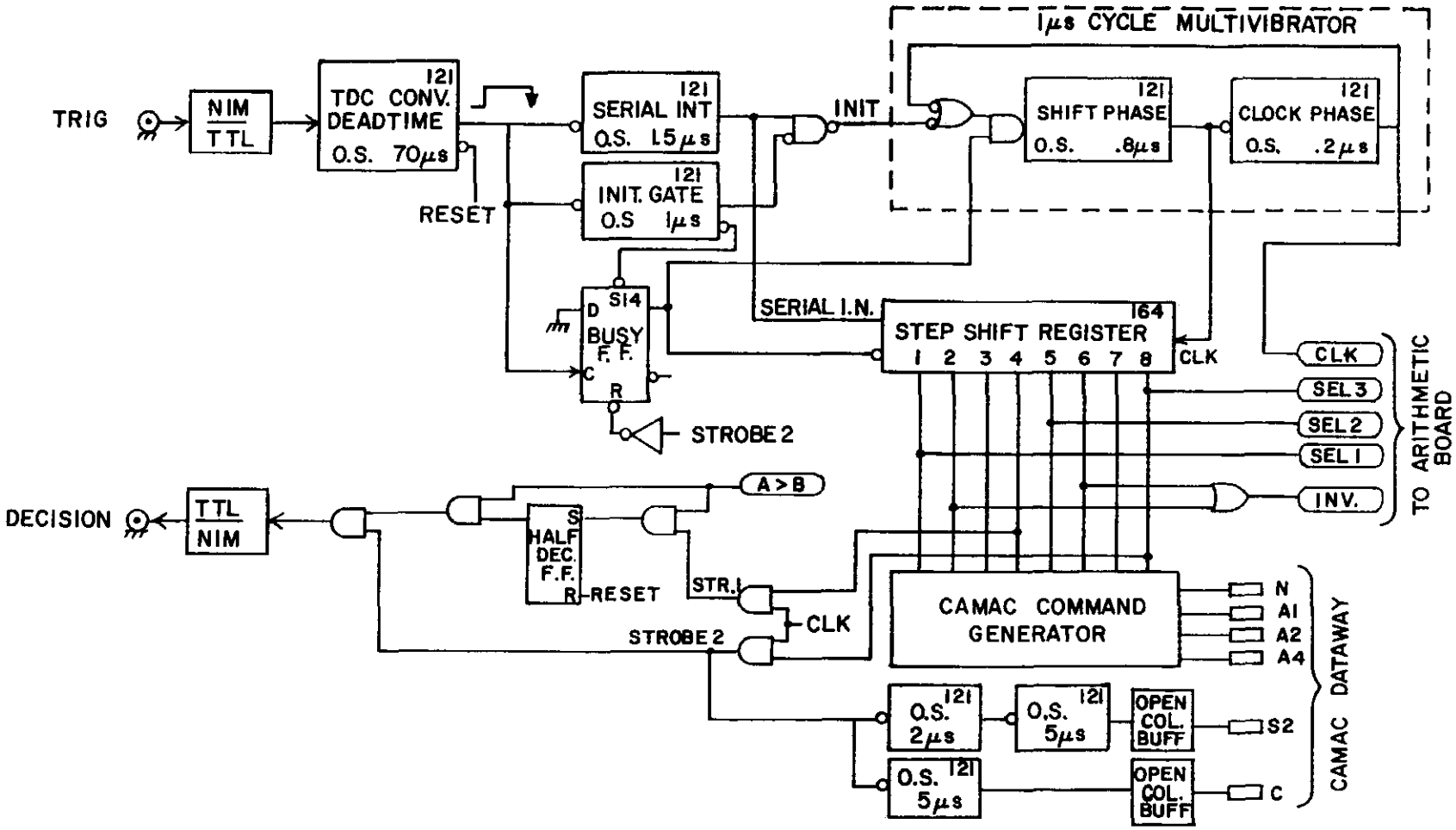


Fig. 5. Block diagram of control circuit of the discrete version.

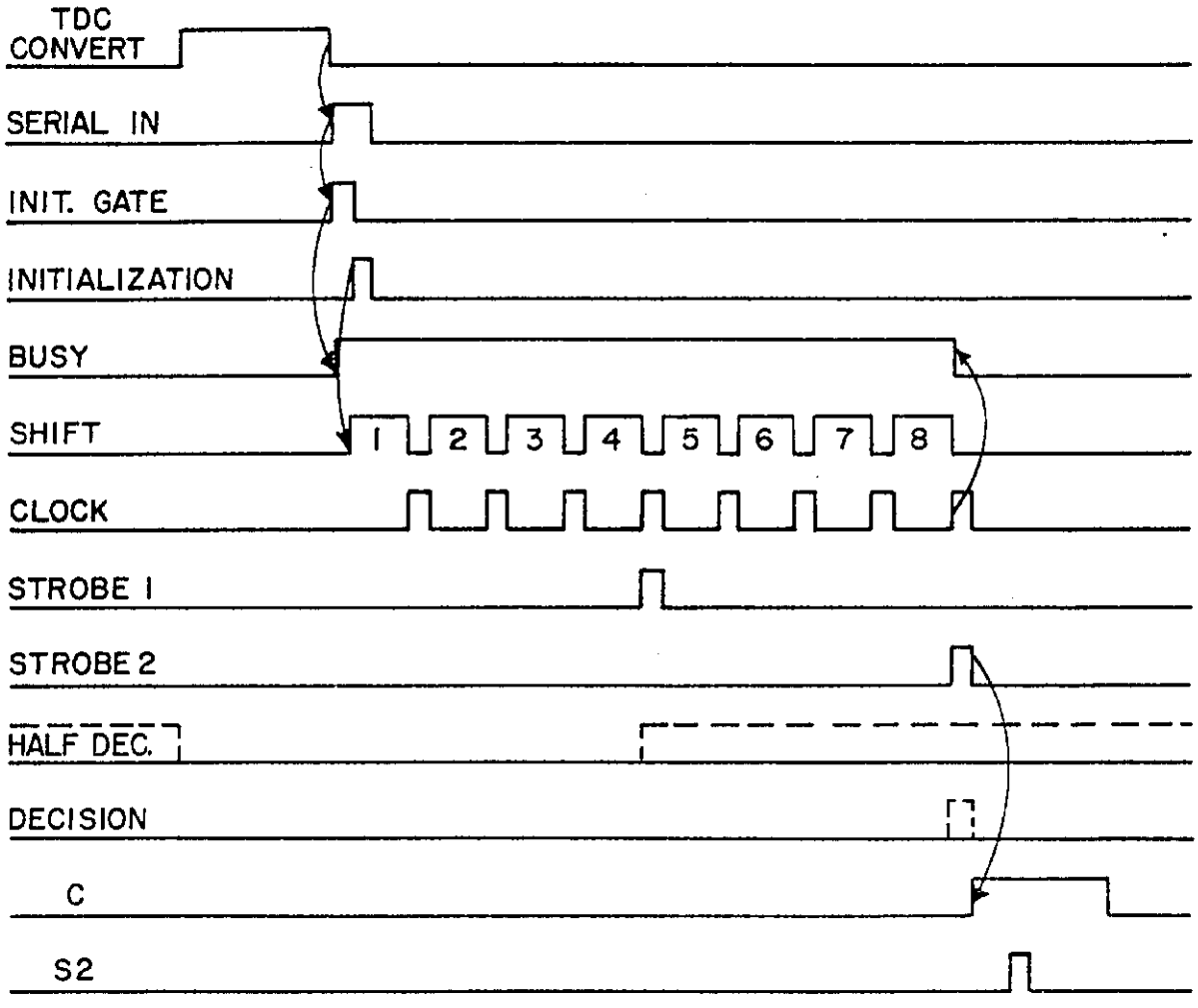
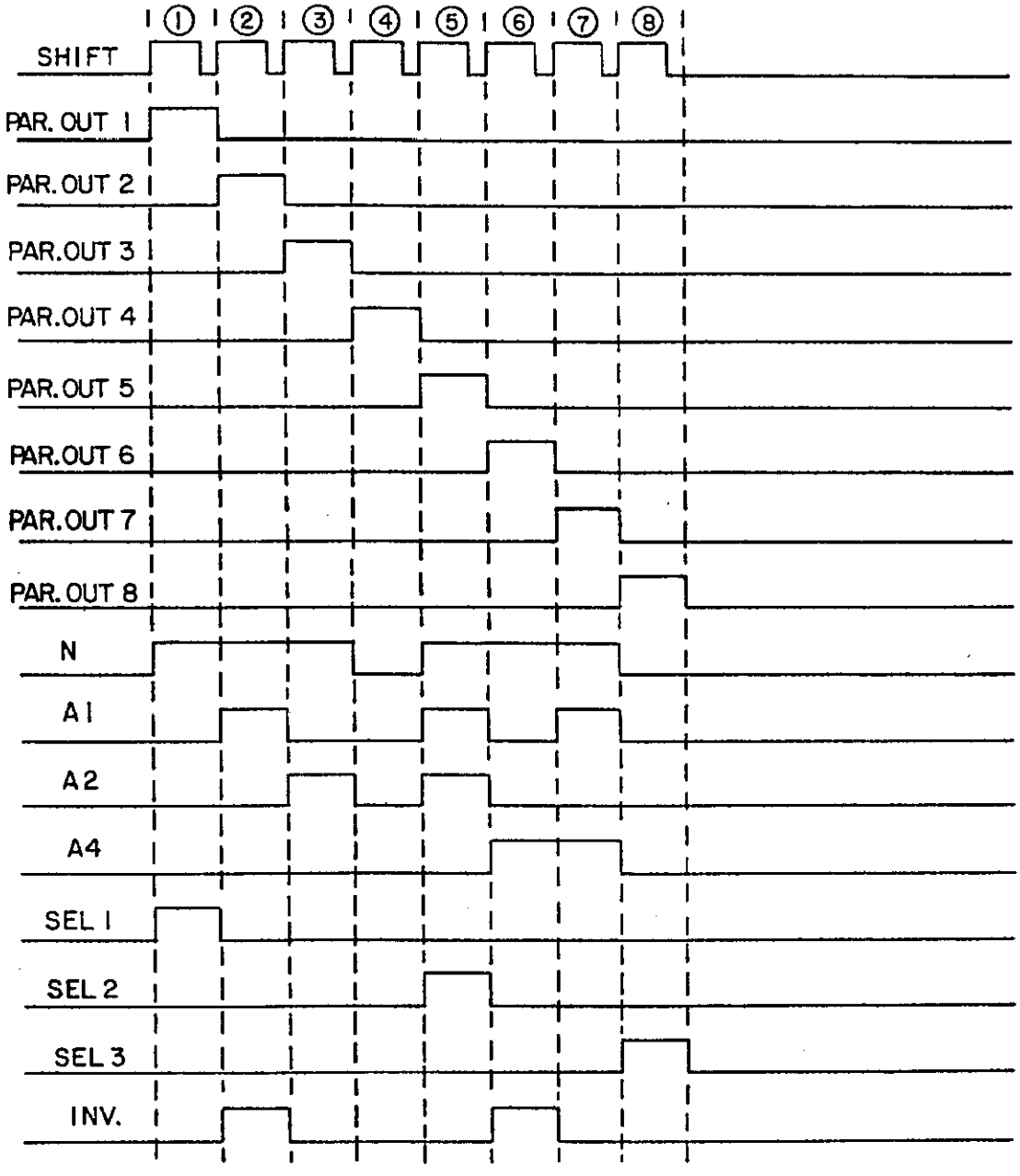


Fig. 6. Timing diagram of the discrete system.



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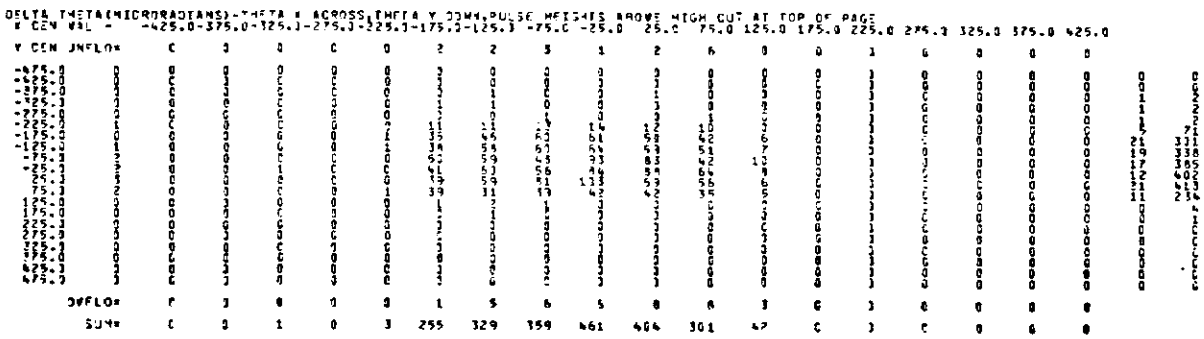

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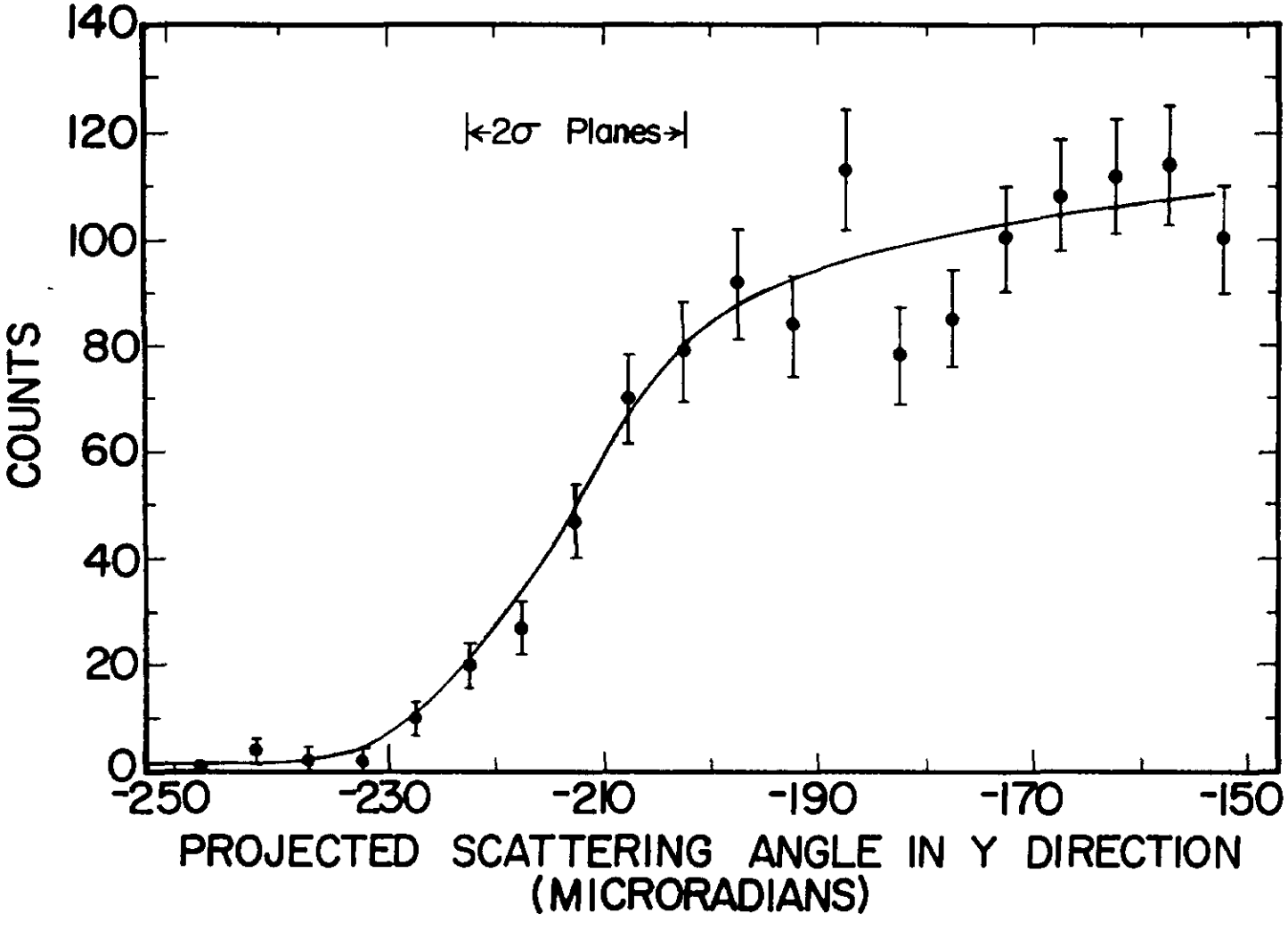

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