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The System Crate — A Modular Method of Controlling Camac Systems

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Science Research Council

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THE SYSTEM CRATE - A MODULAR METHOD OF CONTROLLING CAMAC SYSTEMS

M J Cawthraw

ABSTRACT

This report describes a range of modules which when plugged into a mechanically standard CAMAC crate make a CAMAC SYSTEM CO-ORDINATOR that can be progressively expanded from a one crate Camac system to a multi-branch multi-source system.

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March 1972

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1 INTRODUCTION

The ESONE report EUR 4100 defines the communication between Camac 'user' modules, the Camac crate dataway and the crate controller.

The ESONE report EUR 4600 defines the communication between (and within) the crate controller and the branch highway.

Neither of these reports attempts to describe how Camac systems are controlled, whether it be a simple one crate system or a multi-branch system.

This report describes how the Rutherford Laboratory HEP Electronics Group has solved the problem of modular construction of Camac system controllers.

This system was developed at the RHEL as a result of discussions on 9, 10 June 1970 at CERN between CEA Grenoble, CERN and RHEL.

2 DESCRIPTION

The system crate (SC) is mechanically identical to a normal Camac crate (including its dataway), but the dataway is not always used as defined in EUR 4100. The SC can use its dataway in two modes.

2.1 The SYSTEM MODE identified by BUSY=0 and non-standard use of the dataway. This mode is always used in every cycle and all SC modules work in this mode.

2.2 The USER (ie true Camac) MODE identified by BUSY=1 and standard use of the dataway. This mode is only used if there are Camac user modules in the SC.

3 SYSTEM CRATE MODULES

All the SC modules are constructed with metalwork and edge connectors that comply with EUR 4100 in all respects, excepting the function of the signals. The SC modules may be arranged into three categories.

3.1 SOURCE modules are the source of Camac command to the Camac user modules. There is at least one in any SC. A computer interface is usually a source module. Only one source can access the Camac system at any given time.

3.2 PRIORITY SORTER (or executive controller) determines which source module shall have exclusive use of the Camac system, and when. It occupies both of the EUR 4100 crate controller positions. There is only one in each SC.

3.3 RECEIVER modules receive the commands from the SC dataway and proceed to access the normal user modules. There is at least one in any SC. A branch driver capable of driving a branch highway in accordance with EUR 4600 is one common type of receiver.

4 ALLOCATION OF THE SC DATAWAY LINES

4.1 The following lines retain their 4100 function when in the system mode.

Power, patch pins, Z, I, X, S1 and Q

(S1 however may be stretched, see 8).

4.2 The usage of the remaining lines is dependent upon B.

B=0 during the system mode and may also be a condition for the removal of suppression of LAM signals from user modules situated in the system crate. EUR 4100 requires that LAM signals be suppressed by B, but at the time of writing this is likely to be replaced by N.

B=1 normal EUR 4100 Camac user mode.

When B=0 the new usage is as follows.

(a) EUR 4100 WRITE lines become READ/WRITE lines, so that both read and write data are conveyed on these lines when in the system mode.

(b) EUR 4100 READ lines are reallocated and used for a 24 bit control word.

EUR 4100 Line	System Mode Usage	
R1	F1	Function Code
R2	F2	
R3	F4	
R4	F8	
R5	F16	
R6	A1	Sub Address
R7	A2	
R8	A4	
R9	A8	
R10	N1	Station Address
R11	N2	
R12	N4	
R13	N8	
R14	N16	
R15	C1	Crate Address
R16	C2	
R17	C4	
R18	Br1	Branch Address
R19	Br2	
R20	Br4	
R21	M	Multi Addressing
R22	G	Grant
R23	S	Spare
R24	H	Hold

(c) EUR 4100 Clear line is used to reset the hold bistable (see 9.2.2).

(d) EUR 4100 S2 line is used to notify receiver units that the control word is steady (see 7.1.1 and 7.1.2).

(e) EUR 4100 N and L lines, it will be remembered, are a unique pair of nonbussed lines from each and every normal station to the control station. Consequently the N and L lines, unlike all the other lines, have their usage determined not by the busy signal but by their associated module type and their (patched) usage in the priority sorter.

Type of module	L line usage	L Line usage	Remarks
Camac user module	normal Camac	normal Camac	Complies with EUR 4100
source module	PLEASE (request to PS to be a source)	GO (permission from PS to be a source)	
receiver module	not used	i COMPOUND BTB state of cycle timing (allied to BTB). ii demand handling (allied to LAM and BD).	Some receivers, and branch drivers in particular, need to access two stations in order to use the two EUR 4100 L lines. i on RH, ii on LH.

5 TYPES OF SC CONFIGURATION AND THE PHASES OF THEIR OPERATION

The types of SC configuration may be divided into three categories.

5.1 A small one crate system as shown in fig 1 comprising:-

(a) one or more source units;

(b) a simple priority sorter-cum-simple crate controller, two widths wide which occupies the control station and at least one other, usually the adjacent one. This unit is also a receiver.

(c) The remaining crate space contains normal Camac user modules complying with EUR 4100.

A complete SC cycle consists of two phases.

(a) A system mode phase followed by

(b) a Camac mode phase.

5.2 A larger multi-crate system as shown in fig 2 comprising:-

(a) One or more source units in the SC;

(b) a general purpose priority sorter-cum-simple crate controller strongly related to that in 5.1 b above:

(c) one or more branch drivers capable of operating as a branch driver port in accordance with EUR 4600. Each accesses Camac user modules via a branch highway and CCA's;

(d) the remaining space in the SC can be occupied by Camac user modules.

In this type of configuration the user modules are situated in both the SC and the other crates dedicated entirely to user modules. The user modules in the SC are accessed in a similar manner to those in 5.1 above. The user modules not situated in the system crate are accessed by a system mode cycle in the SC which generates and runs concurrently with a normal Camac cycle in the crate wherein the user modules are situated.

5.3 In many systems (see fig 3) with several source units and branch drivers the physical room left for user modules in the SC is usually limited and so a simpler system, with fewer types of modules, may be built if the user modules are omitted from the system crate. In most cases the space vacated in the SC can be usefully employed housing 'Camac' units that merely take power from the dataway. Such a system comprises:

(a) one or more source units in the SC;

(b) a general purpose priority sorter (without crate controller facility);

(c) one or more branch drivers.

As in 5.2 above, the user modules are accessed by a system mode cycle in the SC running concurrently with a normal Camac cycle in the user crate.

6 THE INITIAL STAGE OF THE SC CYCLE (see fig.4 and 5)

6.1 Any source unit which wishes to use the system issues the signal PLEASE to the PS (the PS is assumed to be of a suitable type) via its own 'L' line. Note how this signal is similar to the EUR 4100 LAM. (PLEASE is affected by other signals BUSY and HOLD but we need not concern ourselves with these yet, see 9.2.1). Several source units may issue PLEASE simultaneously.

6.2 Only when the PS knows that it is satisfactory to allow the source with the highest priority the sole use of the system does it send the signal GO to the source unit on its own 'N' line. Note how this signal is similar to the EUR 4100 station

number. This constitutes the beginning of an SC cycle.

6.3 Normally a source removes PLEASE on receipt of GO. As will be seen later however, retention of the PLEASE appreciably beyond this time enables the source to extend the dataway cycle.

6.4 On receipt of GO the source puts its 24 bit command word into the EUR 4100 read lines. There is a total of 14 lines for function code, sub-address and station number (5F, 4A and 5N) and they correspond to EUR 4600 usage. The crate is selected by 3 binary coded crate address lines C1, C2 and C4, and the receiver by 3 binary coded branch address lines Br1, Br2 and Br4. The usage of the 4 remaining bits is explained in 9.2, 11 and 12. Up to this point in the cycle the PS (assumed to be suitable for the application) does not know whether it will be required to access Camac modules in the SC or elsewhere. The remaining part of the SC cycle differs according to the information carried by the command word.

7 THE LATER STAGE OF THE SC CYCLE (see fig.4 and 5)

Proceeding on from the initial part (6 above) the simpler alternative is the case where:

7.1 Source unit accessing Camac modules situated outside the SC.

7.1.1 The PS examines the branch and crate address 400nS after it sent GO to the source unit. By this time all information on the SC dataway is stabilised. If the address shows that the Camac module is situated outside the SC then immediately it issues S2. This S2 with NOT BUSY is called S2(1) or receiver strobe.

7.1.2 Immediately the receiver, usually a branch driver, recognises by decoding the branch address that it is being addressed at S2(1) it retransmits the CNAF part of the command word (together with write data, if any) onto the branch highway. The function code bits F16 and F8 determine the direction of data flow between the branch highway and the SC dataway. As a precaution against the effects of momentary faulty addressing a small delay occurs before the branch driver generates BTA (see EUR 4600 5.5.1).

7.1.3 The addressed crate answers on its own BTB line and the branch driver computes a single signal COMPOUND BTB as suggested in EUR 4600 5.1. In this case however, the source is only requesting a single crate operation and so the BTB in question, and compound BTB, become essentially the same. Compound BTB is sent to the PS on an 'L' line from the branch driver.

7.1.4 On receipt of compound BTB the PS knows that Q (and read data, if any) is stabilised on the SC dataway and can be examined by the source. The PS indicates this state by issuing S1.

7.1.5 The branch driver removes BTA from the branch highway at a time coincident with the rear edge of S1. The rear edge of S1, instead of 200 nsec after the receipt of the leading edge of BTB, is used since it allows the source to operate an S1 stretch circuit (see 8). S1 can be looked upon as a source strobe.

7.1.6 The removal of BTA produces, in due course, the removal of BTB as described in EUR 4600, section 5. The ensuing removal of compound BTB informs the PS that the addressed CCA has completed its Camac cycle and consequently the SC cycle should also be completed. The PS completes the cycle by removing the GO to the source and this causes the source to remove the control word (together with write data, if any).

Alternatively, the initial part (6 above) may be followed by the more complex case where:

7.2 Source unit accessing Camac modules situated within the SC.

7.2.1 As in 7.1.1 the PS examines the branch and crate address 400 nsec after it sent GO to the source unit. If however, the address shows that the Camac module is situated within the SC then the PS (or rather the crate controller part of the PS) reads, and stores, the relevant part of the control word. The PS then switches the SC to the Camac mode phase by issuing BUSY. Busy instructs the source to remove its control word from the read lines but does not affect the write data, if any, on the write lines. This operation frees all the 24 read lines for their Camac mode usage.

7.2.2 The PS accesses its control word register that it loaded as in 7.1.1 and performs the Camac cycle in the approved EUR 4100 manner. If the function code shows that a read cycle is being executed then the PS reads the data from the read lines and simultaneously retransmits them onto the write lines. Refer to fig 7 of EUR 4600 and see a close parallel with the CCA.

7.2.3 The PS issues S1 400 nsec after the command word. As in 7.1.4 the source examines Q and the read data, if any, from the EUR 4100 write lines at S1.

7.2.4 The PS issues S2 according to EUR 4100 and completes the cycle by removing BUSY and GO. This EUR 4100 type S2 (ie with BUSY) is called S2(2) see 7.1.1.

It is most important to note:

(a) A receiver ignores the S2 line if BUSY is a logical one. It will be remembered that BUSY is mandatory during a Camac cycle.

(b) A Camac module ignores the S2 line if it is not simultaneously addressed by N, Z or C.

8 S1 STRETCH

In some applications it is advantageous to be able to extend the SC cycle under the direction of the source, eg extend the BTA-BTB 'handshake' back to the source.

Under normal circumstances PLEASE is removed upon receipt of GO, but if a source wishes to extend the cycle it does not remove PLEASE until it has examined Q (and read data if any). The SC cycle proceeds as in 7 until either S1 occurs, which has a minimum duration of 200 nsec, or PLEASE is removed, whichever occurs last. The S1 stretch circuit is situated in the PS

9 PRIORITY QUEUING AND THE HOLD LINE

The Rutherford Laboratory PS type RL 211 has the following properties:

9.1 Normal Queuing

The PS allocates the usage of the system to the sources on the 'first come first served' principle, and each cycle is treated afresh. Priority is determined by the patching in the PS. If two or more sources send PLEASE simultaneously to the PS, the PS accepts the source with the highest priority call on the system. The remaining sources retain their PLEASE signal to the PS and at the end of the first cycle the one with the next highest priority is serviced. The first source cannot monopolise the system because it cannot send its second PLEASE sooner than the others as these are already waiting at the PS. This could be overcome by allowing a source to send a second PLEASE before its current GO has ended but this has difficulties, eg possibly invoking the S1 stretch facility. This type of priority structure means that if more than two sources each try to monopolise the system then the two with the highest priority take alternative SC cycles whilst the remainder are locked out completely. It is possible of course, to replace this type of queuing organisation with a cyclical organisation and not disturb the philosophy of the SC.

9.2 Hold Facility

9.2.1 Hold Line

In many instances it is simpler, and sometimes essential that a source be allowed to monopolise the system throughout a consecutive chain of cycles, irrespective of its original priority. The HOLD (H) bit, R24, of the control word enables this to be achieved.

Such a source obtains the use of the system in the normal way by means of the signals PLEASE and GO. The source issues its control word with the H line at a logical 1 and keeps it there as long as the source intends to monopolise the system, but nevertheless it is still removed whenever BUSY is present. The source resets H

to logical 0 sometime after receipt of its last GO. HOLD is not removed between SC cycles. The other sources (ie those not receiving GO) each remove their PLEASE whenever the H line is at 1 or whenever BUSY is present. This frees R24 for its normal usage. As a precaution against breakthrough of unwanted PLEASE(S) it is good practice to delay, by say 200 nsec, the (re-)issue of PLEASE from these unacknowledged sources when BUSY disappears. This delay ensures that the H signal from the currently active source has time to re-establish itself on the SC dataway (after also being gated off by BUSY) and thereby continue to suppress these unacknowledged sources issuing PLEASE.

9.2.2 Hold Time-Out

If a source sets the HOLD line to logical 1 and at the same time, due to hardware or software error, it does not proceed to use the system then a system lockout occurs. Easier fault diagnosis and often fault rectification result from the HOLD line time out circuit in the PS.

If the HOLD line is at a '1' for a period in excess of some predetermined value, and in addition no SC cycle occurs throughout this period, then the PS generates a train of 'clear hold' pulses on the EUR 4100 CLEAR line until this lock up state is removed. All sources disengage themselves from the hold line on receipt of this CLEAR HOLD signal. No S2 pulse is employed, but the effects of possible cross-talk are removed by integration of the CLEAR pulse in each source. Early Camac modules may not gate clear with S2 and consequently cannot be used in the SC with this time out operative.

10 SYSTEM CYCLE TIME-OUT

The timing of the EUR 4600 branch highway is a 'handshake' operation. This type of timing has the disadvantage that if, for any reason, a branch driver does not receive an answer on the correct BTB line when it addresses a crate, then the branch locks up. Similarly, in the SC this possibility applies to the branch address as well. Consequently the PS has a system cycle time out circuit. This circuit detects several types of error state and notifies this fact to the current source by omitting S1 from its current SC cycle. GO is removed automatically by the PS after the allowed time has expired. What the source does in consequence is a matter of source design, but it is sometimes helpful if it generates an interrupt that raises a diagnostic program. It is both simple and useful if there is a time out light on the source's front panel. This light is switched on by the leading edge of GO and switched off by S1 GO. After a little experience with any given set up the lamp brilliance can be very informative, eg

(a) out - source inactive or cycling slowly.

(b) dim - source probably running correctly.

(c) bright - time out has occurred.

The time out circuit detects the following faults.

(a) Compound BTB initially incorrect. This may be due to BTB being high at the beginning of a branch highway operation.

(b) Compound BTB initially correct but does not change. This could be due to BTB being permanently low.

(c) Compound BTB incorrect at a time = value of time out after the SC cycle commenced. This could be due to a faulty crate controller timing circuit.

The Rutherford PS only responds to the compound BTB from the addressed receiver although a simple OR would suffice. This avoids errors due to faulty compound BTB from unaddressed receivers.

11 MULTI-CRATE (OR PARALLEL) ADDRESSING

The EUR 4600 specification permits multi-crate addressing and the seven individual BCR lines are provided for this purpose. The SC, however, has only three binary coded crate address lines and consequently straightforward multi-crate operations are impossible. The SC uses indirect addressing, invoked by the M bit (EUR 4100 R21) of the control word, for multi-crate operations.

In a multi-crate operation the crate addresses are derived from the contents of a seven bit MULTI-CRATE REGISTER situated in the branch driver. Prior to the operation this register is loaded from bits W1-W7 (C1 corresponds with W1 etc) of the SC dataway by the code

M(0) Br (X) C(0) N(30) A(Any) F(16)

The multi-crate operation is executed by the code M(1) Br(X) C(0) allied with the required NAF.

Lamps on the front of the branch driver indicate the contents of the multi-crate register.

12 INTERRUPT HANDLING IN THE SC

According to EUR 4600 when any Camac LAM source requires attention it alerts the branch driver (and all beyond) by means of the single branch demand signal BD. In due course the branch driver performs a grant cycle by issuing BG (accompanied by crate address) and as a result obtains a 24 bit LAM pattern on the read lines. Since the SC complies with EUR 4600 we need only concern ourselves here with what happens to BD after it arrives at a branch driver and up until the consequential BG is transmitted by the branch driver.

The branch driver sends BD on one of its 'old' L lines to the PS. The BD is not affected by SC busy. A Camac user module in the SC sends its LAM to the PS-cum-crate controller in the normal manner. In either case a demand arrives at the PS on an L line. All of these demands request storage in a store. The first demand to arrive at the store is stored and simultaneously makes the store ignore the remainder. Sometimes however, several demands may arrive either simultaneously, or during the inevitable race period of the store's entry gate, and so the store may have more than one demand stored. The contents of the store are put into a (wire patched) priority queue and the highest priority demand present is encoded and transmitted onto the SC dataway during NOT BUSY. The actual information transmitted onto the SC dataway is the branch address of the module generating the LAM demand. The branch address is in binary code and uses the EUR 4100 lines A4, A2 and A1 to convey Br4, Br2 and Br1 respectively.

All sources which service LAM demands examine these A4, A2 and A1 lines during NOT BUSY. Whenever a source recognises a branch address that is of consequence to it in the context of LAM demands, it stores this branch address in a branch register (G). Note that this second branch register is independent of the normal command branch register. What happens thereafter is a matter of source design but a typical computer interface for example, sends an interrupt to its computer. The computer services this interrupt by executing a Camac GRANT cycle, as described in EUR 4600 section 5.2. Alternatively a source unit, upon receipt of this SC demand, could organise a GRANT cycle autonomously.

In order to do this the source issues PLEASE, unless the SC HOLD line is at logical 1, and receives GO exactly as in a command mode operation. On receipt of GO the source issues the control word GBr(X) where G is the GRANT bit (EUR 4100 R23) and Br(X) is the branch address stored in the branch register (G). In order to guarantee contiguous cycles the H bit is normally set as well, but it is not essential: the control word then becomes H.G.Br(X). The addressed branch driver organises the required GRADED L operation and obtains a 24 bit GRADED L PATTERN on the branch highway from all the on-line crates. The branch driver transmits this pattern onto the SC dataway R/W lines in a similar manner to that for a read operation. The computer interface stores this graded L pattern at S1 and it is subsequently (or simultaneously) read by the computer. If the computer wishes to take further immediate action it can guarantee to do so only if it maintains the H line at logical 1 in the meantime.

The EUR 4600 specification allows the system designer complete freedom to choose the format of his 24 bit GRADED L PATTERN. If it is essential to know which branch the L pattern came from then the quick and simple method is to reserve 3 bits in the branch GRADED L PATTERN (ie within the LAM grader patching) so that the interface can insert the branch address in these 3 bits by accessing the contents of the branch register (G). If this option is taken a sensible allocation is bits 8, 9 and 10 for Br1, 2 and 4 respectively since this leaves bits 1-7 for the crates. Alternatively, at the cost of an extra computer input cycle the branch address register (G) can be read as a separate word.

Although not built into the present Rutherford PS it may be that speed is essential when servicing interrupts. If so it is fairly simple to dynamically alter the queuing structure, in the presence of a branch demand, and permit the source which services the demand to jump to the head of the queue.

13 SIGNAL STANDARDS OF THE SC DATAWAY

The possibility of using Camac modules in the SC determines most of the signal standards employed. The only deviation from table VI of EUR 4100 concerns SC modules which receive signals on the EUR 4100 R Q and X lines. This table shows that the total current taken from each of these lines by all modules must not exceed 6.4 ma: this value is determined by the drive capability of existing Camac modules. The use of normal TTL to sense these lines limits the number of receivers to four. Suitable alternative gates are the low power TTL and the OR and NOR gates of the Signetics utilogic 2 series. Low power TTL is reputed to have a much wider spread of input threshold voltage than normal TTL. If so, it may cause trouble in the future due to poor noise immunity at the low voltage (0.8v) threshold even though it is still within the Camac specification. To date we have not experienced malfunctioning due to this cause. The Signetics gates behave excellently in this respect, but unfortunately have a comparatively large power dissipation. It is recommended practice to use the Signetics gates.

ACKNOWLEDGEMENTS

The author wishes to acknowledge the contribution of F Iselin and his coleagues, of CERN, and J Lecompte, of CEA Grenoble, during the initial discussions. The author also wishes to acknowledge the contribution of his colleagues, named in Appendix I, for their many suggestions and refinements, and the encouragement of P Wilde Electronics Group Leader.

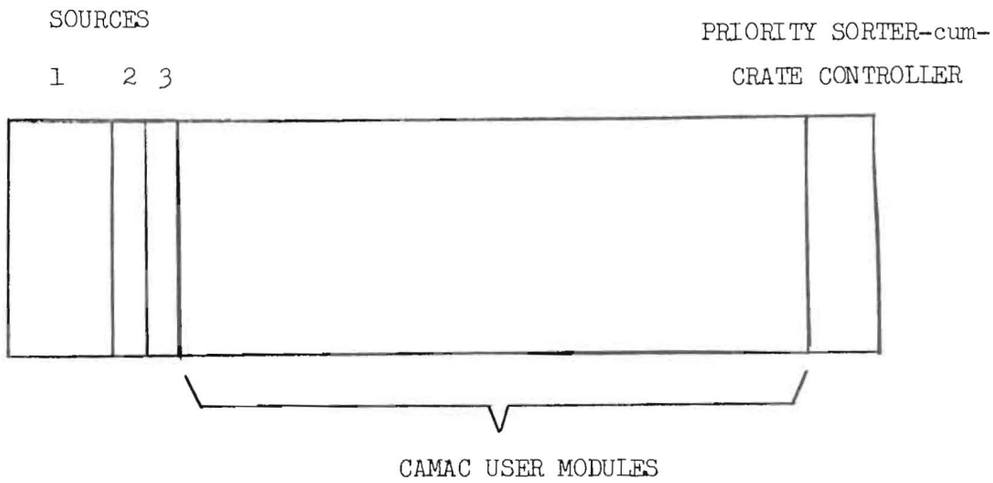

SOURCES
1 2 3
PRIORITY SORTER-cum-
CRATE CONTROLLER
CAMAC USER MODULES

FIG 1

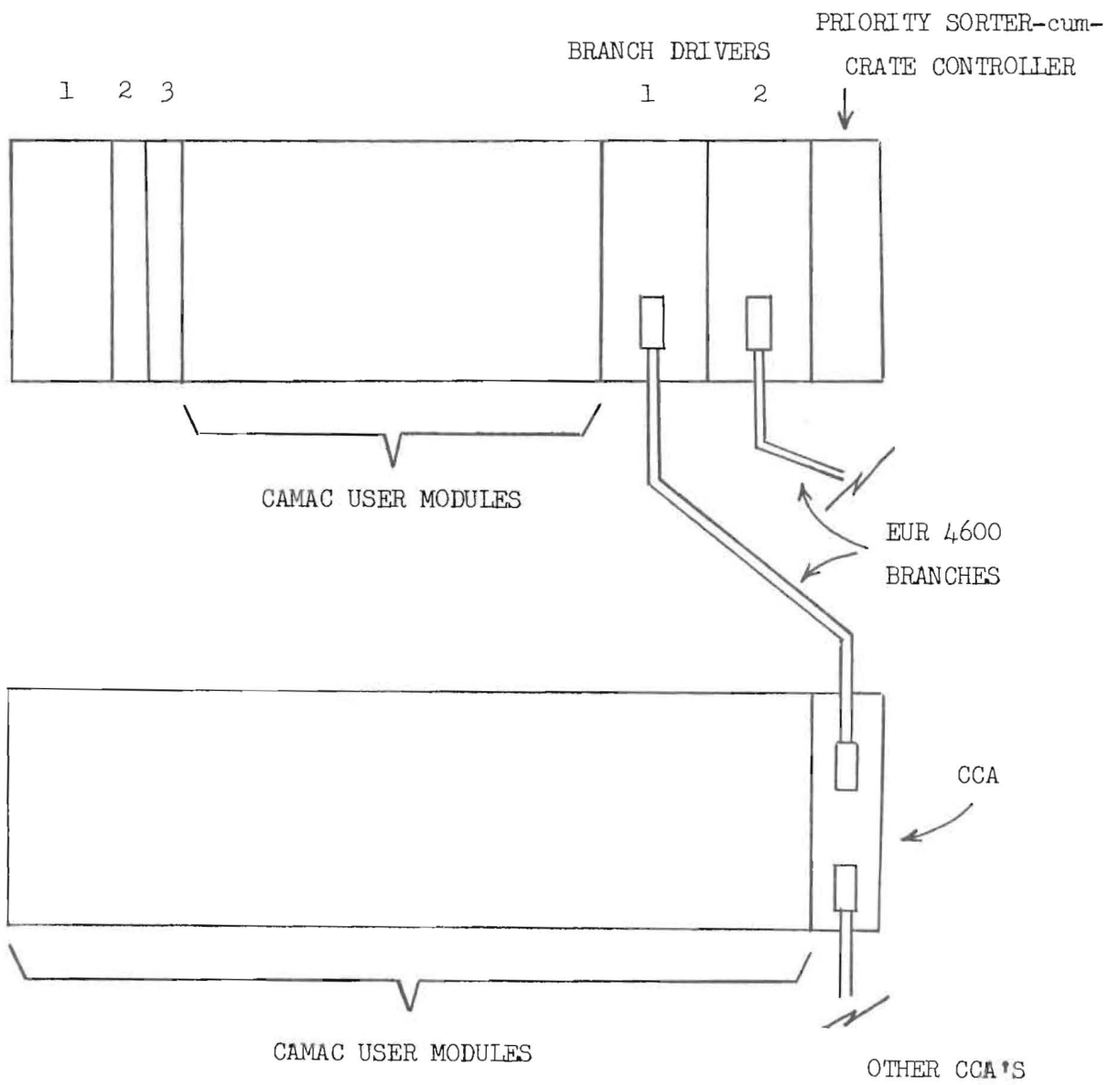

PRIORITY SORTER-cum-
CRATE CONTROLLER
BRANCH DRIVERS
1 2 3
1 2
CAMAC USER MODULES
EUR 4600
BRANCHES
CCA
CAMAC USER MODULES
OTHER CCA'S

FIG 2

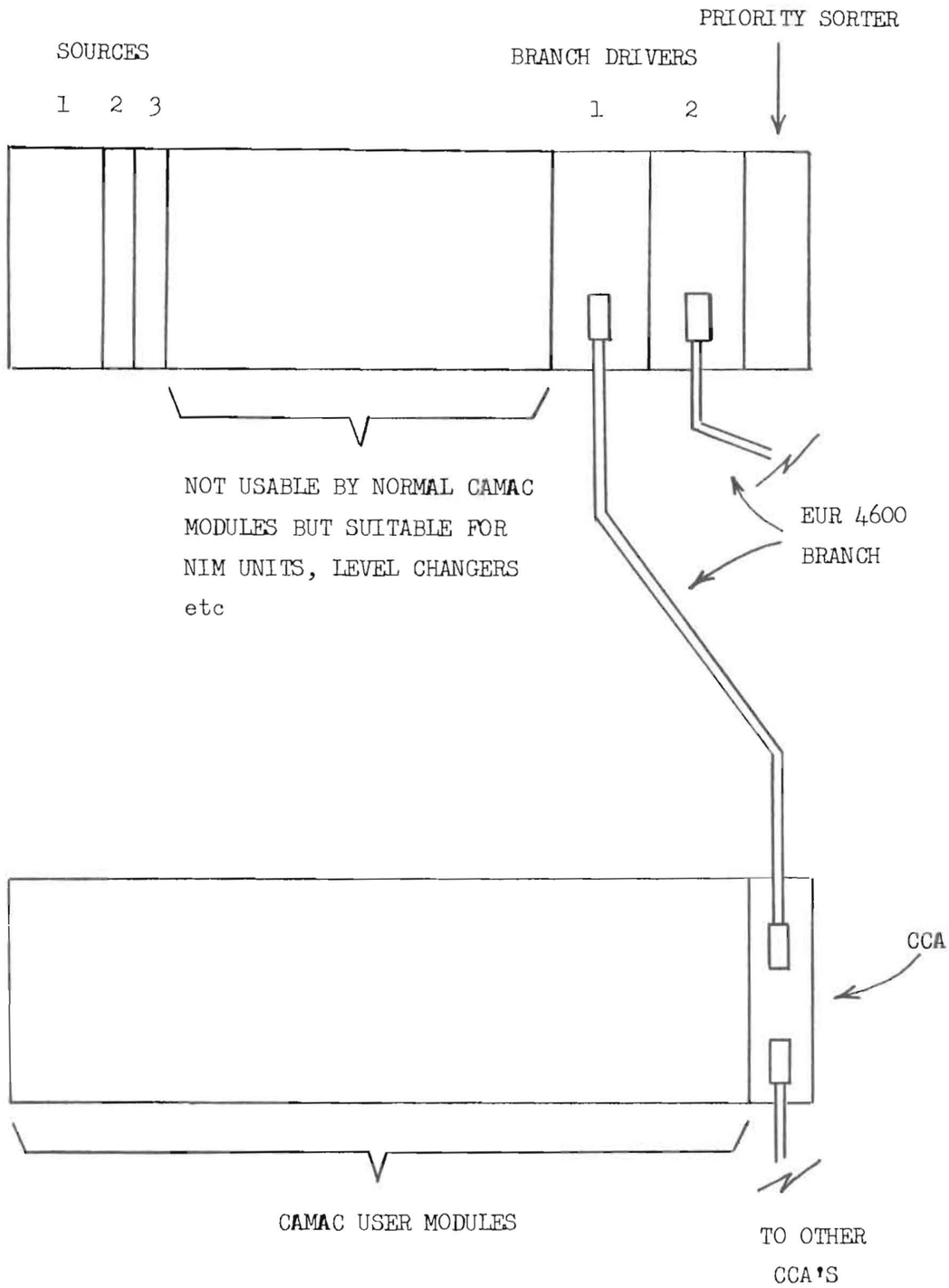

PRIORITY SORTER
SOURCES
BRANCH DRIVERS
1 2 3
1 2
NOT USABLE BY NORMAL CAMAC MODULES BUT SUITABLE FOR NIM UNITS, LEVEL CHANGERS etc
EUR 4600 BRANCH
CCA
CAMAC USER MODULES
TO OTHER CCA'S

FIG 3

SOURCE UNIT DRIVING A BRANCH DRIVER TYPE RECEIVER

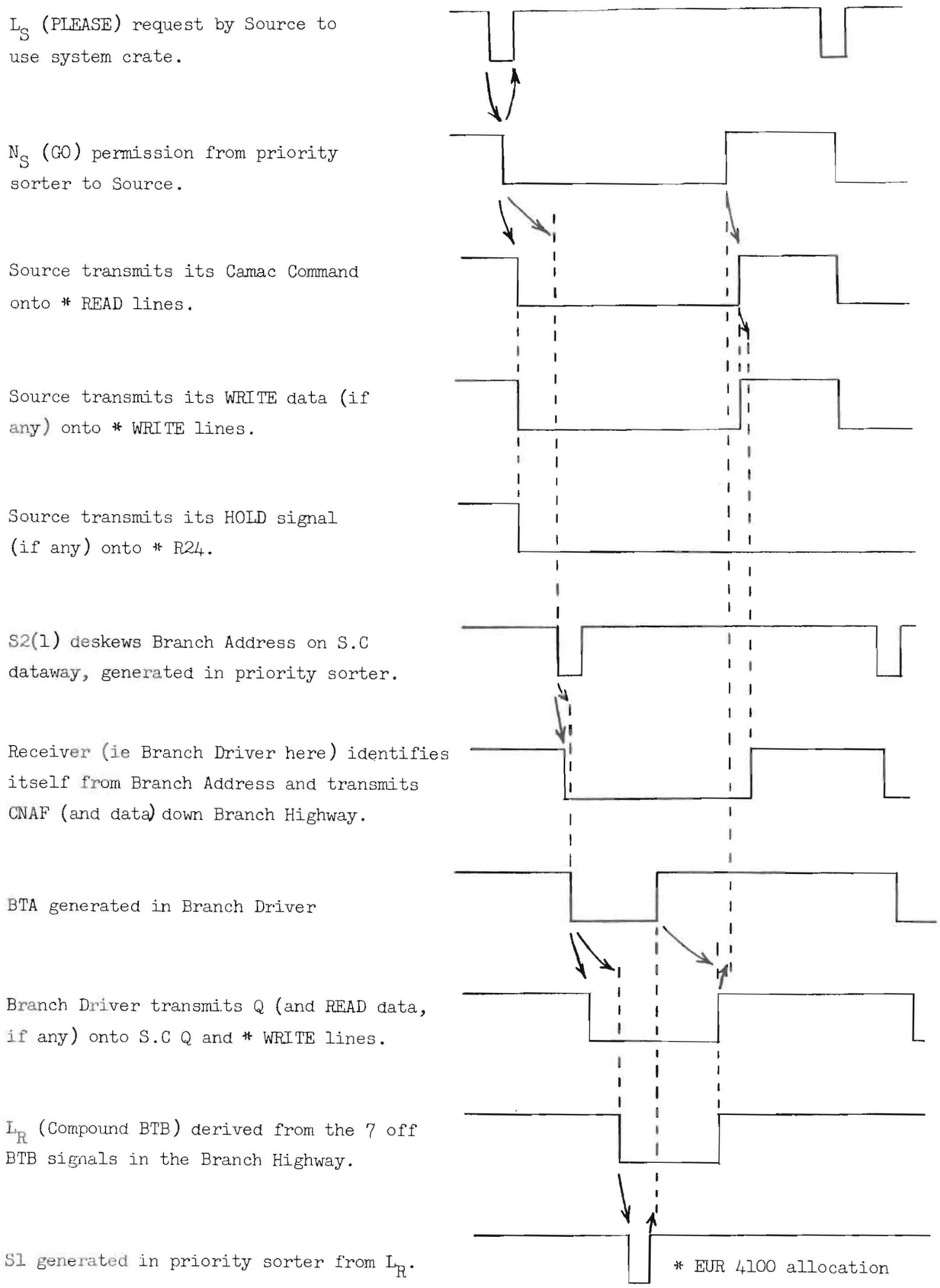


FIG 4

SOURCE UNIT DRIVING A SYSTEM CRATE CRATE CONTROLLER

L_S (PLEASE) request by source to priority sorter to use system crate.

N_S (GO) permission from priority sorter to source.

Source transmits its command word onto * READ lines and subsequently gated off by BUSY.

Source transmits its WRITE data (if any) onto * WRITE lines.

Source transmits its HOLD signal (if any) onto * R24 line.

S2, the S2(1) ie with NOT BUSY is used within the SCCC to store the command word. The S2(2) is the normal Camac S2.

BUSY may be transmitted by SCCC as soon as it has stored the command word at S2(1)

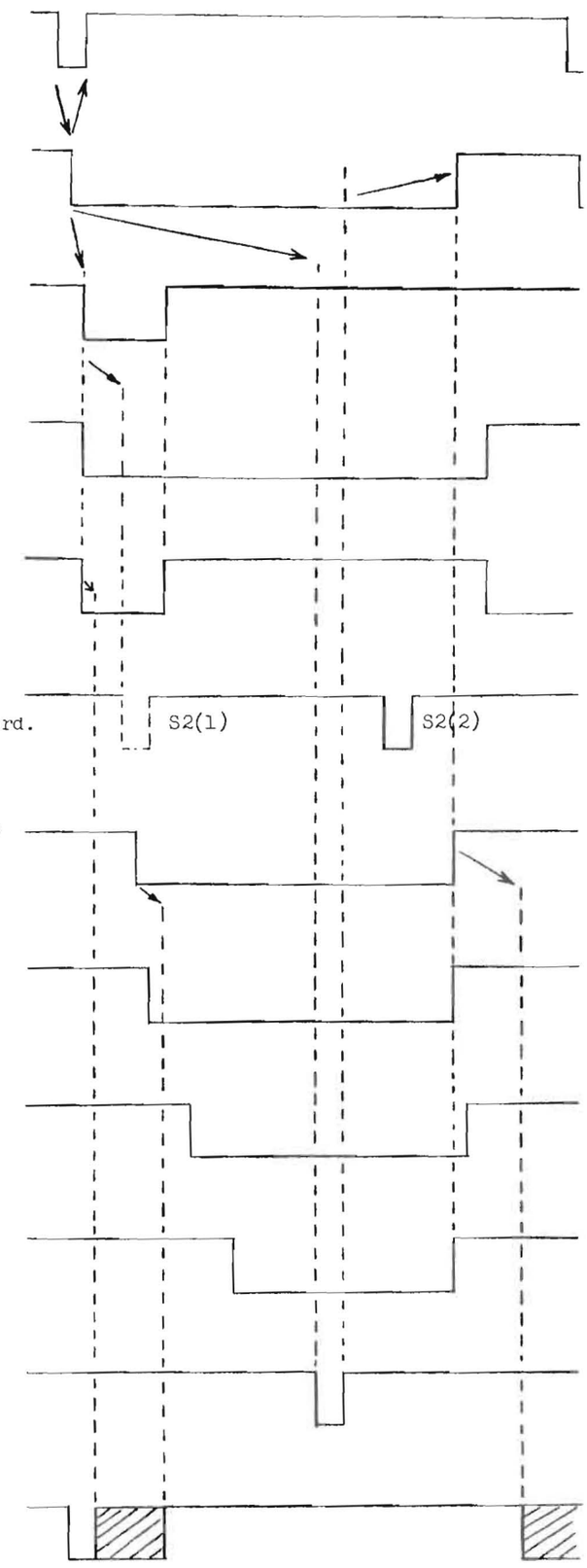
NAF transmitted from SCCC for EUR 4100 cycle.

Q and READ data (if any) on respective lines.

READ data transmitted by SCCC onto WRITE lines.

S1 trailing edge determines end of GO.

PLEASE from a second source suppressed by HOLD (if any) OR stretched BUSY.



* EUR 4100 allocation

FIG 5

APPENDIX I

This appendix outlines the units either in use or about to be, at the Rutherford Laboratory and the Rutherford Laboratory's experiments at CERN. All are finished in rail red colour in order to distinguish them from normal Camac units. The design authority is given in parenthesis.

RL 211 Priority Sorter (M Cawthraw)

This two width module has already been described in the text. It does not cater for Camac modules situated in the system crate.

RL 212 Transfer Controller (R Downs)

This two width source unit transfers data between Camac modules without the aid of a computer.

It contains a 24 bit data register into which data can be written and read. The Camac commands which test for, and carry out, transfers are generated by a remote diode matrix plugboard. The same Camac command sequence is employed for each pair of modules and consequently the modules must interpret these Camac commands in a uniform way. The modules use the Q line as a status flag to indicate their ability to accept or receive data. A standard b asic Camac board is used for interfacing several common devices, eg Computek VDU, GPO Modem, Teletype writer and the Nimrod Hall 3 IBM 1130 terminal computer.

RL 213 System Crate Power Supply (D N Wilson)

Most of the system crate modules only require a +6v supply. A few also require -6v and +200v. The RL 213 has a maximum output of

+6v at 30A
-6v at 5A

Some of the earlier modules require +200v for neon indicators whereas later designs use light emitting diodes. The current for the +200v line is taken from other Camac power supplies. A relay in the RL 213 interrupts the +200v current to the system crate when the RL 213 is 'off'.

RL 214 DDP 516 Interface (D N Wilson)

This four width source unit interfaces a Honeywell DDP 516 16 bit computer to a 24 bit Camac system. It is capable of a graded L operation and transfers in both the Q scan and block transfer mode.

RL 220 DDP 516 DMA & DMC Module (D N Wilson)

This two width unit supplements the RL 214. All the models made to date were similar but have been 'tailored' to fit the type of DMA/DMC option fitted and its mode of usage.

RL 218 PDP 8 Interface (D Gibbings)

This three width source unit interfaces a DEC PDP 8, PDP 8I or PDP 8L 12 bit computer to a 24 bit Camac system. A PDP 8 computer requires a level translator module RL 217 to change the negative voltage signals to a standard CCSL set of signals.

It is capable of a graded L operation.

RL 219 Display Controller (S Maskell)

This three width source unit is used with the RL 199 Decimal Display unit. The RL 199 displays, in decimal, the contents of up to 16 selected binary scalers on a CRT. The scalers may be anywhere within a single branch and are selected by a diode matrix board.

RL 221 Branch Driver (M Cawthraw)

This three width receiver module drives an EUR 4600 type branch highway. It has a stock register of on line crates which is referred to when executing a graded L operation.

RL 338 Display Module (D Gibbings)

This single width diagnostic module stores, and thereafter displays, the contents of the control word during the last system crate cycle executed. The control word is stored at S2. NOT BUSY and displayed by 24 LED lamps.

RL 339 Display Module (D Gibbings)

This unit is very similar to the RL 338 but displays the 24 data bits instead of the control word. Data is stored at S2.NOT BUSY + S1.

RL 250 Branch Receiver (D Jones)

This three width module is a source unit. It accepts an EUR 4600 Branch Highway via the 132 connector and in general it responds to its Branch Driver like an assembly of crate controllers plus termination unit.

The Branch Receiver can address up to seven branches. Station code N(31) is used for internal functions of this unit, eg pre-selecting the branch.

RL 378 Test Controller (R D Downs)

This two width source unit is a development of the RL 212 Transfer Controller. The sequence of the program can be conditioned by the Q response.

RL 383 System Crate Crate Controller (R D Downs)

This two width unit occupies the 'crate controller' position in a system crate. It enables up to two source units to access normal Camac modules in the system crate.

RL 387 Q Search Module (D Jones)

This two width unit is used in conjunction with a source unit. It provides the H Br C N A part of the control word for a source unit that is accessing (usually reading) an assembly of Camac modules in the Q scan mode. A word counter in the RL 387 signals when a predetermined number of cycles, each with Q=1 have taken place.

RL 388 Argus 400 Interface (F Field)

This four width source unit interfaces a Ferranti Argus 400 24 bit computer to a 24 bit Camac system. It has facilities for graded L operation. A RL 387 Q search module may be coupled to it for easier Q scan mode of access.

RL 389 Argus 400 CSA Module (F Field)

This single width module supplies an Argus 400 computer with consecutive core store addresses for operation in the Direct Store Access mode.

APPENDIX II

Principal features of current and proposed system crate usage.

1 Currently Operational

1.1 Muon experiment by a RHEL and University College team at the CERN ISR using PDP 8 and one branch.

1.2 Wide angle spectrometer experiment by a Scandinavian, RHEL and University College team at the CERN ISR using a DDP 516 and one branch.

1.3 Charge exchange polarization experiment by a Glasgow and RHEL team at the RHEL using a DDP 516 and one branch.

1.4 Meson spectroscopy experiment by an Imperial College and Southampton team at the RHEL using DDP 516 and one branch.

1.5 Measurement of associated production experiment by a Cambridge and RHEL team at RHEL using DDP 516 and one branch.

1.6 Pion cross-sections experiment by a Birmingham, RHEL and Surrey team at the RHEL using a PDP 8 and one branch.

2 Currently being Commissioned

2.1 Experiment to study coherent production of baryon states in helium by a University College and CERN team at the CERN PS using a DDP 516 and one branch.

2.2 A second branch 150 metre long has been added to the system crate mentioned in 1.4. This branch will be used to commission a Camac system for a K^+ particle detector with the CERN Omega magnet spectrometer. Early indications are that a branch complying with EUR 4600 is satisfactory over 150 metres.

3 Currently being Built

3.1 It is proposed to add a second branch to each of the systems mentioned in 1.1 and 1.2 so that both computers, together with a third user, may have shared access to additional Camac provided by CERN. The access may be arranged via three branch receivers RL 250 in an additional system crate or two CERN branch mixer boxes.

3.2 Experiment to measure differential cross-sections and elastic scattering by a combined Bristol, RHEL and Southampton team using an Argus 400 and one branch. Later a PDP 11 may be added as well via a branch receiver.