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Development of a Monolithic Constant Fraction Discriminator

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Abstract

A constant fraction discriminator was developed with a bipolar ASIC technology from NEC. Prototype chips were examined for their integrity and performance. We are convinced that our design for a constant fraction discriminator would serve as a superior technique for high density integration.

1 Introduction

In order to pick out timing information, we use following techniques:

1. Leading edge discriminator.
2. The clipping stub technique.
3. The constant fraction technique.

The first method is very common, but with a penalty on time walk. The second method requires use of a cable delay, so it is difficult to achieve stability and high density integration. The constant fraction discriminator (CFD) has been used for many years because of its negligible time walk [1][2][3][4], and a theoretical analysis was done by C. Nowlin[5]. B-factory and SSC experiments require the following for the trigger system or the time measurement system:

1. Decreasing the burden of the slewing correction for TOF analysis and for Drift chamber system.
2. High density integration of electronics.
3. Stability of electronics.

The conventional constant fraction discriminator meets the first two of these requirements. However our work demands that all four requirements be met. Therefore we developed a Constant Fraction technique (DCF: Differentiation Constant Fraction technique), and a prototype of the DCFD IC was made by NEC process. In the following section, the DCF technique is described.

2 Constant fraction discriminator

The CFD maintains a constant timing edge since it is not affected by the amplitude of the input pulse. In order to achieve a constant timing edge, it is customary to use an attenuator and a delay. The input signal is split. One part is delayed, and the other is attenuated. After these two signals are re-mixed, a comparator detects the zero cross points. The timing of the zero cross point is not influenced by the amplitude of the input signal. The delay has a large temperature coefficient, and the component is not suited for the high density integration technique due to their mechanical constraints.

Therefore we designed the DCFD IC. Its block diagram is shown in Figure 1, and its timing chart is shown in Figure 2. A significant feature of this design is that the use of a delay and an attenuator is avoided. The input signal is divided into two parts. One part is fed into a leading edge discriminator (COMP1). The other one is differentiated and mixed with the original signal. The other comparator (COMP2) picks up the zero cross point of the mixed signal. At the last stage the two signals from the comparators are logically ANDed, and output signal is differential ECL. These points were considered in the design:

1. The signal of the differentiator has no ringing or oscillation.
2. The comparator rapidly and accurately detects the zero cross point.
3. The AND circuit is a high slew rate circuit.

If either one has a ripple or oscillation, the zero cross point is adversely affected. The use of a high slew rate circuit is advantageous, because the time fluctuation which is caused by the voltage noise decreases. In the DCFD IC, the most important feature is the speed of the comparator. If that comparator can detect a zero cross point completely, the fluctuation of the timing edge of the output signal decreases to almost zero.

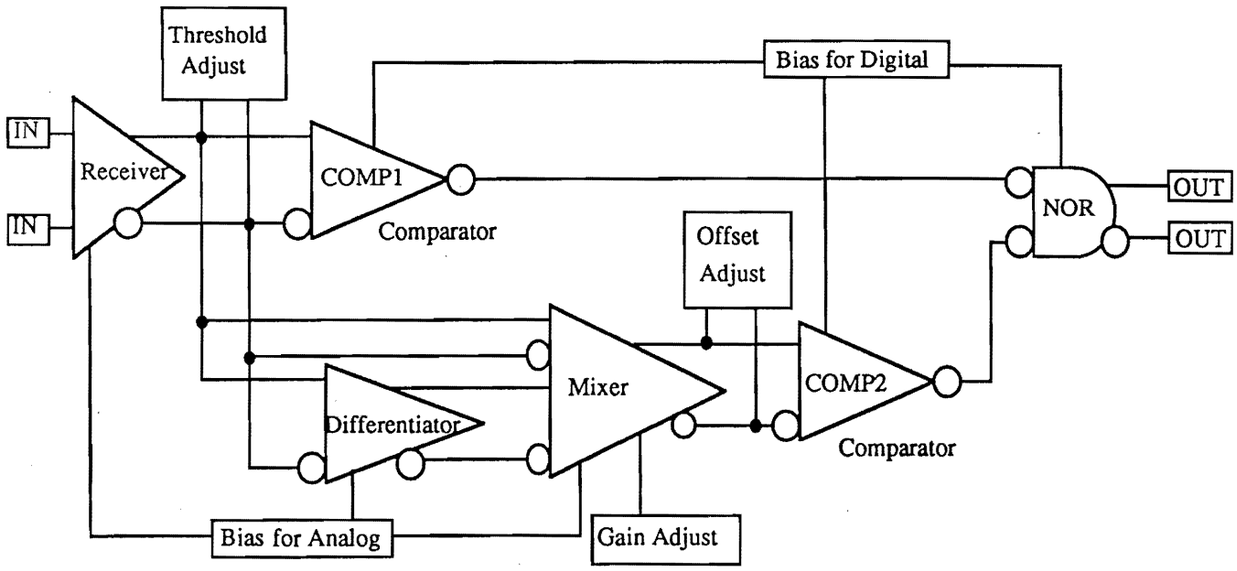

Figure 1: Block diagram of the CFD IC

3 Bipolar process from NEC

The ANALOG MASTER is a semi-custom integrated circuit technology provided by NEC, Tokyo, Japan. The cut-off frequency of npn transistors is 6 GHz; that of pnp transistors is 1 GHz. A resistor of the poly-silicon type is used for this process. The DCFD IC, μPC5102GS-028, has 151 npn and pnp transistors, and the total resistance in this circuit is 487.6 kΩ. The circuit of DCFD IC was designed using the Analog Work Bench on the SUN work station. The SPICE parameters for the circuit simulation were provided by NEC. The ANALOG MASTER, because of its high frequency bandwidth of 6 GHz, was suitable for our proposed design.

4 Evaluation of a prototype chip

4.1 Simulation

Figure 3 shows an input pulse for a functional test, and the pulse from the mixer. These signals were exactly what we had expected as shown in Figure 2. The bandwidth of the comparator for the mixed signal was larger than 1 GHz. We evaluated the time walk by differential trapezoid signal. The time walk was about 100 psec when the range of input pulse was from 10 mV to 600 mV. Figure 4 shows the time walk characteristics of the DCFD IC, when the fraction was set 50 %. The timing fluctuation was about 100 psec over the wide area of input signal range and a

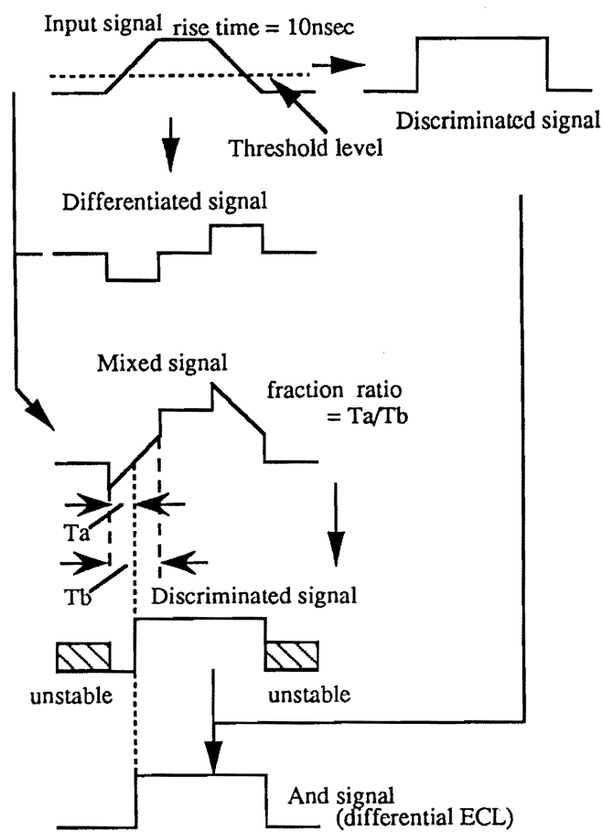

Figure 2: Timing chart of the CFD IC

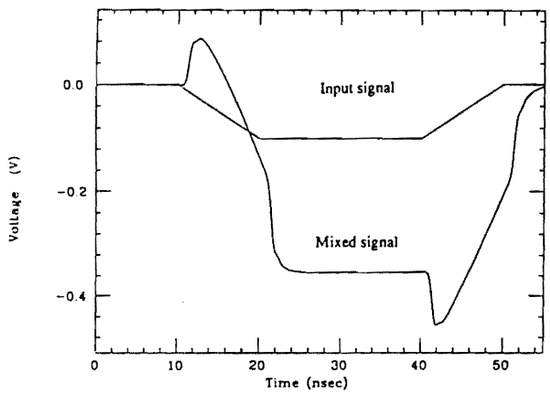

Figure 3: Signals of the DCFD IC on the simulator

1	Input(+)	24	Input(-)
2	GND	23	GND
3	Bias for Analog	22	Bias for Digital
4	V_{CC} for Analog	21	V_{CC} for Digital
5	Threshold voltage	20	Offset voltage
6	GND	19	GND
7	Gain adjust 1	18	COMP1 Output
8	Gain adjust 2	17	GND
9	V_{EE} for Analog	16	COMP2 Output
10	Cap	15	V_{EE} for Digital
11	Output1(+)	14	Output1(-)
12	Output2(+)	13	Output2(-)

Table 1: Pin assignment of the DCFD IC

fraction for discrimination.

The small signal response of the comparator makes the fluctuation greater at small amplitudes, and the differentiator limits the large signal response of the DCFD IC. When the input signal becomes large, the differentiated signal is distorted.

The stability of the IC for the temperature variation was also examined based on a circuit simulation. The result is shown in Figure 5. The variance of the full width was within 0.1 %/°C for the range from 0 °C to 50 °C, and the shift of the absolute value was within 3 psec/°C.

4.2 Bench mark test

The pin assignment of the DCFD IC is shown in Table 1. Pins 16 and 18 are connected to the output stage of two comparators. Signals from those pins are used to adjust the threshold voltage for an input pulse and the offset voltage of the input stage. A tenth of the threshold voltage and the offset voltage at the pin are supplied to the comparators in the DCFD IC.

The output signals from two comparators are shown in

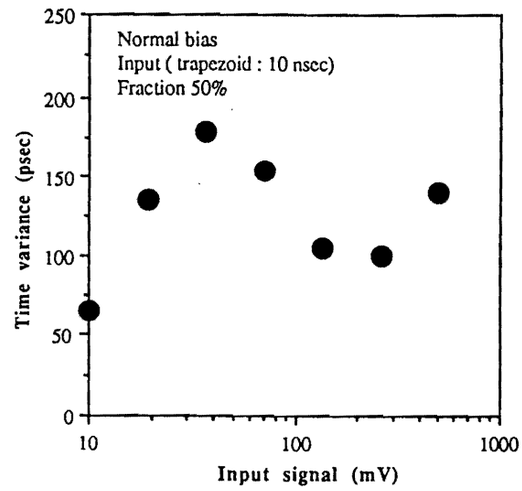

Figure 4: Time walk characteristics of the DCFD IC. The time at the vertical axis was measured at the voltage of -1.3 mV, and the origin of the vertical axis is arbitrary.

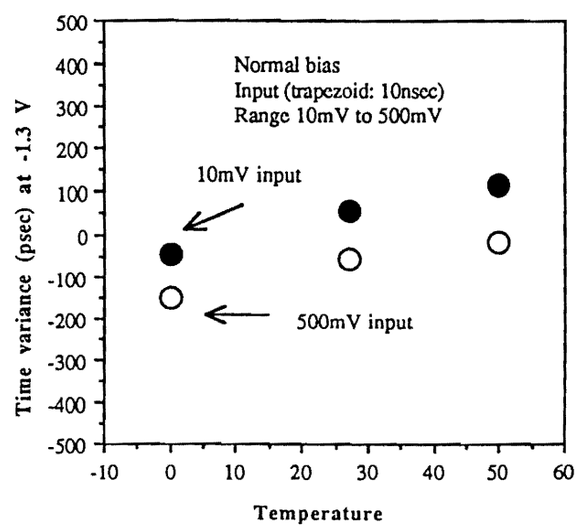

Figure 5: Temperature dependence of the time walk. The origin of the vertical axis is arbitrary.

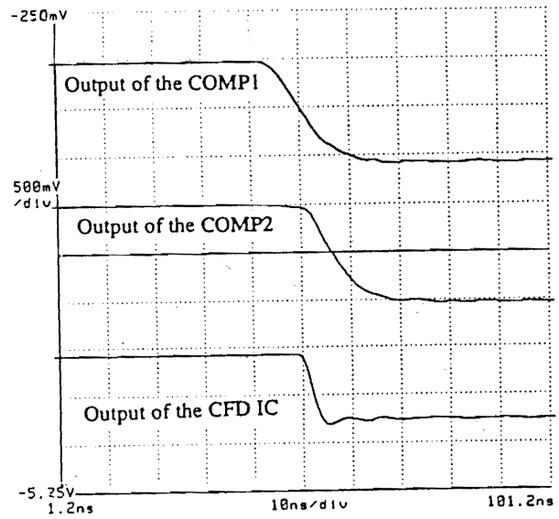

Figure 6: Output signal of the CFD IC. The timing edge was determined by that of the COMP2.

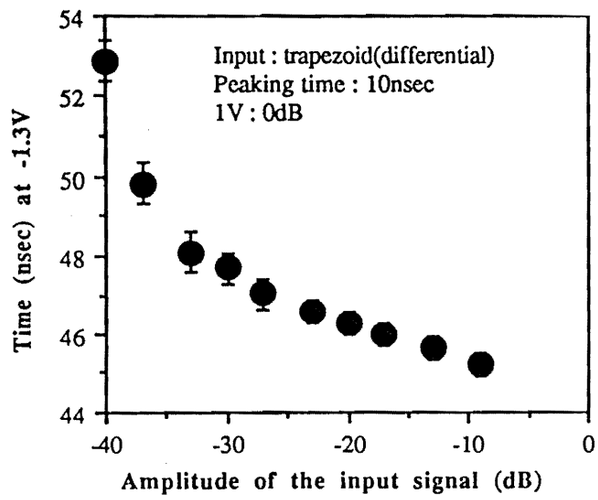

Figure 7: Time walk of the leading edge discriminator (COMP1). The threshold voltage was 16 mV for the differential input signals.

Figure 6. One of the signals (COMP1) controls the timing and the other (COMP2) maintains a stable logic level.

The function of this IC was evaluated. The timing edge of the output signal of the DCFD IC was determined by the COMP2. The performance of the COMP1 is shown in Figure 7. The time walk for the range from 10 mV to 400 mV was about 8 nsec. This value agreed with the calculated result from following equation:

$$\Delta t = (\frac{V_{threshold}}{V_{min}} - \frac{V_{threshold}}{V_{max}})T_{peakingtime}.$$

V_{min} is a minimum input voltage, and V_{max} is a maximum input voltage. We set the $V_{threshold}$ of 8 mV, and $T_{peakingtime}$ was 10 nsec. In order to find the best offset voltage for small walk, we had to make the behavior of the time walk clear for the offset voltage. Figure 8 shows the offset voltage dependence for a fixed amplitude. When the input signal was trapezoidal, the slope of the mixed signal around the zero cross point was the same as that of the input signal. Therefore the offset voltage dependence was described as a solid line in Figure 8. The data larger than 0 mV was consistent with our prediction. The behavior around -1 mV was understood qualitatively in consideration of the difference from the ideal shape. The time walk characteristics for the various offset voltage is shown in Figure 9. This behavior was suited for that of the trapezoidal input. This characteristics can be used to determine the offset voltage. At first, in order to find the offset voltage range where the CFD IC normally functions, we have to take the data as shown in Figure 8. In this range, we examine the behavior of the time walk for the various voltage shown in Figure 9. Figure 10 was obtained by this sequence. In this case, the full width of the time walk was 1 nsec or less. The full width of the time walk in the actual circuit was worse than that from the simulation. Possible sources of the degraded performance were high frequency ripples and random noise on the mixed signal.

5 Summary

We developed a constant fraction technique (ie: differentiation constant fraction technique) without a delay. A prototype was made by a NEC process. This technology has significant advantages over others currently in use for applications in high density integration, and particularly for some large scale experiments such as B-factory and SSC. The performance of this differentiated constant fraction integrated circuit was tested by the trapezoidal input signal. The function of the DCFD IC was exactly what we expected, and the full width of the time walk was 1nsec or less. In order to decrease the effect of the input voltage noise and to examine under the realistic condition, the CFD IC will be evaluated with a filter..

ACKNOWLEDGEMENTS

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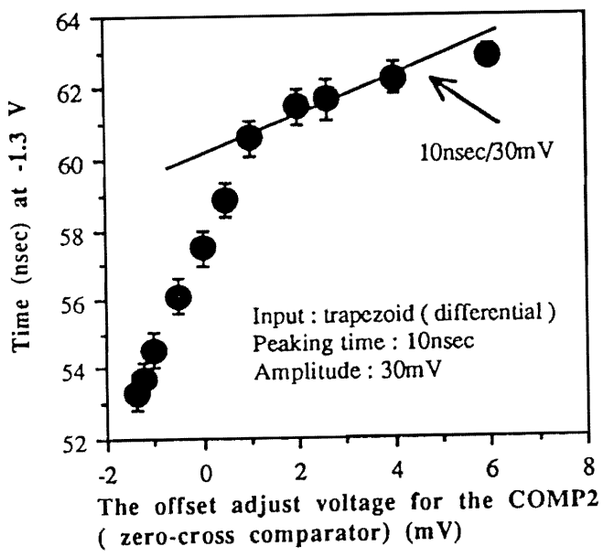

Figure 8: Offset voltage dependence of the timing for a input signal. The amplitude of the input signal was 30 mV, and the peaking time was 10 nsec.

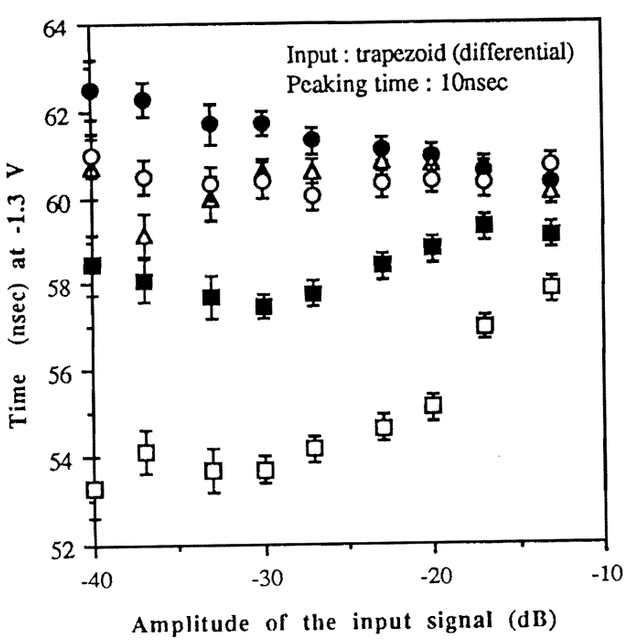

Figure 9: Offset voltage dependence of the time walk. Input signal rage was from 10 mV to 500 mV.

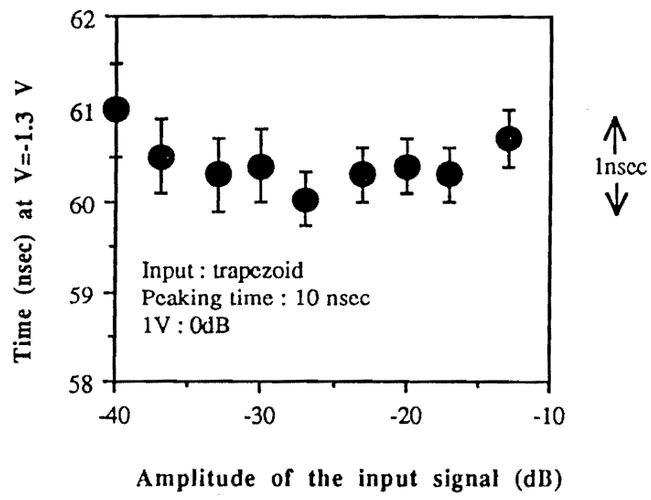

Figure 10: Time walk of the DCFD IC. Either the voltage noise or the ripples on the mixed signal increased the timing fluctuation.

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● 2.8mV
△ 1.0mV
■ 0.0mV
□ -1.2mV
○ 0.7mV