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Lecture Note on Circuit Technology for High Energy Physics Experiment

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Lecture Note on Circuit Technology for High Energy Physics Experiment*

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ABSTRACT

This lecture gives basic ideas and practice of the circuit technology for high energy physics experiment. The program of this lecture gives access to the integrated circuit technology to be applied for a high luminosity hadron collider experiment.

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1. Introduction

1.1. GENERAL DESCRIPTION

The design concepts on the electronics system for high energy physics experiment meet with a drastic innovation of methodology and/or technology. Traditional way was to put preamplifiers on the detector end, whose outputs are transmitted via a large bundle of cables to an electronics hut to be processed by data acquisition modules. The accelerator operation cycle was $5\mu s$ to 20 μs, which was enough to compensate for latency of the trigger decision circuit. This approach does not work for the recent high luminosity collider experiment. In order to meet with high trigger rate, large data size, radiation damage issues, and an enormous number of readout channels, we have try to apply VLSI technologies to the detector instrumentation for the high energy physics experiment. The front-end VLSIs have complicated digital control capabilities as well as analog processing functions, which are directly mounted on the high density printed circuit board. The back-end digital circuits are operated with high frequency clock signal where a pipe-line operation takes an essential role. These electronic system are designed with an aid of circuit simulators based on analog oriented (SPICE) method and/or digital oriented (VHDL) method. In this text we would like to give access to an analog circuit design in terms of SPICE. We never try to describe circuit in terms of "equivalent 4-terminal network", but to characterize electronic devices in terms of mathematical model. Basic ideas about radiation measurements are covered also together with some ideas related with semi-conductor physics. Digital circuit technologies and radiation damage issues are not covered in this text, on which we expect some lectures will be arranged elsewhere. You can find some reference literatures on these items in the reference list of the next section.

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2. Electronic devices

The basic physics constants used in this lecture are listed in Table 1. The basic equations for the semiconductor are shown in Appendix A. The device models are based on the SPICE model.

2.1. Diode

The operational behavior of the p-n junction diode is characterized as:

$$I_D = I_S(exp(\frac{V_D}{nV_T}) - 1) \tag{2.1}$$

$$Q_D = \tau_t I_D + C_{j0} \int_0^{V_D} \frac{1}{(1 - V/\phi_B)^m} dV \tag{2.2}$$

V_D: diode voltage
I_D: diode current
I_S: saturation current
n : emission coefficient
V_T: kT/q
C_{j0}: zero-bias depletion capacitance
ϕ_B: built-in potential
m : grading coefficient
τ_t: transit time
R_S: ohmic resistance

n_i: intrinsic carrier density

N_c: effective density of states in the conduction band

N_v: effective density of states in the valence band

E_G: band gap energy

The capacitance (C_D) of the diode is defined as a derivative of Q_D:

$$C_D = \frac{dQ_D}{dV_D} = \frac{\tau_t}{r_D} + \frac{C_{j0}}{(1 - V_D/\phi_B)^m} \tag{2.3}$$

where r_D is:

$$r_D = \frac{dV_D}{dI_D} = \frac{nV_T}{I_D} \tag{2.4}$$

r_D is about 26 Ω for $I_D = 1mA$, n=1 and junction temperature of 300 $°K$. Taking into account I_s's temperature dependence:

$$I_S \propto D_n n_i^2 = KT^2 exp(-\frac{E_G}{V_T}) \tag{2.5}$$

V_D shows negative temperature coefficient:

$$\frac{dV_D}{dT} = \frac{1}{T}(-V_G + V_D - 2V_T) \tag{2.6}$$

which is about -2mV/$°C$. The emission coefficient comes from two current generation mechanisms, diffusion current (n=1) and recombination current (n=2). The reality is between the two.

In terms of intrinsic carrier concentration, the thermal equilibrium is characterized as:

$$pn = n_i^2 \tag{2.7}$$

For the intrinsic semiconductor (i.e. which has no impurity doping concentration) there stands:

$$p = n = n_i \tag{2.8}$$

The origin of the built-in potential is explained in Appendix C. The SPICE diode model parameters are listed in Table 2. A complete set of SPICE model consists

of 14 parameters. A SPICE deck including diode is shown below:

```
EXAMPLE-1
.MODEL M1SXXXX D IS=.... RS=.... N=.... TT=.... CJ0=....
RR3 3 1 1K
DD2 1 0 M1SXXXX
VC 2 3 0.
VA 2 0 PULSE ( -1. 1. 200.N 5.N 5.N 200.N )
.TEMP 27
.OP
.TRAN 5.E-8 1.E-6 0
.END
```

The zero-voltage power supply VC was introduced to measure the current flow through this supply. Applying a square pulse from the voltage terminal VA, you could find a capacitive nature of diode about the current flow. The circuit schematic is shown in Figure 1.

2.2. BJT

There are two type of Bipolar Junction Transistors; they are pnp and npn transistor. The BJT is described as 4-terminal device; i.e. collector, base, emitter, and substrate. The BJT's are characterized as:

$$I_E = \frac{I_s}{\alpha_F}(e^{V_{BE}/V_T} - 1) - I_s(e^{V_{BC}/V_T} - 1) \tag{2.9}$$

$$I_C = I_s(e^{V_{BE}/V_T} - 1) - \frac{I_s}{\alpha_r}(e^{V_{BC}/V_T} - 1) \tag{2.10}$$

The capacitance characteristics are:

$$C_{BE} = \frac{\tau_f I_s}{V_T} e^{V_{BE}/V_T} + \frac{C_{je0}}{(1 - V_{BE}/\phi_e)^{m_e}} \tag{2.11}$$

$$C_{BC} = \frac{\tau_r I_s}{V_T} e^{V_{BC}/V_T} + \frac{C_{jc0}}{(1 - V_{BC}/\phi_c)^{m_c}} \tag{2.12}$$

The capacitance between the substrate and the collector terminal is:

$$C_{SC} = \frac{C_{jcs}}{(1 - V_{SC}/\phi_s)^{m_s}} \tag{2.13}$$

The base current is evaluated as:

$$I_B = I_E - I_C = \frac{1}{\beta_F} I_s (e^{V_{BE}/V_T} - 1) - \frac{1}{\beta_R} I_s (e^{V_{BC}/V_T} - 1) \tag{2.14}$$

The forward current gain is defined as:

$$\beta_F \simeq \frac{I_C}{I_B} \tag{2.15}$$

which is related with α_F:

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{2.16}$$

In the same way the reverse current is:

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R} \tag{2.17}$$

The common emitter transconductance (g_m) is defined as:

$$g_m = \frac{1}{r_e} \longrightarrow \frac{dI_E}{dV_{BE}} = \frac{I_E}{V_T} \tag{2.18}$$

The SPICE parameters for the BJT are listed in Table 3. The other parameters, VA and VAR, are also essential to characterize bipolar transistor. The formula for I_C and I_E could be modified by a factor of $1 + V_{BC}/V_A$ and/or $1 + V_{BC}/V_{AR}$ for each term. A complete set of SPICE model consists of 40 parameters. A SPICE deck including BJT is shown below:


```
EXAMPLE-2
.MODEL M2SCXXXX NPN IS=.... BF=.... BR=.... RB=.... RC=....
+ RE=.... CJE=....
QQ13 4 4 1 M2SCXXXX
QQ12 6 5 7 M2SCXXXX
QQ11 6 7 3 M2SCXXXX
QQ10 2 1 3 M2SCXXXX
RR9 8 1 470
RR8 0 5 50
RR7 8 7 470
RR6 8 3 220
RR5 0 2 50
RR4 4 0 50
VV3 6 0 6
VV2 0 8 5.2
VA 5 0 PULSE (0. -0.8 200.N 5.N 5.N 200.N )
.TEMP 27
.OP
.TRAN 5.E-8 1.E-6 0
.END
```

The circuit is just a toy circuit to demonstrate a NIM-to-ECL and an ECL-to-NIM converter simultaneously. $QQ12$ is an emitter follower, which translate the NIM level signal to the ECL level signal. The switch stage consists of $QQ11$ and $QQ10$. The base of $QQ10$ is biased at the mid-point of the ECL-logic swing. The circuit schematic is shown in Figure 2.

2.3. MOS

In the operation of BJT, the minority carrier takes an essential part. On the other hand, MOS transistor (MOST) is a majority carrier device. There are two types of MOS transistor; n channel MOST and p channel MOST. MOST could be separated further; enhancement MOST and depletion MOST.

The characteristics of MOS transistor are described below. The MOST is described as a 4-terminal device; i.e. drain, gate, source, and substrate. In the linear region (or before pinch-off):

$$I_D = \frac{1}{2}k_p\frac{W}{L}(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2) \tag{2.19}$$

In the saturation region (or after pinch-off):

$$I_D = \frac{1}{2}k_p\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{2.20}$$

where k_p is called as process gain (transconductance) factor which depends on details of semiconductor fabrication. The break-down of the process transconductance factor is shown below:

$$k_p = \mu C_{ox} \tag{2.21}$$

$$C_{ox} = \frac{\epsilon_{sio_2}\epsilon_0}{t_{ox}} \tag{2.22}$$

$$C_G = WLC_{ox} \tag{2.23}$$

The transconductance of the MOS transistor at the pinch-off condition is:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{2.24}$$

$$g_m = k_p\frac{W}{L}(V_{GS} - V_{TH}) \tag{2.25}$$

$$g_m = \sqrt{2\frac{W}{L}k_pI_D} \tag{2.26}$$

The gate voltage on which the MOS transistor begin to work is V_{TH}:

$$V_{TH} = V_{TO} + \gamma(\sqrt{\phi_B + V_{SB}} - \sqrt{\phi_B}) \tag{2.27}$$

where V_{TO} is expanded again:

$$V_{TO} = V_{FB} + \phi_B + \frac{1}{C_{ox}}\sqrt{2qN_{sub}\epsilon\epsilon_o\phi_B} \tag{2.28}$$

where V_{SB} is measured from source to bulk terminal; that is usually positive. The parameters that determines the threshold voltage are the material and doping level of the gate; i.e. flat-band voltage (V_{FB}). The radiation damage incorporates fixed oxide charge, which affects on the threshold voltage also. It should be note that the concept of the MOS transistor based on the effect of surface inversion. The surface inversion changes semiconductor type from p-material to n-material. The surface potential of the MOS transistor could be derived from the consideration of balance between the diffusion current and the drift current:

$$V_s = V_T ln\frac{n_s N_A}{n_i^2} \tag{2.29}$$

where V_s is the surface voltage , and n_s is the surface carrier concentration. The strong inversion layer is generated when

$$n_s = N_A \tag{2.30}$$

The condition to generate strong inversion is:

$$V_s = 2V_T ln\frac{N_A}{n_i} = 2\phi_i \tag{2.31}$$

The SPICE parameters for the MOS transistor are listed in Table 4. These SPICE parameters are Level-1 MOS parameters. These SPICE parameters has some redundancy. There are many varieties of MOS parameters which are introduced to

fit to the most advanced MOS devices. A SPICE deck including MOS transistors is shown below:

```
EXAMPLE-3
.MODEL MPMOS PMOS VTO=-0.88 TOX=26N UO=216. PB=...
.MODEL MNMOS NMOS VTO=0.88 TOX=26N UO=661. PB=...
VV6 1 0 5
MQ5 4 5 1 1 MPMOS L=1.4U W=3.6U
MQ4 4 3 1 1 MPMOS L=1.4U W=3.6U
MQ3 4 5 2 0 MNMOS L=1.2U W=3.6U
MQ2 2 3 0 0 MNMOS L=1.2U W=3.6U
.TEMP 27
.OP
.TRAN 5.E-8 1.E-6 0
.END
```

The circuit is a 2-input NAND circuit. The n-MOS transistors are located in series, while the p-MOS transistors are in parallel. The substrate of nMOS transistor are tied to ground (V_{ss}), and that of pMOS transistor are tied to +5V (V_{dd}). The circuit configuration is a Complementary MOS (CMOS) circuit. You should note that the SPICE convention gives negative value for VTO of p-MOS , while VTO for n-MOS is positive. The surface mobility UO of the p-MOS is one third of the n-MOS transistor. The surface carrier mobility is half or less of the carrier mobility in the bulk. The low power nature of CMOS circuit provides benefit to implement large scale digital circuits. The circuit schematic of the CMOS NAND circuit is shown in Figure 3.

2.4. JFET

The JFET is a depletion mode device; in the normal operating condition the gate voltage is lower than the source voltage for n-channel JFET. The characteristics are described below. In the linear region (before pinch-off):

$$I_D = \frac{\beta}{2} V_{DS}(2(V_{GS} - V_{TO}) - V_{DS})(1 + \lambda V_{DS}) \tag{2.32}$$

In the saturation region (after pinch-off) :

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TO})^2(1 + \lambda V_{DS}) \tag{2.33}$$

The capacitance characteristics are:

$$C_{GS} = \frac{C_{GSO}}{(1 - V_{GS}/\phi_B)^{1/2}} \tag{2.34}$$

$$C_{GD} = \frac{C_{GDO}}{(1 - V_{GD}/\phi_B)^{1/2}} \tag{2.35}$$

β could be evaluated as:

$$\beta = \mu C_g \frac{W}{L} \tag{2.36}$$

where C_g is the unit capacitance of the FET gate. The total gate capacitance C_G is:

$$C_G = WLC_g \tag{2.37}$$

The SPICE parameters for JFET are listed in Table 5. A SPICE deck including JFET is shown below:

```
EXAMPLE-4
.MODEL M2SCXXXX NPN IS=.... BF=....
.MODEL M2SAXXXX PNP IS=.... BF=....
.MODEL M2SKXXX NJF VTO=.... BETA=....
QQ21 6 7 8 M2SCXXXX
QQ20 6 2 7 M2SCXXXX
QQ19 2 4 5 M2SCXXXX
QQ18 4 4 9 M2SCXXXX
QQ17 2 1 3 M2SAXXXX
RR16 11 8 2K
RR15 11 7 7.2K
RR14 3 6 400
RR13 11 5 100
RR12 11 9 100
RR10 1 6 4.7K
RR9 0 1 3.3K
RR8 10 8 10MEG
JQ7 3 10 0 M2SKXXX
VV6 6 0 8
VV5 0 11 8
CC4 1 0 0.1U
CC3 10 8 0.5P
CC2 10 12 1.P
VA 12 0 PWL (0. 0. 400.N 0. 410.N -0.1)
.TEMP 27
.OP
.TRAN 5.E-7 1.E-5 0
.END
```

The circuit consists of a common source n-channel JFET ($JQ7$), a folded cascode

transistor ($QQ17$), and Darlington transistors for output ($QQ20$ and $QQ21$). $QQ19$ is for a high impedance load. The feed back elements consist of $RR8$ and $CC3$. $CC2$ is for a test pulse injection. The circuit schematic is shown in Figure 4.

2.5. Passive elements

Capacitor The capacitors used for integrated circuit design are diode capacitance, MOS capacitance, metal-insulator-metal (MIM), and polysilicon-insulator-polysilicon (double poly capacitor). The diode capacitance and the MOS capacitance have a voltage dependent nature. The usable capacitance value for integrated circuit design is around 1 pF. A capacitance of 10pF is quite large. A capacitance of 100pF is almost unrealistic. The unit capacitance of MIM and/or double poly capacitor is less than 1 $fF/\mu m^2$.

Resistor There are two way to fabricate resistor for the integrated circuit. One is to use a process step of p^+ diffusion into n-well area for the p-MOS transistor. Another way is to use poly-silicon strip with appropriate impurity dosage. These resistor has inherently temperature dependent nature. The absolute value of these transistor is not better than $\pm$ 10 %. The design practice of the integrated circuit is not to rely on the absolute value of the resistor, but on the relative matching of the resistors.

3. Basic circuits and ideas

3.1. Building blocks of circuit

Follower

Emitter follower:

The output impedance of the emitter follower is evaluated as:

$$Z_{out} = r_e = \frac{V_T}{I_e} \tag{3.1}$$

The input impedance is measure from the base node:

$$Z_{in} = \beta_F R_L \tag{3.2}$$

High drive follower:

The characteristics of a high drive follower is hown below.

$$Z_{out} = \frac{r_e + R_0}{1 + R_1/R_2} \tag{3.3}$$

$$Z_{in} = \beta_{F1}(R_0 + R_L(1 + R_1/R_2)) \tag{3.4}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{R_0}(1 + R_1/R_2)/(1/R_L + (1 + R_1/R_2)/R_0)) \tag{3.5}$$

In the limit of $R_2/R_1 \rightarrow \infty$, the output impedance tends to zero, the input impeance goes to infinity, and the transfer gain is 1. A SPICE deck including the high drive follower is shown below:

```
EXAMPLE-5
.MODEL M2SCXXXX NPN
.MODEL M2SAXXXX PNP
QQ17 1 5 6 M2SCXXXX
QQ16 7 7 9 M2SCXXXX
QQ15 6 7 8 M2SCXXXX
QQ14 2 1 3 M2SAXXXX
QQ13 1 1 4 M2SCXXXX
RR12 0 5 50
RR11 2 6 50
RR10 0 12 50
RR9 10 9 100
RR8 10 8 100
```



```
RR7 7 14 1K
RR6 4 15 500
RR5 3 13 50
VV4 11 0 12
VV3 0 10 12
VE 0 14 0.
VA 5 0 SIN ( 0. 5.E-1 5.E+6 1.E-7 1.E+6)
VB 11 15 0.
VC 11 13 0.
CC2 12 2 0.1U
.TEMP 27
.OP
.TRAN 5.E-8 1.E-6
.END
```

In order to evaluate eq. (3.5), we put $R_0 = R11$, $R_1 = RR6$, $R_2 = RR5$, and $R_L = RR10$. The circuit schematic is shown in Figure 5.

Darlington circuit

Two V_{BE} drop configuration: In this circuit the emitter node of one transistor is connected to the base node of another transistor.

$$Z_{out} = r_e = \frac{V_T}{I_e} \tag{3.6}$$

$$Z_{in} = \beta_{F1}\beta_{F2}R_L \tag{3.7}$$

We can obtain very high input impedance and/or very high effective forward current gain. A possible problem is that there is two V_{BE} drop ($\sim$ 1.5V) from the input node to the output node. One V_{BE} drop configuration: In this circuit collector of the input transistor is connected to the base node of another transistor. The emitter of the input transistor and the collector node of the second transistor

are tied together at the output node. This configuration could be understood as the limiting case of the high drive follower. The output impedance could be less than 1 Ω:

$$Z_{out} = \frac{r_e}{\beta_{F2}} \tag{3.8}$$

$$Z_{in} = \beta_{F1}\beta_{F2}R_L \tag{3.9}$$

differential pair

The differential pair of the bipolar transistor is a basic building block for analog/digital application. Switching:

The emitter coupled transistor pair is frequently used for a switch circuit. The differential input voltage of about 100 mV is sufficient enough to switch the current flow from one transistor to another.

Common mode rejection ratio:

The differential pair is less sensitive for the common mode input voltage. The ratio of the common gain relative to the differential gain is called common mode rejection ratio.

Power supply noise rejection ratio:

The idea of power supply noise rejection ration is not inherent for the differential amplifier. We would like to mention its definition here. The voltage disturbance of the power supply rail propagates to the output of the amplifier. The amplifier gain from the power rail to the amplifier output is called power supply rejection ratio. The preamplifier circuits are often deteriorated in terms of the power supply rejection ratio when the detector capacitance is very large.

Current mirror

The circuits are biased with current mirror circuits and or a voltage reference circuits. We shows here some examples of simple current mirror, Wilson's current mirror, and a temperature compensated bias circuit.

A SPICE deck including these circuit blocks are shown below:


```
EXAMPLE-6
.MODEL M2SCXXXX NPN
.MODEL M2SAXXXX PNP
QQ21 10 10 14 M2SCXXXX
QQ20 13  6 10 M2SCXXXX
QQ19  4 12  9 M2SCXXXX
QQ18  6 10 11 M2SCXXXX
QQ17  1  8  9 M2SCXXXX
QQ16 15  4 16 M2SCXXXX
QQ15  6  3  7 M2SAXXXX
QQ14  4  1  5 M2SAXXXX
QQ13  3  3  0 M2SAXXXX
QQ12  1  1  2 M2SAXXXX
VA 8 0 SIN ( -5.E-1 5.E-1 5.E6 0. 1.E+6 )
RR11 11 17 100
RR10 15  2 100
RR9  15  5 100
RR8   3 17 4K
RR7  15  7 4K
RR6  14 17 100
RR5  16 17 4K
RR4  12 16 100
VV3  15 0  8
VV2  0  17 8
VC  9  0  0.
.TEMP 27
.OP
.TRAN 5.E-8 1.E-6 0.
.END
```

The current mirror configuration might be used for a constant current source and also for a high impedance load. The current mirror with $QQ12$ and $QQ14$ is for a high impedance load. Transistors $QQ18$, $QQ20$, and $QQ21$ are elements for the Wilson's current mirror to provide a constant current source. The circuit elements $RR7$, $RR8$, $QQ13$ and $QQ15$ provides a temperature compensated current reference. The circuit schematic is shown in Figure 6.

3.2. Amplifier

This section describes basic concept of the feed-back amplifier. The negative feed back stabilizes and/or improves:

1. DC operation condition
2. Gain versus frequency response
3. Linearity
4. S/N ratio
5. Z_{in}, Z_{out} characteristics.

Operational Amplifier

Inverting amplifier:

The inverting amplifier consists of an amplifier with an open loop gain of $-G$, a feedback resistor of R_2, and a input resistor R_1 which is series to the input terminal. The amplifier gain is:

$$A = -\frac{R_2}{R_2/G + R_1(1 + 1/G)} \tag{3.10}$$

which could be written as:

$$A = A_\infty \frac{T(j\omega)}{1 + T(j\omega)} \tag{3.11}$$

where

$$A_\infty = -\frac{R_2}{R_1} \tag{3.12}$$

and

$$T(j\omega) = \frac{R_1 G(j\omega)}{R_1 + R_2} \tag{3.13}$$

In general:

$$A_\infty(j\omega) = -\frac{Z_2}{Z_1} \tag{3.14}$$

Non-inverting amplifier:

The amplifier gain is:

$$A = \frac{R_1 + R_2}{R_1(1 + 1/G) + R_2/G} \tag{3.15}$$

which could be written as:

$$A = A_\infty \frac{T(j\omega)}{1 + T(j\omega)} \tag{3.16}$$

where

$$A_\infty = 1 + \frac{R_2}{R_1} \tag{3.17}$$

and

$$T(j\omega) = \frac{R_1 G(j\omega)}{R_1 + R_2} \tag{3.18}$$

where $R_1/(R_1 + R_2)$ is a feed-back fraction. In general:

$$A_\infty(j\omega) = 1 + \frac{Z_2}{Z_1} \tag{3.19}$$

Input impedance The input impedance of the inverting amplifier is:

$$Z_{in} = R_1 + \frac{R_2 + R_0}{1 + G} \tag{3.20}$$

where R_0 is the internal impedance series to the output port of the operational amplifier. When $R_1 = 0$, the amplifier is a current sensitive amplifier, or formally called as a trans-impedance amplifier. When $R_1 = 0$ again and R_2 is replace with a capacitor, the circuit is a charge sensitive amplifier, or formally called as a trans-conductance amplifier.

Output impedance The output impedance of the inverting amplifier is:

$$Z_{out} = \frac{R_0//(R_1 + R_2)}{1 + T} \tag{3.21}$$

Blackman's formula A general formula to obtain Z_{in} and/or Z_{out} is due to Blackman's formula:

$$Z = Z_0 \frac{1 + T_s}{1 + T_o} \tag{3.22}$$

where

Z_0: input(output) impedance when amplifier is removed from the circuit.

T_s: feed-back when input(output) terminal is grounded.

T_o: feed-back when input(output) terminal is open.

Equations (3.20) and (3.21) could be confirmed with this Blackman's formula. In the case of the input impedance of the inverting amplifier, there stands:

$$Z_0 = R_0 + R_1 + R_2 \tag{3.23}$$

$$T_s = \frac{R_1 G}{R_0 + R_1 + R_2} \tag{3.24}$$

$$T_o = G \tag{3.25}$$

The output impedance is evaluated with:

$$Z_0 = R_0//(R_1 + R_2) \tag{3.26}$$

$$T_s = 0 \tag{3.27}$$

$$T_o = \frac{R_1 G}{R_0 + R_1 + R_2} \tag{3.28}$$

Circuit stability

The stability/instability condition is analyzed in terms of:

1. Bode diagram:
   If the phase of $G(j\omega)$ goes near 180° or $G(j\omega)$ is on the -12dB/oct slope at the frequency of $G(j\omega) \simeq A_\infty$, the amplifier is potentially unstable.
2. Nyquist diagram
   The circuit is stable when the coordinate (-1,0) is outside of the $T(j\omega)$ trajectory for -∞ to ∞ of ω.
3. Z_{in} and Z_{out}.
   The two-port network is said to be unconditionally stable at a given frequency if the real part of Z_{in} and Z_{out} are greater than zero for all passive load and source impedances. If the two-port is not unconditionally stable, it is potentially unstable.

The first method will be useful to use an operational amplifier. The second way is quite powerful to analyze the automatic control system in a mathematical way where the frequency response is known a priori. The last method with I/O impedance is most powerful for circuit simulation with SPICE. The approach is usable for non-feed back circuit, but with stray feed back loop. The approaches to fix circuit oscillation are:

1. Move pole or substitution of pole position

2. Pole/zero cancellation

3. Attenuation of open loop gain

4. and elimination of unwilling feedback route.

4. Application for data acquisition

4.1. Decision circuit

The decision circuit generates a logic signal when the input analog signal satisfies a certain condition about its pulse height.

Leading edge discriminator The most simple decision circuit is a leading edge discriminator, which is commonly used for timing pick-off of the photo-multiplier signal. Because the discrimination condition is just a single threshold, the timing edge suffers from "Time-walk" due to pulse height variation.

Zero crossing discriminator The zero crossing discriminator incorporates two leading edge discriminator internally. One discriminator generates a logic high during a time interval where the input signal is larger than the threshold level. Another discriminator is provided for the differentiated signal of the input to pick-off zero-crossing timing of the signal, which is insensitive to pulse-hight. The output signal is a logical AND from these two discriminators.

Constant fraction discriminator
The other way for pulse-height insensitive decision circuit is to use an idea of constant fraction discriminator. The output logic signal has a timing edge at a certain fraction of the peaking time of the input signal. This circuit is superior than the zero-crossing discriminator, because we can set the fraction where the signal's rise time is maximum. The jitter due to electronic/electric noise could be optimized with use of the constant fraction discriminator.

Schmitt trigger circuit The Schmitt trigger circuit employs two threshold levels; one is for low to high transition of decision circuit, another is for high to low transition. Usually the former threshold is chosen as higher than the latter one, which increases noise immunity of the decision circuit. The circuit is commonly used for a repeater capability for long distance digital signal transmission.

4.2. Time interval measurement

We have two ways of time interval measurement: one is in fully digital, and another is in analog way.

Digital implementation
Interval counter:
The number of pulse between a START and a STOP pulse are directly counted with incorporation of a high frequency clock generator and a high speed counter integrated circuit. The technical limitation for measurement resolution is around 10 nsec.
Shift register:
The input signal (START) is shifted-in to a shift register chain for each clock leading edge. The location of the START signal at the timing of STOP signal gives timing interval information. The shift register could be operated with a clock frequency of 1 GHz.
Gate delay with memory (Time-Memory-Cell):
A reference signal is generated for each predetermined time interval to propagate it through a delay element chain. A coincidence of the START and the tap signal from the delay element chain gives timing information. This idea is quite adequate for implementation with CMOS VLSI technology. The reference clock frequency is not more than 30 or 40 MHz. The technical limitation for the measurement resolution is around 0.5 nsec.

Analog implementation
The analog circuit to measure time interval is base on the principle of Time-to-

Amplitude converter (TAC). A constant current source is routed to a capacitor during the interval between START and STOP. The voltage appeared at the capacitor terminal is proportional to the timing interval. The technical limitation for the measurement resolution is around 25 psec.

4.3. Charge measurement

Current splitter A current splitter circuit is employed for a wide range charge integrator system. The circuit is essentially a common base transistor array. The voltage appeared at the emitter node is amplified and fed to the base node. With this mechanism the input impedance of the emitter node could be as low as 1 Ωor less. The transistors shares equal fraction of the input current.

There are two ways of charge measurement one is to use a charge integrator, and another is to use a peak hold circuit together with an appropriate shaping amplifier. The charge integrator circuit accumulates input charge for a certain gated interval. The technical limitation for the minimum gate width is around 20 nsec. The maximum charge which could be measured with resonable measurement accuracy is called dynamic range. The linearity of the charge measurement system is characterized by integral non-linearity and also by differential linearity. The integral non-linearity is a measure of the maximum deviation from an ideal linear response over the entire region of the dynamic range. The differential non-linearity is a measure of the local monotony. The output offset for null input signal is called pedestal level. The ideas about hold-settling time and droop are specific for the peak hold circuit. The peak hold circuit can not catch a very fast signal with reasonable accuracy. The technical limitation about the peaking time of the input signal is about 50 nsec.

Wave form sampling
The most versatile way of analog signal measurement is due to wave form sampling, which is commonly used for a digitizing oscilloscope. Some techical words used for the wave form sampling are listed below.

Sampling theorem:
The theorem says that the analog signals whose maximum frequency are less than half of the sampling frequency could be reconstruct very precisely.
Aliasing noise:
The higher frequency component than 50 % of the sampling frequency generates a fake signal in the lower frequency region; this illusion of reconstructed signal is called aliasing noise.
Aperture jitter:
The jitter associated with sampling interval deteriorates measurement accuracy.
Aperture delay time:
The effective sampling timing might be delayed from the nominal sampling timing, which deteriorates phase measurement accuracy of the input wave.
Feed-through:
The wave form sampling system is driven by a large swing logic signal; the interference through the analog switch is called clock feed-through.

5. Noise characteristics of electronic devices

5.1. Source of electronic noise

The electronic noise could be subdivided into three parts due to their generation mechanism, i.e. shot noise, thermal noise, and 1/f noise.

1. Shot noise: The power spectrum of the shot noise is characterized as:

$$i_n^2 = 2qI \quad A^2/Hz \tag{5.1}$$

The origin of the shot noise is explained in Appendix D.

2. Thermal noise: In terms of voltage generator, the thermal noise is written

as:

$$v_n^2 = 4kTR \quad V^2/Hz \tag{5.2}$$

The thermal noise could be presented as a current generator also:

$$i_n^2 = \frac{4kT}{R} \quad A^2/Hz \tag{5.3}$$

The origin of the thermal noise is explained in Appendix E.

3. 1/f noise: 1/f noise is characterized as a voltage generator whose noise power spectrum has 1/f characteristics:

$$v_n^2 = \frac{K_{1/f}}{f} \quad V^2/Hz \tag{5.4}$$

5.2. Pulse shaping

In the case of low input impedance amplifier, the noise sources are characterized as a current generator:

$$I_n^2 = i_n^2 + \frac{v_n^2}{Z_s^2} \tag{5.5}$$

i_n: parallel noise in $A/\sqrt{Hz}$

v_n: series noise in $V/\sqrt{Hz}$

Z_s: source impedance

The impulse response of the amplifier chain is $h(t)$, whose Fourier transform is:

$$H(\omega) = \int_{-\infty}^{\infty} h(t)e^{-j\omega t}dt \tag{5.6}$$

The signal we use here is an impulse response for simplicity of discussion:

$$I_s(\omega) = q_s = \int_{-\infty}^{\infty} q_s\delta(t)e^{-j\omega t}dt \tag{5.7}$$

The signal is evaluated as:

$$\frac{1}{2\pi}\int_{-\infty}^{\infty} I_s(\omega)H(\omega)e^{j\omega t}d\omega \tag{5.8}$$

for low impedance amplifier. The noise power is evaluated as:

$$\int_{-\infty}^{\infty} I_n^2|H(\omega)|^2df \longrightarrow \int_{-B}^{B} 2q^2 < n > (2B)^{-2}df = 2q^2\frac{< n >}{2B} \tag{5.9}$$

where $q\sqrt{< n > /2B}$ could be interpreted as the equivalent noise charge. With an assumption that Z_s is purely capacitive, i.e. $Z_s = 1/j\omega C_D$, and i_n^2 and v_n^2 have no frequency dependence:

$$enc^2 = i_n^2\int_{-\infty}^{\infty} h(t)^2dt/2 + v_n^2C_D^2\int_{-\infty}^{\infty} h'(t)^2dt/2 \tag{5.10}$$

where we have used formulae:

$$\int_{-\infty}^{\infty} |H(\omega)|^2df = \int_{-\infty}^{\infty} h(t)^2dt \tag{5.11}$$

and

$$\int_{-\infty}^{\infty} \omega^2|H(\omega)|^2df = \int_{-\infty}^{\infty} h'(t)^2dt \tag{5.12}$$

The noise analysis in terms of $h(t)$ ($H(\omega)$) is called time domain analysis (frequency domain analysis). The time domain analysis could handle complicated signal shapes which are quite tedious in the frequency domain analysis. Assuming

a lowest order shaping function:

$$h(t) = \frac{t}{t_m} exp(1 - \frac{t}{t_m}) \tag{5.13}$$

or equivalently:

$$H(\omega) = \frac{e}{t_m(j\omega + 1/t_m)^2} \tag{5.14}$$

the input equivalent noise charge is:

$$enc^2 = \frac{e^2}{4}(i_n^2 t_m + \frac{v_n^2 C_D^2}{t_m})/2 \tag{5.15}$$

$$t_m(opt) = \sqrt{\frac{v_n^2}{i_n^2}} C_D \tag{5.16}$$

The signal to noise ratio is:

$$S/N = \frac{q_s}{\sqrt{enc^2}} \tag{5.17}$$

On the other hand for the high input impedance amplifier, the total noise is evaluated in terms of an effective voltage generator:

$$V_n^2 = Z_s^2 i_n^2 + v_n^2 \tag{5.18}$$

The signal is amplified with a voltage amplifier. The transfer function for the analog chain is taken as:

$$G(\omega) = \frac{eC_D j\omega}{t_m(j\omega + 1/t_m)^2} \tag{5.19}$$

This transfer function can keep compatibility with the previous discussion. In the

time domain that yields:

$$g(t) = C_D h'(t) \tag{5.20}$$

The output noise power is:

$$\int_{-\infty}^{\infty} V_n^2 |G(\omega)|^2 df \tag{5.21}$$

The output signal is:

$$\frac{1}{2\pi} \int_{-\infty}^{\infty} Z_s I_s(\omega) G(\omega) e^{j\omega t} d\omega \tag{5.22}$$

These results give identical results either for low impedance amplifier chain or high impedance amplifier chain. The last discussion is about 1/f noise:
In terms of I_n^2 the 1/f noise is :

$$I_{1/f}^2 = 2\pi C_D^2 K_{1/f} \omega \tag{5.23}$$

The contribution to the electronics noise is:

$$\int_{0}^{\infty} I_{1/f}^2 |H(\omega)|^2 df = C_D^2 K_{1/f} e^2/2 \tag{5.24}$$

which gives a value independent of t_m. This is a specific characteristics of 1/f noise.

6. Fast amplifier system

6.1. Laplace transformation

$$H(s) = \int_0^\infty h(t)e^{-st}dt \tag{6.1}$$

If we take:

$$h(t) = \frac{t}{t_m}e^{1-t/t_m} \tag{6.2}$$

its Laplace transform is:

$$H(s) = \frac{e}{t_m}\frac{1}{(s+1/t_m)^2} \tag{6.3}$$

The inverse-Laplace transformation:

$$h(t) = \frac{1}{2\pi j}\int_{\sigma-j\infty}^{\sigma+j\infty}\frac{e}{t_m}\frac{e^{st}}{(s+1/t_m)^2}ds \tag{6.4}$$

gives a correct answer for $h(t)$.

6.2. Pole/zero cancellation

The transfer function to get pole-zero cancellation is:

$$\frac{1+t_s s}{1+t_f s}\frac{t_f}{t_s} \tag{6.5}$$

where

$$t_s > t_f \tag{6.6}$$

6.3. Common base amplifier

Input impedance The input node of the common base amplifier is at the emitter of the base grounded transistor, whose input impedance is:

$$Z_{in} \simeq \frac{V_T}{I_E} \tag{6.7}$$

Noise characteristics Because this amplifier is an open-loop amplifier, the noise performance is inferior to the common emitter amplifier configuration.

Amplifier tail The common base amplifier is easy to be affected by a stray capacitance at the high impedance gain node, which is an origin of the so-called amplifier tail. This tail could be compensated for with a scheme of pole-zero cancellation. A SPICE deck of the common base amplifier is shown below:

```
EXAMPLE-7
.MODEL M2SCXXXX NPN
QQ11 4 0 5 M2SCXXXX
QQ10 2 1 3 M2SCXXXX
QQ9  2 4 1 M2SCXXXX
VA 7 0 PWL ( 0. 0. 5.E-8 0. 5.1E-8 -2.E-2 )
RR8 4 2 10K
RR7 3 1 720
RR6 6 3 10K
RR5 6 5 10K
VV4 2 0 12
VV3 0 6 12
CC2 5 7 1P
.TEMP 27
.OP
.TRAN 1.E-8 2.E-7 0
.END
```

The base of the input transistor $Q11$ is grounded. Transistors $QQ10$ and $QQ9$ are configured as a Darlington pair. The circuit schematic is shown in Figure 7.

6.4. Common emitter amplifier

Input impedance The input impedance of the common emitter amplifier is:

$$Z_{in} = \frac{R_F}{1 + G(j\omega)} \tag{6.8}$$

Miller capacitance The effect of Miller capacitance is inherent for the high open-loop gain amplifier unless a cascode configuration is taken: The input impedance of the common emitter transistor without an aid of a cascode transistor is:

$$Z_{in} = \frac{1 + j\omega C_{BC} R_L}{j\omega C_{BC}(1 + g_m R_L)} \tag{6.9}$$

The real input capacitance C_{BC} is magnified by a factor of open-loop gain:

$$C_{in} \simeq g_m R_L C_{BC} \tag{6.10}$$

The high impedance collector load is the direct reason of large Miller capacitance. The cascode configuration has a lower collector load; the collector load of the input transistor is an emitter impedance of the cascode stage transistor.
A SPICE deck of the most primitive common emitter amplifier is shown below:

```
EXAMPLE-8
.MODEL M2SCXXXX NPN
QQ9 1 4 0 M2SCXXXX
QQ8 2 1 3 M2SCXXXX
VA 5 0 PWL ( 0. 0. 5.E-8 0. 5.1E-8 -2.E-2 )
```



```
RR7 1 2 4.5K
RR6 0 3 720
RR5 4 3 20K
VV4 2 0 6
CC3 4 5 1P
CC2 4 3 0.1P
.TEMP 27
.OP
.TRAN 1.E-8 2.E-7 0
.END
```

The emitter of the input transistor $QQ9$ is grounded. The feed back element is $RR5$. The circuit schematic is shown in Figure 8. The next SPICE deck of the common emitter amplifier has a cascode transistor:

```
EXAMPLE-9
.MODEL M2SCXXXX NPN
QQ13 3 2 7 M2SCXXXX
QQ12 7 6 0 M2SCXXXX
QQ11 4 3 5 M2SCXXXX
QQ10 2 2 1 M2SCXXXX
QQ9  1 1 0 M2SCXXXX
VA 8 0 PWL ( 0. 0. 5.E-8 0. 5.1E-8 -2.E-2 )
RR8 2 4 4.5K
RR7 3 4 4.5K
RR6 0 5 720
RR5 6 5 20K
VV4 4 0 6
CC3 6 5 0.1P
CC2 6 8 1P
```

```
.TEMP 27
.OP
.TRAN 1.E-8 2.E-7 0
.END
```

$QQ13$ is the cascode transistor, which is located just above the input transistor $QQ12$. $QQ9$ and $QQ10$ are incorporated to provide bias voltage for the cascode transistor. The circuit schematic is shown in Figure 9.

6.5. $1/t$ TAIL AND ITS CANCELLATION

The signal from the gas ionization chamber with thin wire electrode is:

$$i_s = \frac{i_0}{1 + t/t_0} \tag{6.11}$$

where i_0 is:

$$i_0 = \frac{q_s}{2t_0 ln(r_c/r_a)} \tag{6.12}$$

t_0 is:

$$t_0 = \frac{r_a}{2\mu_+ E_a} \tag{6.13}$$

It is common to approximate the 1/t tail with a few exponential time constant.

$$0.79e^{-t/1.6t_0} + 0.185e^{-t/13.5t_0} + 0.024e^{-t/113.t_0} \tag{6.14}$$

The origin of the 1/t tail is explained in Appendix F.

6.6. AMPLIFIER CHAIN

It is usual to use three pole approximation:

$$i_s(s) = i_0 t_0 \left(\frac{1.26}{1 + 1.6t_0 s} + \frac{2.50}{1 + 13.5t_0 s} + \frac{2.71}{1 + 113t_0 s}\right) \tag{6.15}$$

The pole-zero cancellation stage compensates for the second pole:

$$PZ_{1/t} = \frac{1 + 13.5t_0 s}{1 + st_m} \frac{t_m}{13.5t_0} \tag{6.16}$$

Neglecting the contribution of the third term of i_s, the signal response with the 1/t tail cancellation is approximately:

$$i_{PZ}(s) = \frac{q_{eff}}{1 + st_m} \tag{6.17}$$

where

$$q_{eff} = i_0 t_0 (1.26 + 0.185 \frac{t_m}{t_0}) \tag{6.18}$$

The preamplifier is assumed to have a single pole:

$$\frac{R_p}{1 + t_p s} \tag{6.19}$$

The pole-zero cancellation for the amplifier tail is:

$$PZ_{pr} = e \frac{1 + st_p}{1 + st_m} \frac{t_m}{t_p} \tag{6.20}$$

The total response of the signal processing chain is:

$$\frac{q_{eff} R_p}{t_p} \frac{e t_m}{(1 + st_m)^2} \longrightarrow \frac{q_{eff} R_p}{t_p} \frac{t}{t_m} e^{1 - t/t_m} \tag{6.21}$$

6.7. Noise characteristics

The possible noise source of the common emitter amplifier is characterized as follows:

$$i_n^2 = 2q(I_D + \frac{I_C}{\beta_F} + \frac{4kT}{R_f}) \tag{6.22}$$

$$v_n^2 = 4kT(r_{bb'} + r_e/2 + R_s) \tag{6.23}$$

I_D: detector leakage current

β_F: forward current gain of the input transistor

I_C: collector current of the input transistor

R_f: feed-back resistor of the amplifier

$r_{bb'}$: base spreading resistance

r_e: inverse of transconductance of the input transistor

R_s: series resistance additionally attached to the input of the amplifier

6.8. Timing resolution

The electronic nois affects on the timing resolution of the decision circuit. The timing jitter due to V_{noise} is:

$$\delta t = \frac{V_{noise}}{dV/dt} \tag{6.24}$$

It is apparent that the steep wave form gives better timing resolution. In practice in the case of lowest order shaping:

$$\delta t = \frac{1}{2Q_s}\sqrt{i_n^2 t_m^3 + v_n^2 C_D^2 t_m} \tag{6.25}$$

where the threshold level of the decision circuit is zero, and Q_s is the input impulse signal charge.

6.9. Counting rate due to electronic noise

It looks something wrong about the previous discussion. What is missing is the counting rate of the decision circuit. An ideal timing pick-off circuit should have higher threshold and keep reasonable timing resolution. The counting rate of the decision circuit is:

$$f_n = \frac{1}{\sqrt{3}} B e^{-V_{TH}^2/V_N^2} \tag{6.26}$$

where B is the noise frequency bandwidth, V_{TH} the threshold voltage, and V_N the r.m.s. voltage of noise.

Higher order shaping Applying a higher order shaping:

$$h(t) = (\frac{t}{t_m})^n e^{1-t/t_m} \tag{6.27}$$

the maximum of dV/dt appears at finite value of amplitude. With an aid of constant fraction decision circuit we can have lower hit frequency due to noise without deteriorating timing resolution. In practice the most steep slope appears at the fraction of:

$$(1 - \frac{1}{\sqrt{n}})^n e^{\sqrt{n}} \tag{6.28}$$

7. Low noise Amplifier system

7.1. Charge sensitive amplifier

Circuit configuration A circuit schematic of a typical charge sensitive amplifier is shown in "EXAMPLE4".

Signal chain

Signal source:

$$i_s = Q_s\delta(t) \tag{7.1}$$

Preamplifier:

$$\frac{R_f}{1+sC_fR_f} \tag{7.2}$$

Pole-zero canceller:

$$\frac{1+sC_fR_f}{1+st_m}\frac{t_m}{C_fR_f} \tag{7.3}$$

Integrator:

$$\frac{e}{1+st_m} \tag{7.4}$$

Total response:

$$\frac{Q_s}{C_f}\frac{et_m}{(1+st_m)^2} \longrightarrow \frac{Q_s}{C_f}\frac{t}{t_m}e^{1-t/t_m} \tag{7.5}$$

Electronic noise

The electronic noise charge of the JFET-input charge sensitive amplifier is:

$$enc^2 = \frac{e^2}{4}\left(\frac{2}{3}\frac{4kT}{g_m}\frac{(C_D+C_G)^2}{t_m} + \left(2q(I_D+I_G) + \frac{4kT}{R_F} + \frac{4kT}{R_B}\right)t_m\right)\Big)/2 \tag{7.6}$$

where

g_m: transconductance of the input FET

C_D: detector capacitance

C_G: gate capacitance of the input FET

I_D: detector leakage current

I_G: gate leakage current of the input FET

R_F: feed back resistor of the amplifier

R_B: detector bias resistor

7.2. High capacitance detector

There are two techniques which are inherent for operation of the high capacitance detector.

Capacitance matching Reminding that the transconductance of the JFET is:

$$g_m = \mu C_g\frac{W}{L}(V_{GS} - V_{TO}) \tag{7.7}$$

it is apparent that the transconductance is proportional to the total gate capacitance C_G, i.e. WLC_g. The first term of eq. (7.6) is proportional to:

$$\frac{(C_D+C_G)^2}{C_G} = C_D(\sqrt{C_D/C_G} + \sqrt{C_G/C_D})^2 \tag{7.8}$$

which gives minimum when $C_D = C_G$.

Transformer coupling When the source capacitance is very large and it is very hard to reach the capacitance matching condition, the way to solve the problem is to use a transformer. The I/V relations of the lossless transformer are:

$$n_1I_1 = n_2I_2 \tag{7.9}$$

$$V_1I_1 = V_2I_2 \tag{7.10}$$

Then we have a impedance conversion relation:

$$\frac{Z_1}{n_1^2} = \frac{Z_2}{n_2^2} \tag{7.11}$$

The source impedance could be increase by a factor of n^2 while the signal is decreased by a factor of n^{-1}, where $n = n_2/n_1$, and $Z_1 = 1/j\omega C_D$. We can improve the S/N ratio by a factor of n. The capacitance matching condition is:

$$\frac{C_D}{n^2} = C_G \tag{7.12}$$

7.3. Cold termination

The detectors which have tranmission characteristics may be terminated with their poper impedance at the preamlifier end. A resistor is a bad practice for signal termination, because resistive elements are source of electronic noise. The cold termination is an idea to terminate the detector signal with no resistive elements. Assuming an effective impedance Z_L at the high impedance node of the amplifier (node 2 in the example-4), the input impedance is evaluated as:

$$Z_{in} = \frac{Z_f}{g_m Z_L} \tag{7.13}$$

where Z_f is the impedance of the feed back elements, g_m is the transconductance of the input transistor. Locating a few ten's of pF of capacitor (C_L) for Z_L, and assuming that the feed back impedance is approximated as capacitive (C_f), the input impedance is purely resistive:

$$Z_{in} = \frac{C_L}{g_m C_f} \tag{7.14}$$

as far as low frequency characteristics are concerned.

7.4. Subsidiary effects

pile-up:
The output of the shaping amplifier has commonly slow tail. When the input signal rate is very high, two or more signals have a chance to pile up, which potentially deteriorates measurement resolution. baseline-restorer:
It is quite common to have an undershoot in an AC coupled system with unipolar shaping. The base line restorer suppresses undershoot swing of voltage. The bipolar shaping is free from base-line shift under an ideal condition. ballistic deficit:
Because the signal from radiation detector takes a finite period instead of delta impulse, a signal processing system with short integration time uses only a fraction of the detector generated charge. The ballistic deficit is a measure of the inefficiency of signal integration.

8. Silicon strip detector

The silicon strip detector is reverse biased p-i-n diode, whose operational behaviors are characterized in terms of the depletion property of the diode structure. The detector thickness is 300 μm with n-type bulk material, whose resistivity is 4 to 6 $k\Omega$ cm.

8.1. Depletion property

Assuming a step junction, the potential filed in the depletion region is:

$$\phi_- = \frac{qN_A}{\epsilon\epsilon_0}(x^2/2 + l_p x) \tag{8.1}$$

$$\phi_+ = \frac{qN_D}{\epsilon\epsilon_0}(-x^2/2 + l_n x) \tag{8.2}$$

where
ϕ_-: potential in the p-type region
ϕ_+: potential in the n-type region
ϵ: dielectric constant of silicon
N_A: acceptor concentration in the p-type material
N_D: donor concentration in the n-type material
l_p: width of the depletion region developed in the p-type region
l_n: width of the depletion region developed in the n-type region
x: coordinate measured from p-side to n-side, whose origin is located at the junction boundary.
These solutions are from Poisson equations:

$$\frac{d^2\phi_-}{dx^2} = \frac{qN_A}{\epsilon\epsilon_o} \tag{8.3}$$

$$\frac{d^2\phi+}{dx^2} = -\frac{qN_D}{\epsilon\epsilon_o} \tag{8.4}$$

The electric filed is given as:

$$E_- = \frac{qN_A}{\epsilon\epsilon_0}(x + l_p) \tag{8.5}$$

$$E_+ = \frac{qN_D}{\epsilon\epsilon_0}(-x + l_n) \tag{8.6}$$

The electric field should be continuous at $x = 0$:

$$E_+(0) = E_-(0) \tag{8.7}$$

$$N_A l_p = N_D l_n \tag{8.8}$$

The electric field shows its maximum at $x = 0$:

$$E_{max} = \frac{qN_A}{\epsilon\epsilon_0} l_p = \frac{qN_D}{\epsilon\epsilon_0} l_n \tag{8.9}$$

The potential difference across the diode is:

$$\phi(x = l_n) - \phi(x = -l_p) = V_{bi} - V \tag{8.10}$$

where V_{bi} is a build-in potential. If we assume:

$$l_n \gg l_p \tag{8.11}$$

and also

$$N_A \gg N_D \tag{8.12}$$

for example $l_n = 300\ \mu m$, and $l_p = 1\ \mu m$, the potential drop across the p-

implantation is negligible. Then we have:

$$V_{bi} - V = \frac{1}{\rho\mu_e}\frac{2l_D^2}{\epsilon\epsilon_0} \tag{8.13}$$

where ρ is the bulk resistance of silicon:

$$\rho = \frac{1}{q\mu_e N_D} \tag{8.14}$$

μ_e is the mobility of electron carrier, and l_D is the depletion width:

$$l_d = l_p + l_n \tag{8.15}$$

8.2. Junction capacitance

The junction capacitance is:

$$C = \frac{\epsilon\epsilon_0}{l_d}\ F/m^2 \tag{8.16}$$

$$C = \frac{C_{j0}}{\sqrt{1 - V/V_{bi}}} \tag{8.17}$$

where

$$C_{j0} = \sqrt{\frac{2\epsilon\epsilon_0}{\rho\mu_e V_{bi}}} \tag{8.18}$$

8.3. Leakage current

The leakage current of the p-i-n diode under the reverse bias condition is:

$$I_{gen} = \frac{1}{2} q \frac{n_i}{\tau_0} l_d \quad A/m^2 \tag{8.19}$$

where τ_0 is the effective carrier life time. In Appendix B, we have shown that the leakage current is well described by the SHR model.

8.4. Charge transport

Drift

The carrier velocity is:

$$v_{e,h} = \mu_{e,h} E \tag{8.20}$$

where μ_e, and μ_h are mobilities of electron and hole, E is the electric field.

Diffusion

The diffusion equation is:

$$\frac{\partial n}{\partial t} = D \frac{\partial^2 n}{\partial x^2} \tag{8.21}$$

where

$$D = V_T \mu \tag{8.22}$$

Assuming a Gaussian distribution which is centered at x=0:

$$n = \frac{n_0}{\sqrt{2\pi}\sigma(t)} exp(-\frac{x^2}{2\sigma(t)^2}) \tag{8.23}$$

We obtain an approximate solution:

$$\sigma(t) = \sqrt{2Dt} \tag{8.24}$$

Hall coefficient

The magnetic field affects on the drift property of carrier; this is from the Lorentz force:

$$tan(\theta) = \mu_H B \tag{8.25}$$

where μ_H is a Hall mobility, and B is the strength of magnetic field in Tesla.

8.5. Signal Generation

An infinitesimal electrode is introduced in the sensitive volume of the detector, where we locate signal charge q_s. The readout electrode is indexed as 1, and the hypothetical electrode is indexed as 2. When q_s=0 there stands:

$$Q_1 = C_{11} V_1 + C_{12} V_2 \tag{8.26}$$

$$0 = C_{21} V_1 + C_{22} V_2 \tag{8.27}$$

where C_{ij} is the capacitance matrix elements between the electrodes. When non-zero q_s is located:

$$Q_1 + Q = C_{11}(V_1 + \Delta V_1) + C_{12}(V_2 + \Delta V_2) \tag{8.28}$$

$$q_s = C_{21}(V_1 + \Delta V_1) + C_{22}(V_2 + \Delta V_2) \tag{8.29}$$

Using symmetric property of the capacitance matrix:

$$\frac{q_s - C_{22}\Delta V_2}{\Delta V_1} = \frac{Q - C_{11}\Delta V_1}{\Delta V_2} \tag{8.30}$$

Neglecting the second order infinitesimal term:

$$Q = q_s \frac{\Delta V_2}{\Delta V_1} \tag{8.31}$$

When q_s moves towards the readout electrode, signal current is induced on there:

$$i = \frac{dQ}{dt} = q_s \frac{d}{dx}\left(\frac{dV_2}{dV_1}\right)\frac{dx}{dt} \tag{8.32}$$

$$i = -q_s \frac{dE}{dV_1} v \tag{8.33}$$

$$\frac{dE}{dV_1} = -\frac{1}{l_d} \tag{8.34}$$

$$q = \int_{t_1}^{t_2} i dt = \int_{x_1}^{x_2} \frac{q_s}{l_d} dx = \frac{q_s}{l_d}(x_2 - x_1) \tag{8.35}$$

The ionization charge which is generated in the vicinity of the readout electrode and moves towards the readout electrode does contribute negligible part for signal generation.

9. VLSI electronics for silicon strip detector

In order to meet with narrow pitch of the silicon-micro strip detector, an advanced MOS technology is a mandatory part for electronic system design.

9.1. CMOS AMPLIFIER

The CMOS amplifier chain for the silicon strip detector consists of a large input FET, cascode transistor, cascode load, feed back capacitor, reset switch, and sample hold circuits. They are described below separately.

Large CMOS input FET

In order to get high value of g_m, we use a very large transistor with large W/L aspect ratio.

Cascode transistor

The Miller capacitance is approximately:

$$C_M = C_{GD}\frac{g_{m1}}{g_{m2}} \tag{9.1}$$

where g_{m1} is the transconductance of the input transistor, and g_{m2} is that of the cascode transistor. Without the cascode transistor g_{m2} might be replace by an amplifier's internal load, that is larger than g_{m2} by 10^2 to 10^3.

Cascode load

The output impedance of the cascode transistor could be much higher than the single transistor:

$$Z_{out} = rd_1 + rd_2 + rd_1 rd_2 g_{m2} \tag{9.2}$$

where rd_1 and rd_2 are drain output impedance. In order to drive this result, it should be note that there stands :

$$i_d = v_{gs} g_m + \frac{v_{ds}}{r_d} \tag{9.3}$$

Reset switch The restoration mechanism for the amplifier is due to an analog switch instead of a large feedback resistance for the JFET charge amplifier.

Sample and hold

The sample and hold circuit consists of an analog switch, a capacitor, and a high imput impedancce buffer. The analog output of the preamplifier is sampled and held at the capacitor for each predetermined time step.

A SPICE deck of the cascode CMOS amplifier is shown below:

EXAMPLE-10

.MODEL MPMOS PMOS VTO=-0.88 TOX=26N LEVEL=3...

```
.MODEL MNMOS NMOS VTO=0.88 TOX=26N LEVEL=3...
MQ66 38 9 1 1 MPMOS L=1.4U W=9U
MQ65 11 38 1 1 MPMOS L=1.4U W=40U
MQ64 11 10 1 1 MPMOS L=1.4U W=40U
MQ63 10 9 1 1 MPMOS L=1.4U W=40U
MQ62 10 11 1 1 MPMOS L=1.4U W=40U
MQ61 38 9 0 0 MNMOS L=1.2U W=3.6U
MQ60 37 38 0 0 MNMOS L=1.2U W=32U
MQ59 11 10 37 0 MNMOS L=1.2U W=32U
MQ58 10 11 36 0 MNMOS L=1.2U W=32U
MQ57 36 9 0 0 MNMOS L=1.2U W=32U
*
II55 2 0 70U
VV54 1 0 5
RR53 27 30 10K
RR52 26 31 10K
RR51 28 5 2K
*
MQ50 2 2 33 3 MPMOS L=1.4U W=100U
MQ49 33 35 3 3 MPMOS L=1.4U W=100U
MQ48 6 2 35 3 MPMOS L=1.4U W=100U
MQ47 35 35 3 3 MPMOS L=1.4U W=100U
MQ46 5 6 34 3 MPMOS L=4.2U W=100U
MQ45 34 35 3 3 MPMOS L=4.2U W=100U
MQ44 31 4 0 0 MNMOS L=1.2U W=40U
MQ43 3 30 31 0 MNMOS L=1.2U W=40U
MQ42 1 6 4 0 MNMOS L=3.6U W=40U
MQ41 6 6 32 0 MNMOS L=3.6U W=40U
MQ40 4 4 0 0 MNMOS L=1.2U W=40U
MQ39 32 4 0 0 MNMOS L=1.2U W=40U
```



```
MQ38 29 26 0 0 MNMOS L=1.2U W=40U
MQ37 5 6 29 0 MNMOS L=3.6U W=40U
MQ36 27 4 0 0 MNMOS L=1.2U W=40U
MQ35 3 5 27 0 MNMOS L=1.2U W=40U
*
CC34 5 0 1P
CC33 4 0 1P
CC32 35 0 1P
CC31 30 0 0.3P
CC30 26 28 0.2P
CC29 26 27 1P
*
CC27 7 0 1P
RR26 13 7 2K
RR25 12 24 10K
RR24 17 14 10K
*
MQ23 24 10 22 8 MPMOS L=2U W=3.6U
MQ22 15 10 17 8 MPMOS L=2U W=3.6U
MQ21 21 10 8 8 MPMOS L=2U W=20U
MQ20 25 5 8 8 MPMOS L=1.4U W=100U
MQ19 7 6 25 8 MPMOS L=4.2U W=100U
MQ18 19 10 8 8 MPMOS L=2U W=20U
MQ17 22 11 20 0 MNMOS L=2U W=20U
MQ16 20 4 0 0 MNMOS L=1.2U W=20U
MQ15 7 6 23 0 MNMOS L=3.6U W=40U
MQ14 23 12 0 0 MNMOS L=2U W=1200U
MQ13 0 1 16 0 MNMOS L=2U W=40U
MQ12 15 11 17 0 MNMOS L=2U W=3.6U
MQ11 18 4 0 0 MNMOS L=1.2U W=20U
```

```
MQ10 17 11 18 0 MNMOS L=2U W=20U
MQ9 19 7 17 0 MNMOS L=1.2U W=20U
MQ8 21 14 22 0 MNMOS L=1.2U W=20U
MQ7 24 11 22 0 MNMOS L=2U W=3.6U
*
CC6 12 16 0.2P
CC5 12 15 1P
CC4 14 0 0.3P
CC3 12 13 0.2P
IF 0 12 AC 1. 0.
*
VB 9 0 5.
VE 1 8 0.
VJ 1 3 0.
*
.TEMP
.OP
.AC DEC 17 1000 1.E+9
.END
```

The input n-channel MOS FET is $MQ14$. The bias current for this transistor is chosen as 70 μA. The cascode transistor $MQ15$ is located located above $MQ14$. The cascode load consists of p-MOS transistors $MQ19$ and $MQ20$. The feed back element is a 0.2 pF capacitor ($CC3$). $CC6$ is provided for test pulse injection. The SPICE deck is organized to study the input impedance under the "RESET" condition. The SPICE deck includes subsidiary digital circuit to control the reset circuit of the amplifier. The schematic appeared in Figure 10 shows only the amplifier core.

9.2. Double correlated sampling and noise characteristics

The preamplifier gives step-like response for an impulse charge. The amount of charge could be measured if we know the output voltage "before" and "after" the signal arrival. The scheme is a double correlated sampling. The impulse response of the effective signal filtering function is as follows:

$$h(t) = (1 - e^{-t/t_0})/(1 - e^{-\tau/t_0}) \quad for\ t < \tau \tag{9.4}$$

$$h(t) = e^{(\tau - t)/t_0} \quad for\ t \geq \tau \tag{9.5}$$

where

t_0: rise time of the amplifier

τ: sampling interval

9.3. Noise characteristics

The equivalent noise charge is :

$$enc^2 = \frac{i_n^2}{2}\int h(t)^2 dt + \frac{v_n^2}{2}(C_D + C_G)^2 \int h'(t)^2 dt \tag{9.6}$$

The first integral gives:

$$\frac{\tau - 2t_0(1 - exp(-\tau/t_0)) + (t_0/2)(1 - exp(-2\tau/t_0))}{A^2} + t_0/2 \tag{9.7}$$

The second integral gives:

$$\frac{1}{t_0 A} \tag{9.8}$$

where

$$A = 1 - e^{-\tau/t_0} \tag{9.9}$$

In the limit of

$$\tau \gg t_0 \tag{9.10}$$

the equivalent noise charge is:

$$enc^2 = \frac{i_n^2}{2}\tau + \frac{v_n^2}{2}(C_D + C_G)^2\frac{1}{t_0} \tag{9.11}$$

The noise behavior is quite different from the case of time continuous shaping scheme. The parallel noise is approximately proportional to τ, while the series noise is inversely proportional to t_0.

10. Summary

The circuit design is enhanced with aid of SPICE simulation. Stability analysis is an essential part of circuit design. Noise could be estimated with SPICE. The analytical formula will help to understand the origin of noise and its optimization. Integrated circuit technology was introduced in the area of high energy physics to meet with the narrow pitch readout of the Silicon micro-vertex detector. The technology is proliferated to every area of data acquisition system including both analog and digital. This text is just an entrance to wide spread electronics technology for the high energy physics experiment. We would like to encourage you to consult on the reference literatures for further study.

APPENDIX A

Continuity equation

$$\frac{\partial n}{\partial t} = \frac{1}{q} div J_n - U_n \tag{A.1}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} div J_p - U_p \tag{A.2}$$

Carrier transport equation

$$J_n = -q\mu_e n \nabla \phi_n \tag{A.3}$$

$$J_p = -q\mu_h p \nabla \phi_p \tag{A.4}$$

where ϕ_n and ϕ_p are quasi Fermi potential for electrons and holes (Boltzmann approximation):

$$\phi_n = \psi - \frac{kT}{q} ln \frac{n}{n_i} \tag{A.5}$$

$$\phi_P = \psi + \frac{kT}{q} ln \frac{p}{n_i} \tag{A.6}$$

Poisson equation ψ is determined from charge distribution:

$$\epsilon\epsilon_0 \nabla^2 \psi = -q(p - n + N_D - N_A) \tag{A.7}$$

Schockley-Read-Hall recombination The major recombination mechanism is based on SHR and Auger recombination. The SHR recombination is:

$$U_{SHR} = \frac{pn - n_i^2}{\tau_p(n + n_i exp((E_t - E_i)/kT) + \tau_n(p + n_i exp((E_i - E_t)/kT))} \tag{A.8}$$

where

τ_p: carrier life time of hole

τ_n: carrier life time of electron

E_t: energy level of the trap

E_i: center of the band gap

You should note again that $pn = n_i^2$ in the "thermal equilibrium". U_{SHR} has a finite value for "steady state" , but zero for "thermal equilibrium".

APPENDIX B

Generation-recombination current in the depletion region In the depletion region there stands:

$$p, n \ll n_i \tag{B.1}$$

When the trap band is located at the center of the band gap (i.e. $E_t = E_i$), U_{SHR} is maximized. When we take these approximation, there stands:

$$U_{SHR} = -\frac{n_i}{\tau_p + \tau_n} \tag{B.2}$$

Assuming a new parameter as an average of τ_n and τ_p, we get:

$$U_{SHR} = -\frac{n_i}{2\tau_0} \longrightarrow I_{gen} = \frac{1}{2} q \frac{n_i}{\tau_0} l_d A_J \tag{B.3}$$

APPENDIX C

Built-in potential

The built-in potential comes from balance between the diffusion and the drift due to electric field:

$$qD\frac{dn}{dx} - q\mu n\frac{dV}{dx} = 0 \tag{C.1}$$

Integrating the equation, we get:

$$\int_{x_2}^{x_1} V_T \frac{1}{n}\frac{dn}{dx} = V_1 - V_2 \tag{C.2}$$

When x_1 is in the n-type region, and x_2 is in the p-type region, $n_1 = N_D$ and $n_2 = n_i^2/N_A$:

$$V_1 - V_2 = V_T ln(n_1/n_2) = \frac{kT}{q} ln \frac{N_A N_D}{n_i^2} \tag{C.3}$$

This intrinsic potential difference is called built-in potential. In this discussion we have assumed 100% ionization of donor and/or acceptor.

APPENDIX D

Shot noise

The electronic current could be expressed as a series of delta like spike due to discrete nature of electronic charge. The Fourier transform for a single impulse charge is:

$$q\delta(t) \longrightarrow f(\omega) = q \tag{D.1}$$

The power for the frequency bandwidth of B is:

$$W = \int_{-B}^{B} |f(\omega)|^2 df = 2q^2 B \tag{D.2}$$

Assuming the average current is $I_s =< n > q$, the noise power is

$$< n > W = 2q(< n > q)B \longrightarrow i_n^2 = 2qI_sB \tag{D.3}$$

where B is the frequency bandwidth.

APPENDIX E

Thermal noise

Assuming that the resistor R is connected to a transmission line with $Z_0 = R$, the noise power transmitted via the transmission line is:

$$P_n = 2(\frac{1}{2}kT)B \tag{E.1}$$

where the factor of 2 comes from two-component nature of electro-magnetic wave. In terms of resistance R and rms noise voltage v_n due to resistance R, the power fed into the transmission line is:

$$P_n = \frac{v_n^2}{4R} \longrightarrow v_n^2 = 4kTRB \tag{E.2}$$

APPENDIX F

Signal Generation of cylindrical ionization chamber Assuming a coaxial geometry for the ionization chamber, the potential is:

$$\phi = -\frac{V_0 ln(r/r_c)}{ln(r_c/r_a)} \tag{F.1}$$

where

V_0: voltage on the inner electrode

r_c: radius of the outer electrode

r_a: radius of the inner electrode

The outer electrode is tied to ground, and signals are detected on the inner electrode. The electric field is a derivative of the potential:

$$E = -\frac{d\phi}{dr} = \frac{V_0}{rln(r_c/r_a)} \tag{F.2}$$

The current induced on the inner electrode is:

$$i = q_s\frac{dE}{dV_0}v \tag{F.3}$$

where v is the velocity of the positive ion moving toward the outer electrode, which is:

$$v = \mu_+E \tag{F.4}$$

μ_+: mobility for the positive ion

With these equations we get:

$$i = -q_s\frac{V_0\mu_+}{r^2(ln(r_c/r_a))^2} \tag{F.5}$$

In order to get a time-dependent development of the current signal we evaluate the

relation between time (t) and the radial location of the positive ion (r):

$$t = \int_{r_a}^{r} \frac{1}{v} dr = \frac{ln(r_c/r_a)}{\mu_+ V_0} \frac{1}{2}(r^2 - r_a^2) \tag{F.6}$$

which could be reduced to:

$$1 + t/t_0 = r^2/r_a^2 \tag{F.7}$$

where

$$t_0 = \frac{r_a}{2\mu_+ E_a} = \frac{r_a^2}{2\mu_+ V_0} ln(r_c/r_a) \tag{F.8}$$

E_a: electric field at the surface of the inner electrode

Eventually we get $1/t$ nature of the current signal:

$$i = -\frac{i_0}{1 + t/t_0} \tag{F.9}$$

where

$$i_0 = \frac{q_s V_0 \mu_+}{r_a^2 (ln(r_c/r_a))^2} \tag{F.10}$$

TABLE CAPTIONS

1: Physics constants used in this lecture

2: SPICE parameters for Diode

3: SPICE parameters for the BJT

4: SPICE parameters for MOS transistor

5: SPICE parameters for JFET

Table 1 Physics parameters used in this lecture

Properties	unit	
Permittivity of vacuum (ϵ_0)	F/cm	8.854E-14
Dielectric constant of silicon	-	11.9
Dielectric constant of silicon dioxide	-	3.9
Thermal voltage (kT/q)	V	0.0259
Intrinsic carrier concentration(n_i)	cm^{-3}	1.45E+10
Energy gap at 300K (E_G)	eV	1.12
Mobility (μ_e, μ_h)	$cm^2/Vsec$	1350(electron) 480(hole)
Hall mobility (μ_H)	T^{-1}	0.15 (electron) 0.035 (hole)
Diffusion constant (D)	cm^2/sec	35 (electron) 12 (hole)
Break-down voltage of Silicon	$V/\mu m$	$\sim$ 30
Energy to generate e/h pair	eV	3.6

Table 2 SPICE parameters for Diode

Symbol	Name	Parameter name	Units	Default	Example
I_s	IS	Saturation Current	A	1.0E-14	1.0E-14
r_s	RS	Ohmic resistance	Ω	0	10
n	N	Emission coefficient		1	1.0
C_{j0}	CJ0	Zero-bias depletion capacitance	F	0	2.0E-12
ϕ_0	VJ	Built-in potential	V	1	0.8
m	M	Grading coefficient		0.5	0.5
τ_t	TT	Transit time	s	0	1.0E-10

Table 3 SPICE parameters for BJT

Symbol	Name	Parameter name	Units	Default	Example
I_s	IS	Saturation current	A	1.0E-16	1.0E-15
β_F	BF	Forward current gain		100	100
β_R	BR	Reverse current gain		1	1
r_b	RB	Base resistance	Ω	0	100
r_c	RC	Collector resistance	Ω	0	50
r_e	RE	Emitter resistance	Ω	0	1
C_{je0}	CJE	BE zero-bias depletion capacitance	F	0	1.0E-12
ϕ_e	VJE	BE built-in potential	V	0.75	0.8
m_e	MJE	BE junction grading factor		0.33	0.5
C_{jc0}	CJC	BC zero-bias depletion capacitance	F	0	0.5E-12
ϕ_c	VJC	BC built-in potential	V	0.75	0.7
m_c	MJC	BC junction grading factor		0.33	0.5
C_{js0}	CJS	Zero-bias collector-substrate capacitance	F	0	3.0E-12
ϕ_s	VJS	Substrate junction built-in potential	V	0.75	0.6
τ_F	TF	Forward transit time	s	0	1.0E-10
τ_R	TR	Reverse transit time	s	0	1.0E-8

Table 4 SPICE parameter for MOS

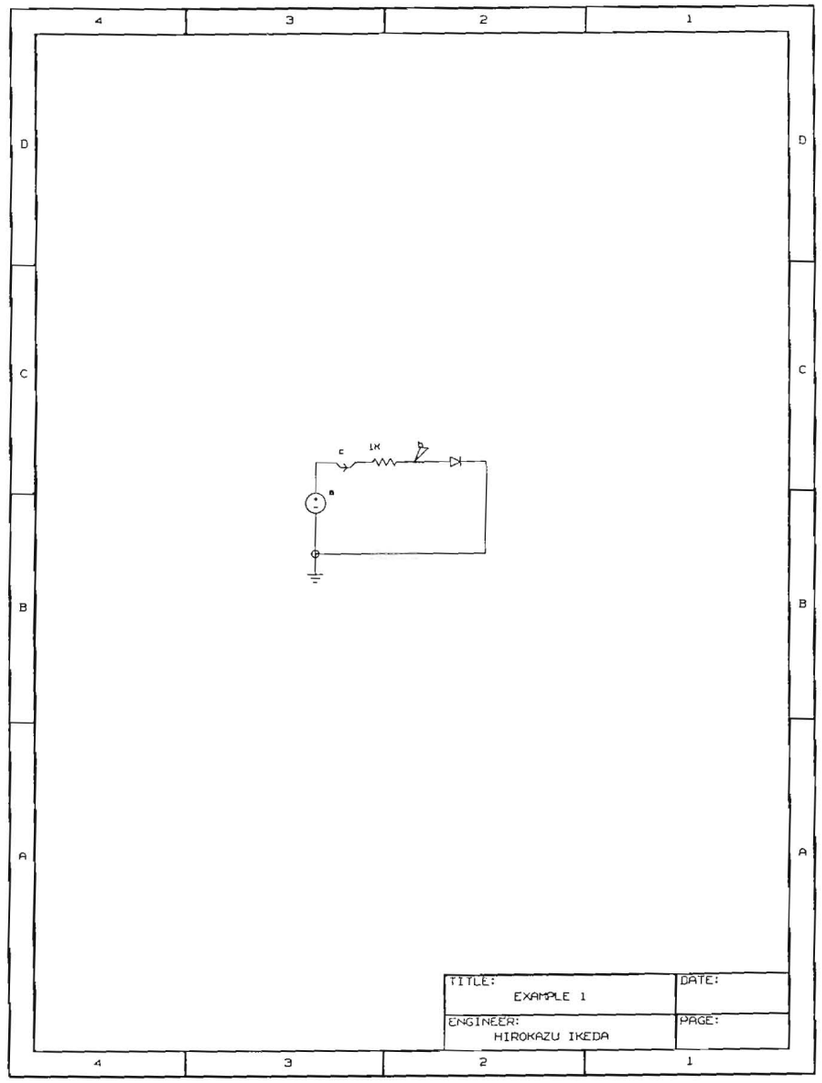
Symbol	Name	Parameter name	Units	Default	Example
V_{TO}	VTO	Threshold voltage	V	.0	1.0
β	KP	Transconductance	A/V^2	2.0E-5	3.1E-5
γ	GAMMA	Bulk threshold parameter	$V^{1/2}$	0.0	0.37
ϕ $(2\phi_i)$	PHI	Surface potential	V	0.6	0.65
λ	LAMDA	Channel length modulation	V^{-1}	0.	0.02
r_D	RD	Drain resistance	Ω	0.	1.
r_S	RS	Source resistance	Ω	0.	1.
C_{BD}	CBD	Zero-bias B-D junction capacitance	F	0.	2.0E-14
C_{BS}	CBS	Zero-bias B-S junction capacitance	F	0.	2.0E-14
I_s	IS	Bulk junction saturation current	A	1.0E-14	1.0E-15
ϕ_B	PB	Bulk junction potential	V	0.8	0.87
C_{GSO}	CGSO	Gate-source overlap capacitance	F/m	0.	4.0E-11
C_{GDO}	CGDO	Gate-drain overlap capacitance	F/m	0.	4.0E-11
C_{GBO}	CGBO	Gate-bulk overlap capacitance	F/m	0.	2.0E-19
r_{SH}	RSH	Drain/source diffusion sheet resistance	Ω/sq	0.	10.
C_J	CJ	Zero-bias bulk junction bottom capacitance	F/m^2	0.	2.0E-4
m_J	MJ	Bulk junction bottom grading coefficient		0.5	0.5
C_{JSW}	CJSW	Zero-bias bulk junction sidewall capacitance	F/m^2	0.	1.0E-9
m_{JSW}	MJSW	Bulk junction sidewall grading coefficient		0.33	-
J_s	JS	Bulk junction saturation current	A/m^2	-	1.0E-8
t_{ox}	TOX	Oxide thickness	m	1.0E-7	1.0E-7
n_s	NSUB	Substrate doping	$1/cm^3$	0.	4.0E15
X_J	XJ	Metallurgical junction depth	m	0.	1.0E-6
L_D	LD	Lateral diffusion	m	0.	0.8E-6
μ_O	UO	Surface mobility	cm^2/Vs	600	700

Table 4 SPICE parameter for JFET

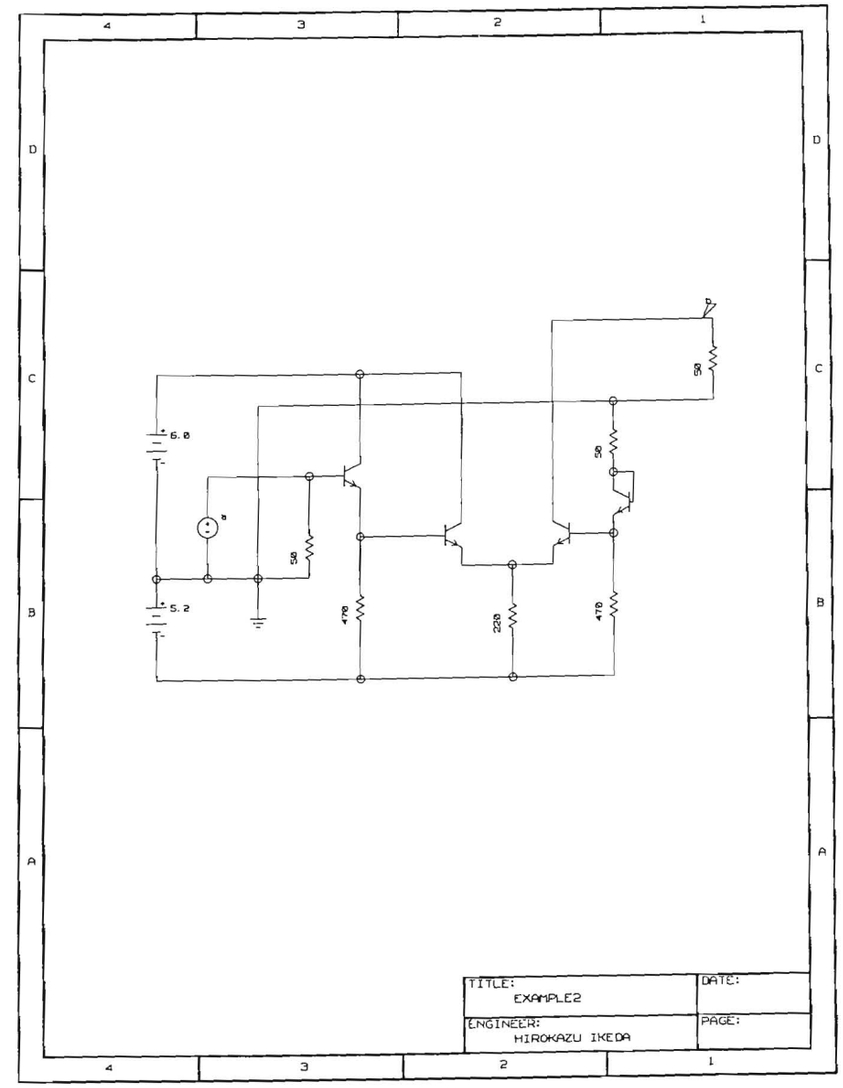
Symbol	Name	Parameter name	Units	Default	Example
V_{TO}	VTO	Threshold voltage	V	-2.0	-2.0
β	BETA	Transconductance	A/V^2	1.0E-4	1.0E-3
λ	LAMDA	Channel length modulation	V^{-1}	0	1.0E-4
r_D	RD	Drain resistance	Ω	0.	100.
r_S	RS	Source resistance	Ω	0.	100.
C_{GS}	CGS	GS zero-bias depletion capacitance	F	0.	5.0E-12
C_{GD}	CGD	GD zero-bias depletion capacitance	F	0.	1.0E-12
ϕ_S	PB	Gate junction potential	V	1.0	0.6
I_s	IS	Gate junction saturation current	A	1.0E-14	1.0E-14

FIGURE CAPTIONS

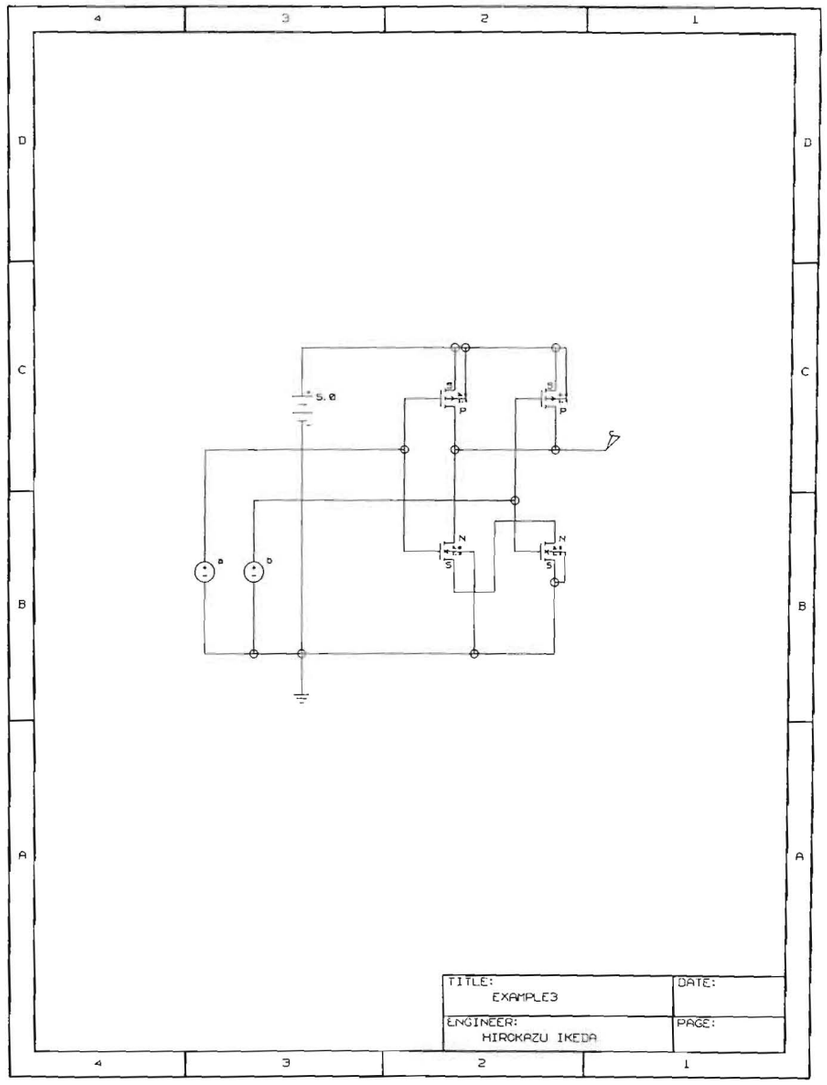
1) Example-1: Diode operation
2) Example-2: NIM-to-ECL and ECL-to-NIM converter
3) Example-3: CMOS NAND circuit
4) Example-4: Charge amplifier with n-channel JFET
5) Example-5: A follower circuit with low impedance cable driving capability
6) Example-6: Unity-gain buffer with current mirror and temperature compensated bias circuit
7) Example-7: Common base amplifier
8) Example-8: Common emitter amplifier
9) Example-9: Common emitter amplifier with cascode transistor
10) Example-10: CMOS charge amplifier



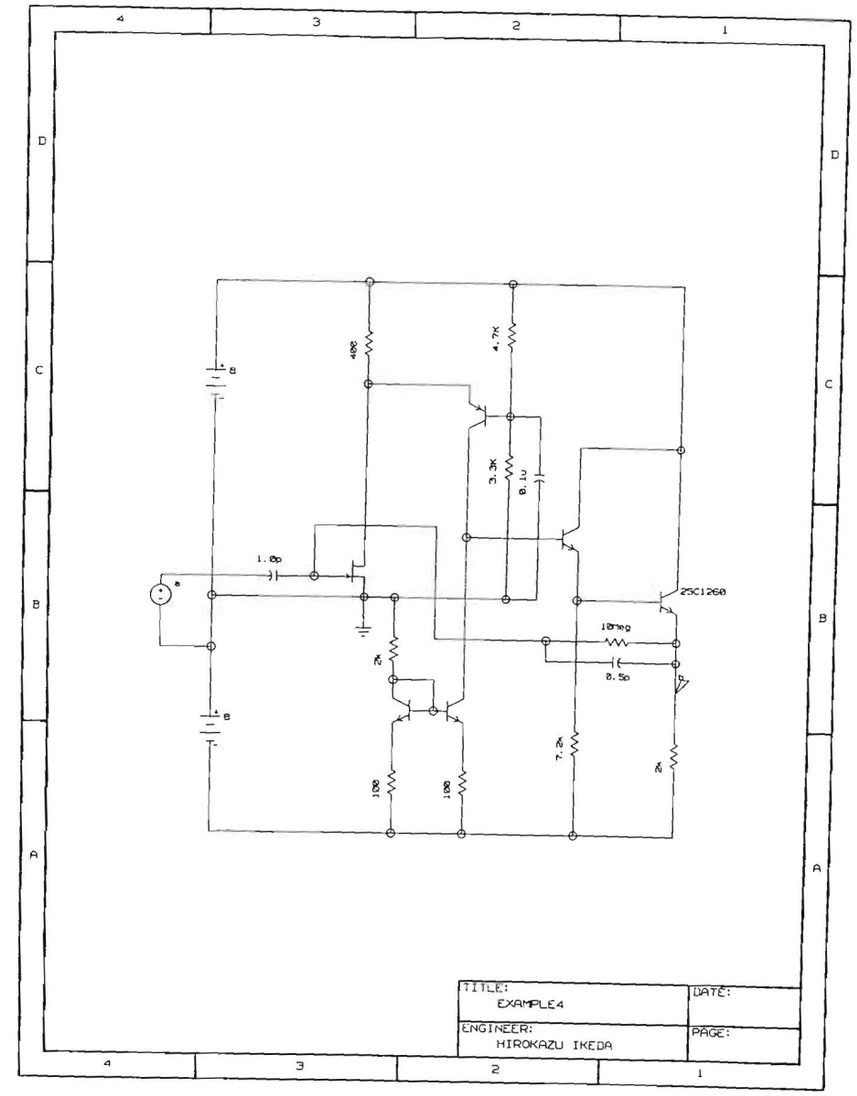
1) Example-1: Diode operation



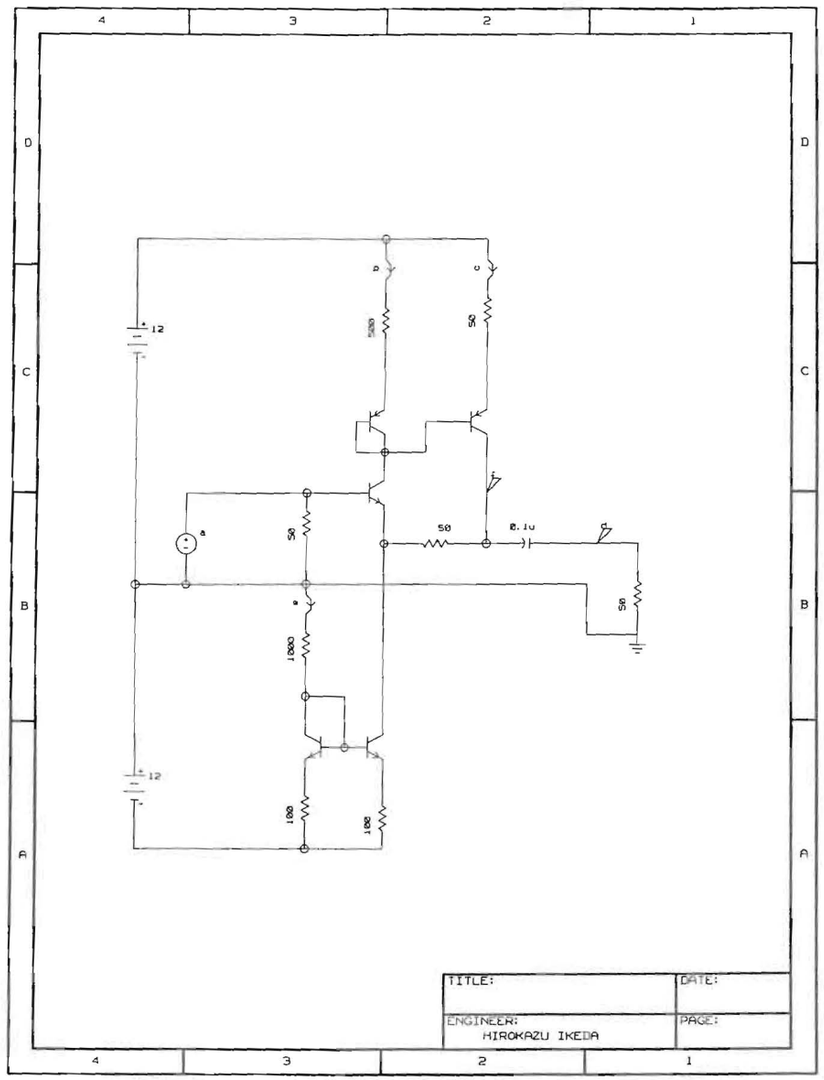
2) Example-2: NIM-to-ECL and ECL-to-NIM converter



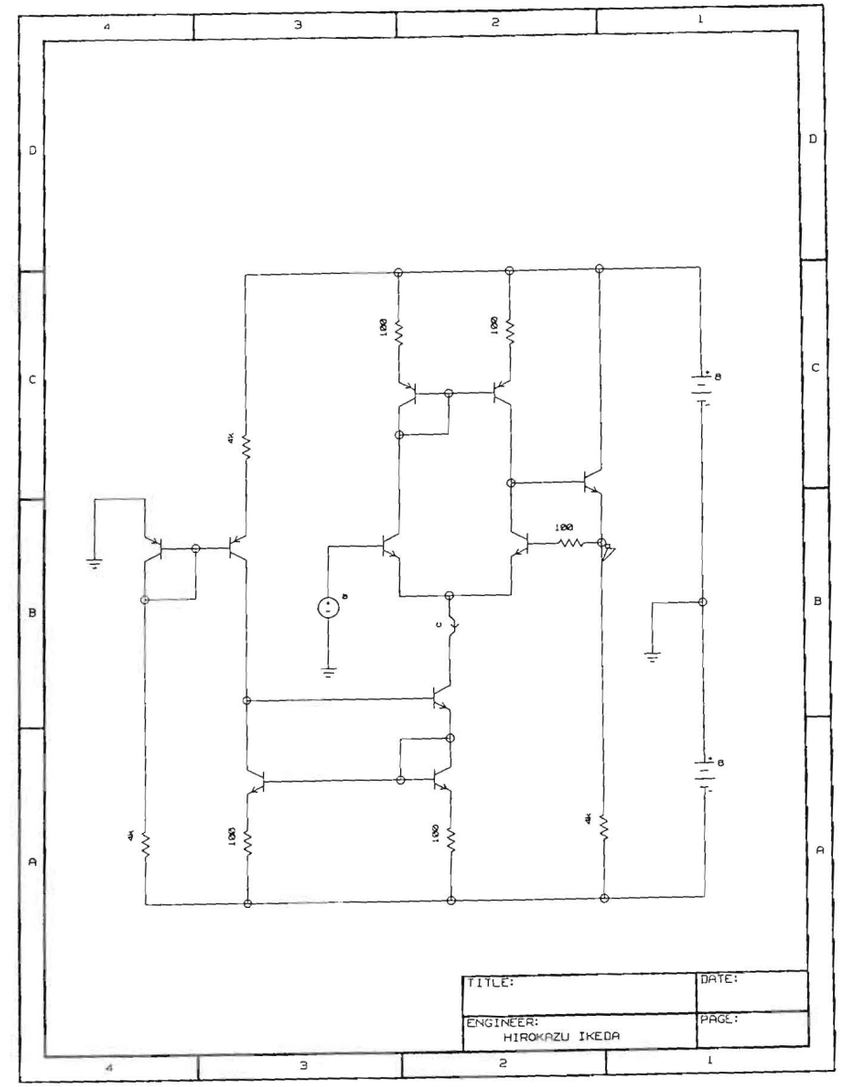
3) Example-3: CMOS NAND circuit



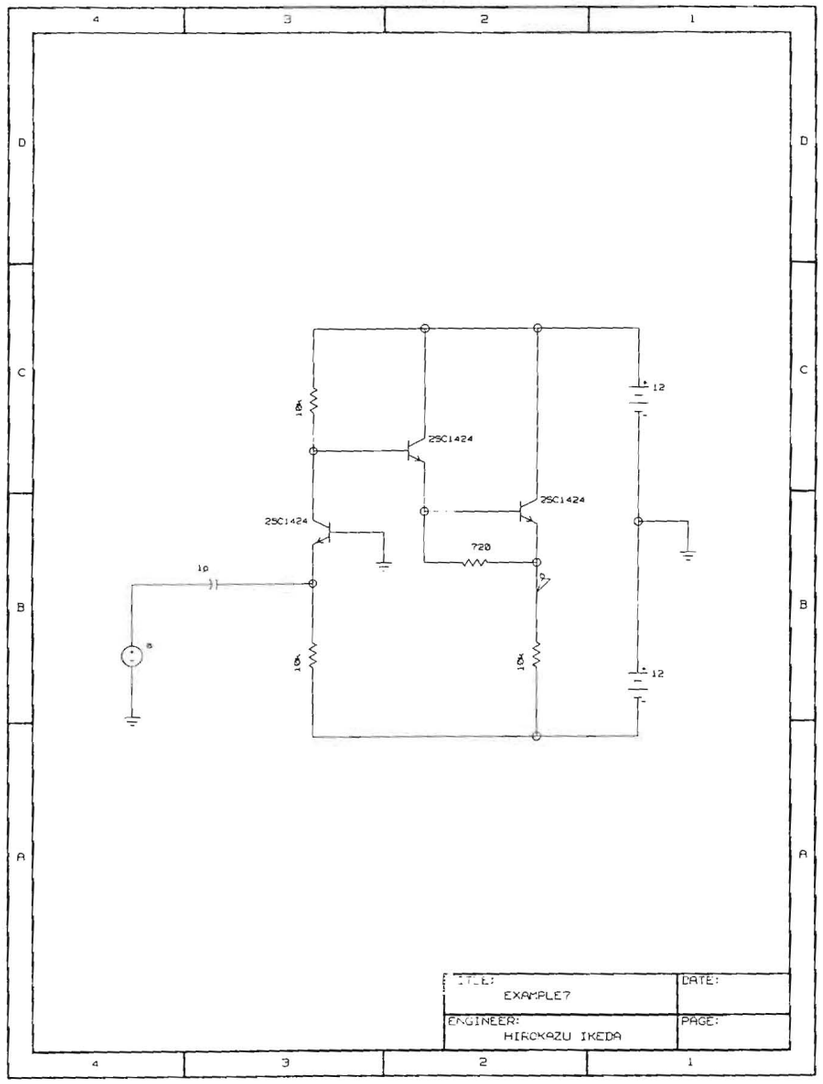
4) Example-4: Charge amplifier with n-channel JFET



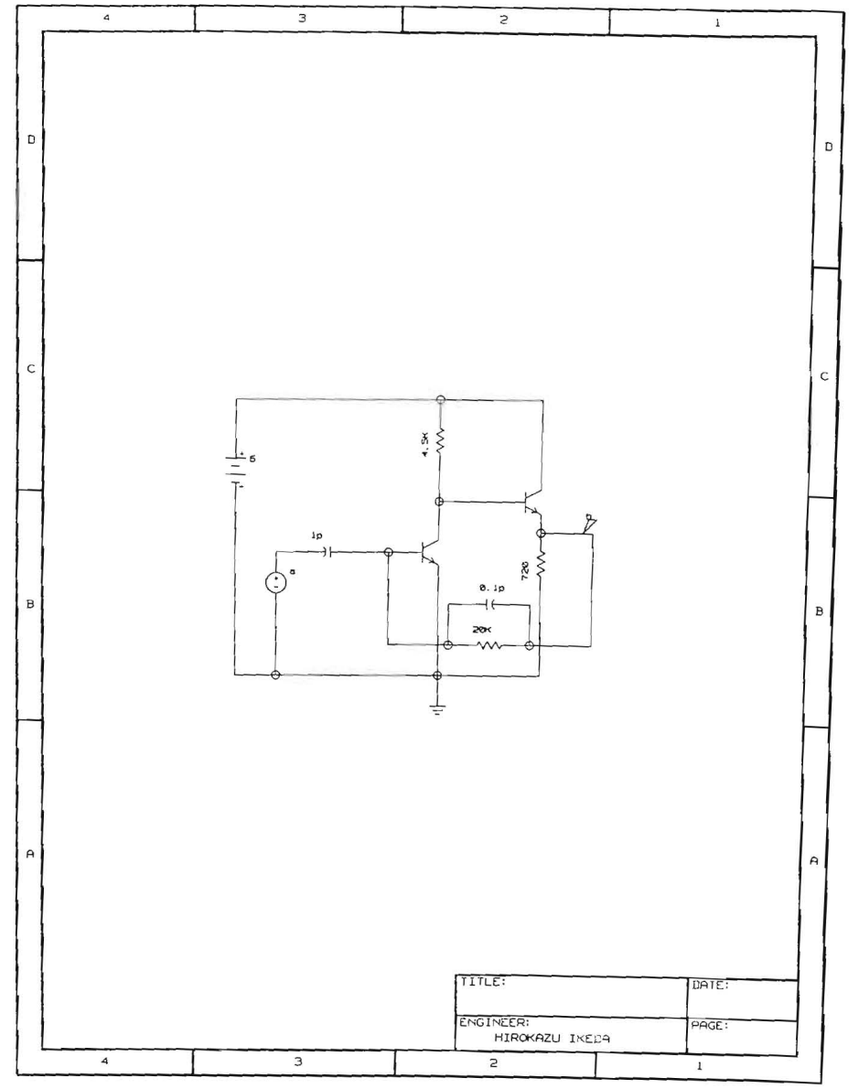
5) Example-5: A follower circuit with low impedance cable driving capability



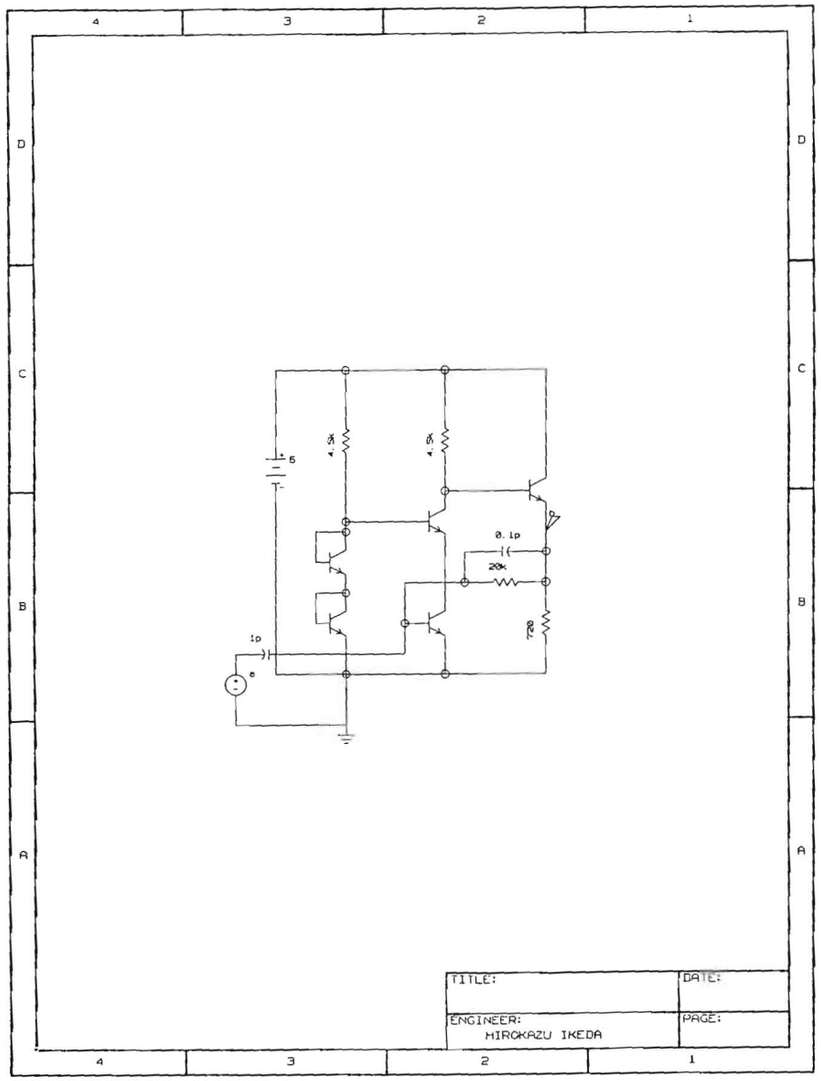
6) Example-6: Unity-gain buffer with current mirror and temperature compensated bias circuit



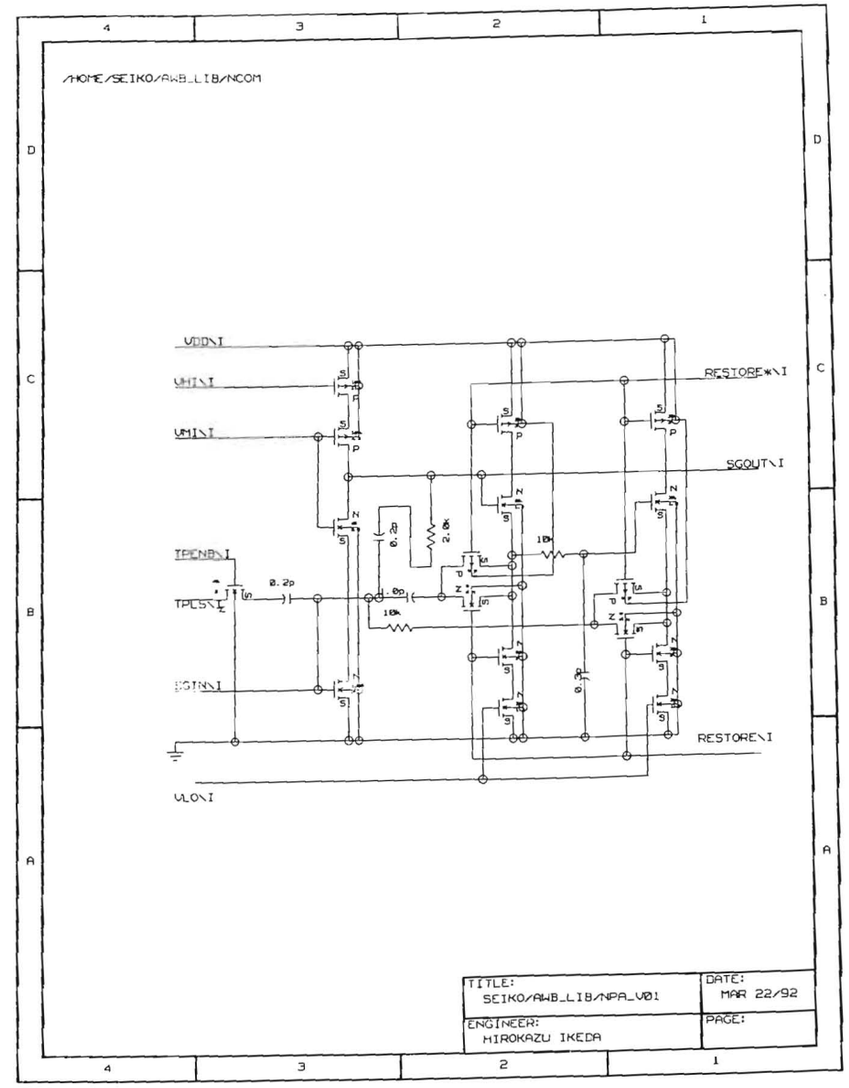
7) Example-7: Common base amplifier



8) Example-8: Common emitter amplifier



9) Example-9: Common emitter amplifier with cascode transistor



10) Example-10: CMOS charge amplifier