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CHARGED PARTICLE TRIGGER FOR THE L3 DETECTOR

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ABSTRACT

The charged particle trigger in L3 will process analog signals generated by the central tracking detector, a drift chamber with axial wires based on the Time Expansion Principle (TEC). Systems are being built for the first- and second-level triggers.

1. First-Level TEC Trigger

The first-level TEC trigger searches for tracks pointing to the interaction region in the plane normal to the beam axis. A segmentation into 96 $R\phi$ slices has been chosen to allow for an adjustable $P_\perp$ threshold ($\sim$ 600, $\sim$ 300, and $\sim$ 150 MeV/c for tracks contained in 1, 2, or 3 slices, respectively). This implies a division of each of the 24 TEC segments into four sub-segments. The trigger decision is made on the total number of tracks found, on the number of pairs of tracks with acoplanarity angles smaller than a programmable value, and on more complicated topologies. The various trigger conditions and their combinations are programmable. To meet the time requirements imposed by the drift-time of the ionization charge in the TEC (up to $10\mu s$) and by the eventual 8 by 8 bunch operation of LEP (interval between bunch crossings of $11.1\mu s$), a parallel processing technique based on look-up tables is used to make the trigger decision in less than $1\mu s$. The first-level TEC trigger is realised with modules of three different types.

1.1 "Segment Divider" Modules

For each TEC segment a "Segment Divider" module (S.D.) divides the total drift-times into two bins and solves the left-right ambiguities by means of pick-up signals induced on the grids located at the right and left of the anode plane. A diagram of one S.D. channel is shown in Figure 1. The signal from the anode wire goes through a discriminator, the threshold of which sets the efficiency of the corresponding channel. The pick-up signals from the left and right grid wires are fed to a differential amplifier located in the front-end TEC electronics. At the entrance of the S.D. module, the output signal from the differential amplifier is discriminated for positive (left side) and negative (right side) pulses. Incorrect side determination can arise from large random fluctuations of the differential signal. This source of error is reduced by a coincidence between the anode signal and the left (right) differential pulse. The logic shown in the upper right part of Fig. 1 generates four output bits, *i.e.* 2 time-bins $\times$ 2 sides (left and right). The circuit in the lower right part of Fig. 1 contains a 20 MHz clock and defines the two time-bins. If the differential signal is below threshold, the left-right ambiguity is not solved, and the left and right bits are set to one. This generates one extra hit but no loss in track-finding efficiency.

The S.D. module has been tested in a beam with a TEC prototype. Fractions of left-right ambiguous hits smaller than $\sim 5\%$ have been obtained. This can be seen from Fig. 2 which shows the amplitude distribution of the differential signal with and without tracks (the distribution is symmetric *w.r.t.* zero; only half of it is shown). The S.D. module does not add inefficiency to the analog electronics chain.

In each TEC segment, 14 wires out of 62 are used by the first-level trigger. They are distributed approximately as $\sim 1/R$, between $R = 178mm$ and $R = 413mm$. Thus, after processing by the S.D. modules, the first-level TEC trigger information consists of a 96×14 bit matrix.

1.2 "Track Finder" Modules

A flexible "Track Finder" module (T.F.) has been designed which is able to deal with different background conditions and TEC inefficiencies. The 96×14 input signals are used to address Random Access Memories (RAM) which contain the topologies of all relevant tracks. Track candidates or 'masks' are searched for in parallel in all 96 slices.[1] A schematic diagram of the T.F. module is shown in Fig. 3. Three types of tracks are found:

- Tracks with polar angle $42° \lesssim \theta \leq 90°$ and with transverse momentum $P_\perp \gtrsim 600$ MeV/c. This is realised with a 16K×1 RAM addressed by the 14 bits of a single slice (second horizontal branch in Fig. 3). The RAM-output bit is set to one when the 14-bit pattern matches one of the predefined masks. The lower limit of 42° on the polar angle of the track is set by the TEC geometry. Tracks with smaller polar angle leave the TEC through the end-flanges and miss the outer-most wires.
- Tracks with $\theta > 42°$ and $P_\perp \gtrsim 150$ MeV/c. Such tracks cross up to three adjacent slices. The corresponding S.D. modules provide 5×14 bits of information, *i.e.* one times 14 bits from the "reference slice" plus two times 2×14 bits from the two adjacent pairs of slices. To keep the size of RAM memory to a manageable level it is necessary to reduce this information. We have chosen to group the 14 bits from a single slice, radially, two by two. The grouping is a programmable AND or OR, independent for each pair of bits (lower branch in Fig. 3). In this way, if background conditions are good all pairs can be set to OR to maximize trigger efficiency. If background conditions are bad all pairs can be set to AND so as to

increase the rejection of spurious tracks. As a compromise, if the background is localised at small radii, the signals in this region can be set to AND, the others, at larger radii, to OR.

In a given T.F. module, the only masks considered are those which correspond to tracks leaving the TEC in the reference slice. An example of a mask is shown in Fig. 4. Each hit pattern is associated with a mask. There are 29 different types of masks. Each type corresponds to a given $P_\perp$ range and a given sign of curvature. In practice 25 out of the 5×7 bits provided by the S.D. modules are sufficient to address all 29 masks. The amount of RAM per T.F. module is $\sim$ 320 K-bits. Thus, in total, $\sim$ 30 M-bits of RAM are used in the first-level trigger.

- Forward tracks with $\theta \gtrsim 25°$ and $P_\perp \gtrsim 100$ MeV/c. The search for small polar angle tracks is performed with the seven inner-most wires. No AND or OR is done. The system described above is applied seqentially in time, first to find the forward tracks ($25° \lesssim \theta \lesssim 42°$), and secondly to find central tracks ($42° \lesssim \theta \leq 90°$). However, as exactly the same masks are used in both cases, the $P_\perp$ cuts will be lower for the forward tracks. Because of the difference in the maximum drift-time between inner and outer wires, no time is lost in the sequential search. The search for forward tracks can begin after $5\mu s$, $\sim 5\mu s$ before the central track search.

1.3 "Track Adder" Module

The "Track Adder" module (T.A.) counts the total number of tracks found and the number of pairs of tracks with acoplanarity angle smaller than some programmable value. It takes the first-level TEC trigger decision and sends charged track information (24 bits indicating the presence of tracks in 24 $R\phi$ segments) to the other first-level trigger processors.

2. Second-Level TEC Trigger

The second-level of the L3 trigger system is based on fast programmable processors, XOP, which are designed to reduce the trigger rate from about 100Hz at the first-level by a factor of at least ten.[2] The XOP receive, in particular, the first-level TEC trigger data, which consist of the hit pattern in the $R\phi$ projection and of the result of the track search (list of masks), and charge and drift-time measurements from charge division wires. Each TEC segment is equipped with ten resistive wires read-out at both extremities. The hit position along the wire is determined from the charge asymmetry. Charge division resolved in time has the advantage of defining track coordinates in three-dimensions.

The second-level TEC trigger is based on a single type of electronics module ("Rz" module) in which charge and drift-time are digitized and stored (Fig. 5). The charge integrating electronics has a time resolution comparable to the signal widths (typically $100ns$) and multihit capability to ensure high detection efficiency. Such a circuit requires gates directly derived from the signals to be integrated and, in order to overcome their relatively slow reset time of more than $100ns$, the use of three integrators in turn as well as analog storage of accumulated charge. The integrators have been developped at CERN by A. Beer *et al.* .[3]

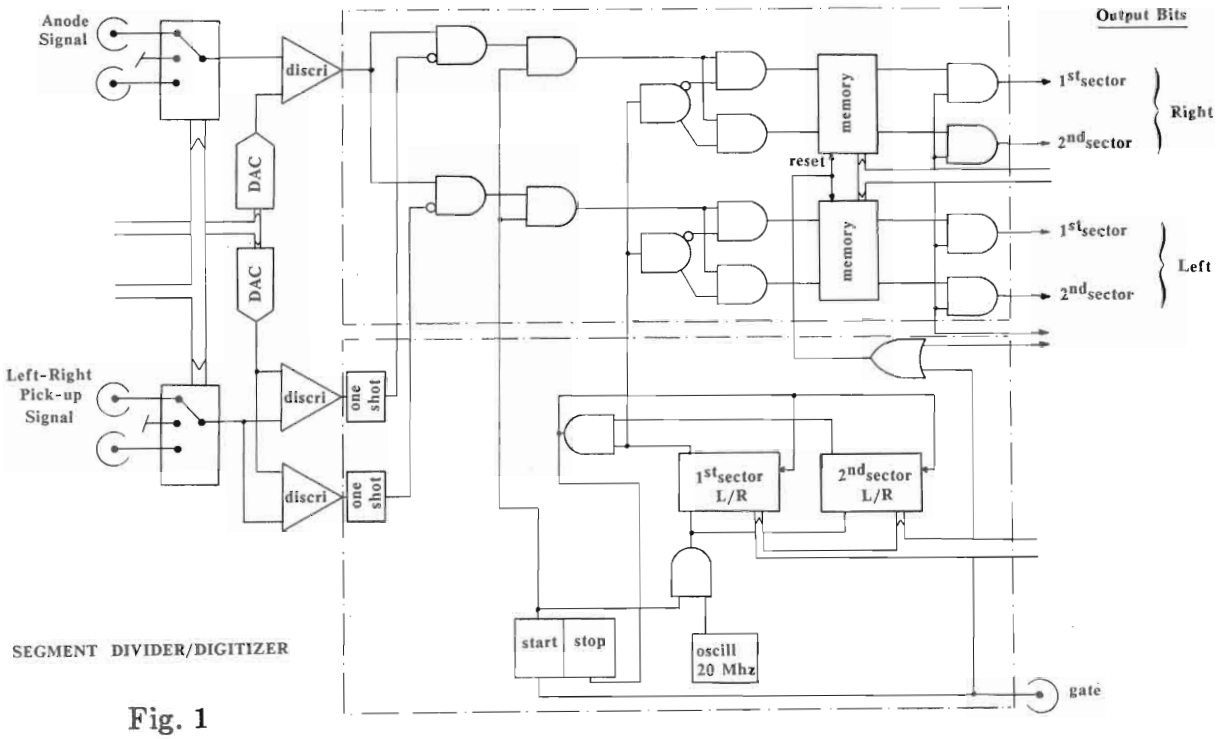
Tests done with "low" resistivity wires ($300\Omega/m$) lead us to expect a resolution $\sim 2\%$ of the wire length, *i.e.* $\sim 2cm$, with "high" resistivity wires ($\sim 2000\Omega/m$).

3. Readout

Both charged particle trigger systems are implemented in FASTBUS. The first-level TEC trigger will be housed in three FASTBUS crates, each containing 8 S.D. and 8 T.F. modules. Similarly, the second-level will be housed in three crates containing 20 Rz modules each. The trigger data are readout and transferred to the second level input memories by Lecroy 1821 Segment Manager/Interface modules (Fig. 6). A transfer speed of $0.5\mu s$ per 32-bit word has beeen obtained.

REFERENCES

1. The same method was used in the CELLO experiment at PETRA. See H.J. Behrend, Comp. Phys. Comm. 22 365 (1981).
2. J. Lecoq, "The Second-Level Trigger of L3 Experiment", this conference.
3. A. Beer, G. Critin, and G. Schuler, Nucl. Instr. Meth., A234, 294 (1985).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Output Bits
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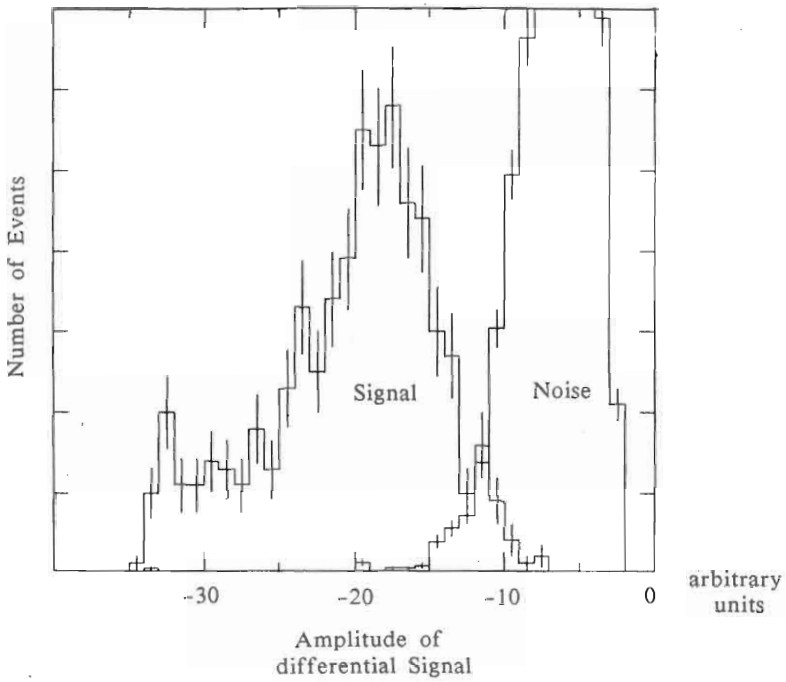
DAC
DAC
memory
memory
reset
1st sector
2nd sector
Right
1st sector
2nd sector
Left
Left-Right Pick-up Signal
discri
one shot
discri
one shot
1st sector L/R
2nd sector L/R
start
stop
oscill 20 Mhz
gate
SEGMENT DIVIDER/DIGITIZER

Fig. 1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Signal
Noise
-30
-20
-10
0
arbitrary units
Amplitude of differential Signal

Fig. 2

Track Finder (1 of 96).

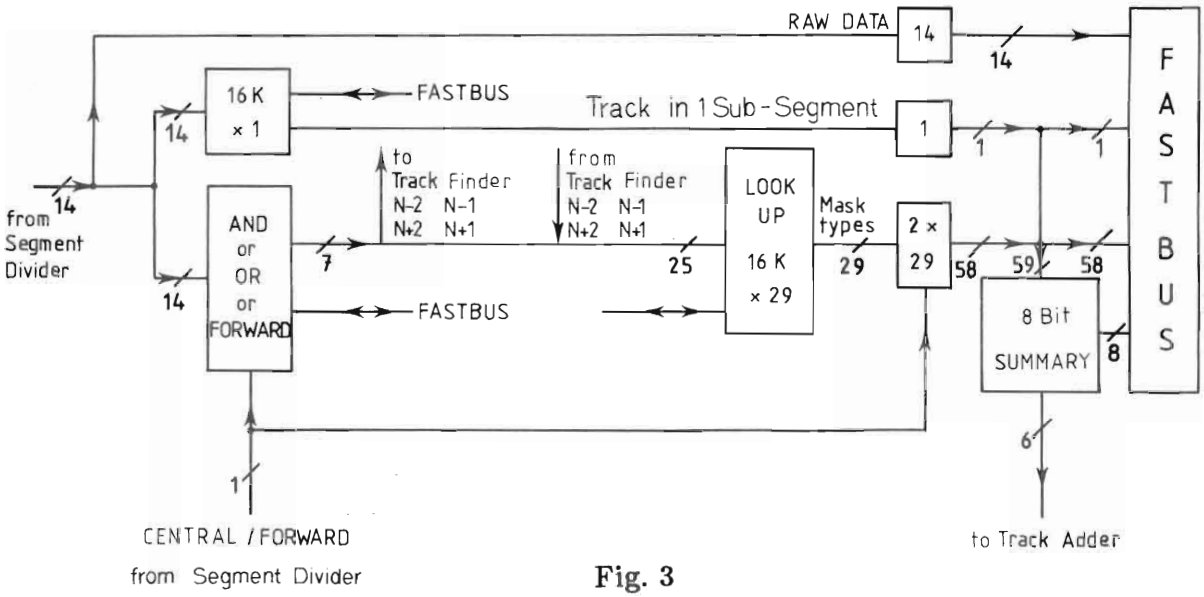
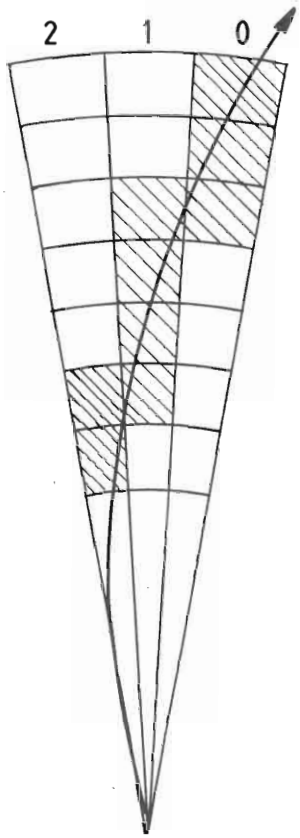


Fig. 3



MASK:

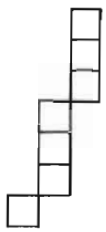


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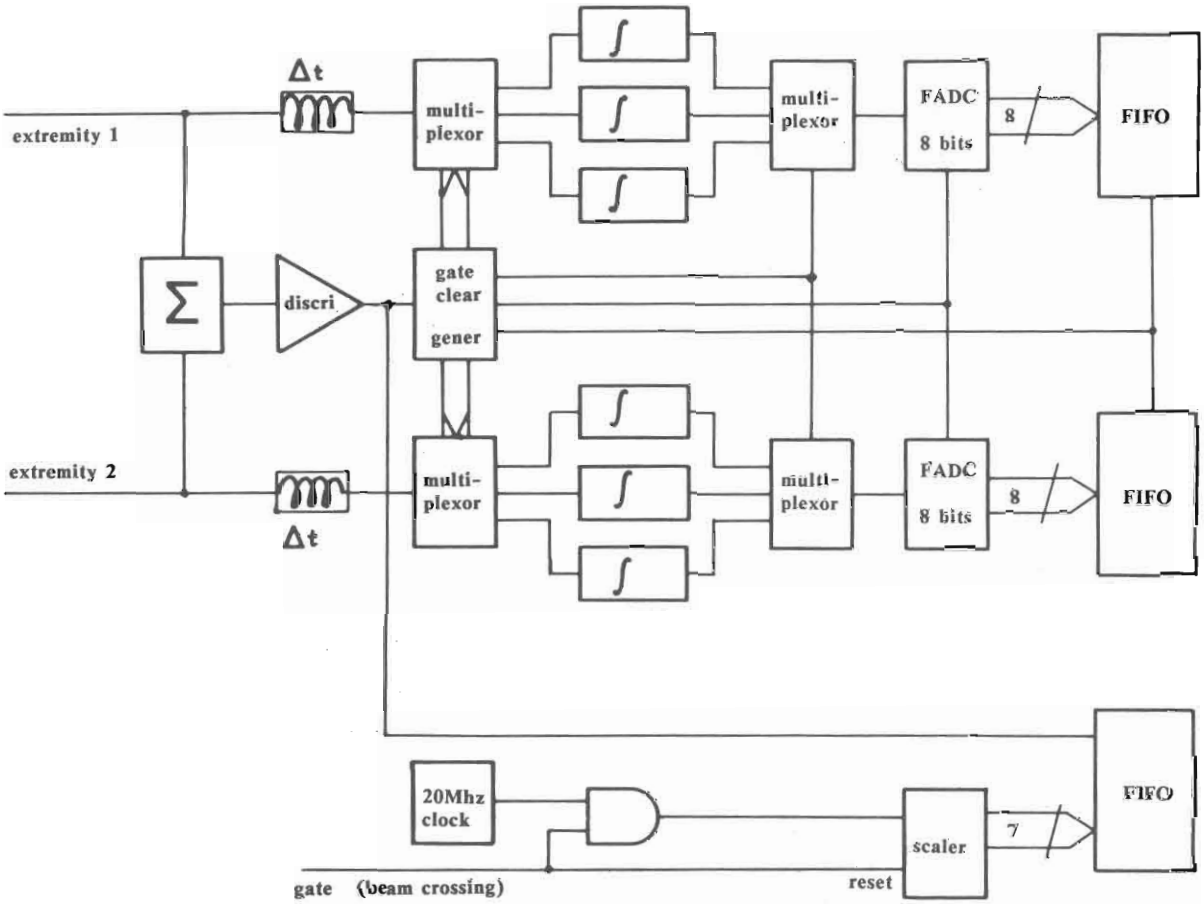
Fig.4



SECOND LEVEL TEC TRIGGER DIGITIZER

Fig. 5

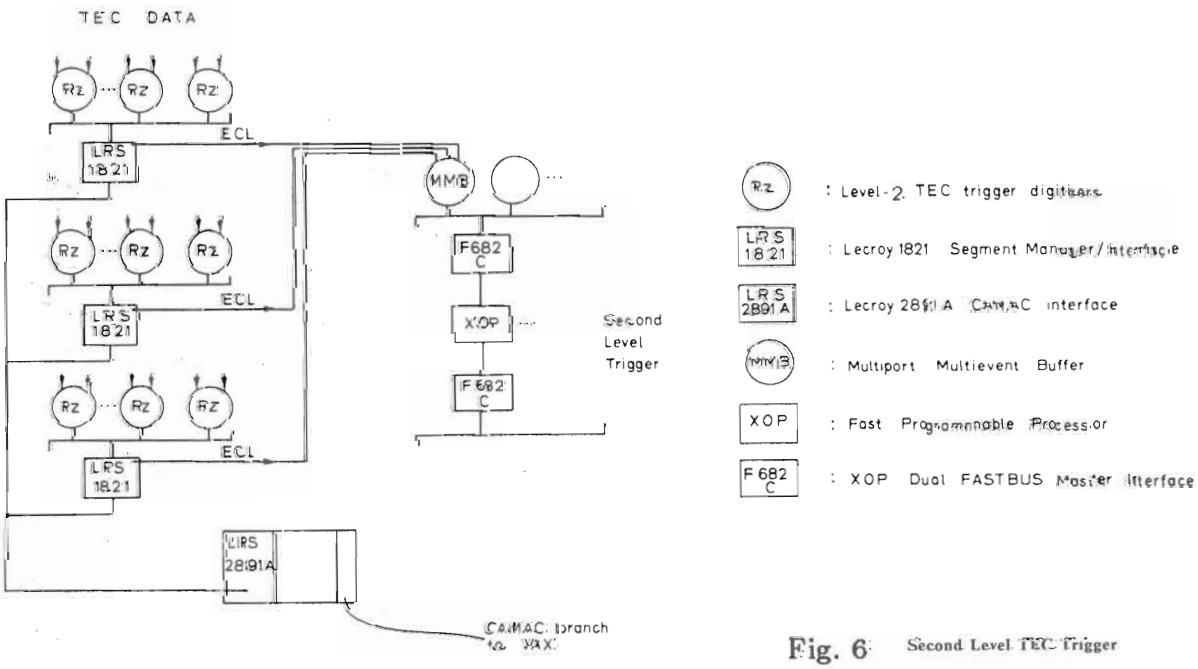


Fig. 6 Second Level TEC Trigger