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PERFORMANCE OF A SILICON MICROSTRIP DETECTOR IN A HIGH RATE ENVIRONMENT

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ABSTRACT

A new design for a silicon microstrip detector in hypernuclei electroproduction studies is examined. The detector performances are analysed in order to establish the noise level and charge collection efficiency and the working time in a high electron flux density.

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INTRODUCTION

The spectroscopic study of Λ hypernuclei in $(e,e' K^+)$ reaction on carbon target will be extended to heavier nuclei in order to reveal the spin - orbit interaction [1]. Due to its high missing mass resolution the Hall C TJNAF spectrometer is a perfect tool for such spectroscopic studies. The data taken in 1996 in $(e,e' K^+)$ reaction on proton give an insight of the resolution achieved in the experiment [2].
The SOS momentum resolution is about 500 keV for 1 GeV/c and dominates over the beam momentum, scattering angle and electron momentum resolution. The electron spectrometer has a resolution of 150 keV/mm in the focal plane. Even with a half millimeter pitch a silicon microstrip detector has a momentum resolution better than the overall resolution. According to these considerations a simpler and cheaper strip detector has been designed for the electron arm focal plane. The real problem of this silicon detector is the surface damage due to the high electron flux density in the focal plane. In the high flux electron environment, during the working time, the noise increases, the signal to noise ratio decreases and the efficiency is reduced, limiting the lifetime of the detector.

SSD DESIGN

The SSD (Silicon Strip Detector) is 72 mm long, 50 mm wide and 325 μm thick. It is placed in the electron spectrometer focal plane.

Electrons are incident on the detector at an angle varying between 30 and 60 degrees. The strips are transverse with a pitch of 500 μm, the strip width is 350 μm. The readout is AC coupled, biasing is through polysilicon . A floating guard ring is foreseen to avoid high leakage currents [3].
The strip structure proposed is shown in fig.1.

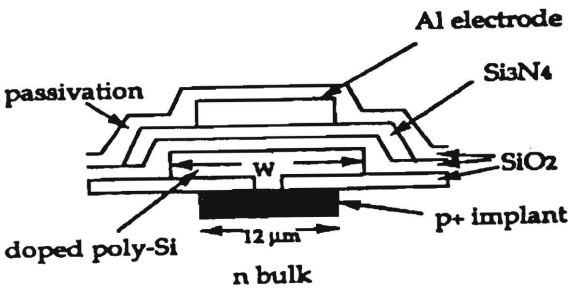

Fig.1 Schematic view of strip structure

As long as we do not need a high spatial resolution, the pitch of 500 μm is sufficient and such a choice will decrease the cost of the readout electronics.
The depletion voltage is given by

$$V_{dep} = \frac{1}{\rho\mu_e} \cdot \frac{t^2}{2\varepsilon_o \varepsilon_{Si}} = 83V$$

for ρ = 4.5 kΩ cm

μ_e = 1350 cm²/Vs

t = 0.0325 cm.

To ensure prompt collection of the charge a bias voltage of 20 V above full depletion will be used to operate SSD. This reduces the effect of drift and diffusion.
AC coupling silicon microstrip detector has the advantage of avoiding large detector currents flowing into the preamplifier. This means that the first capacitor is built within the detector by strip implantation, the oxide above it and the metal layer on top of the oxide. Furthermore it is possible to run implantation and metal at slightly different voltages. This could be used to reduce electric fields in the substrate and across the oxide in order to minimise the irradiation induced surface defect density.
The electron accumulation layer between the implanted p^+ strips plays an important role. It is established due to the positive charges within the SiO_2 and at its interface to the silicon. The defects which dominate the electronic properties of the Si/SiO_2 interface are analysed in [4].
The result is the existence of positive charges within the SiO_2 and at its interface to the silicon. The density N_{ox} is about 2 10^{11} cm^{-2} for unirradiated high quality SiO_2 grown on silicon with an <111> crystal orientation. Under ionising radiation it increases and saturates at values of several 10^{12} cm^{-2}. The increase of positive charges ΔN_{ox} is related to the flatband voltage by the relation [5]:

$$\Delta N_{ox} = \frac{\varepsilon_{Si}\varepsilon_o}{q d_{ox}} \cdot \Delta V_{fb} \text{ where } d_{ox} = 0.22\ \mu\text{m}.$$

For detectors biased at a voltage much higher than the flatband voltage the data show a saturation value of ΔV_{fb} of about 40 V. This value is increasing for smaller strip distances.
The same result is simulated by Richter et al. [6].
At N_{ox} = 3.10^{12} the depletion voltage is decreasing from about 200 V at 5 μm strip width to 120 V at 50 μm strip width.

T. Ohsugi et al. [3] measured the onset voltage of microdischarge and the leakage current for various strip geometries as a function of gamma dose. The less sensitive structure is a double layer structure with SiO_2 and Si_3N_4 shown in fig.1

CHARGE COLLECTION EFFICIENCY

As we have stressed previously [7] the charge collection efficiency is related in the first place to the ratio of the capacitances: the strip to background capacitance C_g, the interstrip capacitance C_s, and the readout capacitance C_R. The charge induced by the detected particle is shared between the two readout strips through the interstrip capacitance and the strip to background capacitance. The charge induced on C_g is lost and gives rise to charge collection inefficiency. For strip detectors with $C_g << C_s$ this inefficiency is very small.

For detectors with large pitch C_s is about equal to C_g and the resulting inefficiency must be considered.

A rough evaluation of the charge collection efficiency is given by:

$$CE \cong \frac{2C_s}{2C_s + C_g} = \frac{2}{2 + \frac{C_g}{C_s}}$$

For $C_g/C_s = 1/10$, CE = 95%, but for $C_g/C_s = 0.4$, CE = 83%.

In order to improve the efficiency of charge collection one has to increase the ratio C_s / C_g which can be done by increasing the p^+ implant width keeping the strip pitch constant.

We computed this ratio according to the formula given in [8]:

$$\frac{C_g}{C_s} = \frac{\ln(p_{st} / w_{st})}{\ln(4t^2 / p_{st} \cdot w_{st})} \qquad (1)$$

For our choice:

p_{st} = 500 μm, w_{st} = 350 μm, t = 325 μm, the ratio is 0.4. For a strip to ground capacitance of about 1.6 pF/cm the interstrip capacitance will be 4.0 pF/cm.

Krammer [9] showed that an overlap metal - layer implant increases the interstrip capacitance in addition to the capacitance obtained from the width to pitch ratio. The charge collection efficiency is increasing with the interstrip capacitance and structures with overlap show a further increase in efficiency.

Fig. 2 gives the efficiency for detectors with one or three strips with metal overlap.

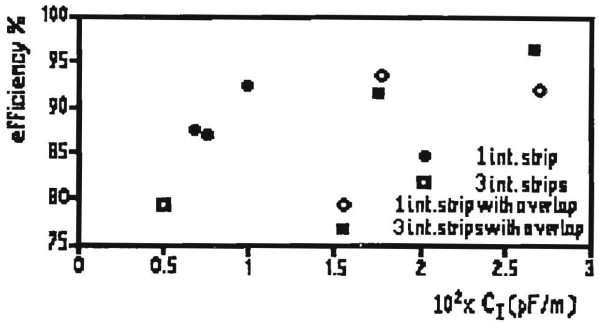

Fig. 2 Charge collection efficiency as a function of interstrip capacitance C_I

The charge collection efficiency is defined as a ratio of the charge collected from all hits to the charge collected from hits close to the readout strips.

Though intermediate floating strips would decrease with some percents the collected charge, the charge division would improve the spatial resolution with one order of magnitude for the same readout pitch, that is the same cost of the electronics.

The dependence of the efficiency on the interstrip capacitance measured by Krammer shows that for C_s = 3.5 pF/cm the efficiency is higher than 95% even for 1 or 3 intermediate strips.

The complete charge transfer to the preamplifier through the readout capacity is ensured by a high readout capacity which will be much larger than 100 pF.

Another aspect of the charge collection efficiency is the effect of the limited lifetime of the carriers. The distance traversed by the particle before recombination is d = μEτ. For 100 V bias voltage and considering the minority carriers (holes) with μ_h = 480 cm² / Vs and τ = 60 ns, d = 0.0886 cm.

The charge collection efficiency is given by:

$$CE = \frac{Q_{coll}}{Q_{ion}} = \frac{d}{t}\left(1 - \exp\left(-\frac{t}{d}\right)\right) = 0.84$$

and decreases the overall charge collection efficiency in signal detection.

NOISE CONSIDERATIONS

The price to pay for the improvement in the charge collection efficiency is the increase of the detector capacitance ($C_s + C_g$) which will increase the noise.

Following the procedure used in [7] we find for the total input capacity of the detector C_t = 38 pF, and a peaking time T_p = 225 ns:

- echivalent noise charge for channel noise
  ENC_{ct} = 1387 (e rms)
- echivalent noise charge for bulk resistance noise
  ENC_{br} = 409 (e rms)

Echivalent noise charge for flicker noise is negligible.
The last two components of the noise are related to the radiation damage which increases the leakage current and decreases the bias resistance.
Recently many papers discuss the surface damage due to high dose exposures.
In our experiment the dose will not be higher than 30 kGy. At such doses the surface generated current reaches a saturation. For a detector which has an overlap region between the electrode and the oxide, the current in the depleted zone underneath the oxide for a biased detector is given by [5]:

$$\frac{\Delta I}{A} = a[1-\exp(-b\cdot D)] \qquad (2)$$

where ΔI is in μA, A is the depleted area under the oxide in cm^2, a = 2.0 $\mu A/cm^2$ which is already the saturation value. For the saturation value we have ΔI = 500 nA/strip for a detector biased at 80 V.
There an is increase of the bulk current due to the high dose ionisation. It has been measured at Hamburg University [10]. The total bulk current measured is given by:

$$\frac{\Delta I}{V} = \alpha_\gamma \cdot D \text{ where } \alpha_\gamma = 3.9\cdot 10^{-11} \text{ A/cm}^3\text{ Gy}$$

For 30 kGy, ΔI = 0.95 nA which can be neglected.
The bulk leakage current has been computed according to the formula:

$$\frac{\Delta I}{V} = \alpha\,\Phi \qquad \text{where} \qquad \alpha = 14.4\cdot 10^{-19} \text{ A/cm}$$

For a fluence of $2.16\cdot 10^{13}$ e/cm^2 (after 600 hours work) the bulk leakage current estimated is I_{vol} = 250 nA/ strip.
Using the total leakage current we can evaluate the detector noise as:

$$ENC_{det} = \frac{e}{q}\sqrt{\frac{qI_{lk}T_p}{4}} = 1441 \text{ (e rms)}$$

Polysilicon resistors are the best candidates to provide a bias scheme integrated on the wafer itself and substantially insensitive to radiation [11]. A 10 MΩ polysilicon resistor will be used for biasing the detector. So the last term in the noise contribution will be:

$$ENC_{R_p} = \frac{e}{q}\sqrt{\frac{kTT_p}{2R_p}} = 114 \text{ (e rms)}$$

The total noise at the end of the exposure (600 h) will be:

$$ENC_{tot}^2 = ENC_{ct}^2 + ENC_{br}^2 + ENC_{det}^2 + ENC_{R_p}^2$$

$$ENC_{tot} = 2044 \text{ (e rms)}$$

The strip structure designed by Hamamatsu has been tested after irradiation with a ^{60}Co source with a dose rate of 1-2 kGy/hour up to the integrated dose of 15 kGy.
The conclusion is that Si_3N_4 coverage decreases the surface leakage current with respect to the ordinary strip structure and an extended polysilion electrode performs much better radiation hardness of the surface leakage current. Using one floating guard ring with an extended aluminium electrode the microdischarge is not observed up to 500V.

SIGNAL TO NOISE RATIO

The signal is given by the number of electron - holes created by a minimum ionising electron in the depleted volume of the detector. For tracks inclined at 45^0 the number of electron - holes created by a mip is about 50,000. For a 500 μm pitch the charge is collected by at most two readout strips.
We expect a signal of 25,000 ÷ 50,000 electrons.
Taking into account the inefficiency due to carrier lifetime and the loss of charges to the ground we can have a signal of 20,000 ÷ 40,000 electrons.
Corresponding to the calculated ENC we considered the effect of the noise to the signal distribution. The distribution of the signal for a 300 μm silicon detector is given in fig. 3.

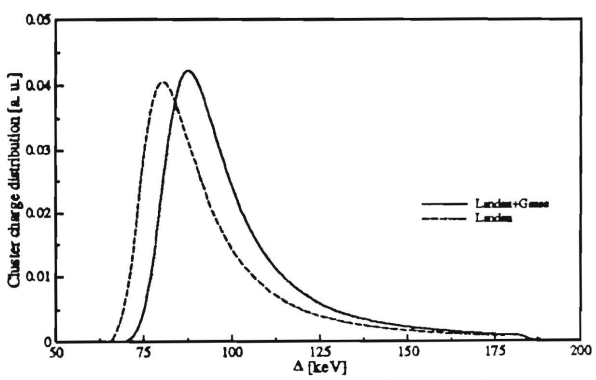

Fig. 3 Cluster charge distribution for signal and noise

The curve labelled „Landau" represents the Landau distribution which characterizes the signal [13], while for the combined signal+noise curve, we folded the signal distribution with a Gaussian with the mean value of the noise of 7.38 keV corresponding to the ENC value.

As we can see the effect of the noise is a shift according to the average noise, but the shape of the distribution remains roughly the same.

Calculating the noise distribution as the difference of the corresponding normalised integral distributions, we obtain a rather constant noise, which results mostly in a scaling of the distribution if we plot it versus the signal-to-noise ratio. (see fig. 4)

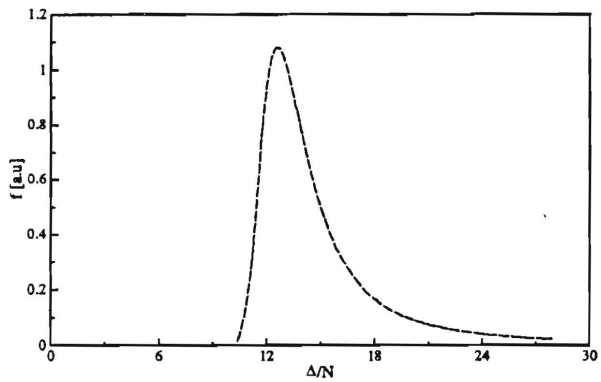

Fig. 4 Charge collection distribution versus signal to noise ratio

The most probable value of the signal-to-noise ratio will be S/N = 12.5 at the end of the run. If we cut hits at S/N = 3, we still have a detection efficiency of 100%.

Another aspect we should discuss is the effect of noise augmentation due to the increase of the interstrip capacitance. If using low noise electronics but relatively slow, this effect is small [12]. For a fast front end electronics like that required by the TJNAF experiment the slope of noise per input capacitance will be larger, in the range of 60 - 80 e/pF, value which could give a noise twice that estimated in section 4. This value will have a significant impact on the signal to noise ratio, limiting drastically the detector efficiency.

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