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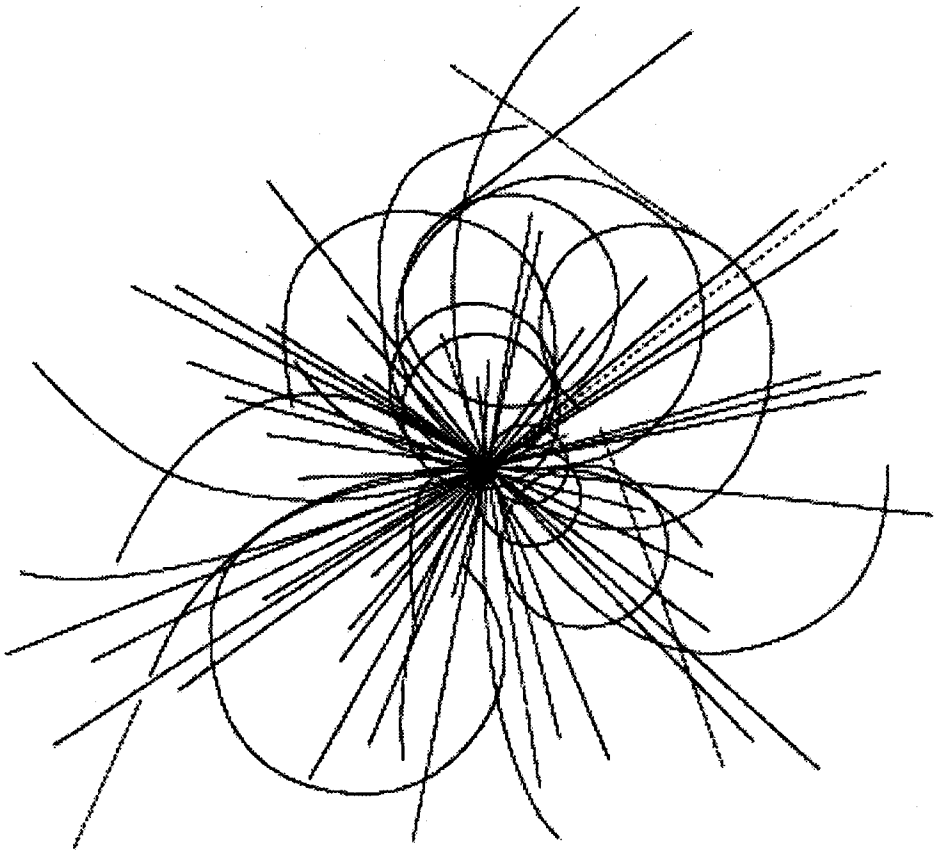
Close-out Report: Schematics and Documentation



Superconducting Super Collider Laboratory

SSCL-SR-1238

Close-out Report: Schematics and Documentation

E. Medvedko

Superconducting Super Collider Laboratory*
2550 Beckleymeade Ave.
Dallas, TX 75237 USA

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1.0 PEAK BEAM POSITION MONITOR

"Throwing pebbles into water, watch the circles left by it, otherwise your exercise is merely waste of time."

Kozma Proutkov (Russian sofa philosopher)

The main task of this work is investigation of peak detector circuit possibilities using the SPICE program. The main idea of the circuit, which was proposed by Comlinear Corporation,[1] is that the voltage on the storing capacitor (Figure 1) precisely repeats input voltage. This is done by using negative feedback. Advantage of the schematic is that during the storing process of the input signal, diode d1 is in linear regime even at small amplitudes of the input signal. (Minimum amplitude of the input signal is 20 mV.[1])

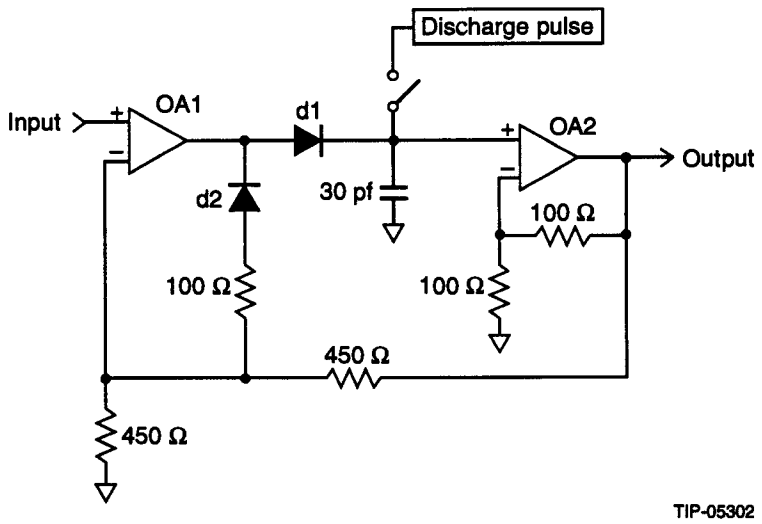


Figure 1. Peak detector circuit.

The main principle of circuit operation was described in Reference 1 and in my previous note about SPICE calculations. Some results from the previous note are repeated here as an aid in understanding the process taking place in the circuit. Simulating in the first part of my work variant of the circuit (Figure 1) differs from the schematic in Reference 1 by output buffer construction. Operational amplifier CLC400 was used as output buffer. Using CLC400 as a buffer allowed us to do circuit simulation and make a working model of the circuit. Results of the computer simulation are confirmed with the results obtained on the model. Using CLC400 as a buffer has the following disadvantages: discharge of the storing capacitor by the amplifier input current in the hold time (~150 mV during 500 ns), and increase time of the feedback closing, by comparison with circuit, using as a buffer voltage follower.

In the first part of the work sinusoidal signal as input signal was used. At the input signal frequency 1 MHz (1 V amplitude) at the time of detecting diode opening, "buildup" was noticed on the storing capacitor. The buildup looks like voltage steps on the capacitor (Figure 2(a)). At the input signal frequency (10 MHz) at the beginning of the storing process, the burst on the output of the input amplifier OA1 was registered (Figure 2(b)). Burst value is ~500 mV. That does not allows us to register the top of the input signal (*i.e.*, maximum amplitude). Resulting amplitude of the output signal is approximately 200 mV higher than input amplitude.

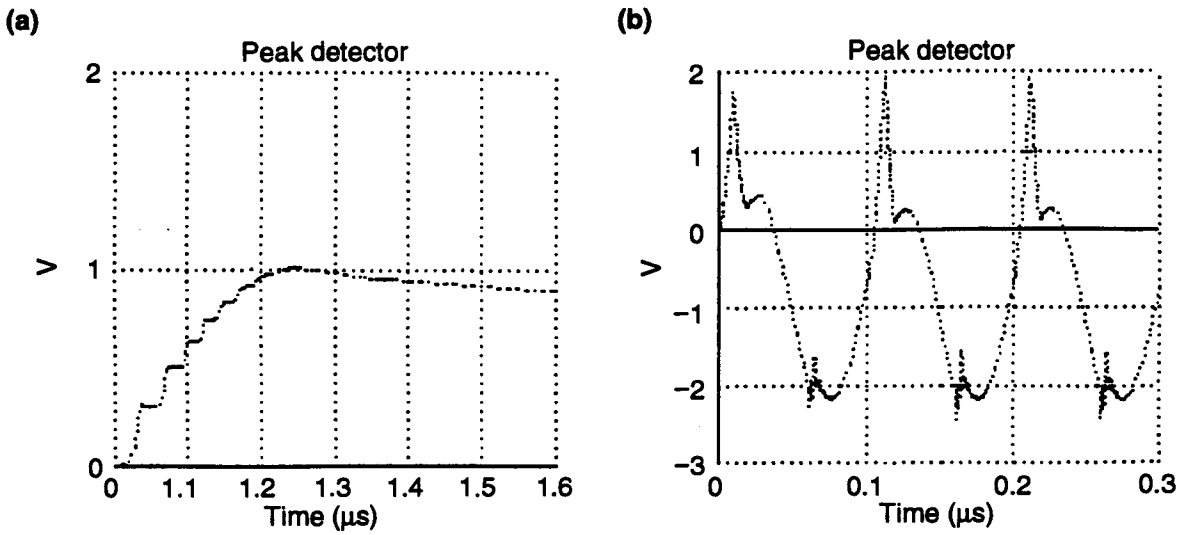


Figure 2. (a) Buildup on the capacitor; (b) burst on the OA 1 output.

One can explain the effects of the buildup on the capacitor and voltage burst on the OA1 output as follows: buildup on the capacitor can be explained by the oscillation character of the circuit transfer characteristic. The detecting diode breaks the feedback on the top of the first peak of the transfer characteristic, and the capacitor stores this peak amplitude. One can approximate the transfer characteristic by changing diode d1 to resistor 10 ÷ 15 Ω (dynamic resistance of the open diode at the linear part of diode forward characteristic). Unfortunately, a result of changing the diode to a resistor is excitement of the circuit, a fact that points to poor circuit stability.) In the second part of the work (after changing the output buffer amplifier to a voltage follower), the experiment was repeated. The transfer characteristic of the circuit had oscillatory character; that confirmed our assumption.

Let's return to the amplifier OA1 output burst. Burst is a result of the following process: during the same time period feedback is not closed. Consequently, the amplifier is open and tries to follow input voltage with maximum speed:

$$\frac{dV_{out}}{dt} = k_0 \bullet \left(\frac{dV}{dt}\right)_{\max}, \tag{1}$$

where k_0 is static operational amplifier gain. Time constant (τ) when feedback begins to be closed is:

$$\tau = \sqrt{\tau_{OA1}^2 + \tau_{dc}^2 + \tau_{OA2}^2}, \tag{2}$$

where τ_{0A1} and τ_{0A2} are time constants of OA1 and OA2, respectively, and τ_{dc} is the circuit diode-capacitor time constant. Feedback time constant may be estimated very roughly, because at the time of switching, amplifiers are in a nonlinear regime. From the obtained pictures one can assume that the feedback closing time is approximately 1–2 ns.

In the second variant of the schematic (Figure 3), we changed the output buffer amplifier to a classic combination of FET and BJT transistors, as voltage follower.

As a result of this change, circuit stability has increased, and leakage current from the capacitor has disappeared (Figure 4).

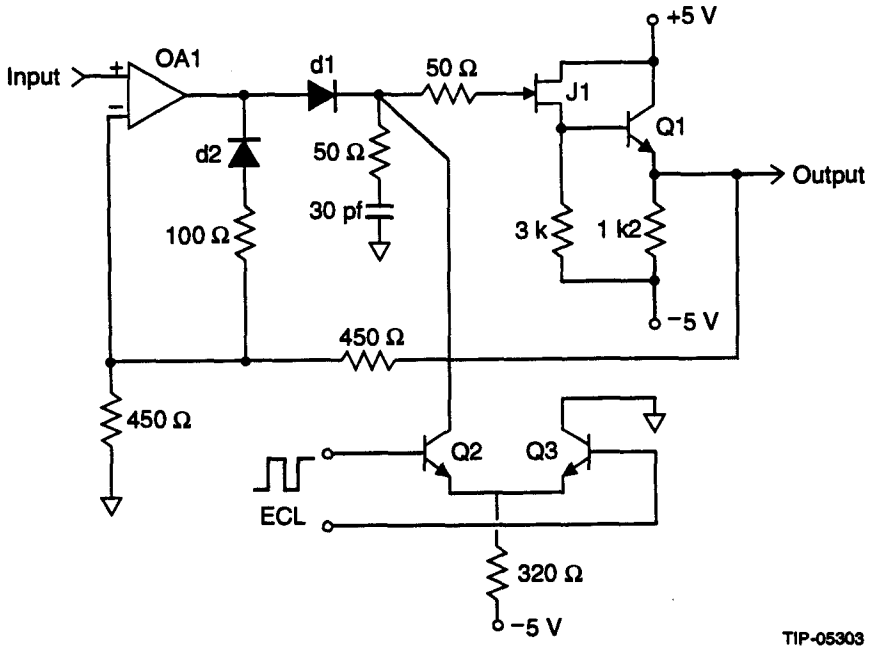


Figure 3. Peak detector schematic, second variant.

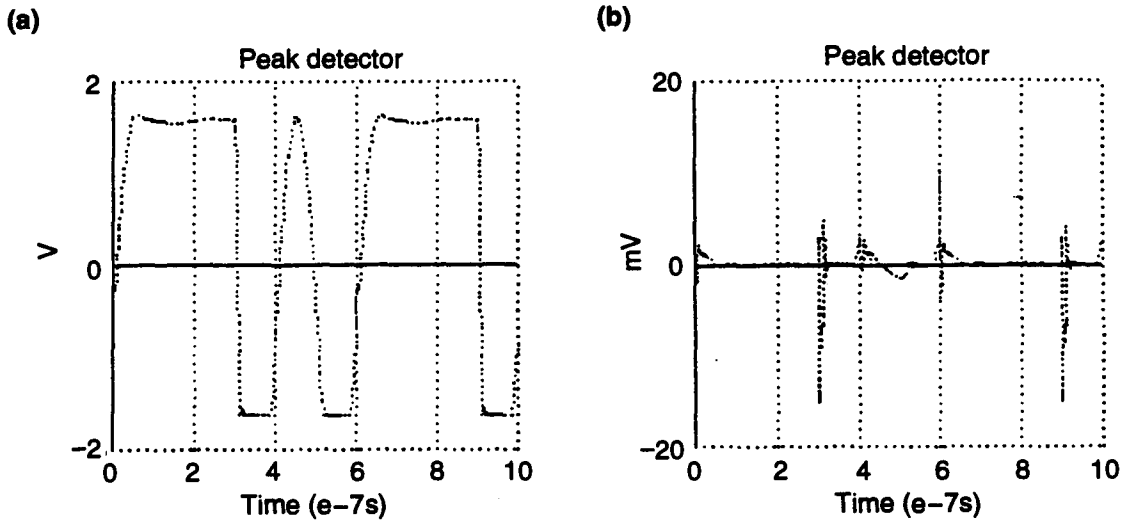


Figure 4. (a) Signal at the capacitance; (b) voltage on the resistance serially connected with the FET gate.

The transfer characteristic has oscillating character, as was noted above. Correction of the transfer characteristic can be done by selecting a resistor in the charge capacitance circuit (R ~ 50 Ω). Transfer characteristic without correction and with correction are shown in Figure 5(a) and 5(b), respectively.

Discharge circuit differs from first variant discharge circuit. Here it's as a switching current generator (20–50 mA). In the charge time, the current generator is switched off; in the discharge time, the generator is switched on and the diode d1 is open. In this case the voltage at capacitor follows input voltage. In the first variant, discharge took place with closed diode d1. Because of this at the beginning of charging, time feedback through d2 had to open, and had to close through d1. In the new variant of the circuit at the discharge time, diode d1 is open; at the beginning of the charge process feedback is already closed through d1.

This variant gave good results in the case with sinusoidal input signal, 10-MHz frequency (Figure 6). Output voltage $V_{out} = 2 \cdot V_{in_{max}}$, because the amplifier is closed by feedback with coefficient 2. The sinusoidal character of stored voltage may be explained by "creeping" through diode d1 capacitance.

In the next experiment we changed the input sinusoidal signal to a signal similar to that expected from stripline. Absence of reflections in the circuit was supposed. The signal has no Gaussian tails because we cannot simulate it with SPICE. Shape of the input signal is shown in Figure 7. Period of the pulse series is 120 ns. Result of period decrease is the increase of calculation time; that's not convenient for work.

Dynamic characteristics of CLC400 do not allow us to follow this kind of input signal. Shape of the output signal is shown in Figure 7(b) (at the 1.5-V input signal amplitude).

With the SPICE program one can obtain the circuit output characteristic by increasing input of the signal amplitude in each successive program run. Result of the ratio accuracy calculations is shown in Figure 8.

Unlinearity of the beginning part of the curve can be explained by different operations regimes of the elements: small-signal and large-signal regimes at the condition of the CLC400 speed shortage. Figure 9 illustrates deviation of the circuit output characteristic part (80–200 mV range) from approximating polynom. Polynom approximates output characteristic in 0.3–1.5 V range. Output voltages equal to values at some "neighboring" input voltages can be explained by loss of accuracy in the program calculations. Measured values are higher than those predicted by polynom. To my mind, this fact confirms our assumption about different operations regimes of the elements. In the small-signal regime, elements switch faster than in the large-signal regime; consequently, a bigger portion of the signal is followed in time.

One can consider obtained linearity results as approximate because of differences between simulated and real circuits, like parasitic components peculiar to the specific topology not taken into account during simulation, and the fact that all the elements are not ideals, *etc.*

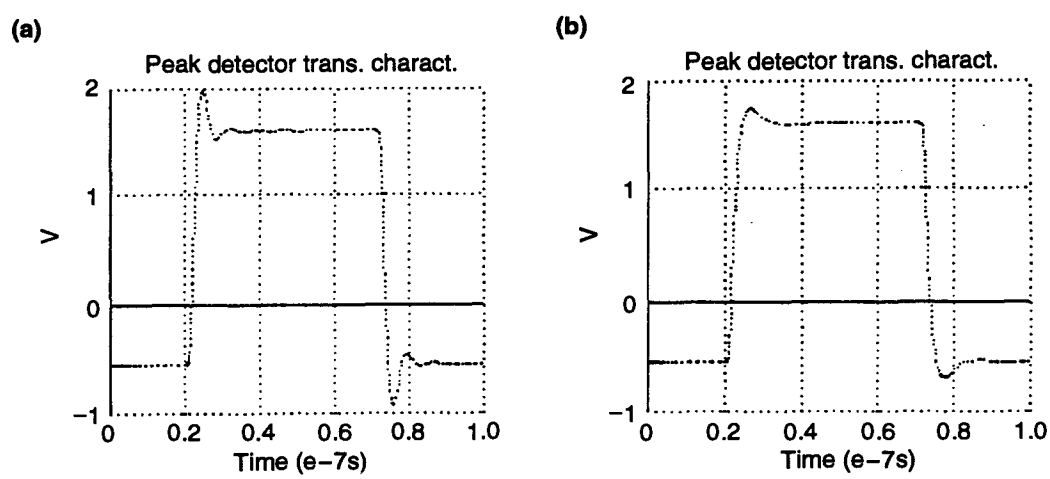


Figure 5. Transfer characteristic without correction (a), and with correction (b).

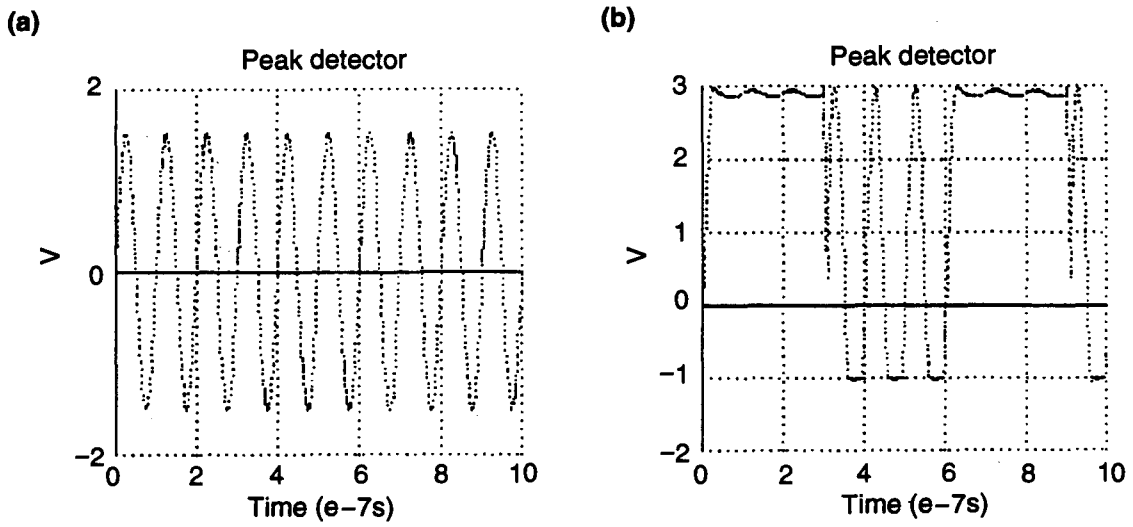


Figure 6. Input (a) and output (b) signals.

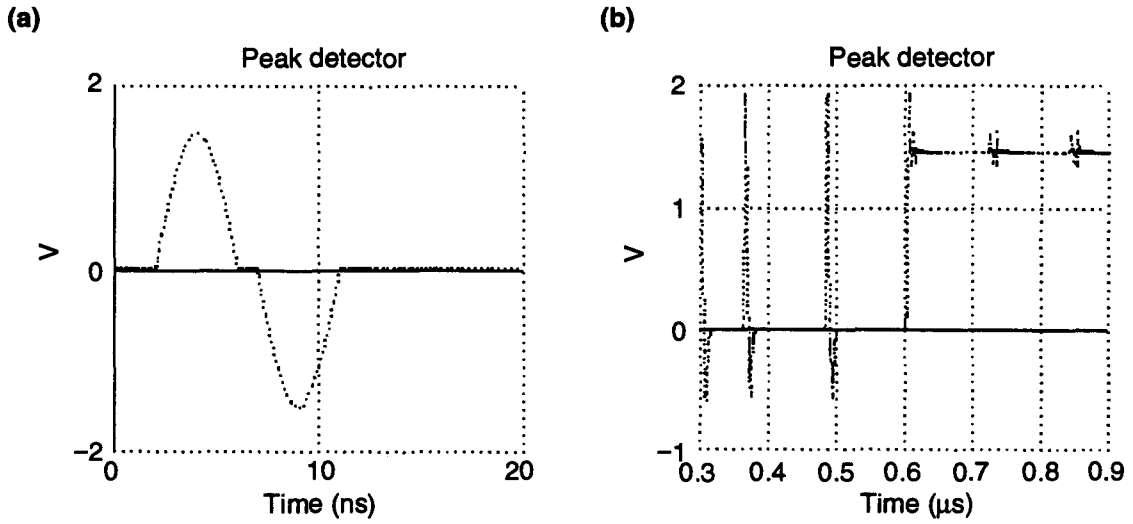


Figure 7. Input signal (a), output signal (b).

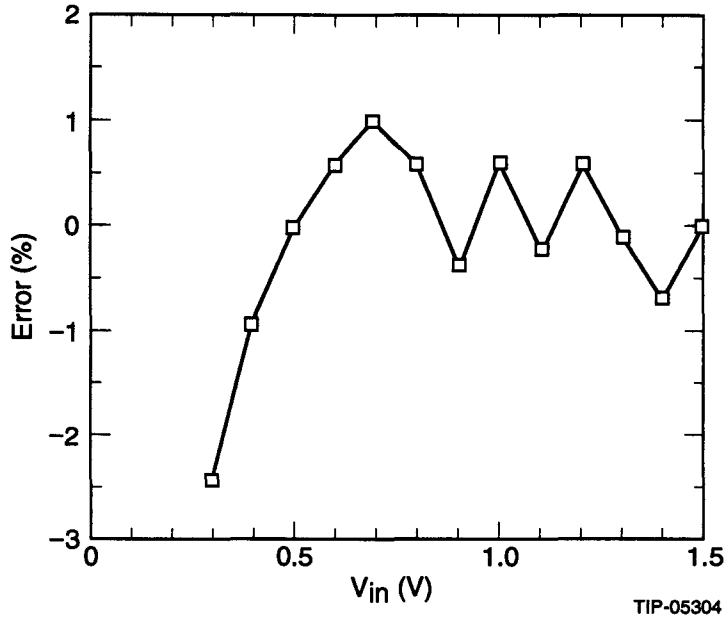


Figure 8. Ratio accuracy versus V_{in}.

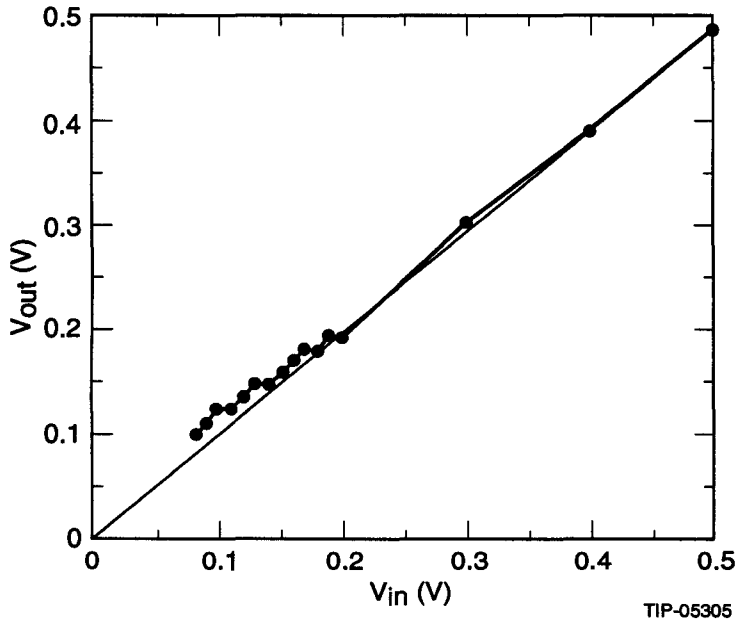


Figure 9. Deviation of the output voltage in the small-signal regime from approximating polynom.

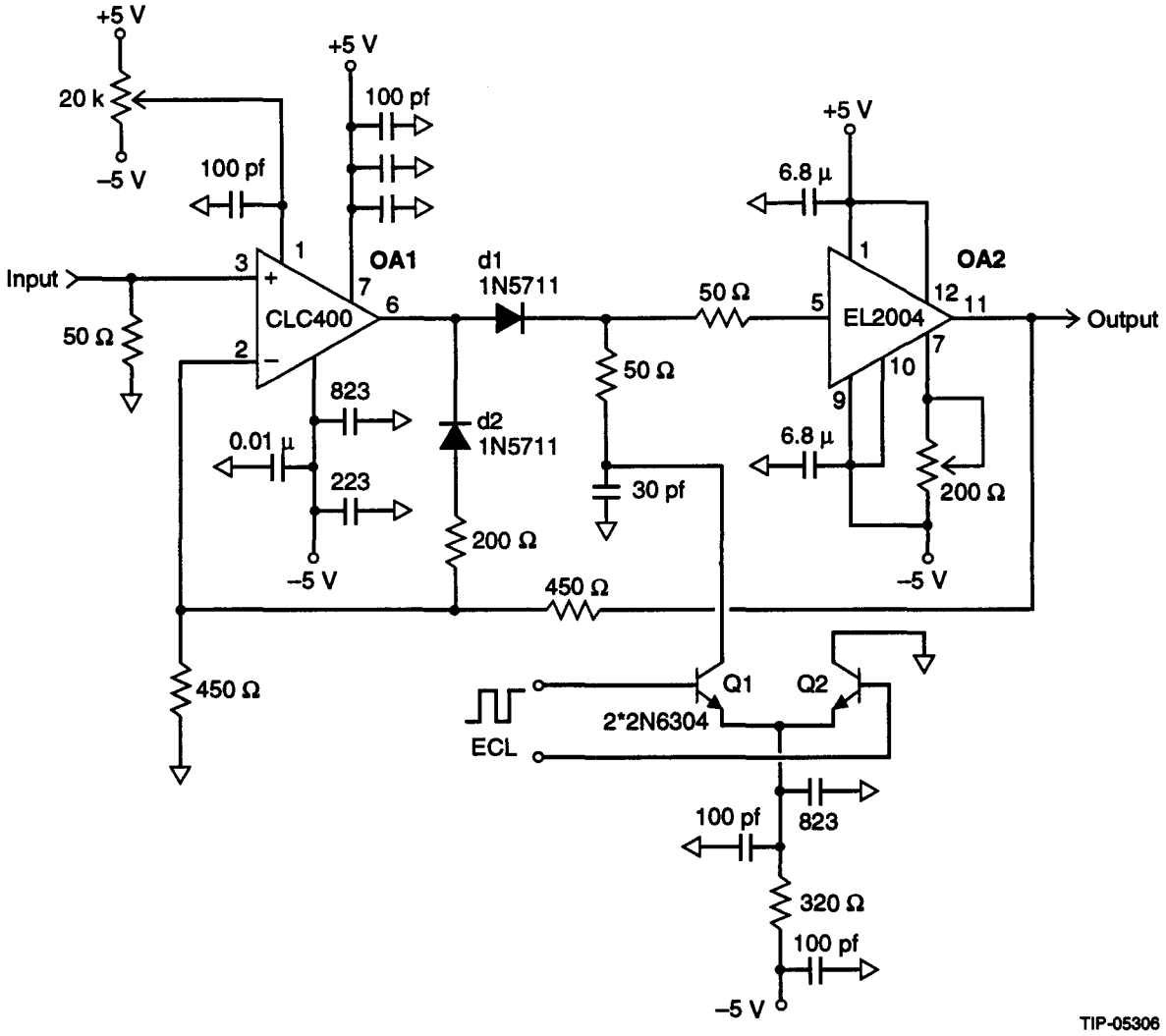

+5 V
20 k
–5 V
100 pf
+5 V
100 pf
Input
50 Ω
3
1
OA1
7
6
2
CLC400
823
0.01 µ
223
–5 V
d1
1N5711
d2
1N5711
200 Ω
50 Ω
30 pf
450 Ω
450 Ω
+5 V
6.8 µ
1
OA2
50 Ω
5
12
11
EL2004
7
10
9
6.8 µ
200 Ω
–5 V
Output
Q1
Q2
2*2N6304
ECL
100 pf
823
320 Ω
100 pf
–5 V
TIP-05306

Figure 10.

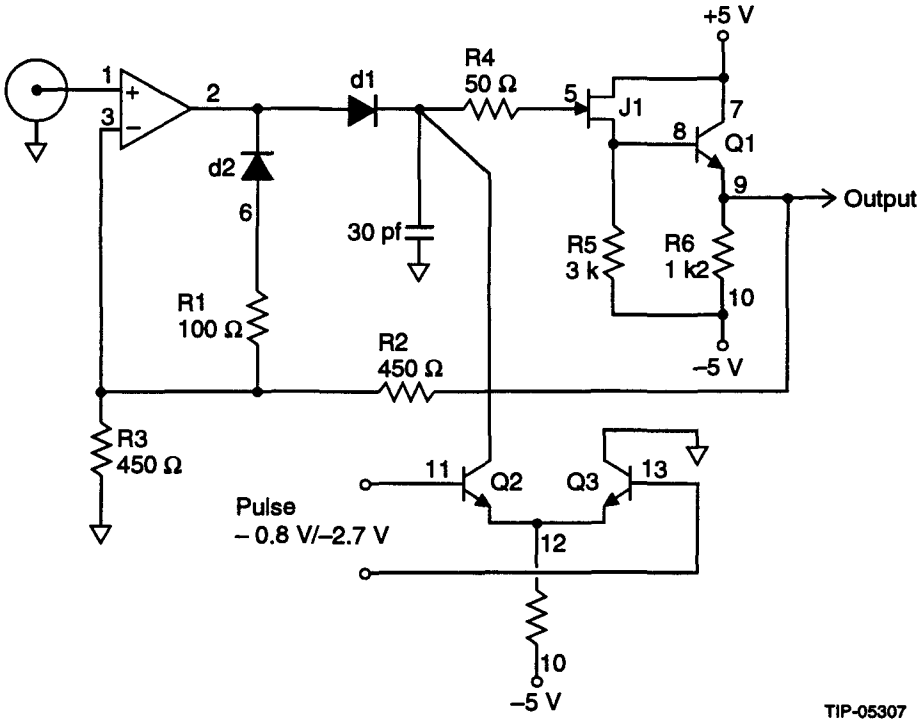

+5 V
R4
50 Ω
d1
1
2
3
5
J1
7
8
Q1
d2
9
Output
6
30 pf
R5
3 k
R6
1 k2
10
R1
100 Ω
R2
450 Ω
–5 V
R3
450 Ω
11
Q2
Q3
13
Pulse
– 0.8 V/–2.7 V
12
10
–5 V
TIP-05307

Figure 11.

```
peak detector
*
*        PDBUFF.SP
*
*v1    1    0    sin    (0 0.1 10meg)
*
x400   1    3    2      c400
*
d1    2    4  diode
d2    6    2  diode
*
c1   44    0     30pf
*
r1    3    6    100
r2    9    3    450
r3    3    0    450
r44   4   44     50
*
*        OUTPUT BUFFER
*
j1    7    5    8    jm
q1    7    8    9    tn
*
r4    4    5    50
b45 45     0    v=v (4) –v (5)
r5    8   10    3k
r6    9   10    1k2
*
v7    7    0    10v
v10 10     0    –5v
*
*        CURRENT SWITCH
*
q2    4   11   12    tn
q3    2   13   12    tn
*
r7       12       10     320
*
v11   11   0   pulse  –0.8  –2.7  0  1ns  1ns  300ns  600ns
v13   13   0   pulse  –2.7  –0.8  0  1ns  1ns  300ns  600ns
*
*        MODELS
*
.include c400 .macro
.model diode d cjo 1pf rs 10 tt 0.1ns
.model jm njf beta 1.0e–2 rd 100 rs 100 cgs  5pf  cgd  1pf
.model tn npn bf 200 rbm 100 re 1 rc 10 cje 1pf tf 0.1ns cjc 2pf
*
*        INPUT SIGNAL MODEL
*
v31     31     0     sin (0 0.1 125meg  2ns)
v32     32     0     pulse (0 1 2ns 1ps 1ps 4ns 120ns)
v33     33     0     sin (0 0.1 125meg  3ns)
v34     34     0     pulse (0 –1 7ns 1ps 1ps 4ns 120ns)
b311  311     0     v=v (31) *v (32)
b312   312     0     v=–v (33) *v (34)
*
*        INPUT  SIGNAL
*
*
b313 1 0 v=v (311) +v (312)
*
*        TRANSIENT  ANALYSIS
*
.tran 0.1ns 900ns 300ns
.end
peak detector trans. charact.
*
*        PDB . SP
*
v1   1   0   pulse ( 0  1  20ns  1ns  1ns  50ns  100ns)
*
x400   1   3   2   c400
*
rd   2   4   15
*
c1  44   0   30pf
*
r2     9     3   450
r3     3     0   450
r44    4    44    50
*
*        OUTPUT  BUFFER
*
j1   7   5   8   jm
q1   7   8   9   tn
*
r4     4     5   50
b45   45     0   v=v (4) –v (5)
r5     8    10   3k
r6     9    10   1k2
*
v7     7     0    10v
v10   10     0    –5v
*
*        MODELS
*
.include c400.macro
.model jm njf beta 1.0e–2 rd 100 rs 100 cgs 5pf cgd 1pf
.model tn npn bf 200 rbm 100  re 1 rc 10 cje 1pf tf 0.1ns cjc 2pf
*
*        TRANSIENT ANALYSIS
*
.tran  0.1ns   100ns  0ns
.end
```

TIP-05401

Figure 12.

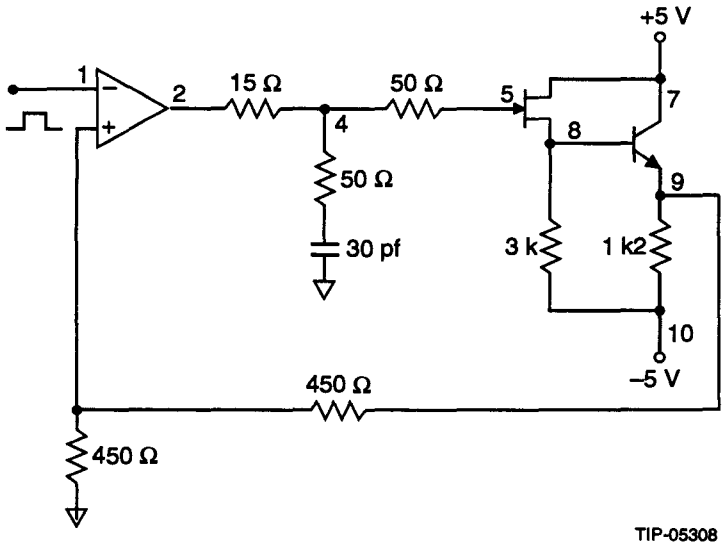


Figure 13.

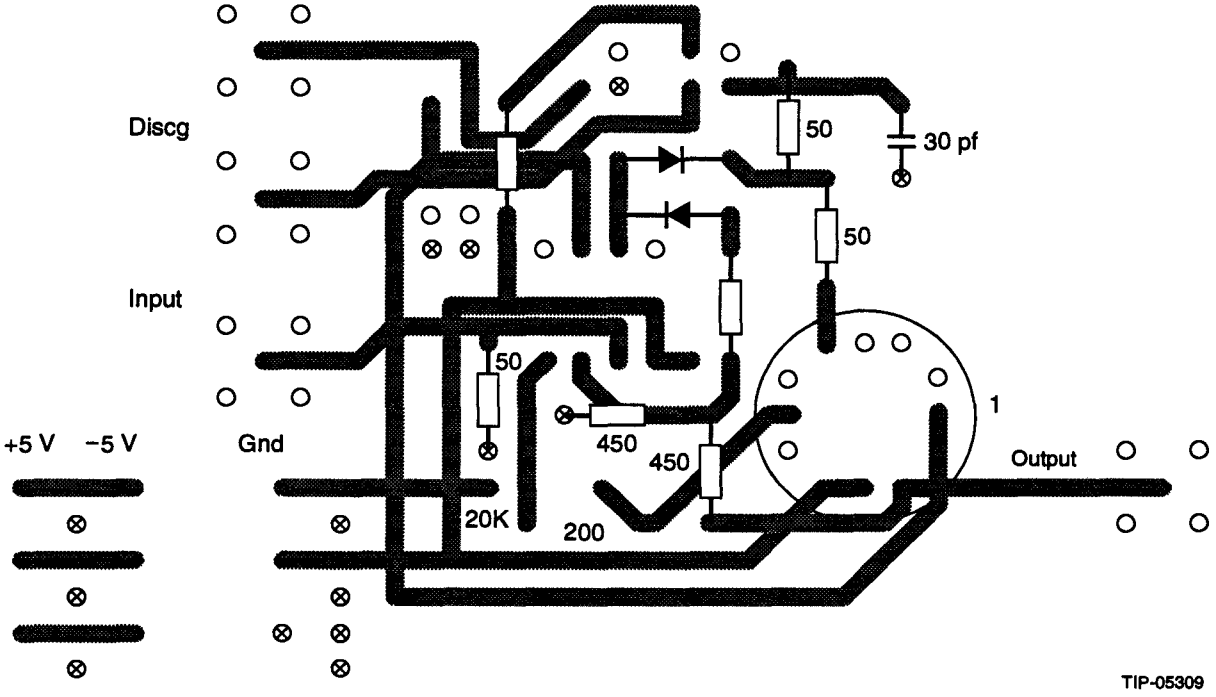


Figure 14.

2.0 TRACING BEAM POSITION MONITOR

2.1 Tuning and Testing of the Tracing Peakup

Tuning consists of two actions:

1. Compensation of the amplifier output offset voltage, and the voltage on the open diode d1 in the circuit, tracing of the signal.
2. Choice of the required dividing coefficient of the buffer amplifier output voltage.

If we ground the circuit input, the diode d1 will be open, and the input voltage of the buffer amplifier will make –Vd1. We can compensate this voltage by using zero offset of the buffer amplifier. With the help of tuning the variable output resistor, we can obtain the required dividing coefficient.

For this purpose, say, a sinusoidal signal should be applied to the circuit input. The amplitude of the signal should be such that all the circuit elements may be operated in the linear regime. In the process of tuning sinusoidal signal, 1-MHz frequency and 1-V amplitude were applied to the circuit input. The dividing coefficient was equal to two.

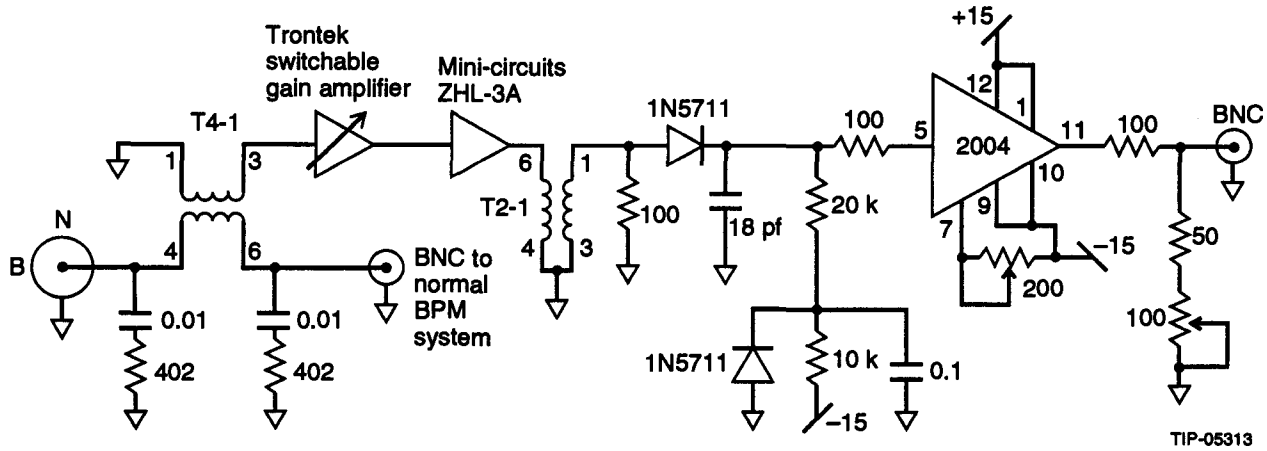
To be successful, tuning should be kept under control at two points in the circuit: the output of the buffer amplifier and the circuit output.

All the measurements were carried out on the Tektronix scope, model 2465BCT. The signal parameters were measured with the help of cursors and were repeated with the program of automatic voltage measurement. Unfortunately, this program has a limited field of application, since it is not currently possible to measure high-frequency signals. The error in the measurement of the 1-MHz frequency signal is 5%.[2] The measurement error in case of the cursors is 2%.[2] All the signals were measured on the first channel of the scope, because scope channels have different ground offsets. The ground offset of the first channel is –0.9 mV. Due to relatively low accuracy of the measurements, the tuning and tests results were considered as preliminary.

With the help of the Fluke 45 voltmeter, we measured the circuit output characteristic V_{out} versus coefficient of the attenuation of the attenuators. Voltmeter measurement accuracy is 0.025% + 2 (percentage of reading + digits).[3]

The temperature drift of the circuit was observed during the measurements. It displays as a shift of the output characteristic of the circuit in the process of the elements heating. Also noted was slow drift of the output signal amplitude of the pulse generator. (The amplitude slowly decreased on the 60 mV during the hour that the device worked.) Unfortunately, this effect can be observed only indirectly, kept under control at some point in the circuit simultaneously. As our task does not include research of the circuit temperature drift, the estimated observation was made. The temperature drift of the circuit does not distort its linearity. In my view only identity of the drift of the peakup different channels is of interest.

The unlinearity of the circuit output characteristic influences the unlinearity of the detecting diode and of the buffer amplifier gain. At the big amplifier input signal (larger than 4 V), the gain of the buffer amplifier increases. It can negatively influence the linearity of the peakup detector circuit.



In the experiments, input of the circuit is the sixth pin of the T2-1 rf transformer.

Figure 15.

2.2 Calibration of the Attenuators

A schematic of the attenuator calibration is shown in Figure 16. The input sinusoidal signal of frequency 60 MHz applies to the power splitter. The signal from one output of the power splitter applies to the two consistently included attenuators. The first attenuator has 11 dB dynamic range and 1 dB step; the second has 110 dB dynamic range and 11 dB step. The amplitude of the sinusoidal signal, applied to the input of the attenuators, is 665 mV. The signal from the second output of the power splitter and the output of the second attenuator applies to the vector voltmeter (HP8508A), the inputs A and B, respectively.

With the help of the vector voltmeter, the next parameters were kept under control: the amplitudes of the input and output signals of the attenuators, V_{out}/V_{in}; V_{out}/V_{in}, dB. The more important dependence for the testing of the peak detector is $V_{out}V_{in}$, dB versus the coefficient of the attenuation.

Ratio accuracy of the vector voltmeter has difficult dependence from the amplitude and ratio levels of the input signals.[4] In the range less than 320 mV, ratio accuracy is 0.3 dB (3.4%); in the range 320 mV and more, the ratio accuracy is 0.6 dB (6.7%). Accuracy of the power splitter (difference between channels) is less than the level of sensitivity of the vector voltmeter. The difference of the fades in the connective cables is less than 0.07 dB. (The input amplitude of the testing signal is 50 mV; absolute accuracy is 0.1 dB.)

A device with the accuracy 0.1 dB is needed to measure the linearity of the attenuators with the 1% accuracy.

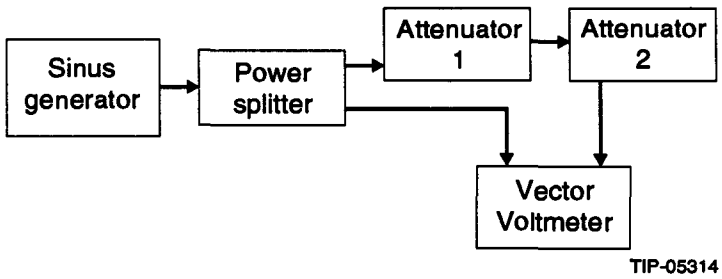


Figure 16. Schematic of the attenuators calibration.

2.3 Possible Dynamic Range of the Tracing Peak Detector Circuit

In the research part of the circuit there are two elements that can limit dynamic range: the detecting diode and the output buffer amplifier.

Diode (lN5711) possibilities cover desirable dynamic range (V_{inmax} = 30 V; V_{RRM} = 70 V; $V_{(BR)}$ = 70 V; IF = 15 mA). In the Data books[4,5] there is no maximum pulse forward current. Usually, pulse forward current is 10–20 times higher than the forward continuous current. In the case of 30-V input voltage, the diode will charge the capacitor with the maximum diode current.

The buffer amplifier is EL2004.[6] Amplifier supply voltage is ± 15 V in this variant of the schematic. In this case maximum amplifier output voltage is ± 14 V. But absolute maximum rating of the supply voltage is ± 40 V. At this supply, the voltage amplifier can work with ± 30-V input voltage. This variant requires a separate voltage source for the buffer amplifier. There are no descriptions of the specifications of the buffer amplifier at high supply voltage. That is why linearity of the circuit can be checked in the measurement process only.

2.4 Measurement of Peak Detector Linearity at 7–13-V Input Voltage Range

Peak forward characteristics are shown in Figure 17. At 11-V input, voltage characteristics begin to bend due to the quick increase of output buffer amplifier gain.

Figure 18 illustrates ratio accuracy per channels. In the ratio accuracy calculation process, approximation of output characteristic in the 7–11-V range was made.

For additional information see Section 2.1.

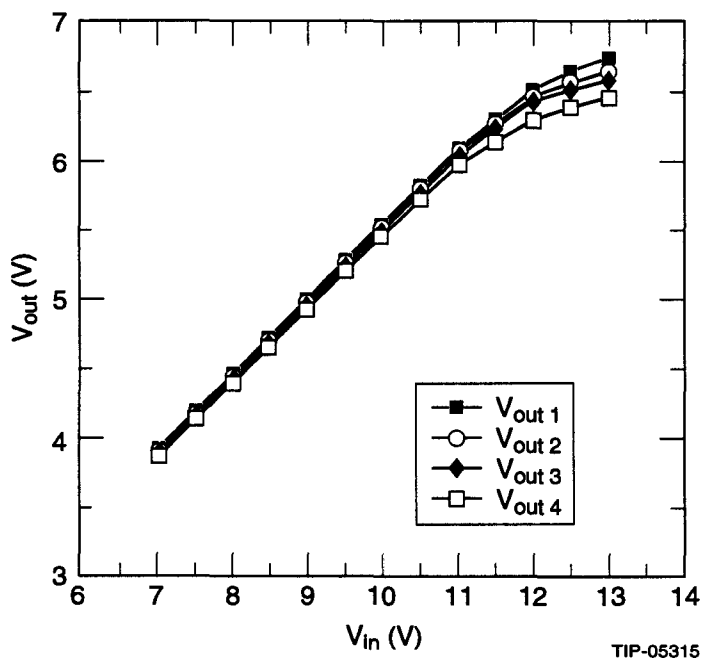


Figure 17. Peakup forward characteristics at 7–13 V voltage range (1–4 channels).

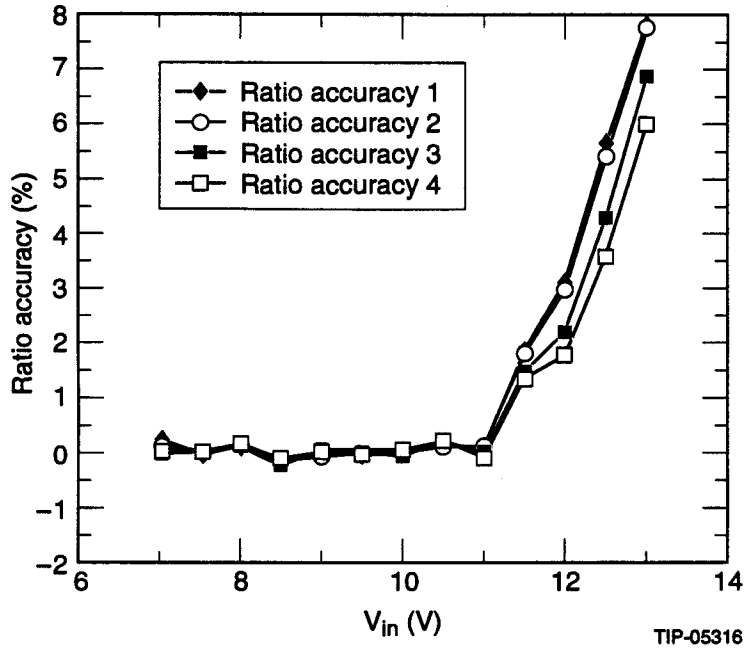


Figure 18. Ratio accuracy (1–4 channels).

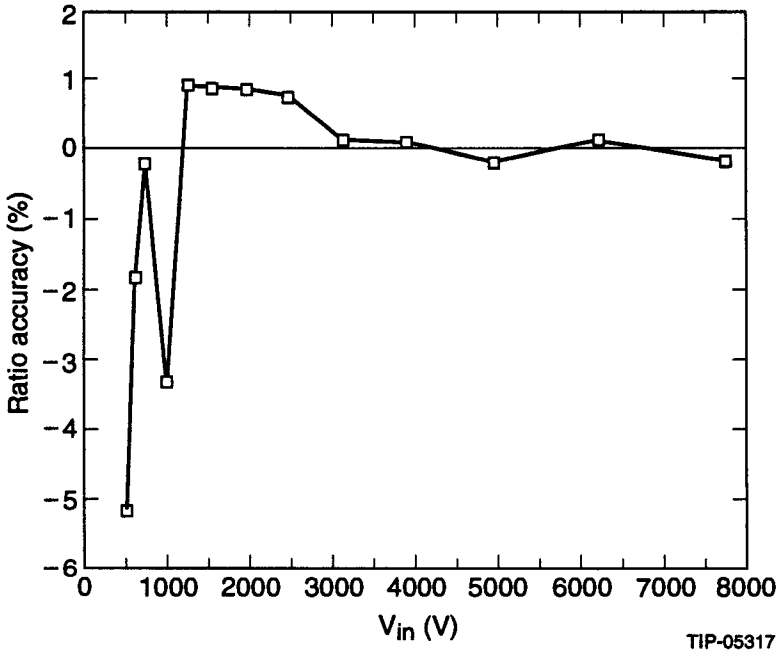


Figure 19. Ratio accuracy, Channel 1 (499 mV–8V).

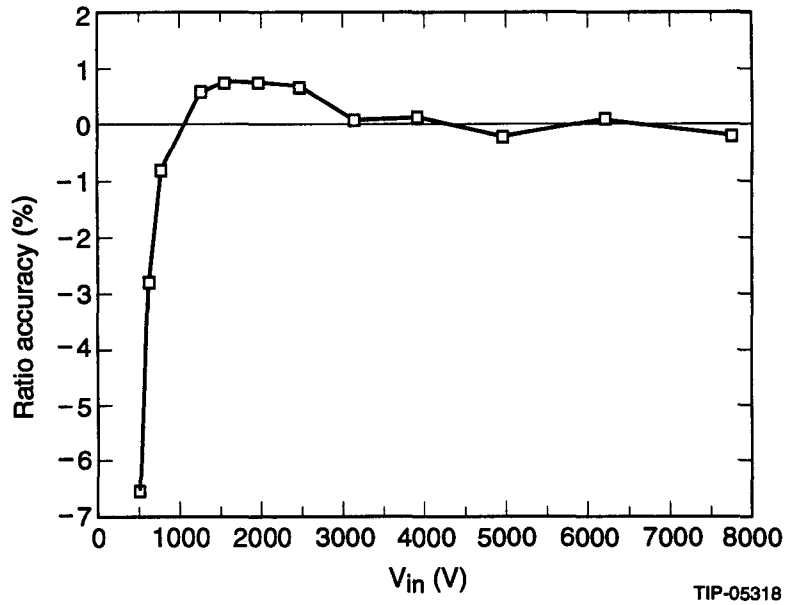


Figure 20. Ratio accuracy, Channel 1 (499 mV–8V) without "burst" at 1-V input voltage.

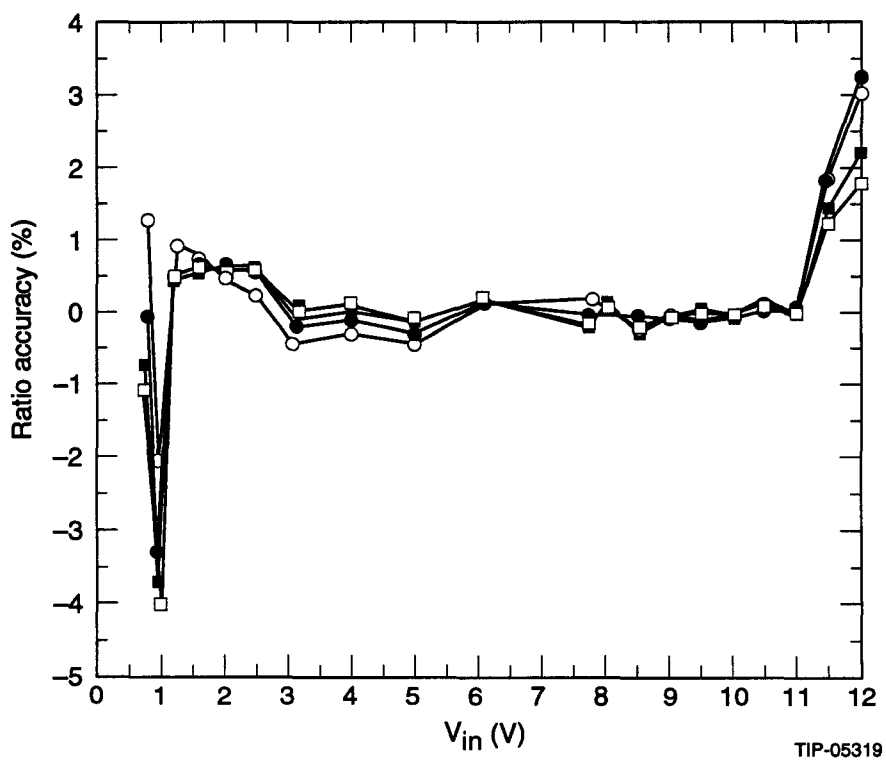


Figure 21. Ratio accuracy, Channels 1–4, at 0.7–12-V input voltage.

3.0 SWITCHING BEAM POSITION MONITOR

3.1 Beam Parameters

The average beam current is:

$$\langle I_b \rangle = Nef, \tag{3}$$

where N is the number of particles per bunch, $N = 8.1 \times 10^9$; f is the beam spacing frequency, $f = 60$ MHz (both parameters are for Collider); e is the charge of the electron, $e = 1.6 \times 10^{-19}$ C. So, the Collider beam current is:

$$\langle I_b \rangle = 8.1 \times 10^9 \times 1.6 \times 10^{-19} \times 60 \times 10^6 = 10^{-3} \approx 80\,\text{mA}. \tag{4}$$

The maximum beam current is:

$$I_{b_{\max}} = \langle I_b \rangle \frac{T}{2\sigma}, \tag{5}$$

where $T = 16.6$ ns is the beam spacing period, $T = 1/f$; $2\sigma \leq 0.7$ ns is the beam size (see Figure 22). Beam size 0.7 ns is taken for the worst case.

So, the maximum beam current is:

$$I_{b_{\max}} = 77.9 \times 10^{-3} \times \frac{16.6 \times 10^{-9}}{0.7 \times 10^{-9}} - 1.85\,\text{A}. \tag{6}$$

The current from the strip line electrode depends on the strip line azimuthal angle ($\Delta\phi$). We can consider that for a beam on the center of the vacuum chamber,

$$\Delta\phi \approx \frac{2\pi}{8}. \tag{7}$$

In this case, the strip line current will be one-eighth of the total beam current. We also should take into account that the induced beam current propagates through the strip line in both directions. So, the strip line output current is twice as low as the total image current azimuthal part.

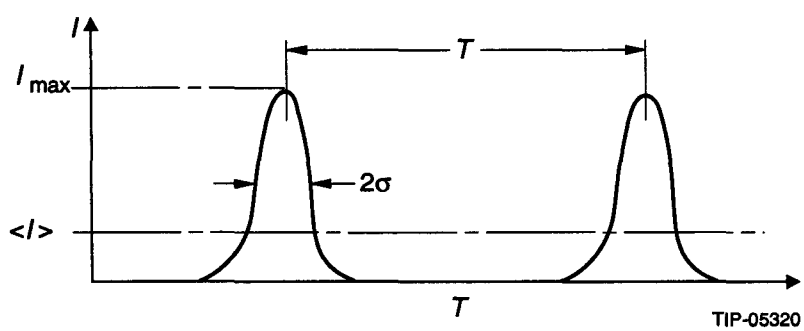
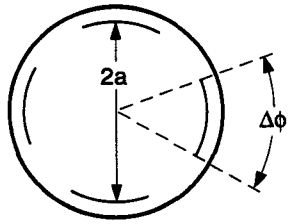


Figure 22. Beam current (I) over time (T); I_{max} is the beam current; <I> is the average beam current; T is the beam spacing period; 2σ is the beam size.



TIP-05311

Figure 23. Beam tube and BPM electrodes. $\Delta\phi$ is the strip line electrodes azimuthal angle; 2a is the aperture.

$$I_{stl_{\max}} = \frac{1}{2}\frac{I_{b_{\max}}}{8}. \tag{8}$$

$$I_{stl_{\max}} = \frac{1}{2}\frac{1.85}{8} = 0.156 \text{ A}. \tag{9}$$

So, maximum voltage from the strip line is:

$$V_{stl_{\max}} = I_{stl_{\max}}\rho = 115.6\times10^{-3}\times50 = 5.78\text{V}, \tag{10}$$

where $\rho = 50\Omega$ is the characteristic impedance of the strip line.

3.2 Sensitivity of the BPM

Sensitivity of the BPM is the differential value. Actually, this is the slope of the voltage-to-beam-position-coordinate characteristic of the BPM electrodes. The dependence of the electrodes voltage ($V_1(x)$ and $V_2(x)$ on the beam position coordinate (x) electrodes 1 and 2 (V-X characteristic) is shown in Figure 24. The curve $V_1(x)$ asymptotically tends to infinity at $x \rightarrow a$ and tends to zero at $x \rightarrow -\infty$; the curves have a linear behavior approximately in the range $\pm(a/2)$, where a is half of the aperture. The dependence $V_2(x)$ is symmetic to the $V_1(x)$ at about $x = 0$.

We can describe the behavior of the $V_1(x)$ and $V_2(x)$ characteristics with the Taylor series using:

$$\begin{cases} V_{1(x)} = V_0 + sx + px^2 + qx^3 + \ldots \\ V_{2(x)} = V_0 - sx + px^2 - qx^3 + \ldots, \end{cases} \tag{11}$$

where s, p, q are the Taylor's series coefficients; also s is the slope of the V-X characteristic,

$$s = \frac{d}{dx}V(x). \tag{12}$$

The difference of $V_1(x)$ and $V_2(x)$ is:

$$V_1(x) - V_2(x) = 2sx + 2qx^3 + \ldots. \tag{13}$$

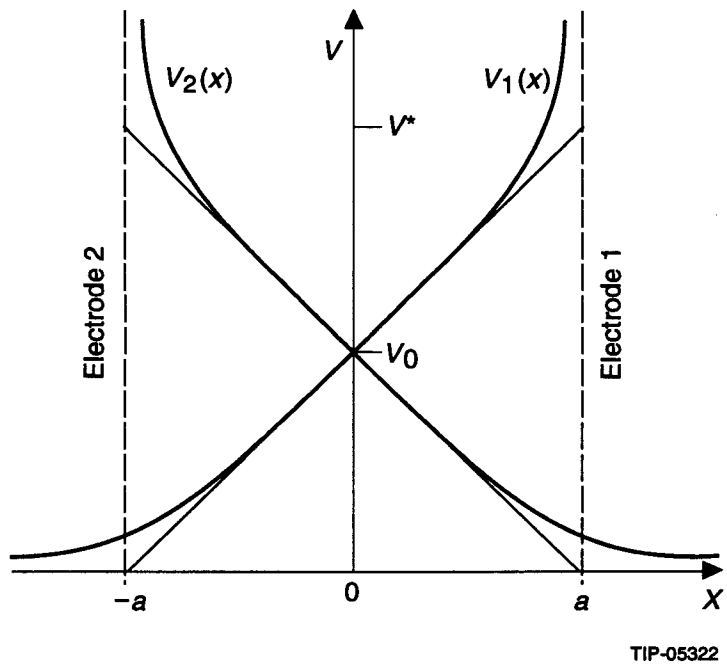


Figure 24. The BPM electrodes voltage dependence on the beam position *x*-coordinate. V_0 is the voltage corresponding to the central beam position (x = 0); *a* is the half aperture.

All the even terms are subtracted, and all the odd terms are added together. The interval of the linearity of the electrodes voltage difference (Eq. (13)) is higher than in Eq. (11) for each electrode.

For the small deviations of the beam from the center ($x << a$) we can neglect the higher terms in Eq. (11) (and Eq. (13), of course). The equation will be:

$$\begin{cases} V_1(x)=V_0+sx \\ V_2(x)=V_0-sx\,. \end{cases} \tag{14}$$

From the boundary conditions for the linear *V*-*X* characteristic approximation (see Figure 24):

$$\begin{cases} x=0 \Rightarrow V_1(0)=V_0 \\ x=a \Rightarrow V_1(-a)=0. \end{cases} \tag{15}$$

We can get the slope *s*:

$$s=\frac{V_0}{a}\,. \tag{16}$$

It can be got:

$$V_i(x)=V_0\left(1\pm\frac{x}{a}\right). \tag{17}$$

Actually $V_0 = V_{stl\,max}$. According to Eq. (10) we can get:

$$V_i(x) = I\rho\left(1+\frac{x}{a}\right). \tag{18}$$

That is,

$$s = \frac{I\rho}{a}, \tag{19}$$

where $I = I_{stl\,max}$.

So, we can note that the slope of the *V-X* characteristic of the electrodes (the BPM sensitivity) also depends on a beam current and on the aperture, and on the electrode strip line impedance.

Note, that all these reasonings are true if the *Z*-coordinate beam displacement is equal to zero. If not, the *Z*-dependent term that appears in the equation for the $V_i\,(x)$ becames $V_i\,(x\ z.)$

I suppose that really the *V-X* electrode characteristic is never rigorously linear. We can consider that in some *X*-interval the *V-X* characteristic just tends to the linear with some accuracy. This fact means that the slope of the *V-X* characteristic is different at the different *X*-interval. So, sensitivity of the BPM electrodes depends on the *X* coordinate.

Besides, I suppose that the *V-X* characteristic of each electrode is individual. I believe that it is necessary to know this characteristic in each particular case and to know the accuracy of the approximation of the electrodes characteristic to the linear characteristic. It seems to me also that it is necessary to have an average characteristic of the electrodes, and a spread of their parameters (as a sensitivity, correspondence of the electrical and geometrical centers of the system, and so on).

3.3 Requirements to the Isolation

Assume that we operate with the circuit shown in Figure 25.

Let there be no losses on a switch. Figure 26 shows the equivalent circuit.

In Figure 26, ρ is the impedance of the lines and load impedance, so switch-to-voltage source and switch-to-load lines are matched; Z_{is} is the transimpedance of the open switch, and $Z_{is} >> \rho$.

Let's suppose that all bunches in the Collider have an equal number of particles, and there are no empty separatrixes. So, there is a constant azimuthal current distribution through the Collider ring.

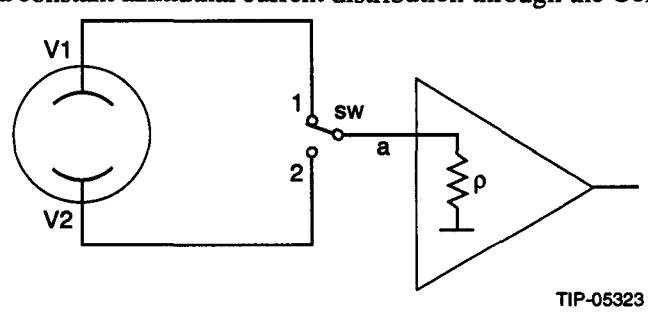


Figure 25. The operation circuit. V1 and V2 are the electrodes voltage; "sw" is a switch; "a" is the load point; ρ is the lines impedance and a load impedance.

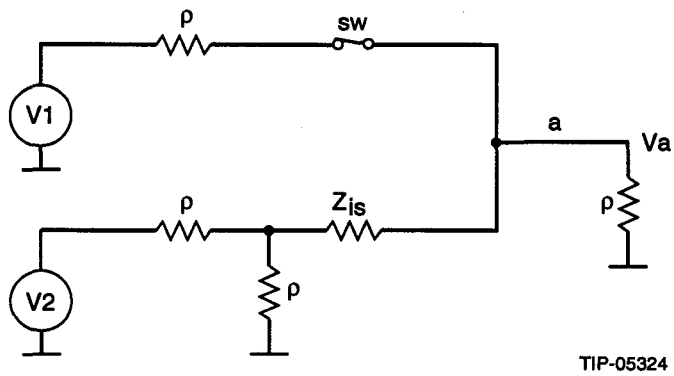


Figure 26. The equivalent circuit. Z_{is} is the transimpedance of the open switch.

The system operates with a signal of 60-MHz frequency. Bandwidth of the system is determined by the BPM electronic bandwidth (approximately, and not more than, 5 MHz). So, we can consider that the circuit (Figure 26) operates with the sinusoidal signals. It means that the complex representation of the circuit transfer function for the estimation of the processes in a circuit can be used:

$$\begin{cases} \overline{V}_{a1} = \overline{V}_1 \dfrac{\rho}{2\rho} = \dfrac{\overline{V}_1}{2} \\ \overline{V}_{a2} = \dfrac{\overline{V}_2}{2} \dfrac{1}{Z_{is}} \dfrac{\rho}{2} = \dfrac{\overline{V}_2}{2} \overline{k}_{is}, \\ \overline{V}_a = \overline{V}_{a1} + \overline{V}_{a2} \end{cases} \tag{20}$$

where $\overline{Z}_{is}$ is the transimpedance complex value of the open switch, and $\overline{k}_{is}$ is the complex value of the isolation coefficient between the channels:

$\overline{k}_{is} = \overline{k}_{12}$ is the isolation coefficient from the channel 1 to 2;

$\overline{k}_{is} = \overline{k}_{21}$ is the isolation coefficient from the channel 2 to 1.

As we can see, the influence of one to another channel appears as a small additional signal to the channel we are looking for. So we need to determine the allowed value of the "beam displacement error" due to the non-ideal isolation. According to Eq. (17) we can express the valid signal (for example, for channel 1) and the additional signal from the other channel (channel 2) in the following way:

$$\overline{V}_1 = \overline{V}_0\left(1+\frac{x}{a}\right) + \overline{V}_0 \overline{k}_{21}\left(1-\frac{x}{a}\right). \tag{21}$$

If $x << a$, we can neglect the term $\bar{k}_{21}\frac{x}{a}$, and get:

$$\bar{V}_1 = \bar{V}_0\left(1 + \frac{x}{a} + \bar{k}_{21}\right). \tag{22}$$

In the same way, for the full signal in channel 2 we get:

$$\bar{V}_2 = \bar{V}_0\left(1 - \frac{x}{a} + \bar{k}_{12}\right). \tag{23}$$

The difference of the full signals of channel 1 and channel 2 is:

$$\bar{V}_1 - \bar{V}_2 = \bar{V}_0\left(2\frac{x}{a} + \bar{k}_{21} - \bar{k}_{12}\right), \tag{24}$$

or

$$\bar{V}_1 - \bar{V}_2 = \bar{V}_0\left(2\frac{x}{a} + \bar{k}_{eff}\right), \tag{25}$$

where $\bar{k}_{eff} = \bar{k}_{21} - \bar{k}_{12}$. I suppose that $\bar{k}_{eff} \neq 0$, because the isolation coefficients are not equal in the real circuit. Put $\bar{k}_{eff} = \bar{k}_{21} = \bar{k}_{is}$. I suppose that this approximation is close to true, but we can check this fact only during a measurement.

So we have a real additional "beam displacement error" signal (x_{err})—the undesirable error of the beam position measurements. This error have been specified as 0.1 mm.

We can suppose that the isolation coefficient $\bar{k}_{is}$ has a Real and an Imaginary part because the impedance of the open switch has a Real and an Imaginary part:

$$\begin{cases} \bar{Z}_{is} = \mathrm{Re}(Z) + j\mathrm{Im}(Z) = R + jx \\ \bar{k}_{is} = \mathrm{Re}(k) + j\mathrm{Im}(k) = k_{isR} + jk_{isI}. \end{cases} \tag{26}$$

We can consider two cases:

1. $$\bar{Z}_{is} = \mathrm{Re}(Z) = R \Rightarrow \bar{k}_{is} = \mathrm{Re}(k) = k_{isR}$$

2. $$\bar{Z}_{is} = j\mathrm{Im}(Z) = -j\frac{1}{\omega C_{is}} \Rightarrow \bar{k}_{is} = j\mathrm{Im}(k) = jk_{isI},$$

where C_{is} is the transcapacitance of the open switch and $\omega = 2\pi f$.

Let's consider a first case: the isolation coefficient consists of the Real term only. According to Eqs. (22) and (23), we have:

$$k_{isR} = \frac{x_{err}}{a}. \tag{27}$$

From the specifications:

$$\begin{cases} x_{err} = 0.1\,\text{mm} \\ a = 20\,\text{mm}. \end{cases} \tag{28}$$

So we can get $k_{isR} = \frac{0.1}{20} = \frac{1}{200}$, or $k_{isR} = -46$ dB;

that is, isolation of the switch should not be worse than –46 dB.

In the second case, the isolation coefficient consists of the Imaginary term only. Apply the jk_{isI} value to Eq. (22):

$$\overline{V}_1 = \overline{V}_0\left(1 + \frac{x}{a} + jk_{isI}\right). \tag{29}$$

Our system is not sensitive to the phase of the signal. In this case we can operate with the module of the $\overline{V}_1$:

$$|\overline{V}_1| = |\overline{V}_0| \times \sqrt{\left(1 + \frac{x}{a}\right)^2 + k^2{}_{isI}}, \tag{30}$$

or

$$|\overline{V}_1| \cong |\overline{V}_0|\left(1 + \frac{x}{a} + \frac{1}{2}k^2{}_{isI}\right). \tag{31}$$

We get:

$$\frac{1}{2}k_{isI}^2 = \frac{x_{err}}{a}. \tag{32}$$

So, $k_{isI} = \sqrt{2\frac{0.1}{20}} = \frac{1}{10}$, or

$$k_{isI} = -20 \text{ dB}. \tag{33}$$

This value–20 dB is a softer requirement for the isolation (in the same way as the isolation calculation for channel 2.)

Thus we can see that the isolation requirements for the two components of the isolation coefficient (Real and Imaginary) are very different. In this case, we need to measure such parameters as isolation of one channel to another one and phase characteristics of the switches. We can answer what really happens after switch parameters have been measured.

3.4 Beam Current Change

Let us suppose that the beam current changes from a low value (I_L to a high value (I_H); one channel is delayed relative to another one (by use of the delay line). Let's also assume that the beam is still in the center, *i.e.*, $x = 0$. This case is shown in Figure 27.

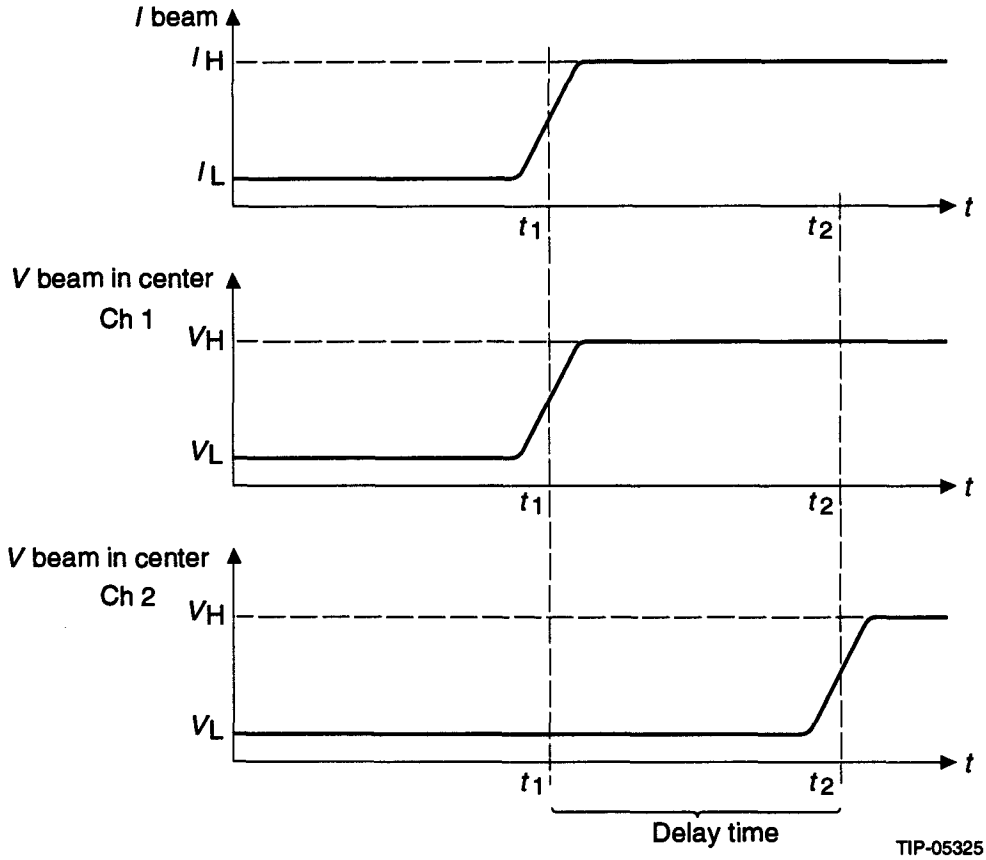


Figure 27. Beam current change.

For ch2 at the delay time:

$$V_{ch2}\Big/_{t_1}^{t_2} = V_L + k_{12}V_H = \rho I_L + k_{12}\rho I_H = \rho I_2\left(1 + k_{12}\frac{I_H}{I_L}\right), \Rightarrow k_{12}\frac{I_H}{I_L} \le \frac{x_{error}}{d}.$$

What is the maximum ratio $\frac{I_H}{I_L}$?

3.5 Single Switch Parameters

Table 1 is a list of single switch parameters.

Table 1. Single switch parameters.

Loss		Control Inputs Impedance	
k_{L21}	−0.5 dB	R_{V_1}	49.0 Ω
k_{L31}	−0.5 dB	R_{V_2}	48.9 Ω
φ_{L21}	−1.3°	C_{V_1}	1.1 pF
φ_{L31}	−1.5°	C_{V_2}	0.9 pF
R_L	3Ω		
Isolation			
$\lvert\bar{k}_{is21}\rvert$	−40 dB		
$\lvert\bar{k}_{is31}\rvert$	−44 dB		
φ_{is21}	95°		
φ_{is31}	100°		
$\lvert\bar{Z}_{is21}\rvert$	2.5 kΩ		
$\lvert\bar{Z}_{is31}\rvert$	4 kΩ		
R_{21}	30 kΩ		
R_{31}	23 kΩ		
C_{21}	1.0 pF		
C_{31}	0.7 pF		
k_{isRe21}	−62 dB		
k_{isRe31}	−60 dB		
k_{isIm21}	−41 dB		
k_{isIm31}	−44 dB		

All these figures are rounded. Accurate values are found in the measurement data sheets. All parameters were measured at 60-MHz frequency; 50Ω impedance at all rf ports; 0V and −5V control voltages. The measurements were done with the help of the HP8753C Network Analyzer. Conclusion: this switch satisfies the requirements stated in Section 3.1.

Figures 28 (a) and (b) show switch SM-IS-2103.

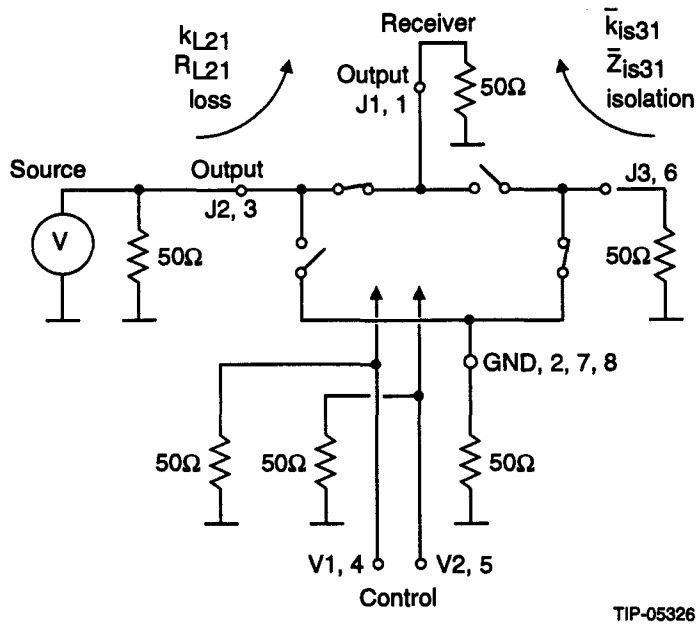


Figure 28. (a) Switch SM-IS-2103 (ST Olectron Corp.), circuit of the measurements.

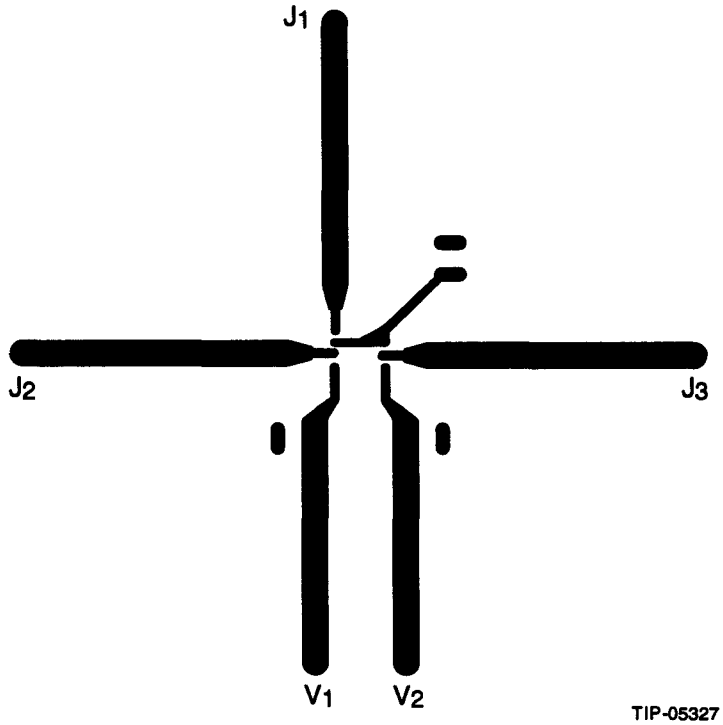


Figure 28. (b).

3.6 Switch and Filter Measurements

The filter's output oscillations dumping process is relatively slow, as seen in Table 2 and Figures 29–35. The figures show the oscillations dumping bunches "step by step," at the convenient scale for each bunch. The amplitude of the undesirable oscillations stays relatively high during the chosen time interval. That is not satisfactory to our goal.

I believe that we need (1) to choose a filter with a wider banwidth, and (2) to change the delay time between two control signals.

Table 2. Amplitude and delay of each oscillation bunch.

t delay (ns)	A pk–pk (mV)	A pk–pk (dBm)	A pk–pk/2 (dBm)	A pk–pk/2 (mV)
0[a]	2400	20.6	14.6	1200
220	350	3.9	–2.1	175
340	120	–5.4	–11.4	60
480	72	–9.8	–15.9	36

[a] This is a desired signal, and a reference point for a measurement time interval.

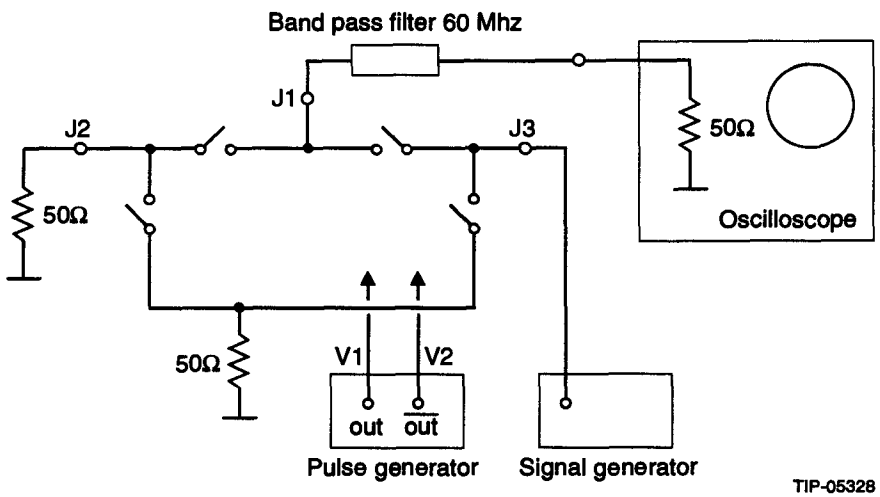


Figure 29.

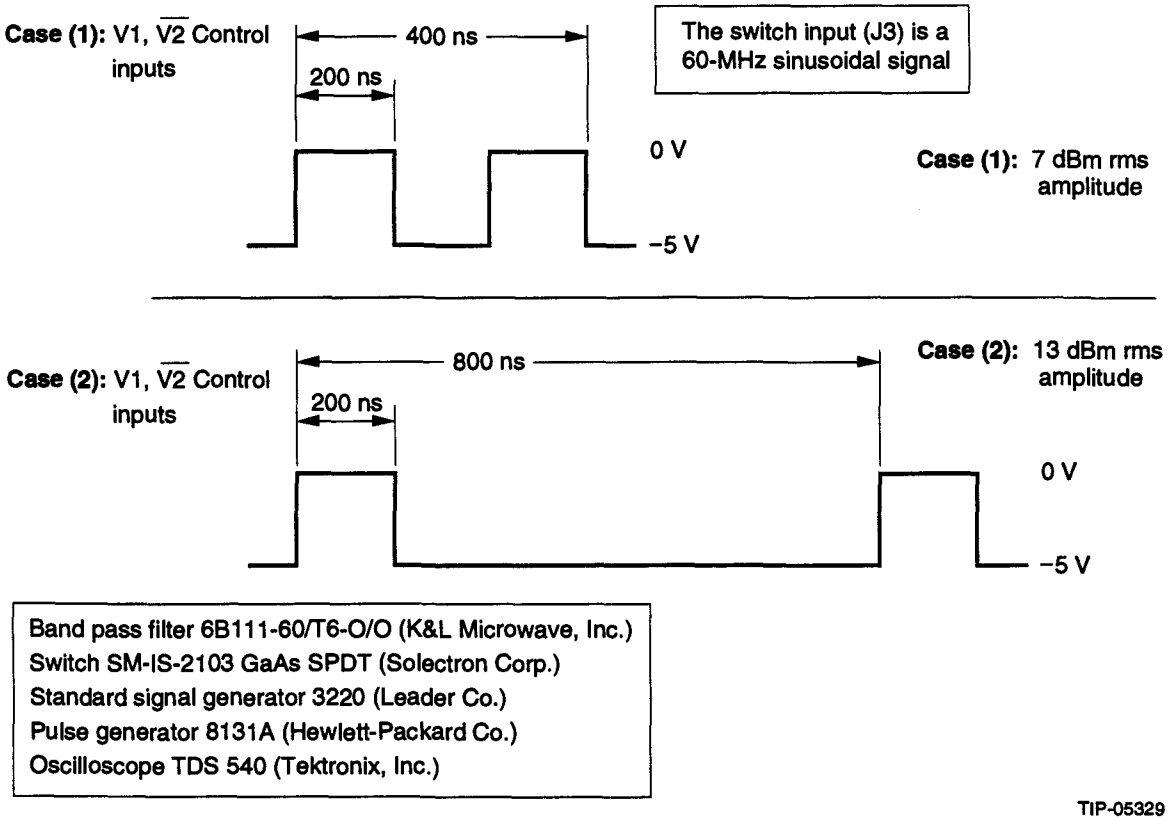


Figure 30.

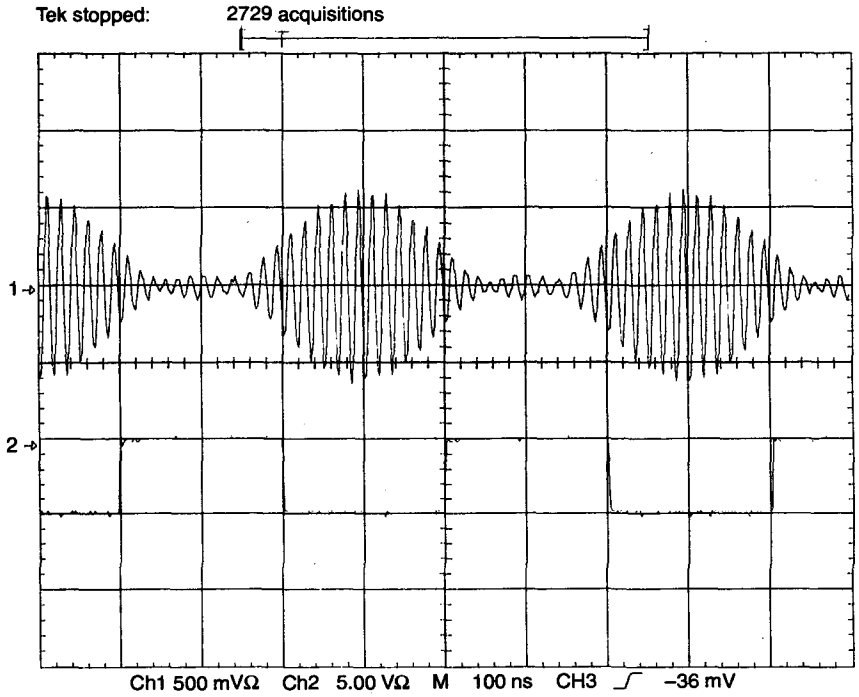


Figure 31.

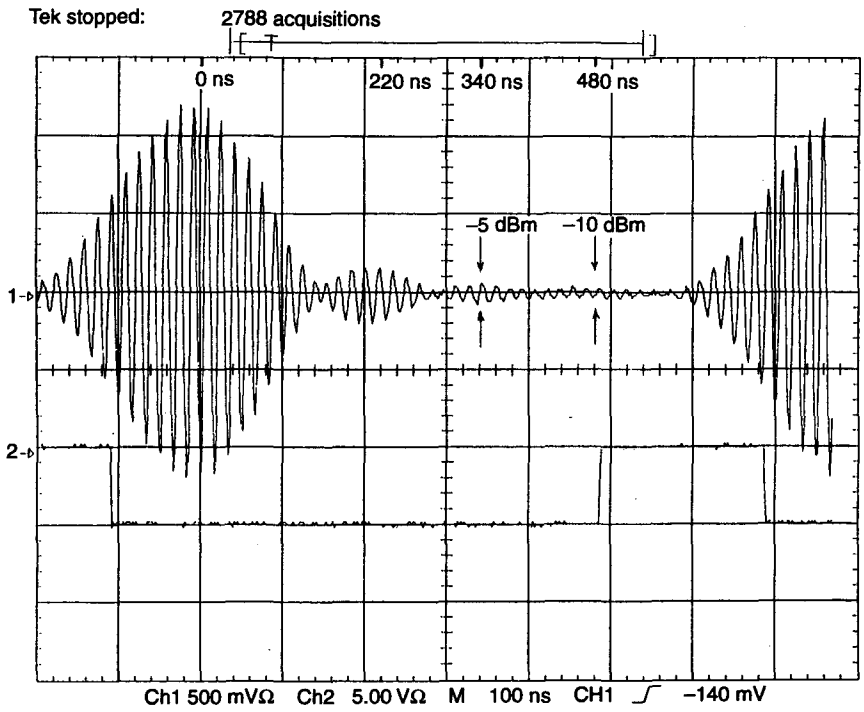


Figure 32.

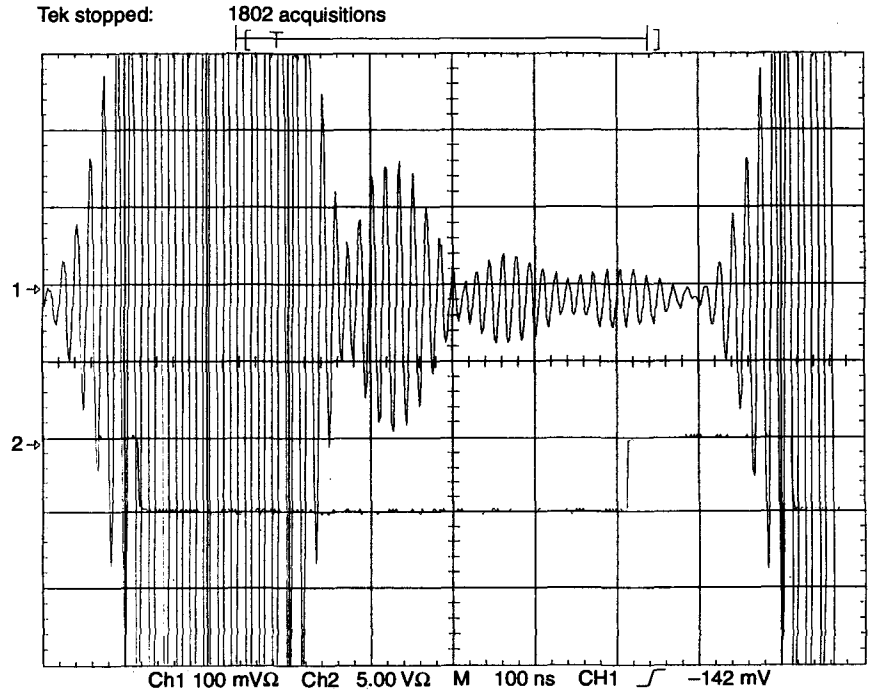


Figure 33.

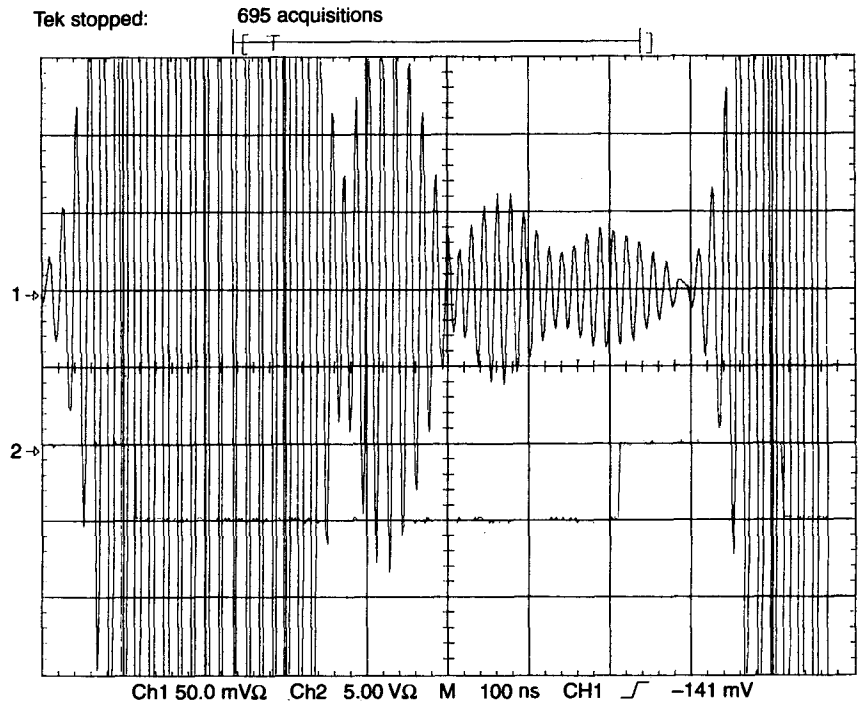


Figure 34.

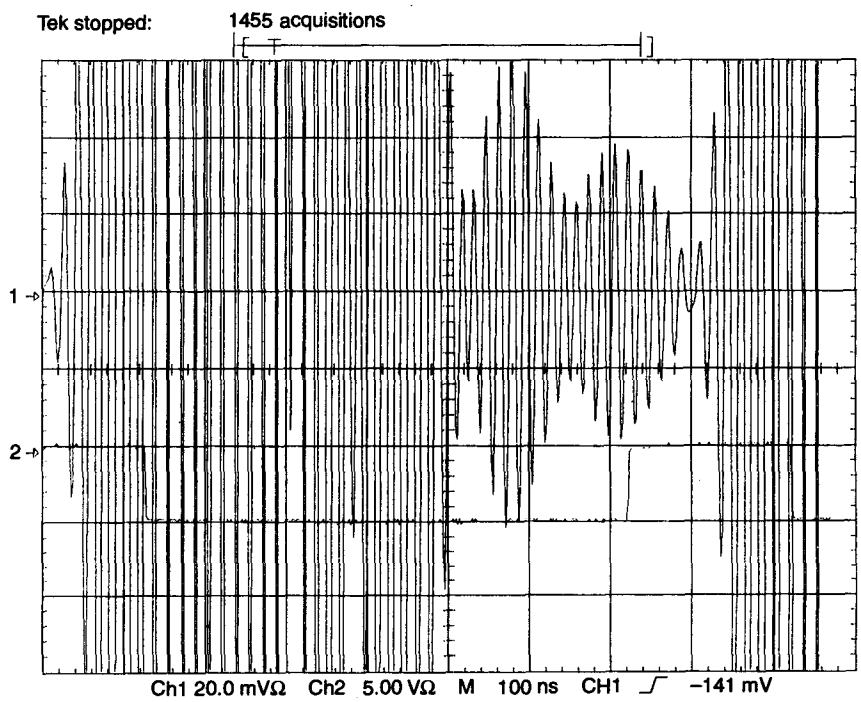


Figure 35.

3.7 Switch and "Simple" Filter Measurements

The filter's output oscillations dumping signal decreases from 2 V to 15 mV (–23 dBm pk–pk, or –30 dBm pk–pk/2) during a 100-ns time interval, as shown in Table 3 and Figures 36–38.

So, for a successful processing of a signal we need to choose a filter with a similar (approximately 14 MHz) bandwidth.

Also, I believe that an increase of the delay time between two control signals is reasonable.

Table 3. Amplitude and delay of filter's output oscillations dumping process.

t delay (ns)	A pk–pk (mV)	A pk–pk (dBm)	A pk–pk/2 (dBm)	A pk–pk/2 (mV)
0[a]	2200	19.9	13.8	1100
80	15	–23.5	–29.5	7.5

[a] This is a desired signal, and a reference point for a measurement time interval.

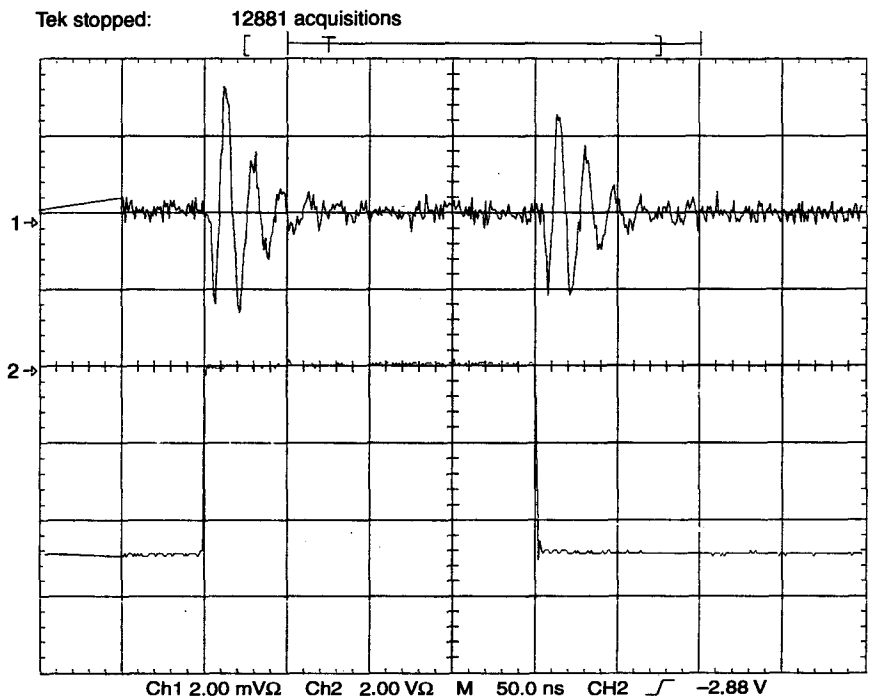


Figure 36.

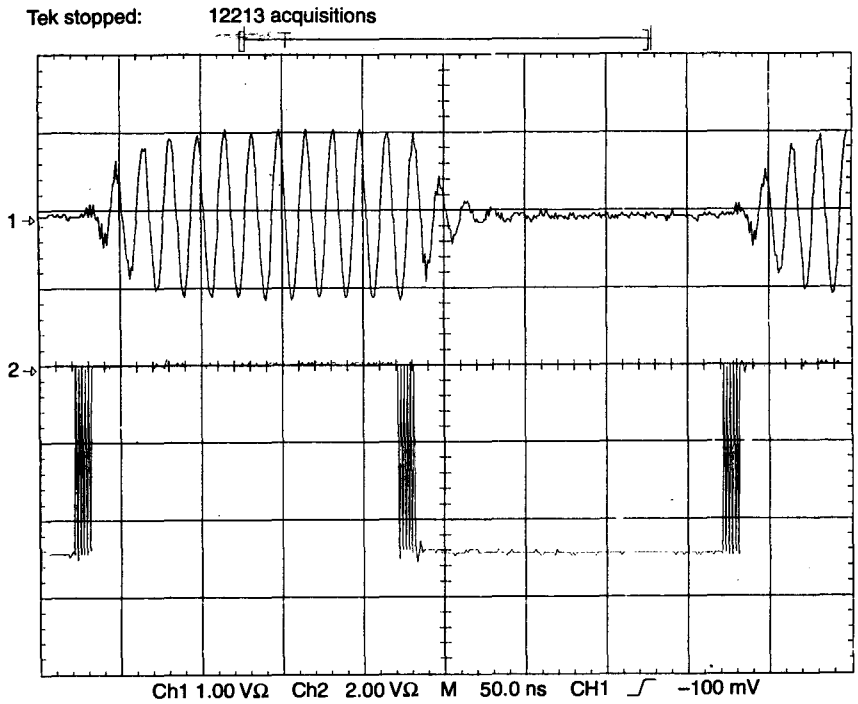


Figure 37.

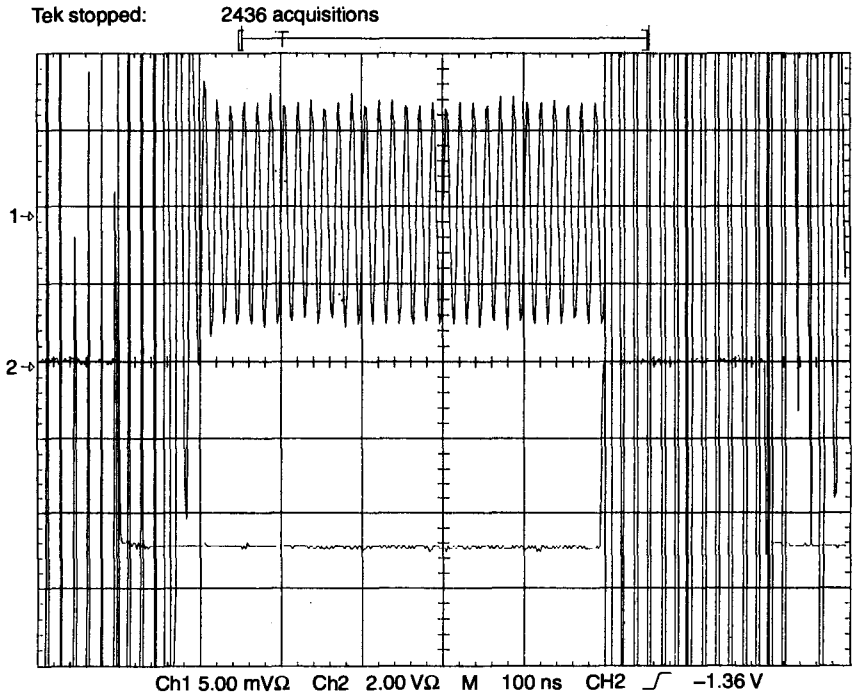
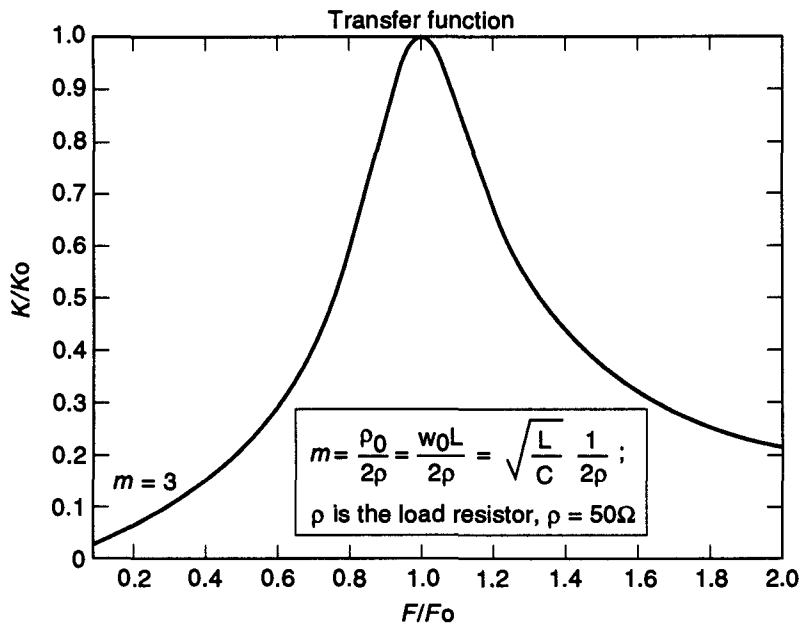


Figure 38.

The circuit, the conditions, the components (except a filter), and the equipment of the switch and "simple" filter measurements are the same, as in the previous series of measurements mentioned in Section 3.6.

The *LC* discrete filter has been used in the present measurements, $L = 1\ \mu H$; $C = 6$ pF.

The filter's calculated frequency characteristic (with the help of MATLAB) and measured frequency (60 MHz central frequency; 15 MHz bandwidth) and phase characteristics (with the help of HP8753C Network Analyzer) are shown in Figures 39–41.




```
% ftclc.m
x = (0.1:0.01:2)
m = (3)
% while m< = 8
% y =1./sqrt (1+m.^2.*(x–1./x).^2)
% plot (x,y)
% semilogx (x,y)
% loglog (x,y)
% hold on
% m = m+1
% end
y = 1./sqrt (1+m.^2.*(x–1./x).^2)
plot (x,y, '—')
% semilogx (x,y)
% loglog (x,y)
% hold on
title ('Transfer Function')
xlabel ('F/Fo')
ylabel ('K/Ko')
grid
```

TIP-05284

Figure 39.

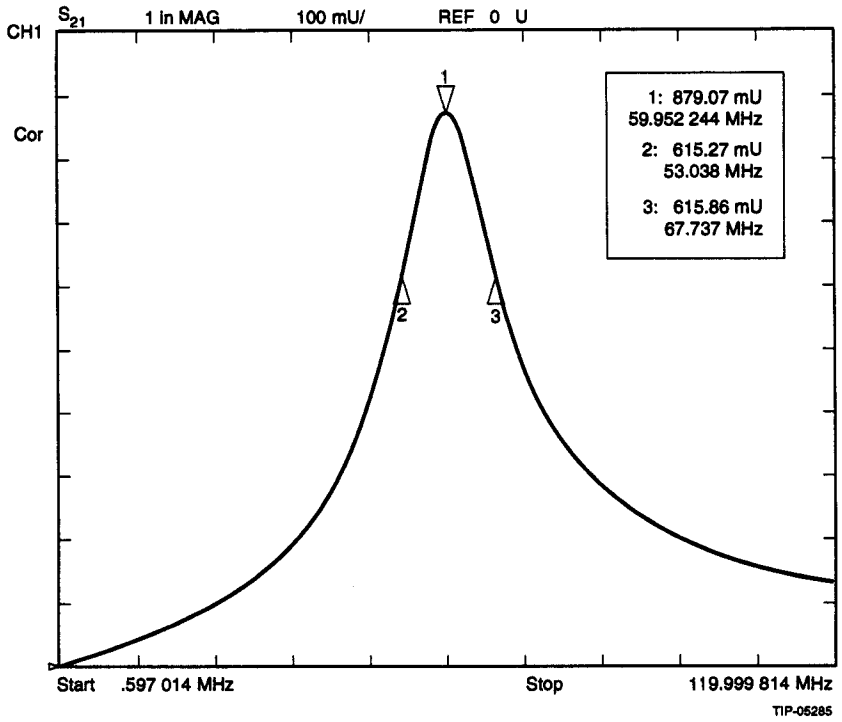


Figure 40.

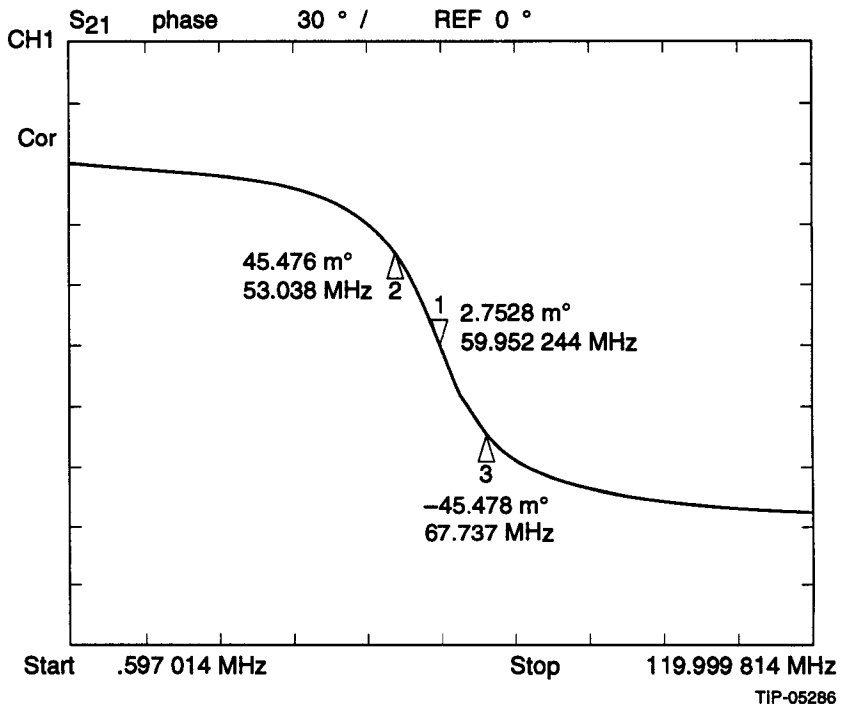


Figure 41.

4.0 BEAM LOSS MONITOR

4.1 Accuracy of the Integrator

Before calculations of the integrator circuit on SPICE, I considered a question about accuracy of the integrator. Because of this, it depends on the choice of the operational amplifier and of all components of the circuit, such as resistors, capacitors, *etc.*

There are two different regimes of the operation of the integrator: dynamic (integration process) and static (hold process). We can analyze both of these processes separately. The integrator circuit is shown in Figure 42.

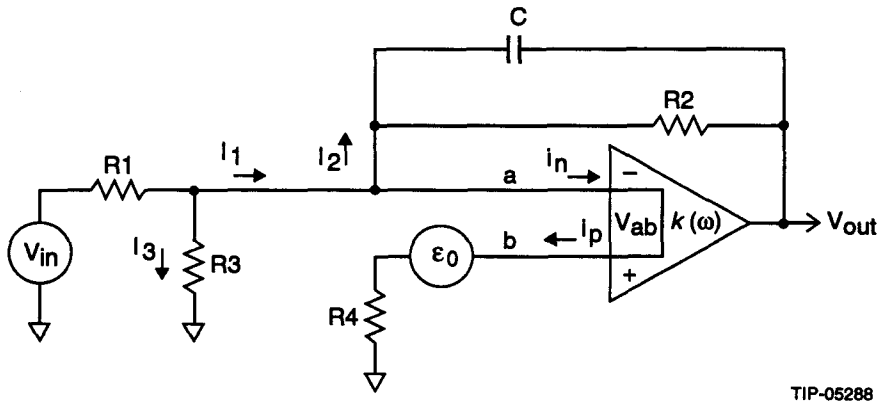


Figure 42. Integrator Circuit. ε_0 is offset voltage of operational amplifier (opamp); i_p is current to positive input of opamp; i_n is current to negative input of opamp; $k(\omega)$ is opamp gain versus frequency. In static analysis we will use value of static gain of opamp k_{st}.

4.2 Static Analysis

For the circuit shown in Figure 42, a set of simultaneous equations is:

$$\begin{cases} I_1 = I_2 + I_3 + i_n \\ I_1 = \dfrac{V_{in} - V_a}{R_1} \\ I_2 = \dfrac{V_a - V_{out}}{Z} \\ I_3 = \dfrac{V_a}{R_3} \\ \varepsilon' = -i_p R_4 \\ V_a = \varepsilon' + \varepsilon_0 + V_{ab} \\ V_{ab} = -\dfrac{V_{out}}{k_{st}} \end{cases}, \tag{34}$$

where $Z = x_c \| R_2$, or

$$Z = \frac{R_2}{1 + j\omega C R_2} . \tag{35}$$

We can rewrite Eq. (34) using values of the currents:

$$\frac{V_{in}-V_a}{R_1}=\frac{V_a-V_{out}}{Z}+\frac{V_a}{R_3}+i_n. \tag{36}$$

Then substitute V_a value and collect V_{out} together; that is,

$$V_{out}\left(\frac{1}{k_{st}R_1}+\frac{1}{k_{st}R_3}+\frac{1}{k_{st}Z}+\frac{1}{Z}\right)=-V_{in}\frac{1}{R_1}+\left(\frac{1}{R_1}+\frac{1}{R_3}+\frac{1}{Z}\right)\left[\varepsilon'+\varepsilon_o\right]+i_n. \tag{37}$$

From here, after transformations, we obtain:

$$V_{out}=-V_{in}\frac{Z}{R_1}\frac{1}{R_1\left(1+\frac{1}{k_{st}\beta}\right)}+\frac{1}{\beta}\frac{1}{\left(1+\frac{1}{k_{st}\beta}\right)}\left(\varepsilon_o-i_pR_4+i_nZ\beta\right), \tag{38}$$

where

$$\frac{1}{\beta}=1+\frac{Z}{R_1}+\frac{Z}{R_2}. \tag{39}$$

The first part of the expression is "classic" dependency between output and input voltage for the operational amplifier in integration regime, with deep negative feedback. The second part is accuracy of the integrator due to the offset voltage and the positive and the negative input currents of opamp.

In modern operational amplifiers, the static gain is really high; it doesn't give essential error to the static process. That is why we can neglect the static gain (k_{st}) and put $k_{st}=\infty$. So, a simple form of Eq. (38) is:

$$V_{out}=-V_{in}\frac{Z}{R_1}+\frac{1}{\beta}\left(\varepsilon_0-i_pR_4+i_n\beta Z\right). \tag{40}$$

Let's analyze this expression a little bit more. This equation hides two sources of error of the output voltage: error due to the offset voltage and both input currents, and error due to the discharge of the capacitor in the static (hold) process. For analysis of the first one, we can put $\omega = 0$, and, therefore, $Z=R_2$. Thus we can rewrite Eq. (40) in the following way:

$$|\bar{Z}_{is31}|\Delta V_{out}=\frac{1}{\beta_0}\left(\varepsilon_0-i_pR_4+i_n\beta_0R_2\right), \tag{41}$$

where

$$\frac{1}{\beta_0}=1+\frac{R_2}{R_1}+\frac{R_2}{R_3}. \tag{42}$$

For error due to the capacitor's discharge, we do not need to consider the offset voltage and the positive current, so we can make them equal to zero. Rewrite Eq. (40), taking into account the full expression for Z:

$$\Delta V_{out} = -V_{in}\frac{R_2}{R_1}\times\frac{1}{1+j\omega CR_2}+i_n\times\frac{R_2}{1+\frac{R_2}{R_1}+\frac{R_2}{R_3}+j\omega CR_2}. \tag{43}$$

These two equations are ready for analysis of behavior of the integrator in the static process. Let's start to do the same calculations for the integration process.

4.3 Dynamic Analysis

For the dynamic (integration) process, we write: $\frac{d\varepsilon_o}{dt}=0, \frac{di_p}{dt}=\frac{di_n}{dt}=0$. So, the set of simultaneous equations (Eq. (34)) will change thusly:

$$\begin{cases} I_1 = I_2 + I_3 \\ I_1 = \frac{V_{in}-V_a}{R_1} \\ I_2 \frac{V_a - V_{out}}{Z} \\ I_3 = \frac{V_a}{R_3} \\ V_a = V_{ab} \\ V_a = -\frac{V_{out}}{k(\omega)}. \end{cases} \tag{44}$$

For output voltage from the equation for I_2 (third equation from the set), we get:

$$V_{out} = -I_2 Z + V_a. \tag{45}$$

Let us express I_2 through the equation for I_1; substitute instead of I_1 and I_3 their values from the third and fourth equations from the set; express V_a through the last equation from the set. After these manipulations, we get:

$$V_{out}\left(1+\frac{1}{k(\omega)}\frac{Z}{R_1}+\frac{1}{k(\omega)}\frac{Z}{R_3}+\frac{1}{k(\omega)}\right) = -V_{in}\frac{Z}{R_1}. \tag{46}$$

Take Z from Eq. (35). Also, we will make the following small changes to Eq. (35):

$R_2 C = \tau, \tau = \frac{1}{\omega_0}$, so $Z = \frac{R_2}{1+j\times\frac{\omega}{\omega_0}}$. After some calculations we get:

$$V_{out} = -V_{in}\frac{R_2}{R_1}\times\frac{1}{1+j\frac{\omega}{\omega_o}}\times\left[\frac{1}{1+\frac{1}{k(\omega)\left(1+j\frac{\omega}{\omega_o}\right)}\times\left(1+\frac{R_2}{R_1}+\frac{R_2}{R_3}+j\frac{\omega}{\omega_o}\right)}\right]. \quad (47)$$

Equations (41), (43), and (47) are ready for analysis of the integration process, and static process of the signal-holding. From the requirements for the integrator, we can choose the operational amplifier and calculate all parameters of the circuit, taking into account dynamic and static "points of view." Probably, analysis of Eq. (47) can be done by using a program such as MatLab. The full circuit can be calculated by SPICe with a proper amplifier.

5.0 COMMENTS ON THE ADC, NOISE, AND SNR

This section is an attempt to recall one part of the big theory of ADC building and testing. It includes the reasoning of noise in ADC, thoughts accompanying this reasoning, and many details—for example, a long deviation of the SNR equation.

Noise of the ideal ADC occurs as a result of quantization (digitizing) of the input signal by level. When the input signal is between two neighboring levels of ADC, the output signal of ADC is a fixed value, equal to the voltage, corresponding to ADC level (Figure 43). In this case, we cannot say exactly what value of the input voltage corresponds to this level.

We can discuss only the approximate range of the input signal that can generate this output level. This range is equal to the step of ADC (width of the ADC quanta). All of these input voltages have the same probability of being found. Otherwise, the probability function (to occur at any voltage in the quanta's range) is rectangular. The difference between input signal and output signal of the ADC is called quantization error (Figure 44).

This is the error of the ideal ADC (of the idea of the digitizing). The probability density function of error is rectangular (Figure 45). By the term "output signal of ADC" I mean the ideal voltage value, corresponding to the ADC binary code after DAC conversion.

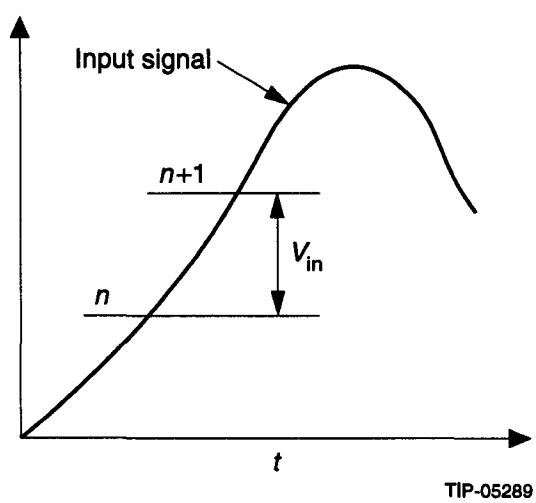


Figure 43. V_{in}—input voltage, which generates n + 1 ADC "level".

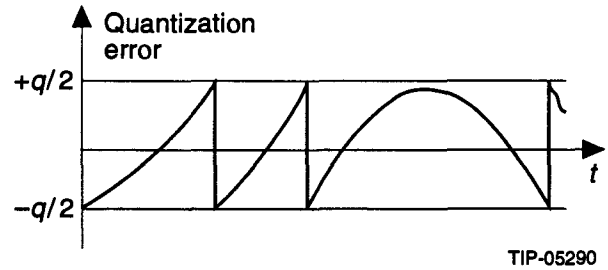


Figure 44. Quantization error.

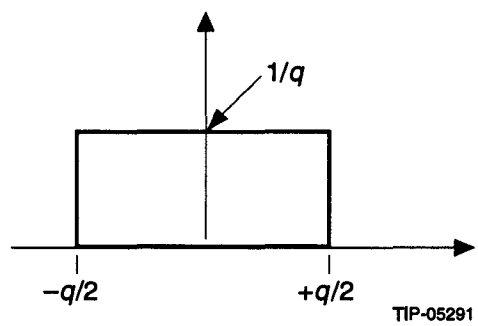


Figure 45. The probability density function of the error.

If the quanta's size is q, then the error can change from $-q/2 + q/2$. The condition of normalization of the mean squared error function is:

$$\int_{-q/2}^{q/2} f(x)dx = 1; \tag{48}$$

hence,

$$f(x) = \frac{1}{q}. \tag{49}$$

The square of the error of the deviation from average is:

$$\sigma^2 = \frac{1}{q} \cdot \int_{q/2}^{q/2} (x - \bar{x})^2 dx = \frac{1}{q} \cdot \int_{q/2}^{q/2} x^2 dx. \tag{50}$$

The result of integration is:

$$\sigma^2 = \frac{q^2}{12}. \tag{51}$$

This means, that in the result of the conversion of the input signal, we obtain "corridor" of the output values (Figure 46), which corresponds to the input signal value. The input signal is inside of this corridor. Width of this corridor is determined by the quantization error. Rms value of this error is equal to the $q/\sqrt{12}$.

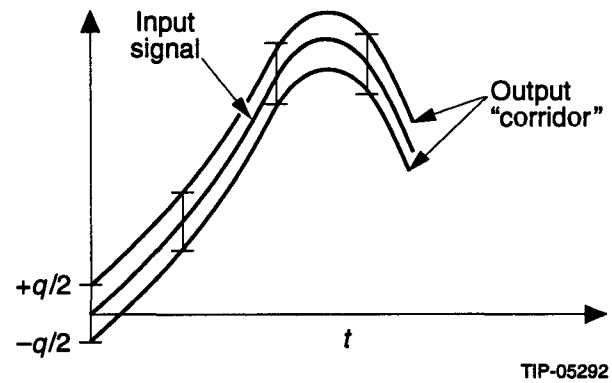


Figure 46. The "corridor" of the output values.

We can rewrite Eq. (51) using the following terms: full-scale voltage range of ADC (A) and ADC resolution in bits (N), then

$$q = \frac{A}{2^N}, \quad \text{and} \tag{52}$$

$$\sigma^2 = \frac{A^2}{12.4^N}. \tag{53}$$

An important characteristic of ADC is the Signal to Noise Ratio (SNR). SNR is the ratio between the power of the input signal and the noise power. We can obtain an equation for SNR from our previous reasoning. If our input signal is a full-scale sinus wave, the rms value for sinusoidal signal (B) is 1/2 peak-to-peak value, divided by $\sqrt{2}$:

$$B = \frac{A}{2\cdot\sqrt{2}}, \text{ or } A = 2\cdot\sqrt{2}\cdot B. \tag{54}$$

In fact, σ^2, which we obtained before, is the noise power. Then SNR is:

$$\frac{B^2}{\sigma^2} = \frac{12\cdot 4^N}{4\cdot 2}, \text{ or in dB:} \tag{55}$$

$$10\cdot\lg\left(\frac{B^2}{\sigma^2}\right) = 10\cdot\lg\left(4^N\right) + 10\cdot\lg\left(\frac{3}{2}\right), \tag{56}$$

$$SNR[\text{dB}] = 6.02\cdot N + 1.76. \tag{57}$$

This is an important and useful equation for the SNR definition. But up until now we were talking only about the ideal ADC. Real ADC has many noise sources, one of which is the differential nonlinearity (DNL), a deviation of the width of the ADC quanta from the ideal value (Figure 47). From the point of view of noise it means that the width of probability function (to occur at any voltaae in the quanta's range) changes. This means that DNL plays an equal part in the equation for the SNR, as a quantization noise. Therefore, DNL increases the noise value. Here, I do not give a strict definition of the DNL. Usually DNL is expressed in terms of LSB. Our definition allows us to understand the influence of DNL on the noise of the ADC.

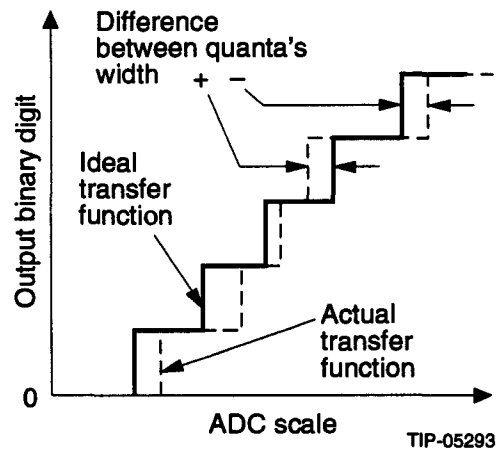


Figure 47. Illustration of the differential nonlinearity.

If σ_a is actual error (error of real ADC), and σ_i and σ_d are ideal (quantization) and differential nonlinearity errors, respectively, then

$$\sigma_a^2 = \sigma_i^2 + \sigma_d^2. \tag{58}$$

By using Eq. (55) we obtain expressions for σ_i and σ_d:

$$\begin{cases} \sigma_a^2 = \dfrac{B^2 \cdot 4 \cdot 2}{4^{N_a} \cdot 12} \\ \sigma_i^2 = \dfrac{B^2 \cdot 4 \cdot 2}{4^{N_i} \cdot 12}, \end{cases} \tag{59}$$

where N_a and N_i are the actual and ideal numbers of bits, respectively. So that

$$\frac{\sigma_i^2}{\sigma_a^2} = \frac{4^{N_a}}{4^{N_i}}, \text{ or} \tag{60}$$

$$2^{2 \cdot N_a} = 2^{2 \cdot N_i} \cdot \left(\frac{\sigma_i^2}{\sigma_a^2} \right). \tag{61}$$

The equation for N_a is:

$$N_a = N_i - \frac{1}{2} \cdot \log_2 \left(\frac{\sigma_a}{\sigma_i} \right)^2 . \tag{62}$$

This equation is well-known, too, as an equation for the SNR, and it shows the dependence between the ideal number of bits (perfect N-bit ADC), ideal and actual rms errors, and actual number of bits.

Now we can obtain an expression for the SNR, taking into account differential nonlinearity.

$$\frac{B^2}{\sigma_a^2} = 4^{N_a} . \frac{12}{4.2}, \text{ or in dB:} \tag{63}$$

$$\text{SNR} = (10 \cdot \lg 4) \cdot N_a + 10 \cdot \lg \left(\frac{12}{4.2} \right), \text{ or} \tag{64}$$

$$\text{SNR} = 6.02 \cdot N_a + 1.76 . \tag{65}$$

Substituting N_a from Eq. (62), we obtain:

$$\text{SNR} = 6.02 \cdot N_i - (10 \cdot \lg 4) \cdot \frac{1}{2} \cdot \log_2 \left(\frac{\sigma_a}{\sigma_i} \right)^2 + 1.76, \tag{66}$$

$$\text{SNR} = 6.02 \cdot N_i - 10 \cdot \log_{10} \left(\frac{\sigma_i^2 + \sigma_d^2}{\sigma_i^2} \right) + 1.76, \tag{67}$$

$$\text{SNR} = 6.02 \cdot N_i - 10 \cdot \lg \left(1 + \frac{\sigma_d^2}{\sigma_i^2} \right) + 1.76, \text{ or} \tag{68}$$

$$\text{SNR} = 6.02 \cdot N_i - 10 \cdot \log \left(1 + \frac{12 \cdot \sigma_d^2}{q^2} \right) + 1.76. \tag{69}$$

Thus, differential nonlinearity decreases the signal-to-noise ratio. Usually it is said not only with regard to the noise of the ideal ADC, or the noise due to DNL. Often the terms used are "total noise" and "effective bits" of the ADC. Effective bits means real, or perfect, resolution of ADC. The term "total noise" means noise due to quantization and differential nonlinearity of the ADC (about which we have spoken previously), missing codes, aperture uncertainty, and own noise. Own noise is a combination of the noise of the reference voltage of the ADC, thermal noise of the components, noise of the power supplies, noise that arrives with the signal, *etc.* These types of noise have a Gaussian probability density function. The theoretical minimal noise of ADC components is the thermal noise.

From this point of view we can change N_a to N_{eff} in Eqs. (62) and (65). (In Eq. (62) it should change σ_a to σ "effective," or "total.") Then for the signal-to-total-noise ratio we obtain (by using N_{eff}):

$$\text{SNR} = 6.02 \cdot N_{eff} + 1.76 . \tag{70}$$

This equation is more useful in the SNR testing of the AD converter, and in determining the width of the noise floor of the ADC. A good illustration of this equation is the Fourier diagram. The floor of the FFT diagram represents noise of the ADC. Differential nonlinearity increases the width of the noise on the FFT diagram. SNR from Eq. (70) represents all noise of the ADC. Usually, we compare the real noise of ADC (obtained with Fourier diagram help) with calculated noise by using Eq. (57) (the ideal SNR level).

In conclusion I want to point out the influence of another parameter of ADC to the shape of the FFT diagram. This parameter is integral nonlinearity (INL). INL is the deviation of the real transfer function of ADC from ideal transfer function in the full-scale range of ADC. This deviation does not change the size of the ADC quanta, but changes the shape of the output signal of the ADC. Distortions of the output signal lead to the appearance of new harmonics on the FFT diagram (but do not change the noise width).

In this discussion we care not about the many other errors of the ADC. Leave them for the future.

6.0 WIRE SCANNER PREAMPLIFIER

Let us begin with some brief notes about noise calculations in SPICE. SPICE can calculate the noise component of each element of the circuit. Noise in the point of the circuit is the sum of the noise of different elements, taking into account various transfer functions in the circuit. By the term "noise" I mean the square average of voltage between the point in the circuit and the ground. To understand how SPICE makes a noise calculation, I looked for a simple example. First, we were stumped by a calculation of thermal noise of the voltage divider (Figure 48). We thought that in this configuration of the circuit, output noise must be equal to the sum of the noises of the resistors:

$$\overline{V}^2_{out} = \overline{V}^2_{R1} + \overline{V}^2_{R2}, \tag{71}$$

where

$$\overline{V}^2_{Ri} = 4kTR_iB. \tag{72}$$

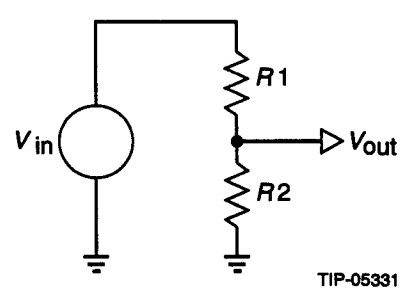


Figure 48. Thermal noise of voltage divider.

But our first impression was wrong. SPICE transforms this circuit to the equivalent circuit for noise calculations, where $R1$ and $R2$ are parallel (Figure 49). In this circuit, output noise is:

$$\overline{V}^2_{out} = \left(\varepsilon_1 \frac{R_2}{R_1 + R_2}\right)^2 + \left(\varepsilon_2 \frac{R_1}{R_1 + R_2}\right)^2. \tag{73}$$

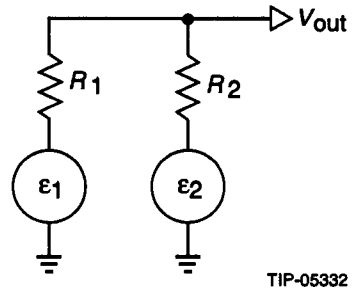


Figure 49. Equivalent circuit for noise calculations.

This result can be obtained by using the equivalent generator theorem. If $R1 = R2 = R$,

$$\overline{V}_{out}^2 = \frac{\varepsilon_1^2}{4} + \frac{\varepsilon_2^2}{4} = \frac{\varepsilon^2}{4}, \tag{74}$$

for $R = 1\Omega$, $\overline{V}_{1\Omega}^2 = 1.65 \cdot 10^{-20} \left[V^2/\mathrm{Hz} \right]$; consequently from Eq. (74),

$$\overline{V}_{out}^2 = 8.25 \cdot 10^{-21} \left[V^2/\mathrm{Hz} \right].$$

Part of resistor noises:

$$\overline{V}_{R_i}^2 = 4.125 \cdot 10^{-21} \left[V^2/\mathrm{Hz} \right].$$

SPICE calculation was:

$$\overline{V}_{out}^2 = 8.288 \cdot 10^{-21} \left[V^2/\mathrm{Hz} \right]$$

$$\overline{V}_{R_i}^2 = 4.144 \cdot 10^{-21} \left[V^2/\mathrm{Hz} \right].$$

I think that this example is a good illustration of a SPICE calculation. Now we can go to our main task.

In our circuit for obtaining real noise results, one should install equivalent noise sources of operational amplifiers. Amplifier noises are modeled by using parallel (current) and series (voltage) noise sources. We use Burr Brown operational amplifier OPA620. OPA620 noises are:

$$V = 2.5 \left[nV/\sqrt{Hz} \right], f = 100 \text{ kHz}$$

$$I = 2.3 \left[pA/\sqrt{Hz} \right], f = 10 \text{ kHz to } 100 \text{ MHz}.$$

In the program, noise sources were created, such as Current Controlled Voltage Source (CCVS) and Current Controlled Current Source (CCCS). To obtain the needed noise, a resistor was used to generate "standard" noise: for example, 1 pA / rt Hz for CCCS, and 1 nA / rt Hz for CCVS. Obtained values of noises were multiplied by gain. In our case gains are 2.3 and 2.5, respectively.

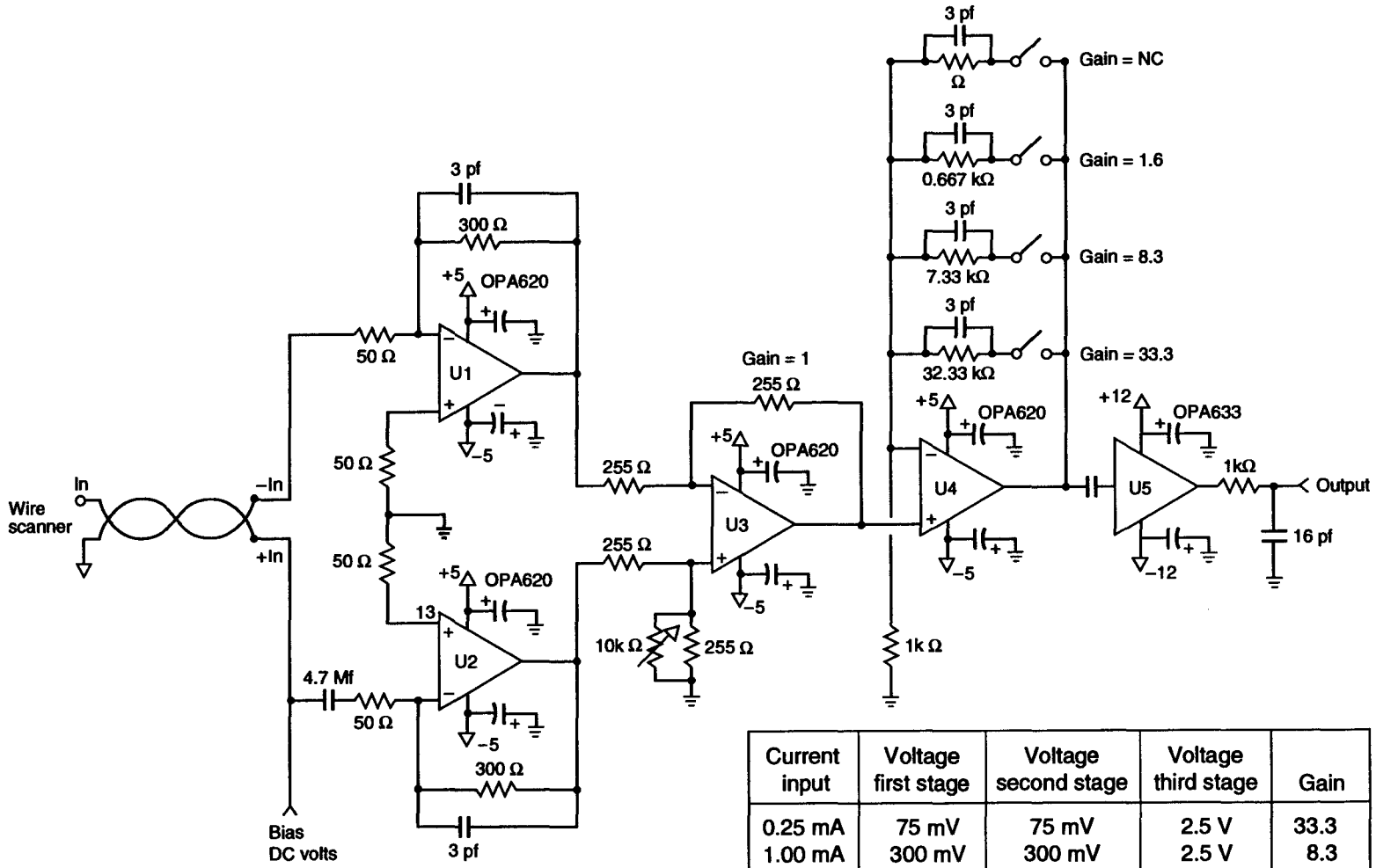
Output noise was calculated for three different gains. Maximum noise obtained was:

$$V_{out_{\max}} = 1.28\left[\mu V / \sqrt{\mathrm{Hz}}\right].$$

To compare these results with Phil Datte's calculations (Figure 50), integrate output noise over frequency. One can make it roughly, multiplying our results by the square root of 10 MHz to obtain:

$$V_{out_{\max}} \approx 3.84\mathrm{mV(rms)}.$$

This value has the same order of magnitude. A better estimation can be had by precise numerical integration. I think this should be our next step in the work. These results mean that in future research we can take into account estimations of noise by SPICE.



Current input	Voltage first stage	Voltage second stage	Voltage third stage	Gain
0.25 mA	75 mV	75 mV	2.5 V	33.3
1.00 mA	300 mV	300 mV	2.5 V	8.3
5.00 mA	1500 mV	1500 mV	2.5 V	1.6

TIP-05294

Figure 50. Phil Datte's circuit (wire scanner preamplifier).

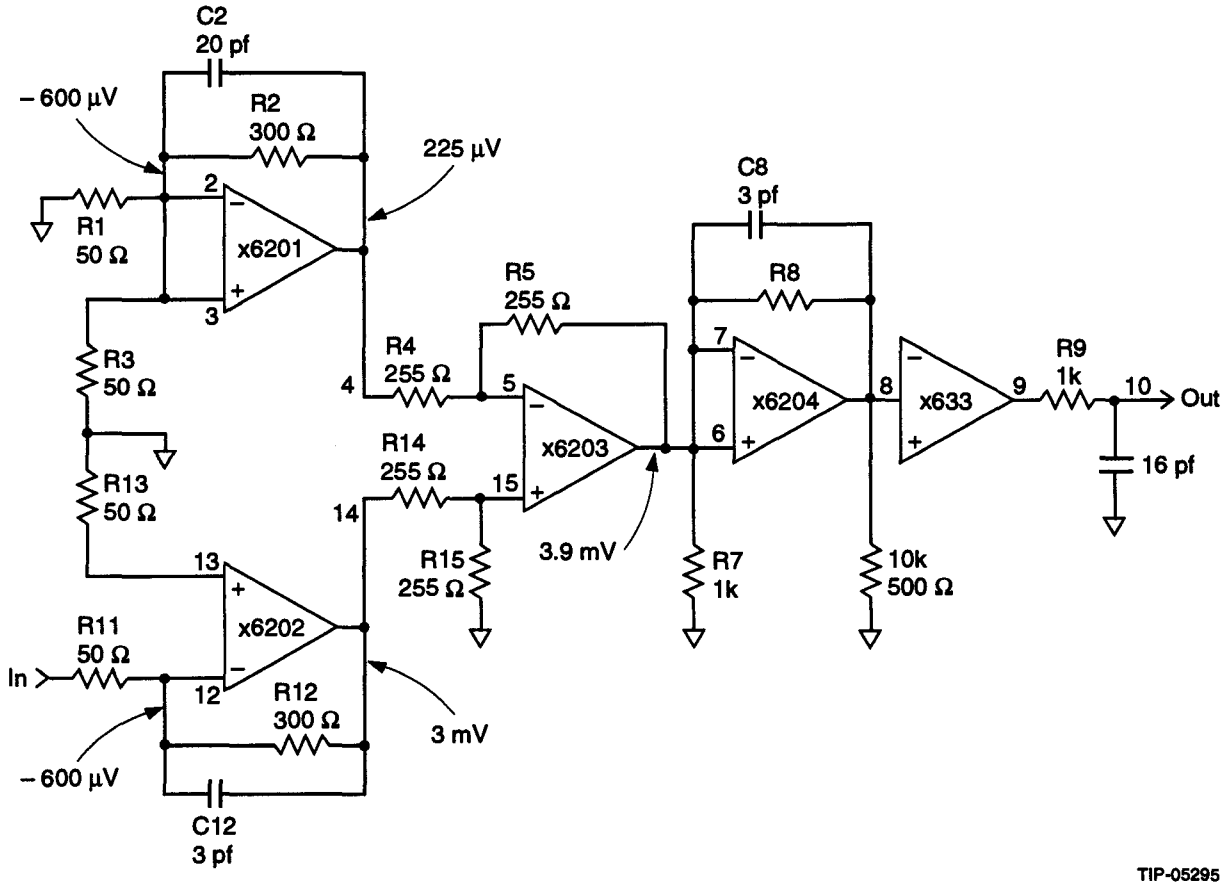

C2
20 pf
– 600 µV
R2
300 Ω
225 µV
2
R1
50 Ω
x6201
3
R3
50 Ω
4
R4
255 Ω
R5
255 Ω
5
x6203
R14
255 Ω
15
R13
50 Ω
14
R15
255 Ω
3.9 mV
13
x6202
R11
50 Ω
In
12
R12
300 Ω
3 mV
– 600 µV
C12
3 pf
C8
3 pf
R8
7
x6204
6
R7
1k
8
x633
9
R9
1k
10
Out
16 pf
10k
500 Ω
TIP-05295

Figure 51.

```
PREAMP
*
I11  11   0  AC    5mA
*0.25mA
*1mA
*5mA
*I11  11  0  PULSE      (0 5mA 0 10ns 1us 2us)
*
R7    7    0   160
RGAIN   7   8    52.8
*52.8
*907
*4.1K
*
*RLOAD 8  0  10K
*
C2    2   4  20pF
C12 12  14  20pF
C8    7   8   5pF
*
*
X6201   3   2  23    24   4 OPA620/BB
X6202  13  12  23    24  14 OPA620/BB
X6203  15   5  23    24   6 OPA620/BB
X6204   6   7  23    24   8 OPA620/BB
*
V23   23  0   5V
V24   24  0  -5V
*V25  25  0   5V
*V26  26  0  -5V
*
.LIB BURR_BRN.LIB
*
R1     0   2   50
R11   11  12   50
*
R2     2   4  300
R12   12  14  300
*
R3     3   0   50
R13   13   0   50
*
R4     4   5  255
R14   14  15  255
*
R5     5   6  255
R15   15   0  255
*
.AC DEC 100 100KHz 100MEG
*.TRAN 10ns 2us
*
.PLOT AC V (8)
*.PLOT DC V(8)
.PROBE
.END
```

Figure 52.

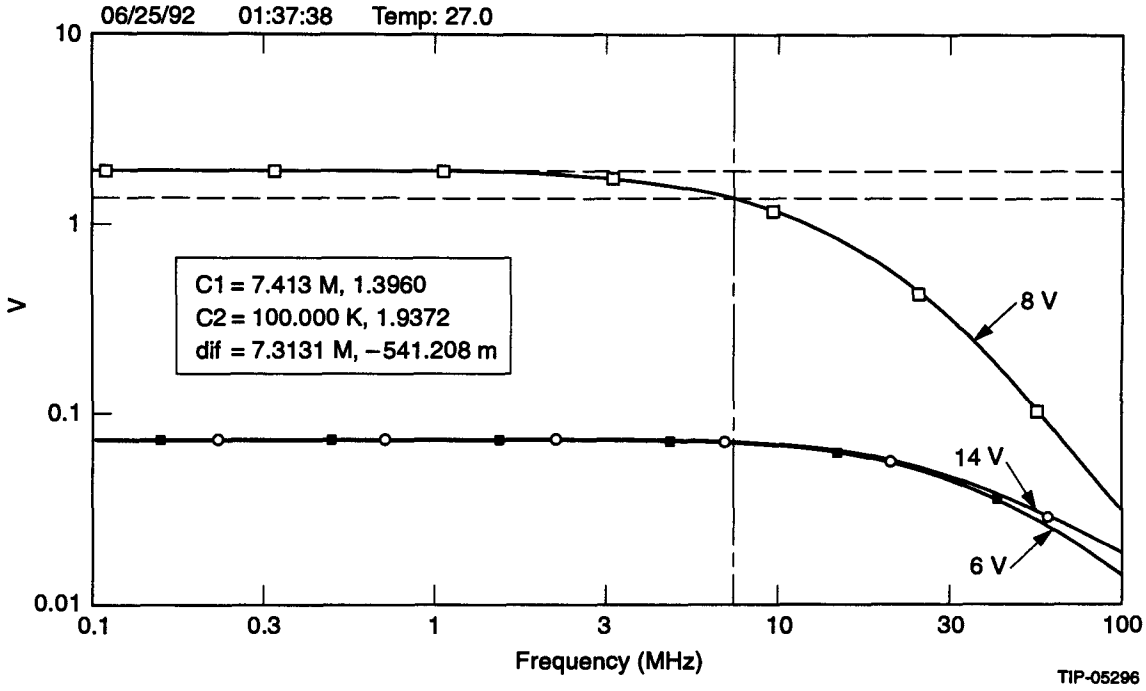


Figure 53.

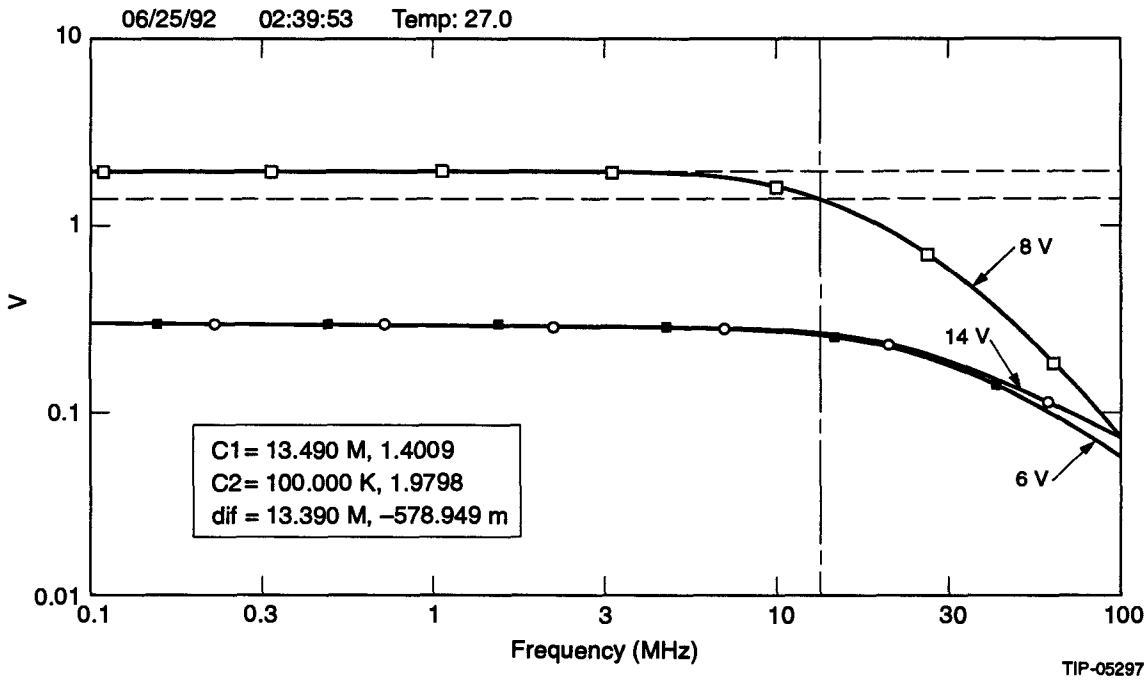


Figure 54.

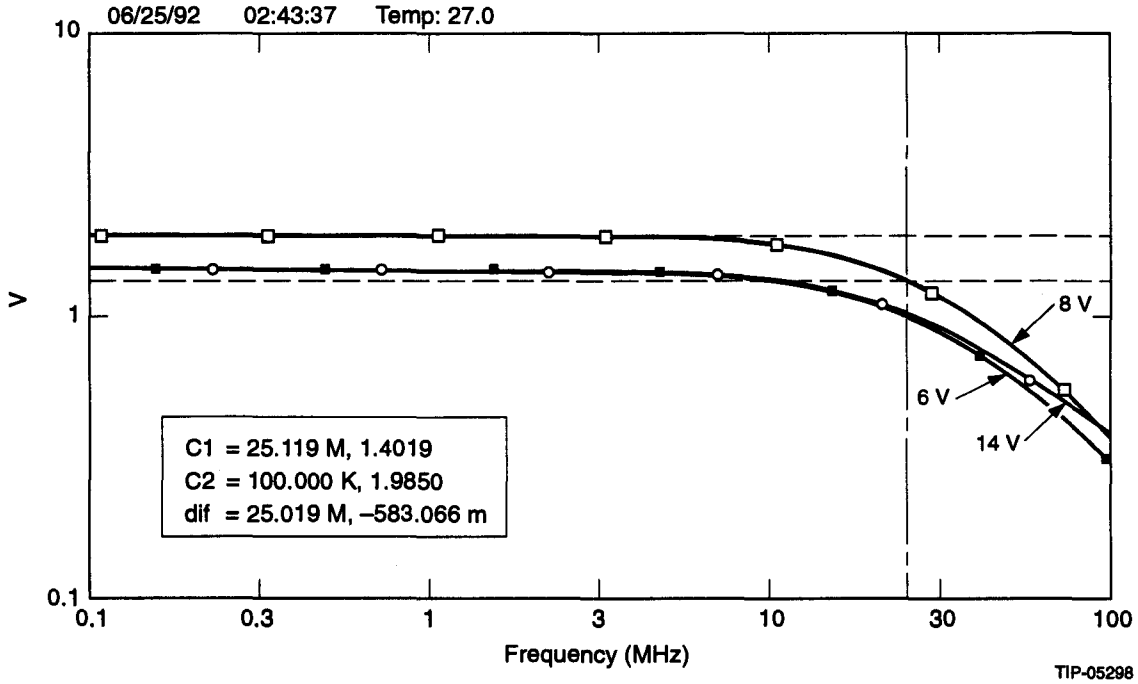


Figure 55.

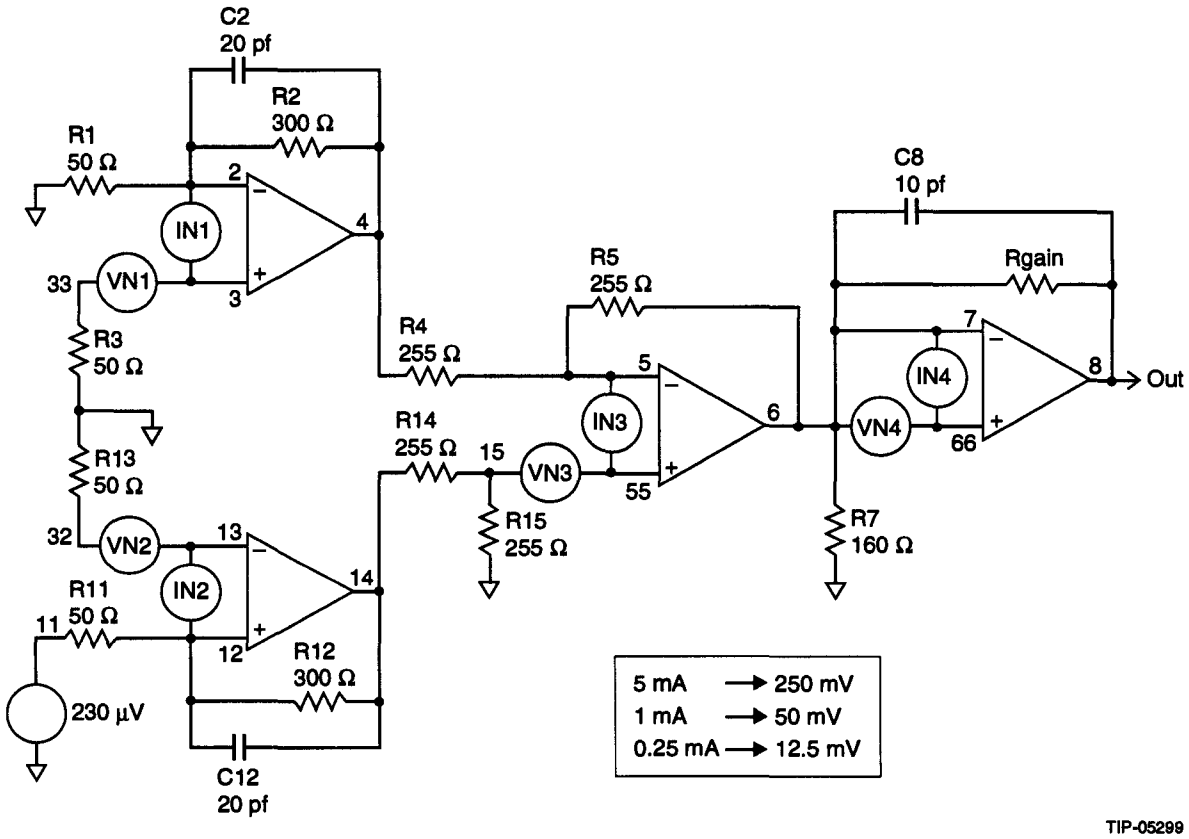


Figure 56.

```
PREAMP. NOISE
*
*  file name NOISE. CIR
*
*  input current, input voltage
*  and third stage feedback resistor.
*
*    5  mA  250  mV   52.8  ohms
*    1  mA   50  mV   907   ohms
* 0.25  mA  12.5 mV  4010   ohms
*
*I11  11   0   AC   5mA
*
V11  11   0   AC  12.5mV
*
RGAIN  7   8    4010
*
*   GAIN = ( 1 + RGAIN/R7 )
*
R7  7   0  160
*
C2    2    4   20pF
C12  12   14   20pF
C8    7    8    5pF
*
*
X6201    3  2  23  24   4  OPA620/BB
X6202   13 12  23  24  14  OPA620/BB
X6203   55  5  23  24   6  OPA620/BB
X6204   66  7  23  24   8  OPA620/BB
*
V23  23   0    5V
V24  24   0   -5V
*
.LIB BURR_BRN.LIB
*
R1     0   2   50
R11   11  12   50
*
R2     2   4  300
R12   12  14  300
*
R3    33   0   50
R13   32   0   50
*
R4     4   5  255
R14   14  15  255
*
R5     5   6  255
R15   15   0  255
*
*  noise sources:
*  modeled by using CCVS    ( H . . . )
*                  and CCCS   ( F . . . )
*
*   16.5mohms  -  1 sq nA / Hz
*   16.5kohms  -  1 sq pA / Hz
*
RV1  70   0   16.5m
VV1  70   0   0
HV1  33   3   VV1  2.5
*
R11  71   0   16.5K
V11  71   0   0
F11   3   2   VI1   2.3
*
RV2  72   0   16.5m
VV2  72   0   0
HV2  32  13   VV2  2.5
*
RI2  73   0   16.5K
VI2  73   0   0
FI2  13  12   VI2   2.3
*
RV3  74   0   16.5m
VV3  74   0   0
HV3  15  55   VV3  2.5
*
RI3  75   0   16.5K
VI3  75   0   DC 0
FI3  55   5   VI3   2.3
*
RV4  76   0   16.5m
VV4  76   0   0
HV4   6  66   VV4  2.5
*
RI4  77   0   16.5K
VI4  77   0   0
FI4  66   7   VI4   2.3
*
.AC   DEC   100   100KHz  100MEG
*
.NOISE  V (8)   V11   100
*
*.PLOT NOISE INOISE ONOISE
.PRINT NOISE ONOISE
*
*.PROBE
.END
```

TIP-05403

Figure 57.

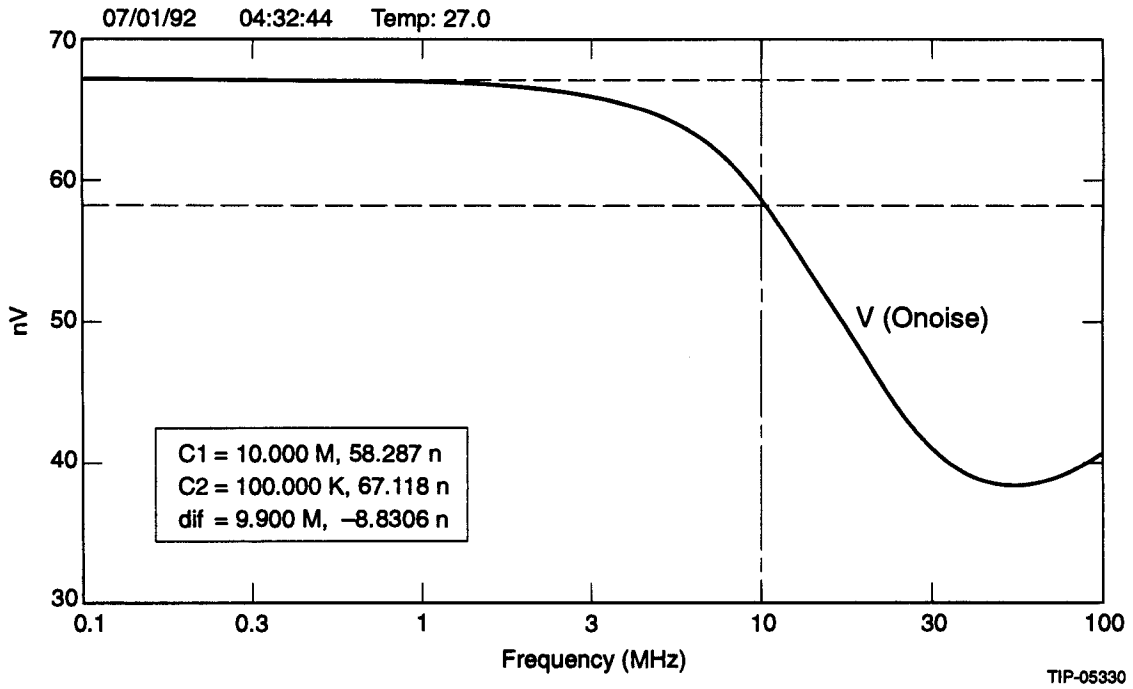


Figure 58. Small gain.

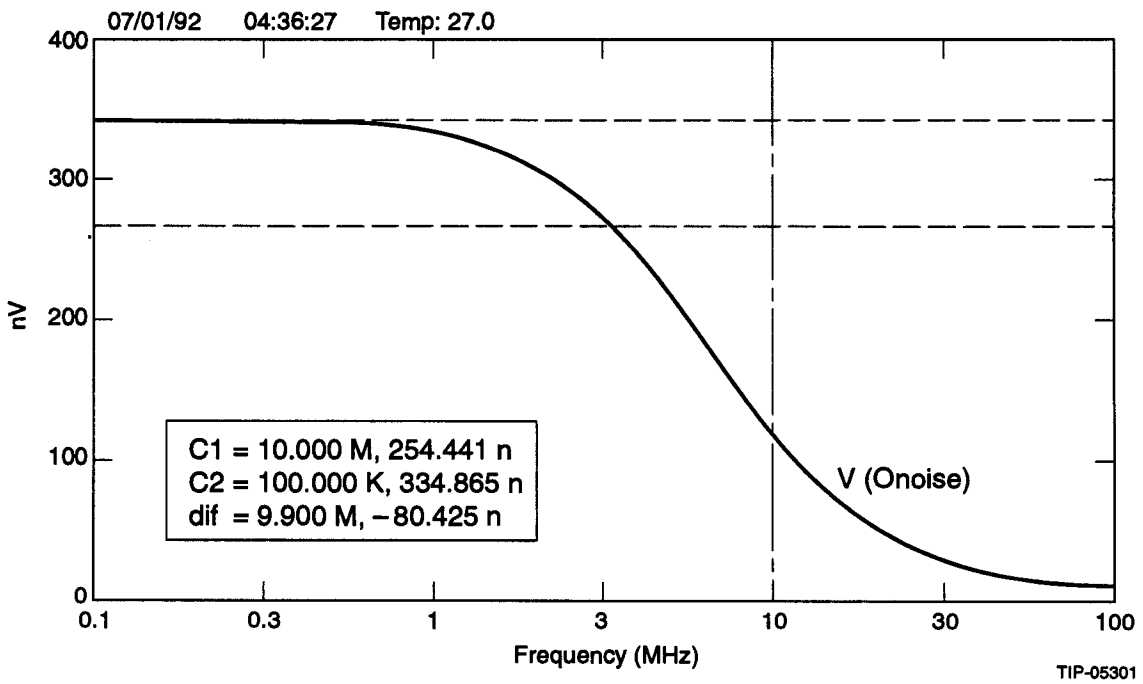


Figure 59. Middle gain.

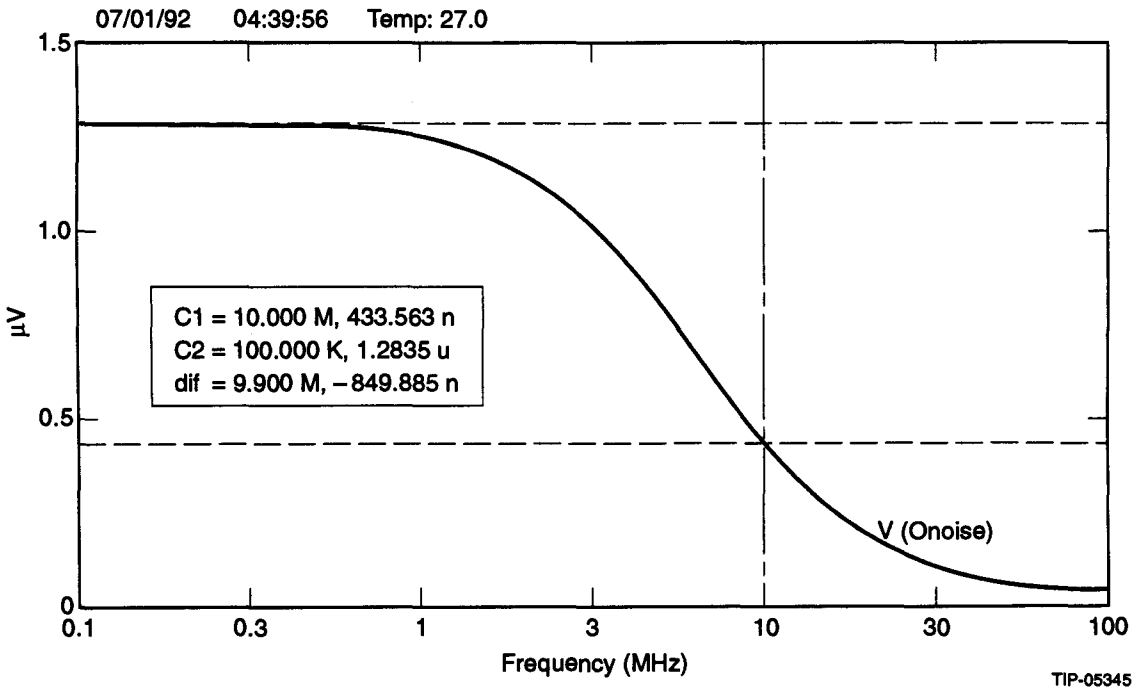


Figure 60. Large gain.

7.0 WEEKLY REPORTS

7.1 Weekly Report, 14–18 September, 1992

This week I have made investigations of the EL2004 buffer (separate model board). I was interested in the buffer gain versus input voltage. Results of the investigations are shown in Figures 61–63.

Before investigations of the linearity of the peak detector, I made some minor changes in the circuit; I also observed transfer function of the circuit. Unfortunately, results of the measurement of linearity are not good. I can't explain "cavity" on the curve (accuracy vs. input voltage) in the range of the small input voltage. I also can't explain deviations of the V_{out} vs. V_{in} curve from approximate polynom.

I measured linearity by using a new Hewlett-Packard scope. This is the best scope I have used. Possibilities of this scope are higher than are needed in our usual work. I think that this scope may help to make highly accurate measurements of the high-frequency signals, or of signals with short rise and fall time, *etc.*

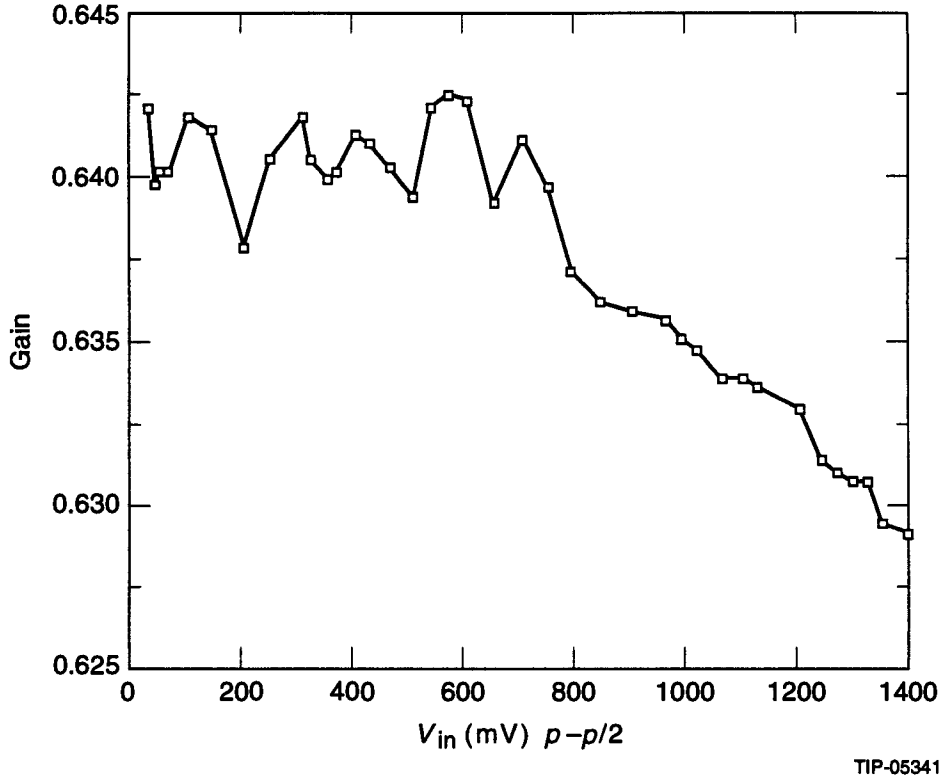


Figure 61. Buffer gain vs. input voltage.

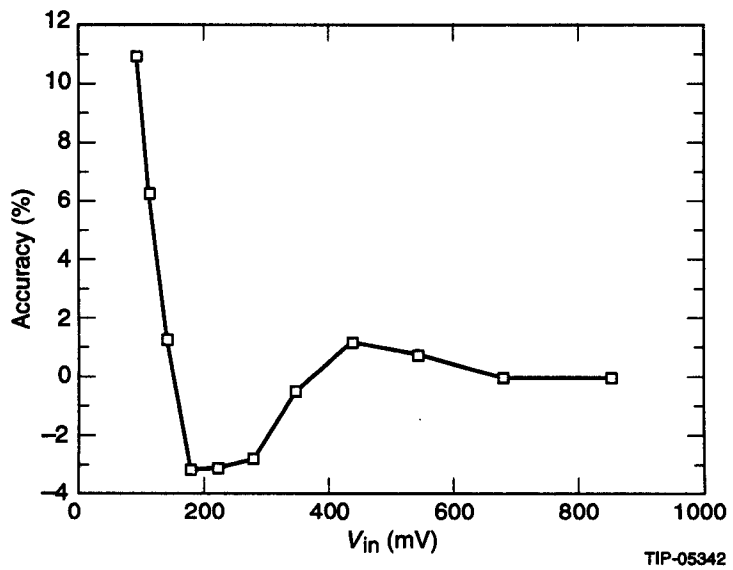


Figure 62. Accuracy vs. input voltage.

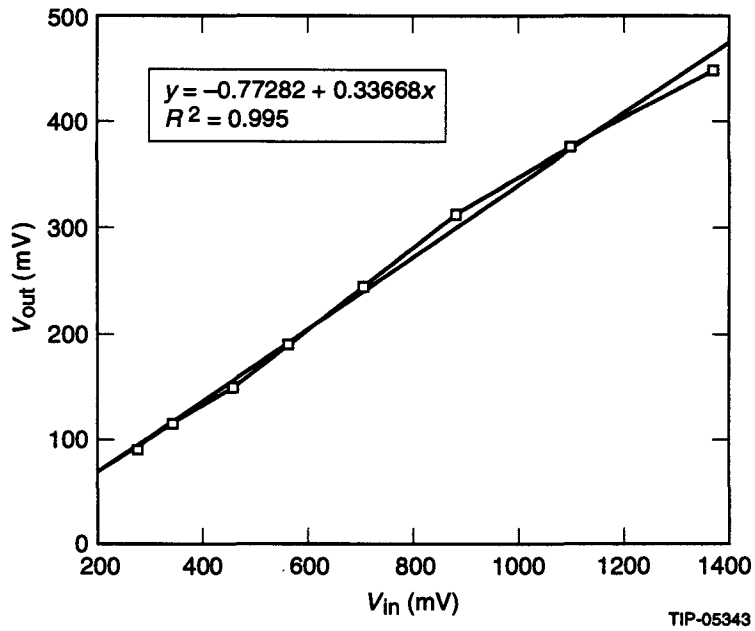


Figure 63. Data from "new.tab."

7.2 Weekly Report, 12–16 July, 1993

I have started to work with the electronic part of the Beam Position Monitor System (BPM), parts of which are being investigated and built in our lab. At the very beginning I investigated the possibility of the switches that we plan to use in a BPM circuit. I started from measurements of the delay line characteristics (Andersen Lab., 07996050). Measurements were done with the help of Network Analyzer HP8753C. This was my first experience of working with this device. Some of the time was spent in study of the Network Analyzer operational principles and users' instructions.

We measured:

- frequency response of the delay line (over the 54–66 MHz frequency range) and insertion loss of the delay line (–2.3 dB at 57.5 MHz and –2.9 dB at 60 MHz)
- electrical delay (delay time) (244 ns at 60 MHz)
- value of reflections of the matched delay circuit; ratio between signal and first reflection is –30 dB
- phase characteristic
- estimation of the temperature variations of the circuit parameters, with the chip having been heated from room temperature (approximately 20° C) to 60–80° C. Variations of the insertion loss over this temperature range lie in a range of –0.01 to –0.007 dB/C°. I observed the temperature dependence of the delay time. The variation of the delay time over the same temperature range is 1.6 ns.

The values of the insertion loss, delay time, and reflections agree with specifications. More accurate measurements of the insertion loss variations over temperature are planned by using a thermostatic oven with high accuracy of temperature adjustment (in rf department). The schedule of the measurements depends on the schedule of the work with the oven.

7.3 Weekly Report, 19–23 July, 1993

This week was devoted to the investigations of a switch problem and of problems joined with a delay line. Some parameters of a cable delay line were measured. We attempted to correct the "chip delay line," described in detail in a previous report.

> The cable delay line is the "semirigid" type, teflon inside, 50Ω impedance. Parameters of a cable delay line over the 54–66 MHz frequency range: electrical delay, 72 ns (delay time); length, 21.6 m; insertion loss, –2.2 dB (at 60 MHz frequency); ratio between the signal amplitude and a first reflection amplitude, 44 dB (for the matched cable). Unfortunately, there is not available a 200-ns or 250-ns cable delay line. So, we need to extrapolate all parameters for 250-ns cable delay line based on the 72-ns delay time. In this case for a 200-ns delay, the insertion loss will be approximately –7 dB.
>
> I have also tried to correct the frequency response and reduce the reflection coefficient of a "chip delay line." I did this because of the operational point of a frequency characteristic (60 MHz) located on a slope of one of the "hills" of a characteristic. Shifting of frequency on ± 180 kHz around 60 MHz leads to shifting of insertion loss to ± 0.35 dB. So, I have tried to make this slope more flat. In addition, the reflection coefficient (–30 dB) is not enough for the BPM circuit. (It needs at least –40 dB.)
>
> Unfortunately, all the corrections that I made did not lead to the desired results. My conclusion is that the "chip delay line" is optimized, and we can't do any significant changes. Maybe this is a reason to look through "chip delay lines" with a "neighboring" delay time, such as 200–280 ns, and choose delay with better (target—flat) frequency domain response around the frequency of 60 MHZ, because the "chip delay line" frequency response has a periodical character with a 2-MHz interval between the neighboring maximums. And I believe that we can find the "chip delay line" with the response that we need.

7.4 Weekly Report, 26–30 July, 1993

We have investigated the problems joined with the Switch Circuit for the BPM electronics. As a first "candidate" for a switch circuit I took SMIS 2103 GaAs SPDT switch (Solectron Corp.). This chip's parameters satisfy our task in general. I have regarded the Switch Circuit, which includes a "Hybrid Junction" device.[7] This is a passive, reciprocal, four-port device with equal power split from the sum port into two "neighboring" ports (in-phase signal to one port, and out-of-phase signal to the other). Opposite ports of the hybrid are isolated from one another. Configuration of the hybrid junctions and switches is shown in Figure 64. This circuit allows us to reduce in-phase parasitic signals from the switches.

Figure 64. Switch Circuit. (In-phase signals from the sw1 and the sw2 cancel each other on ports "a" of h1 and h2. Port "a" gets the signals with the same amplitude and the opposite phases from ports "c" and "d".)

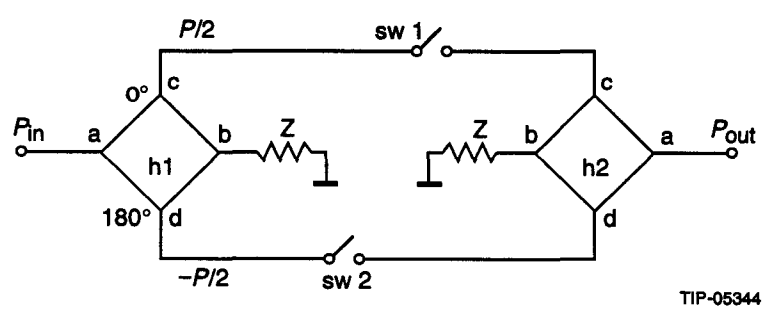


Figure 64. Switch Circuit. (In-phase signals from the sw1 and the sw2 cancel each other on ports "a" of h1 and h2. Port "a" gets the signals with the same amplitude and the opposite phases from ports "c" and "d".)

Output signal of the Switch Circuit is: $P_{out} = (P/2)/2+(-(-P/2)/2)$; *i.e.*, $P_{out} = P/2$, where $P = P_{in}$, input power. For the Switch Circuit I used "180° Two-Way Power Divider" H-81-4 (Anzac Co.). For our particular case, this is the same as a Hybrid Junction. This choice is dictated by the impossibility of buying something now. So I have made my choice from components on hand. Fortunately, I have found this Power Divider. This device is in a connectorized case style. In the future it is reasonable to replace this device with a similar one in a more appropriate case style, such as surface mount, or plug-in, *etc.*

I have measured the general parameters of the chosen Power Divider (all parameters here at the 60-MHz frequency):

- for ports "a" to "c" and "a" to "d": ratio between the signal amplitude and the first reflection amplitude is 43 dB; total transmission loss is –3 dB.
- for ports "c" to "d" and "d" to "c": phase shift is 180.2°; isolation is –29 dB.

Also I have started to discuss the following questions:

- The dynamic range of the signal from BPM electrodes and the dynamic range of BPM electronics.
- Isolation of the Switch Circuit.
- Reasons for choosing the time interval of 200–300 ns for the BPM electronics measurements.

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