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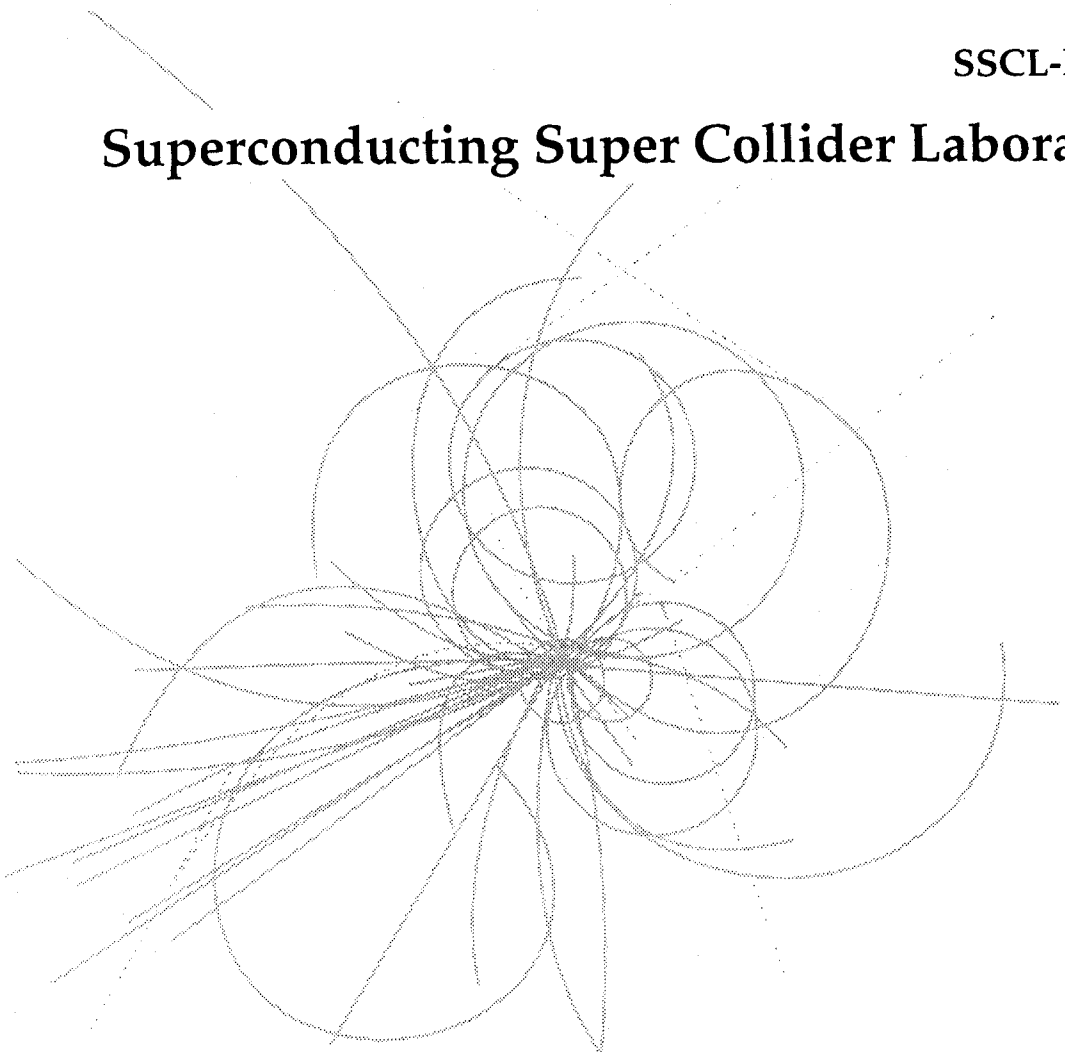

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*Operated by the Universities Research Association, Inc., for the U.S. Department of Energy under Contract No. DE-AC35-89ER40486.

VXIBUS BEAM POSITION MONITOR MODULE

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ABSTRACT

This is a description of a VXIbus Register Based Beam Position Monitor module. This module consists of a sealed analog module that outputs the sum and difference of the log signals for both the X and Y axis of the Beam Position Monitor (BPM). These signals are then digitized by 12-bit analog-to-digital converters. These digitized values are then stored in memory. A selectable number of these digitized values can also be averaged and stored. This will be particularly useful when close orbit information is required.

INTRODUCTION

A general purpose VMEbus[1] multi-channel digitizer board called the Quick Digitizer was design by Michael Shea of Fermilab and the author for use at Fermilab and at the Superconducting Super Collider Laboratory (SSCL). Because of the great acceptance of this module, it was decided to modify the basic design for the VXIbus.[2] The VXIbus format allows for the BPM analog circuitry[3] to be included on the board. VXIbus also allows for better noise shielding than VMEbus. The VXIbus BPM module was enhanced to include 32-bit data reads and writes, an interrupt, and averaging of up to 256 digitized values. The VXIbus BPM module is also software compatible with the Quick Digitizer.

BOARD DESIGN

The present design, shown in Figure 1, includes a sealed analog module, four digitizer-memory channels, four digitizer-averaging channels, the programmable trigger and digitizer clock logic, and the VXIbus interface. This design can use the 12-bit 1-MHz Datel model ADS-112, 12-bit 2-MHz Datel model ADS-117 or the 12-bit 5-MHz Datel model ADS-118 sampling digitizer with 128 k bytes (64 k samples) of memory for each of the four channels. The resulting board appears to the bus as a 512 k-byte-RAM card and a few registers in VXIbus register space for the trigger, digitizer clock, gate control and VXIbus configuration registers. Memory may be accessed from the VXIbus as bytes, words or long words. The registers may be accessed as bytes or words. Provision is made for using internal or external triggers, digitizer clocks and gate signals. This VXIbus module can optionally be dynamically configured.

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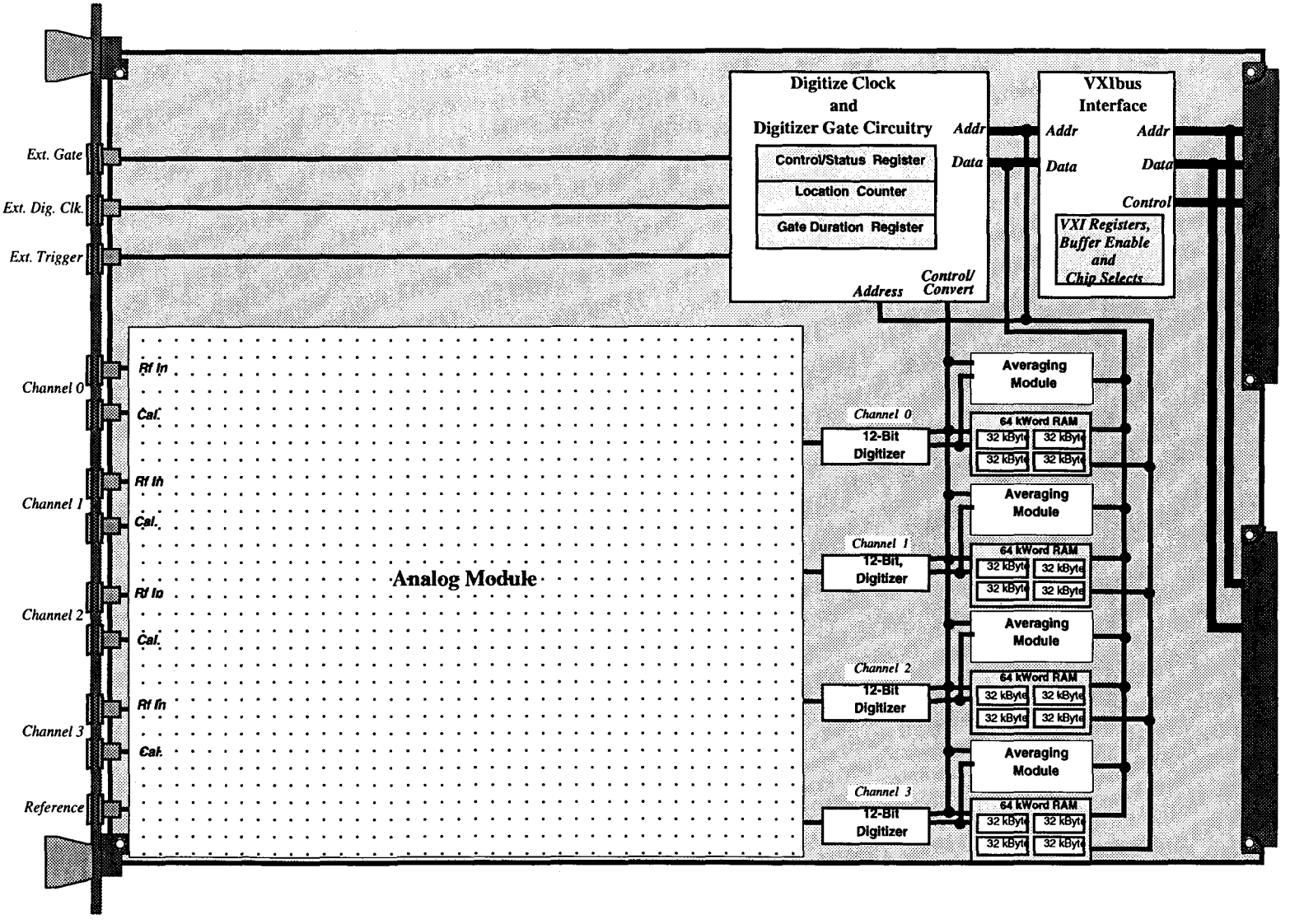

Figure 1. VXIbus Beam Position Monitor Module.

There are fifteen 16-bit status/control registers located in the VXIbus register space. The Digitizer Status/Control, Digitizer Location and Digitizer Gate Duration registers are the same as the Quick Digitizer registers.

VXIbus ID/Logical Address Register: A read of this register provides information about the device configuration. A write is defined by the optional Dynamic Configuration protocol of the VXIbus specification.

VXIbus Device Type Register: This register contains a device-dependent type identifier. The register contains the required memory size and the model code. The model code will not be implemented at this time.

VXIbus Status/Control Register: A read of this register provides information about the module status as defined in the VXIbus specification. A write causes specific actions as defined in the VXIbus specification.

VXIbus Offset Register: This read/write register defines the base address of this module A24 or A32 operational registers.

Digitizer Status/Control Register: This register selects the operating characteristics of the digitizer section of the module.

Digitizer Location Register: This register provides a pointer to the next data sample location to be filled with the digitizer data.

Digitizer Gate Duration Register: This register defines the number of conversions to be performed following a Trigger event.

The following registers are repeated for each of the four channels of digitization (sum and difference for both X and Y axis).

Averaging Status/Control Register: A write to this register enables and determines the number of digitized values to average (2,4,8,16,32,64,128,256). A read provides the status of the averaging(done) and the number of digitized values to average.

Average Register: A read provides the average of the digitized values.

OPERATION

Using the simple architecture described here several operating modes are possible, each of them defined by setting values into the above mentioned registers.

Normal Mode: In the Normal mode, digitizing begins at the external or the selected rate following a trigger and fills the number of memory locations given by the Gate Duration Register. The Auto-Reset bit of the Status/Control Register determines whether the location counter is reset by a trigger event. When the Location Counter is not reset, data following successive triggers is stored sequentially in memory until the memory is filled. If the Auto Reset bit is set, old data is overwritten by new data each time a trigger is received.

The Wrap bit in the Status/Control Register determines if the digitizer stops at the end of memory or wraps around and begins to fill memory at location zero. If the Wrap bit is not set and the memory has been filled, additional triggers are ignored so the host computer can process the captured data at its leisure.

Circular Buffer Mode: In this mode, the digitizer continuously fills memory and is stopped by triggering. As in the Normal Mode, the number of conversions that follow the trigger is given by the value stored in the Gate Duration Register. This allows the capture of data both before and after a trigger, and the trigger may be located at any point within the captured data set.

VXIbus Addressing: The module configuration and status registers are located within a 64-byte block in the A16 address space. The base address of the module registers is

determined by the module unique Logical Address. The Logical Address is the value set by an 8-bit switch and corresponds to bits 6-13 of the module register base address. Bits 14 and 15 of the base address are both 1 and the base address is

$$\text{Base Address} = V*40\text{hex}+C000\text{hex} \quad (1)$$

where V is the module Logical Address. As an example, if the Logical Address is zero then the Base Address is C000 hex in A16 space. If the Logical Address switch is set to all ones, then the Base Address of the module may be dynamically configured.

The 512 k RAM is additional registers in the A24 or A32 address space. The base address of the module's A24 or A32 registers is programmed via the Offset Register in the configuration portion of the module A16 registers.

Memory Map: The following memory map locations, Tables I and II are given in hex.

Table I Register Space
(A16 Space)

Base Address +	
20	Channel 3 Average
1E	Channel 3 Averaging Status/Control
1A	Channel 2 Average
18	Channel 2 Averaging Status/Control
16	Channel 1 Average
14	Channel 1 Averaging Status/Control
12	Channel 0 Average
10	Channel 0 Averaging Status/Control
0E	Digitizer Gate Duration Register
0C	Digitizer Location Register
0A	Digitizer Status/Control Register
08	Offset Register
04	Status/Control Register
02	Device Type Register
00	ID/Logical Address Register

Table II Memory Space
(A24 or A32 space)

Offset Register +	
40004	Channel 3 Data
40003	Channel 2 Data
40002	Channel 3 Data
40000	Channel 2 Data
04	Channel 1 Data
03	Channel 0 Data
02	Channel 1 Data
00	Channel 0 Data

This alternating channel's data allows for a thirty-two (32) bit (long word) read to acquire a word of data from each of two channels, giving the sum and difference of a single BPM axis.

Miscellaneous: This module can average 2, 4, 8, 16, 32, 64, 128, or 256 digitized values. The average is then stored in the Average Register. The number of digitized values to average is determined by the Averaging Status/Control Register. Averaging begins with the first trigger event after the averaging has been enabled.

The internal digitizing clock is derived from the VXIbus 16 MHz bus clock or from an optional onboard 20-MHz oscillator. After a divide by four, either this clock or the external clock may be selected as input to a 16-bit counter. Any one of the sixteen binary related frequencies can be selected as the digitizing rate by setting the bit number into bits 0.3 of the Status/Control Register. Frequencies of 4 MHz, 2 MHz, 1 MHz, 0.5 MHz,... for the 16 MHz clock and 5 MHz, 2.5 MHz, 1.25 MHz, 0.625 MHz,... for the 20 MHz clock are available. The analog input range is selectable 0-10 V or $\pm$5 V for the 1 and 2 MHz digitizers and $\pm$1 V for the 5 MHz digitizer.

This module can cause an interrupt. This will occur when then number of digitizations set by the Gate Duration Register has occurred or the averaging has completed. The level of the interrupt is determined by a switch. The vector returned is FF hex on the upper 8 bits of data and the logical address on the lower 8 bits of data, which corresponds to a "No Cause Given" interrupt as define by the VXIbus specification.

The VXIbus interface is controlled by an Interface Technology Chip (IT9010). The digitizer status and controls circuitry is contained in an Actel 1020 programmable gate array. Also the digitizer averaging circuitry is contained in an Actel 1020. Using the Actel chips, the functionality of the module is contained in parts that can be modified without changing the printed circuit board layout. This would allow for other analog modules to be used on this module.

REFERENCES

1. IEEE Standard for a Versatile Backplane Bus: VMEbus (ANSI/IEEE 1014-1987).
2. VXIbus Consortium, Inc., VMEbus Extensions for Instrumentation System Specification, Revision 1.3, July 14, 1989.
3. G. Roberto Aiello and Mark Mills, American Institute of Physics, Proceedings of the 1992 Accelerator Instrumentation Workshop.