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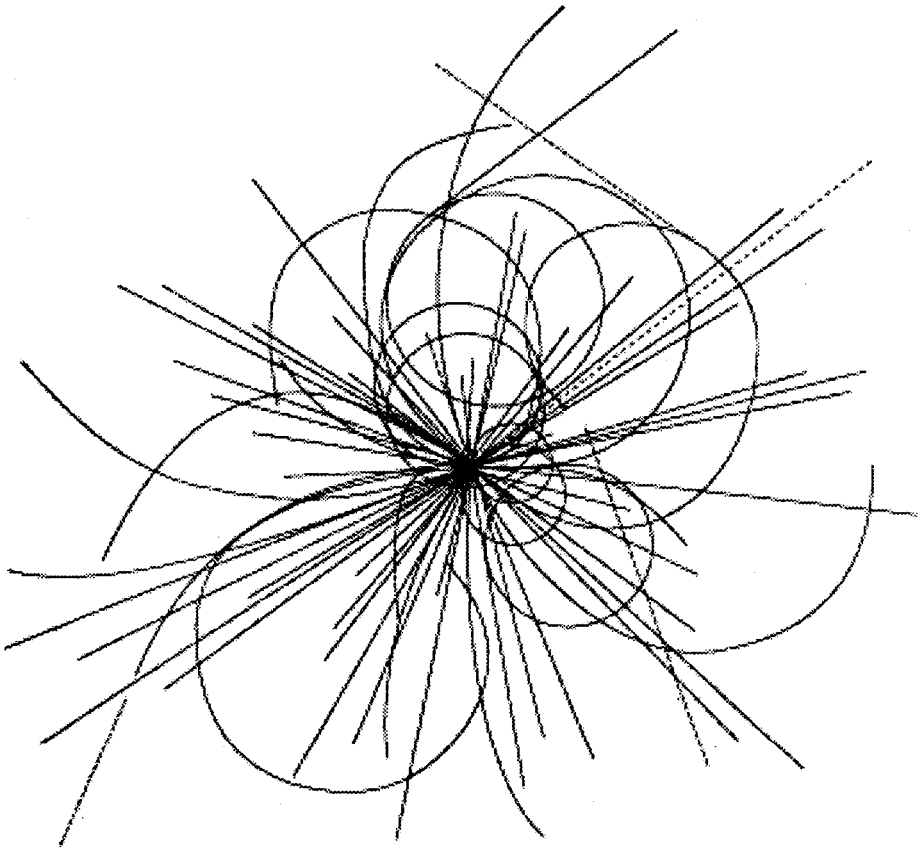
Low-Voltage-Swing CMOS Transceivers



Superconducting Super Collider Laboratory

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Low-Voltage-Swing CMOS Transceivers

G. Vanstraelen and J. Dorenbosch

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1.0 INTRODUCTION

This report gives a brief overview of two new transceiver techniques. The emphasis is on low power dissipation and low noise. Because commonly used techniques such as Emitter Coupled Logic (ECL) and Back Plane Transceiver Logic (BTL) are known to have a high power dissipation, they are not discussed in this article. Instead, two new techniques, named Gunning Transceiver Logic (GTL)[1] and Double Domino Transceiver Logic (D^2TL) will be discussed in detail. Table 1 compares the main characteristics of these four transceiver techniques. In calculating the power dissipation, the model shown in Figure 1 was used. For ECL and BTL the power should be increased with the dissipation of pre-drivers and biasing circuits. The original GTL was modified (MGTL) to give a signal amplitude of 100 mV. Table 1 shows how this reduction in signal level reduces the power dissipation.

In the next section, GTL will be discussed in more detail. For applications where considerations of crosstalk between data links are important, optimized line drivers are needed. Fully-differential drivers give the best result. For this reason a fully-differential version of the GTL driver is explained. Next, a novel driver, called Double Domino Driver or D^3 and used in D^2TL is explained in detail. This driver can be used in cases where low noise is of primary importance and where the noise may be reduced at the cost of speed. Additional features of D^3 are a smooth switching behavior, meaning a gradual turn on and turn off and a reduced output signal amplitude. A differential version of D^3 will be examined. The shape of the differential signal is shown in Figure 2.

In a final part, two types of receivers are discussed, a simple Operational Transconductance Amplifier (OTA) and an OTA with recovery feedback (OTA-RF). With a 3-V power supply, the recovery feedback improves speed from 5 MHz to 89 MHz! Where possible, theory is supported by experimental results obtained from prototypes fabricated in the 1.2 μm p-well Complimentary Metal Oxide Semiconductor (CMOS) from United Technologies Microelectronics Center (UTMC) UTE-R process.

TABLE 1. MAIN CHARACTERISTICS OF DIFFERENT TRANSCEIVER TECHNIQUES.

TECHNIQUE	TERMINATION	SIGNAL	POWER ON CHIP	POWER OFF CHIP
ECL	50 Ω, 3.0 V	0.8 V	35.0 mW	12.8 mW
BTL	50 Ω, 2.0 V	1.0 V	20.0 mW	20.0 mW
GTL	50 Ω, 1.2 V	0.4 V	6.5 mW	13.0 mW
MGTL, D^2TL	50 Ω, 0.0 V	0.1 V	2.8 mW	0.2 mW

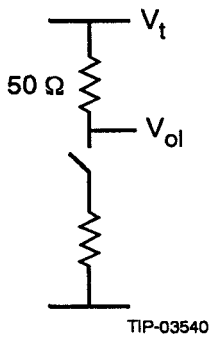

Figure 1. Model Used to Calculate the Power Dissipation.

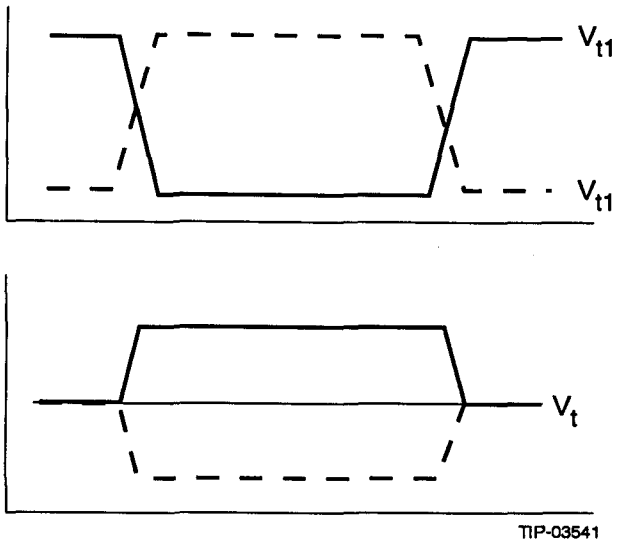

Figure 2. Standard and Modified Differential Signal.

2.0 GUNNING TRANSCEIVER LOGIC (GTL)

2.1 Introduction

Figure 3 shows the schematic for a (M)GTL type driver. For the setup shown in Figure 1, the turn on of the driver is damped by the termination resistance of the line and by the on-resistance of the driver. The turn-off action is undamped and this is what GTL tries to improve. If the input signal V_{in} is low, the driver is turned on. Transistor M2 is activated by a delay circuit formed by two inverters. When V_{in} turns high, M1 is switched on after an inverter delay, the output of the input inverter goes low and will turn off the driver. However, M2 is kept on because of the delay circuit. As a consequence, the feedback path formed by M1 and M2 will delay the complete turn off of the driver. This avoids a sudden change in current, di/dt, and will suppress voltage spikes due to parasitic line inductances.

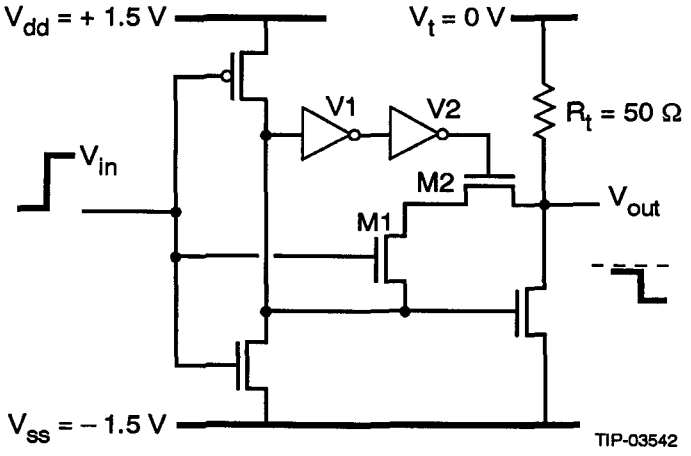

Figure 3. Schematic of a (M)GTL Driver.

Figure 4 depicts a simulation result for a MGTL driver operating on 3 V. Figure 5 shows the same curve for a driver without damped turn off. N_L and N_H are the noise on the low and high level, respectively. Both results are obtained for the bus model shown in Figure 6. In this model the inductance of the bonding wire bringing the signal on and off the chip was taken to be 5 nH. As can be seen, the noise performance is improved by using turn-off damping.

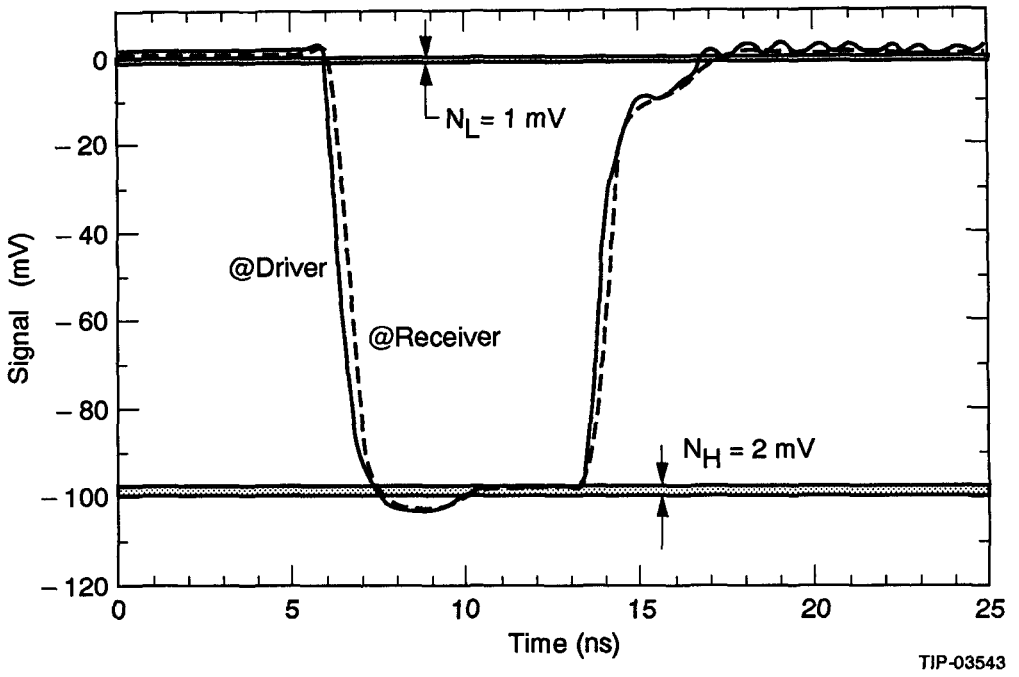

Figure 4. Output of a MGTL Driver for the Setup Shown in Figure 6.

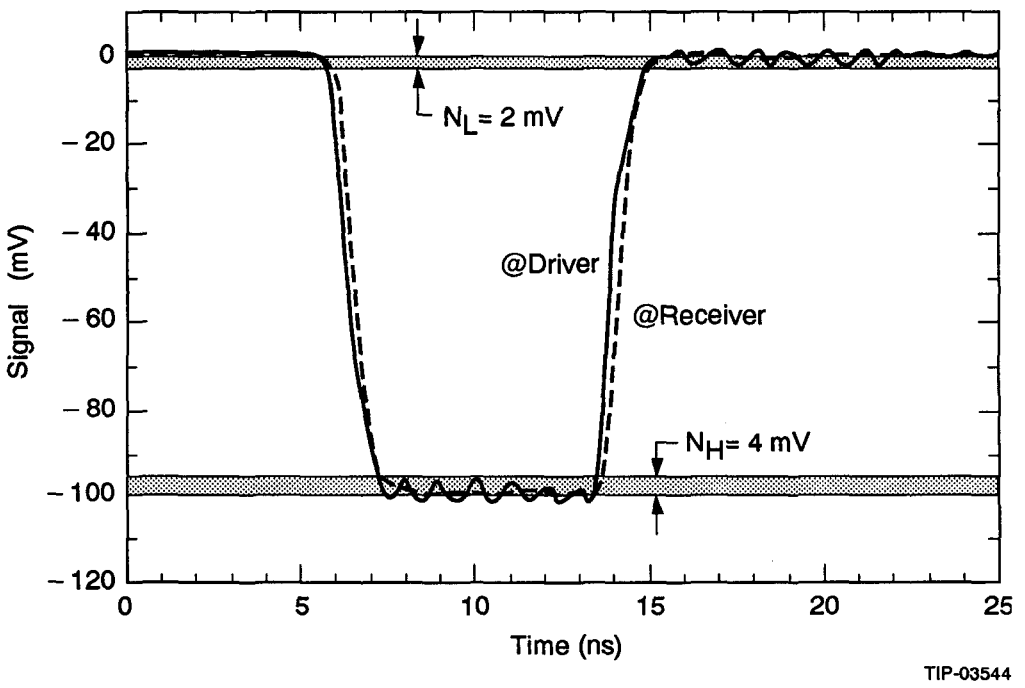

Figure 5. Output of a Driver without Turn-Off Damping for the Setup Shown in Figure 6.

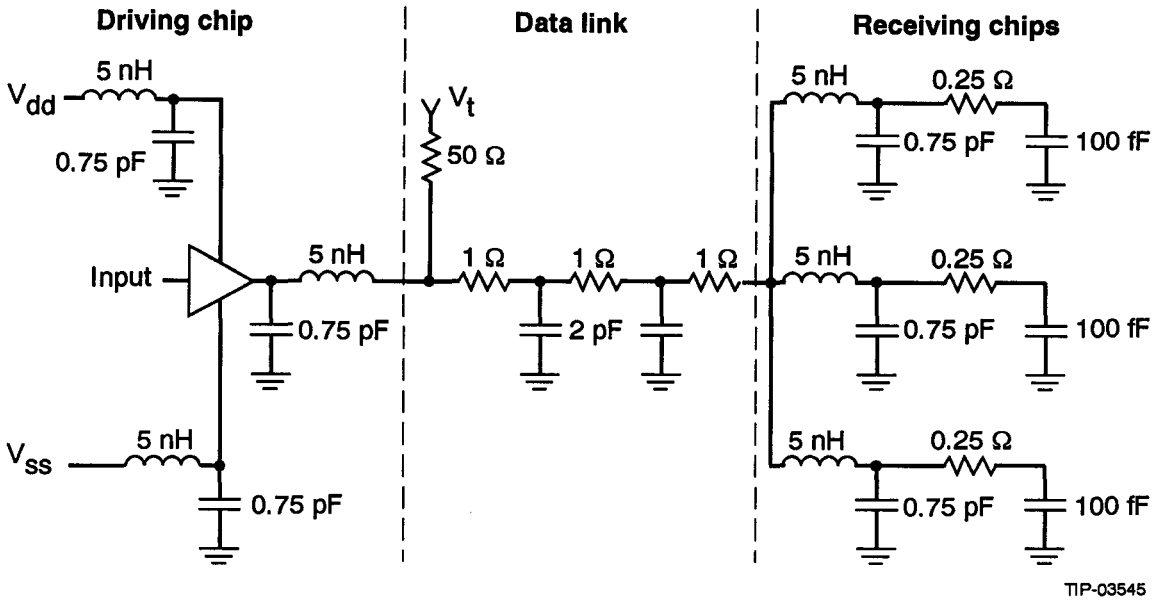

Figure 6. Driver Driving a Bus with Multiple Receivers.

The MGTL driver circuit can be made fully differential as is shown in Figure 7.

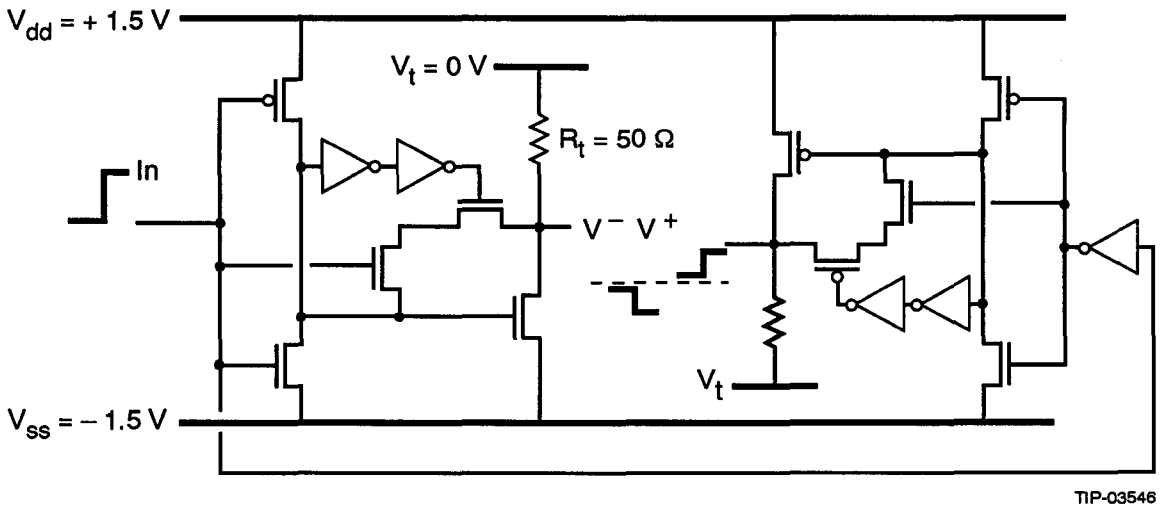

Figure 7. Fully Differential MGTL Driver.

2.2 Experimental Results

Evaluation of a prototype operating on ±1.5 V showed a n-driver delay of 1.8 ns with respect to the input signal and a delay of 1.68 ns for the p-driver output with respect to the n-driver output. The maximum operating frequency was found to be around 200 MHz.

3.0 DOUBLE DOMINO DRIVER* (D^3)

An important characteristic of a driver is the ringing caused by its sudden switching. This effect can be reduced by limiting the speed at which the current through the line inductance changes. The most straightforward way to accomplish this is shown in Figure 8 for a single-ended driver. Here several mini-drivers are turned on or off sequentially. Each mini-driver contributes a fraction of the total current that is needed to accomplish the signal amplitude, as such avoiding a too sudden, large change in current. A similar technique is used in D^3. However, the mini-drivers are switched on (or off) in two steps. During the first step, the devices are switched to an intermediate value halfway between being fully off and fully on. In the second step they are switched fully on. Switching off is done similarly, but in reverse order. This technique halves the number of drivers needed to accomplish a certain number of steps in the output wave form. The schematic for a fully-differential version of this driver is shown in Figure 9. The part providing the negative-going signal corresponds to the upper part, the part providing the positive-going signal corresponds to the lower part. The mini-drivers are switched on sequentially by means of an inverter signal propagated through a delay line. The delay line is built with CMOS transmission gates. The operation is as follows for the negative half (top half with n-channel drivers) of the differential driver. When the input of the inverter goes low, its output goes high and is fed into a delay line made up of CMOS transmission gates. A first voltage wave is propagated through the delay line using only the n-channel devices. As a result, the internal nodes and the output of the delay line are charged to V_{dd}-V_{Tn}, the positive supply voltage minus the threshold voltage of the n-channel devices. The node voltages change with an RC time constant determined by the driver gate capacitance and the impedance of the pass transistor. The output voltage of the delay line is used to generate a control signal that switches the p-channel pass transistors on. This voltage is shown in Figure 10 for both the delay line driving the n-channel drivers and the delay line driving the p-channel drivers. When this happens, a second wave propagates through the line and brings the voltage on the delay line nodes to the full supply voltage. This switches the n-channel drivers fully on. Table 2 gives the Carnaugh diagram for the functions that have to control the gate voltage of the delay line devices. It is easily recognized that the n-channel devices have to be controlled by a NAND gate, and the p-channel devices by a NOR gate. The same principle is used for the complementary driver circuit. In order to obtain a 100 mV voltage swing across a 50 Ω resistor, a total driver current of 2 mA is needed. Figure 11 displays the output signal of the circuit. The dashed line in this diagram corresponds to the voltage at the receiving end of the transmission line depicted in Figure 6.

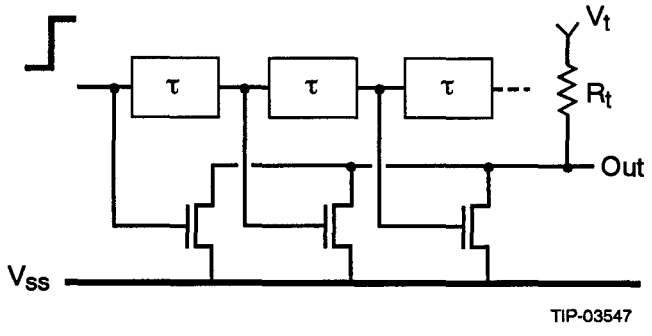

Figure 8. Method to Limit the Rise and Fall Time of the Output Signal.

*Patent pending

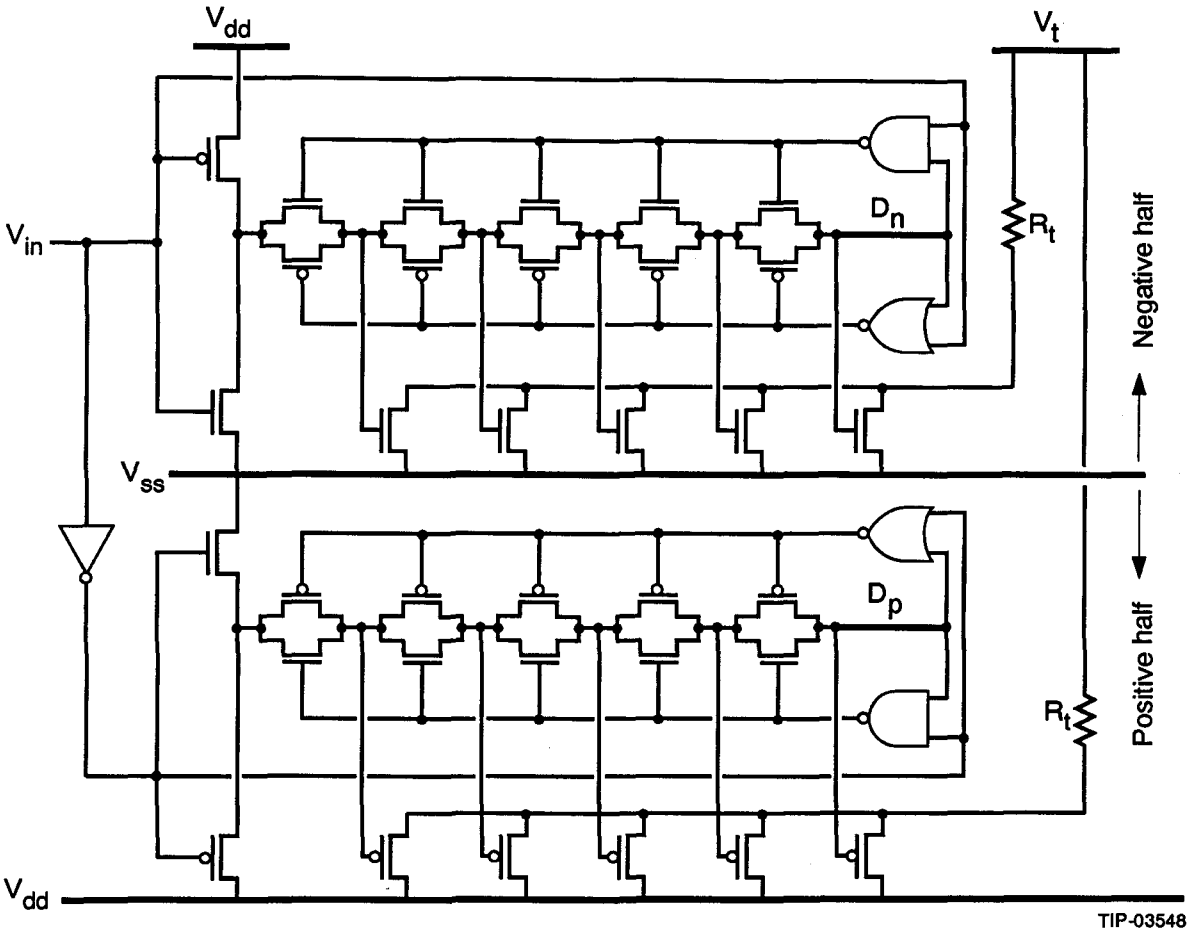

Figure 9. Fully Differential D²TL.

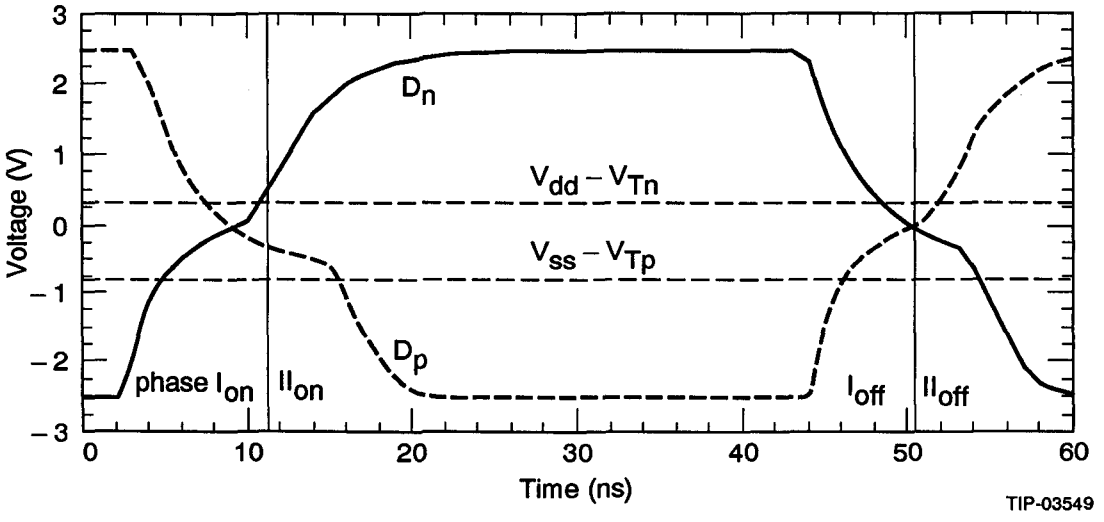

Figure 10. Voltage at the Output of the Delay Line Driving N-Channel and P-Channel Drivers.

TABLE 2. CARNAUGH DIAGRAM FOR THE FUNCTIONS CONTROLLING THE GATE OF N-TYPE (N) AND P-TYPE (P) PASS TRANSISTORS AS A FUNCTION OF THE INPUT SIGNAL IN AND THE DELAY LINE OUTPUT SIGNAL D.

n	D 0	1
in 0	1	1
1	0	0

$n = \overline{in \cdot d}$

p	D 0	1
in 0	1	0
1	0	0

$p = \overline{in + d}$

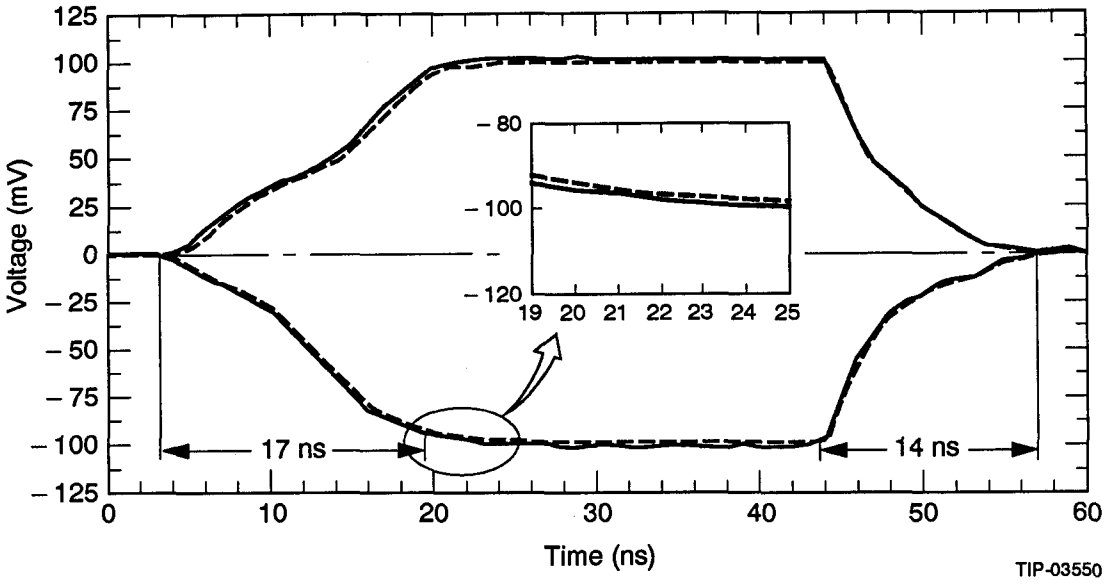

Figure 11. Output Signal for D³.

4.0 PARTY LINE PERFORMANCE

The noise on an unswitched driver is important because it will set the noise margins NM_l and NM_h for the reduced signal levels. A worst case exists for a situation shown in Figure 12. Here several tranceivers, each on a separate chip with bonding wires and capacitances according to Figure 6, are connected to the same bus. When one driver switches, its signal will be reflected by the capacitance of other drivers connected to the same signal line. The setup of Figure 12 was simulated using the software program HSPICE, both for MGTL and D²TL. Figures 4 and 13 show the result. The dashed line corresponds to the signal on the switched driver, the solid line is the voltage on an unswitched driver. It can be concluded that the ground bounce for the Double Domino Driver is in the microvolt range. The signal amplitude of 100 mV will certainly not be a problem.

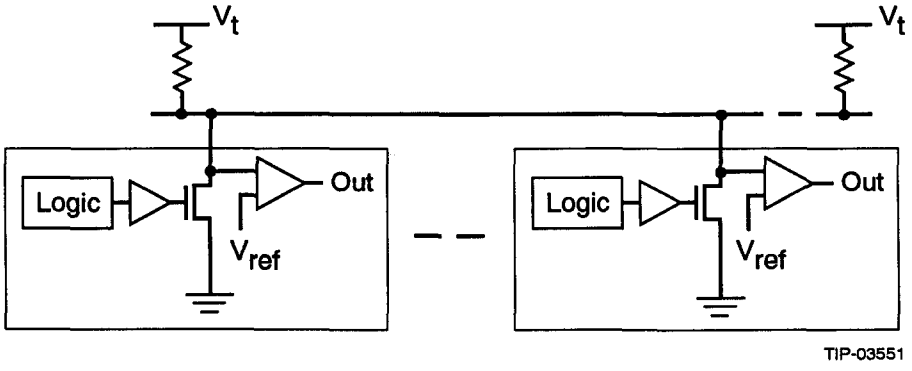

Figure 12. Worst Case Situation for Switching Noise.

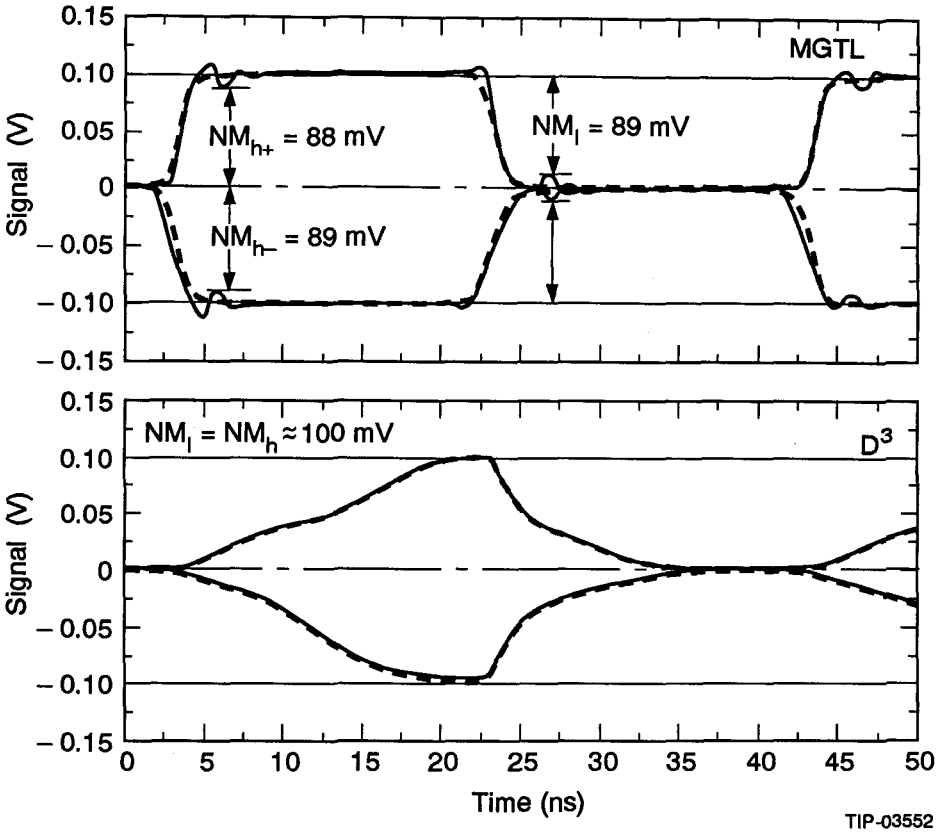

Figure 13. Output Signal for GTL and D²TL, used in the Setup of Figure 12.

5.0 RECEIVERS

This section will focus on two types of receivers. Both are basically comparators followed by an inverter stage to get a full voltage swing. The first type is the most simple and straightforward approach. It is based on an Operational Transconductance Amplifier (OTA)[1,2] and is depicted in Figure 14. A very well known disadvantage of OTA-type comparators is their limited speed and this is why often a differentiator is added. The limited speed is illustrated by the dashed line in Figure 15, showing the response as predicted by HSPICE. It is seen that the speed problem is mainly due to a poor recovery time. In this figure, 'comparator' is related to the comparator only, 'receiver' is related to the comparator including the output inverters. Using Figure 14, an explanation for this handicap is the following. When an input signal is applied, the input branch responds very fast. Its only pole is g_m/C_c, where C_c is the capacitance of the current mirror node C. The response of the input branch is passed on to the second branch, which also reacts very fast to the strong driving signal. When the input signals disappear, the input branch recovers fast. This means that there is no driving signal for the second branch any more, which can cause an extra output voltage recovering current to flow in this branch. The result is that only the very small deviation of the dc current flowing in the second branch is available for the recovery action. Consequently, recovery will take a long time. This situation can be improved by using a dynamic biasing of the output branch, as is shown in Figure 16. In this comparator, which is called OTA with Recovery Feedback* (OTA-RF), the extra device is also added to the input branch in order to keep a symmetrical structure. When a positive input signal is applied, the current mirror node C will show a negative signal. This affects the output and input branch in different ways. In the output branch,

*Patent pending

the signal will cause the output voltage to rise and since the latter is fed to the gate of the upper bias transistor, it reduces the current in the output branch. This will cause the output node to recover. In the input branch, the negative output voltage increases the bias current temporarily, such that the current mirror node C is helped to recover. The recovery feedback does not, as one could expect, kill the output signal or decrease the gain strongly. This is because the recovery feedback only reaches its maximum effect when the output signal is maximum. The solid line in Figure 15 illustrates the speed improvement brought by OTA-RF. Table 3 summarizes the main characteristics of both receiver types.

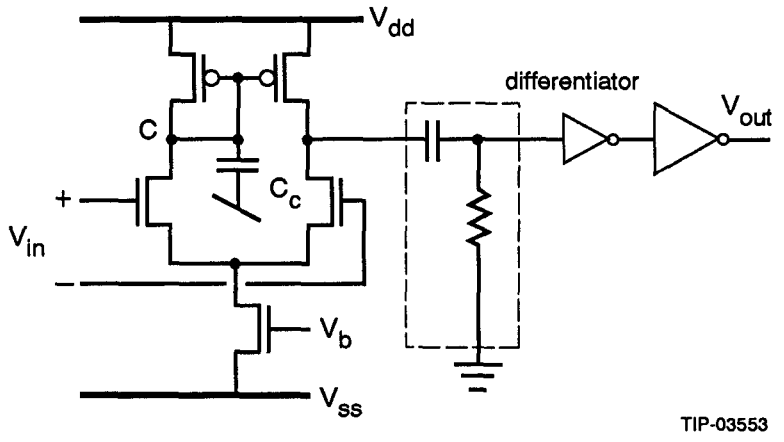

Figure 14. Receiver Based on an OTA.

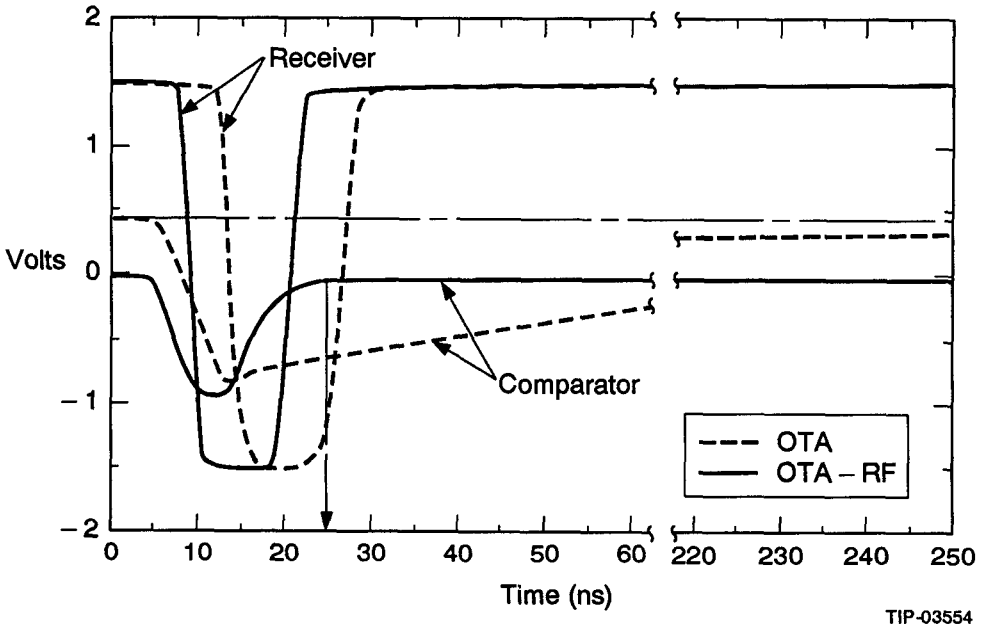

Figure 15. Output Signal of OTA and OTA-RF.

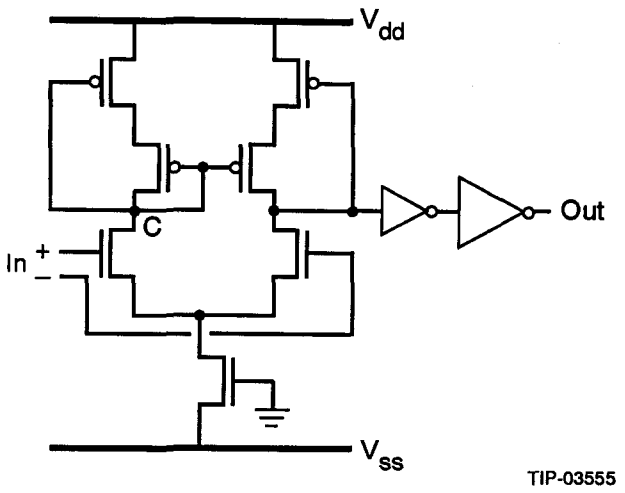

Figure 16. OTA with Recovery Feedback (OTA-RF).

TABLE 3. MAIN CHARACTERISTICS OF THE TWO RECEIVER TYPES.

	OTA (3 V)	OTA (5 V)	OTA-RF (3 V)	OTA-RF (5 V)
Power [mW]	0.132	2.72	0.666	5.3
f_{max} [MHz]	5	50	89	200

A slightly modified version of OTA-RF (Figure 17) was prototyped. In this circuit the gate of the current source is tied to the current mirror node. This is supposed to make the circuit performance less sensitive to process variations. The circuit was optimized for 3 V operation. Table 4 summarizes the simulated and measured characteristics. The simulation results show that compared with the original circuit the speed is decreased, while the power dissipation is increased.

Another important aspect of a receiver is its operation in the presence of a common mode signal. As the simulation result in Figure 18 shows, proper operation is guaranteed for common mode voltage in the range –0.66 V to 0.48 V.

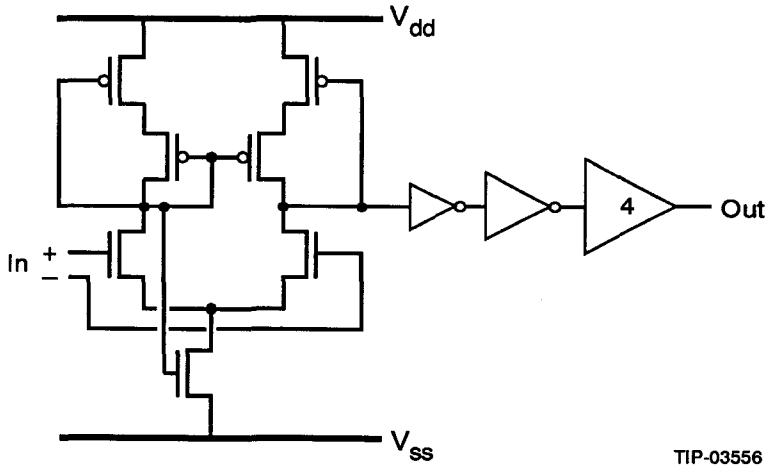

Figure 17. Slightly Modified OTA-RF.

TABLE 4. SIMULATED AND MEASURED CHARACTERISTICS OF THE MODIFIED OTA-RF.

	HSPICE		MEASURED	
Supply voltage	**3 V**	**5 V**	**3 V**	**5 V**
DC power [mW]	0.666	4.9	0.506	4.95
f_{max} [MHz]	62	100	62	51
Resolution [mV]	55	110	65	135
CMR [mV]	+800/–915	+150/–700	+480/–660	+150/–700
Delay [ns]	6.0*	6.0*	7.1	

*Output buffer not included.

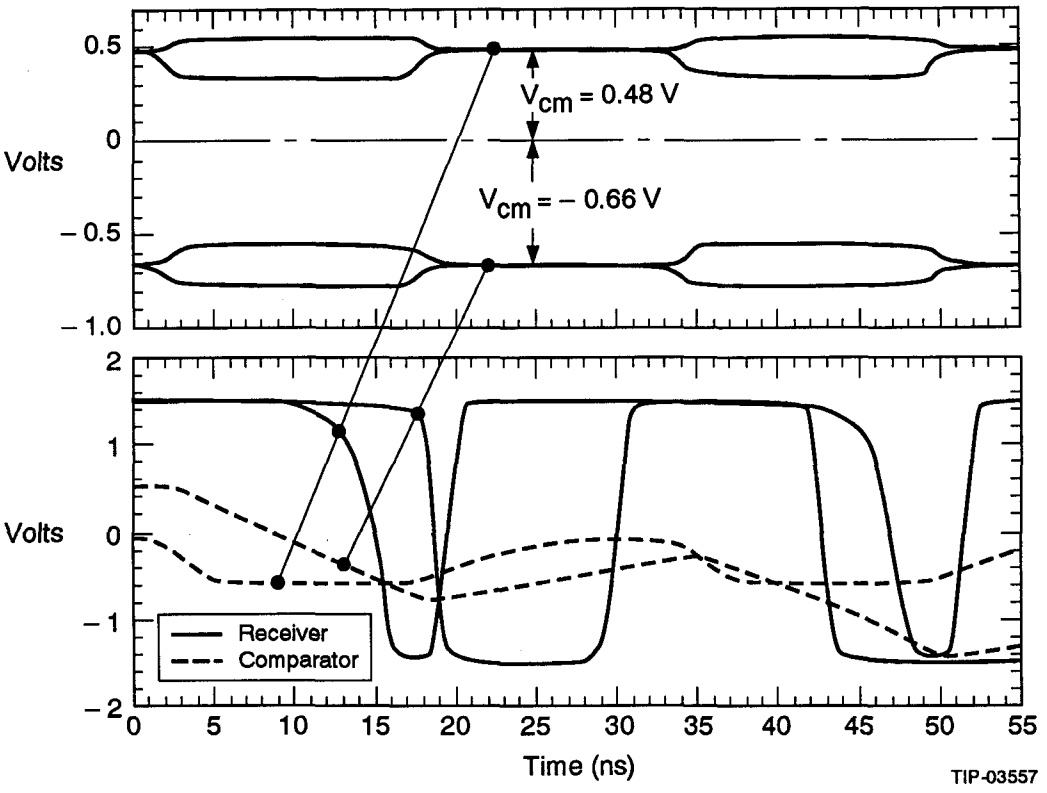

Figure 18. Effect of a Common Mode Voltage on OTA-RF.

6.0 CONCLUSION

Two recently developed data transmission techniques were analyzed, GTL and D²TL. For both techniques a signal amplitude of 100 mV was chosen. This was found to provide a sufficient noise margin for a reliable data transmission. Whereas GTL has fast rise and fall times and can be used for high speed data transmission, D²TL is optimized for low noise data transmission at the cost of speed. Both techniques have a much reduced power dissipation compared to the standard BTL and ECL techniques.

The poor recovery time of a standard OTA-type receiver, limiting its speed to 5 MHz @ 3 V, was improved by introducing recovery feedback. This resulted in OTA-RF, with a maximum operating frequency of 89 MHz. Its operation was verified with a prototype and a good agreement with HSPICE results was found.

Summarizing, for very high speed data transmission (80 MHz to 200 MHz), a combination of MGTL and OTA-RF should be selected, operating on a 5-V supply voltage. For the frequency range 50–80 MHz, 3-V MGTL and for the range 5–50 MHz either 3-V MGTL or 5-V D²TL is appropriate as driver, combined with OTA-RF as receiver. For the lower frequency range, 3 or 5 V D²TL combined with an OTA receiver

is suitable. The power dissipation of these techniques is summarized in Table 5. The standby power dissipation corresponds to the power dissipation of the comparator.

TABLE 5. POWER DISSIPATION FOR THE PREFERRED TRANSCEIVER TECHNIQUES.

	DRIVER	RECEIVER	POWER DISSIPATION [MW]		
			STANDBY	ACTIVE ON/OFF CHIP	
80–200 MHz	5 V MGTL	OTA-RF	5.3	10.1	0.2
50–80 MHz	3 V MGTL	OTA-RF	0.67	3.47	0.2
5–50 MHz	3 V MGTL	OTA-RF	0.67	3.47	0.2
5–50 MHz	5 V D^2TL	OTA-RF	5.3	10.1	0.2
< 5 MHz	5 V D^2TL	OTA	2.72	7.52	0.2
< 5 MHz	3 V D^2TL	OTA	0.13	0.1	0.2

ACKNOWLEDGEMENT

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