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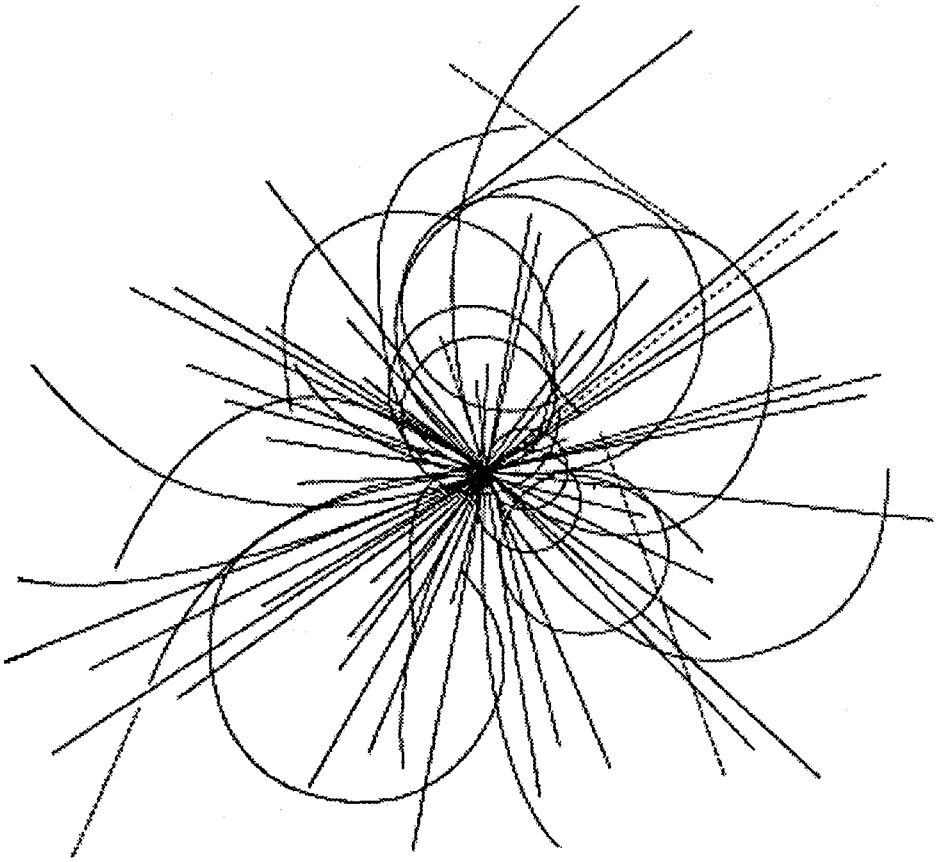

Superconducting Super Collider Laboratory

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Parasitic Experiments on Fermilab Booster LLRF Systems

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1.0 INTRODUCTION

This document gives a brief description of the hardware and software used to conduct the parasitic tests on the booster low-level-rf system at Fermilab. Parasitic tests included: (1) Measurement of the frequency curve while running the booster with and without beam; (2) Delay measurement in the phase loop; (3) Phase-locking the digital frequency source, Direct Digital Synthesizer (DDS), to the Voltage-Controlled Oscillator (VCO) and the beam signal; and (4) Study of the integrated phase error by tracking one bucket in the booster throughout the acceleration. These experiments were done to test the digital low-level-rf system considered for the Superconducting Super Collider (SSC) on an operating machine with beam. Some results of the experiment are shown at the end of the report.

2.0 LOOP DESCRIPTIONS

Several feedback loops are associated with the complete low-level-rf system. They are divided based on their functionalities. Generally, loops associated with the beam control are (1) beam phase loop, (2) radial loop, and (3) synchronization loop. The configuration of these loops can vary. Depending on the frequency source the implementation of the loop hardware can be digital or analog. Figure 1 shows a top-level block diagram of digital implementation for the loop configuration used on the Fermilab Booster. As we understand in the present booster beam control system, a VCO is used as the reference oscillator. The new system proposed for the experiment (see Reference 1) has a DDS in place of the VCO. The DDS uses a 1-Ghz clock to produce the frequency between 30 Mhz to 53 Mhz and a strobe signal to latch the data. Since the Synthesizer needs data in the form of a 32-bit binary word we have designed and developed the hardware using digital electronics. To produce the basic frequency ramp, the DDS data lines are interfaced to the Digital Signal Processor (DSP) #1.

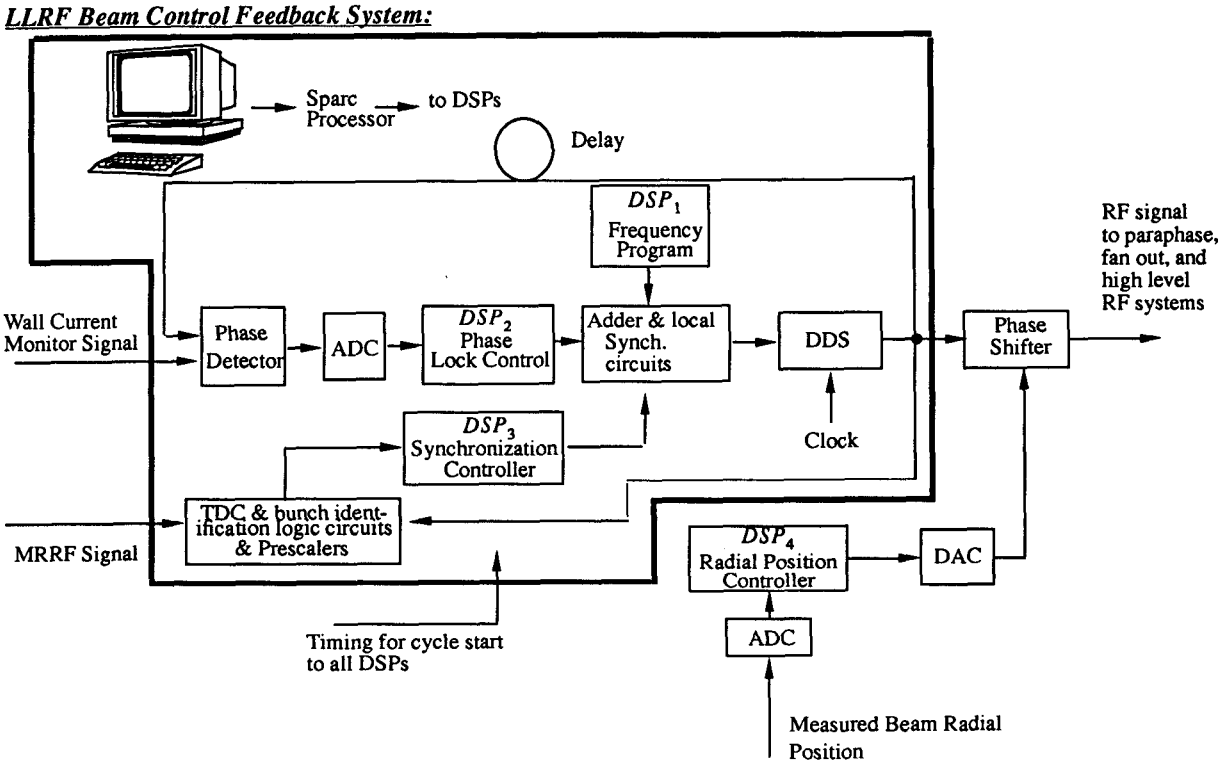


Figure 1. Schematic Loop Diagram of the New LLRF Beam Control System.

2.1 Beam Phase Loop

The beam phase loop has a Phase Detector, a 12-bit Analog-to-Digital Converter (ADC), DSP #2, and additional hardware with external adder circuits. The beam signal is compared with the Synthesizer rf signal through a delay cable in a beam phase detector. The beam phase is then digitized using the 12-bit ADC and the data is read into the DSP. The beam phase data is multiplied inside the Signal Processor by a time-varying gain (if needed). Additional filters or non-linear controllers (if found useful) are used in the Processor in real time. The ADC is sampled at multiples of the DDS strobe signal period. With the hardware we have used in the beam phase loop, a sampling period of less than 3 μs has been achieved in laboratory tests.

2.2 Synchronization Loop

The synchronization loop shown in Figure 1 has been designed to phase lock the DDS rf signal to the target machine rf signal with the target machine oscillator running at its injection frequency. Since we are using the hardware for tests at Fermilab we can name the target machine rf signal as the Main Ring RF (MRRF) signal. It is divided by the main ring harmonic number (1113) to generate the revolution markers. The revolution marker for the Booster rf signal is derived by dividing the booster rf signal by 84 in the bunch identification circuits. Two revolution markers are used as 'Ref' and 'Hit' for the Time-to-Digital Converter (TDC). A 20 ps TDC is used in the synchronization loop. The Booster revolution marker is produced by marking the appropriate bucket to track during the whole acceleration cycle.

Marking the bucket from the Booster rf signal is shown in the timing diagram of Figure 2. The start pulse in this figure is same as the TCLK. The TCLK is assumed to appear whenever there is beam in the ring. The first revolution marker from the MRRF signal after the TCLK is used to start counting the pulses from the Booster rf signal. After a known number of counts (say 40 or any bucket we want to identify) the rf signal is divided by the harmonic number, 84, to generate the revolution marker. This means we have identified a 40th bucket and are tracking at each revolution in the Main Ring. The TDC will output the time interval between two markers. The Signal Processor #3 will read the TDC data each time new data appears. The new data appears each time the revolution marker of the Main Ring rf signal appears (after the TCLK). In the synchronization DSP, this time interval is processed and then compared to the stored values. The data representing the error is then multiplied by a constant to produce the frequency shift on the adder interface circuits at the input end of the DDS. In this way, the hardware provides the ability to phase lock the Main Ring rf signal to the DDS rf signal. Time for closing the synchronization loop can be done at a predetermined count of the revolution marker from the MRRF signal.

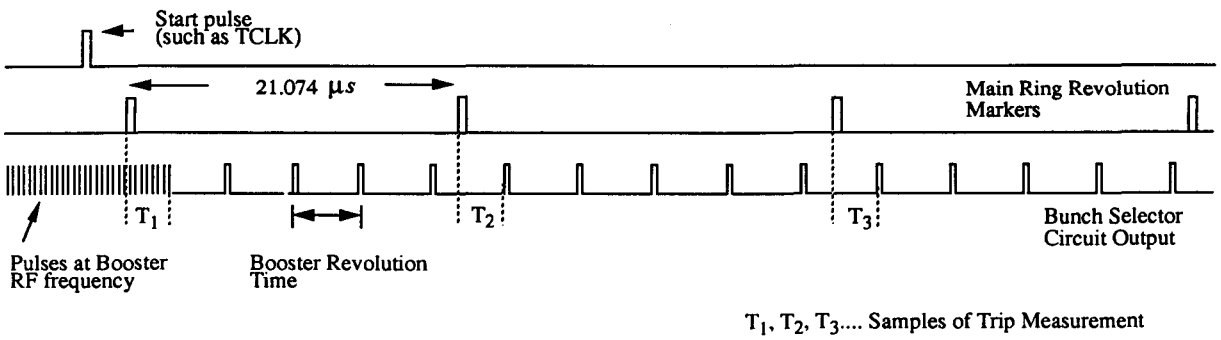


Figure 2. Top Level Timing Diagram of the Signals Used for the Synchronization Loop.

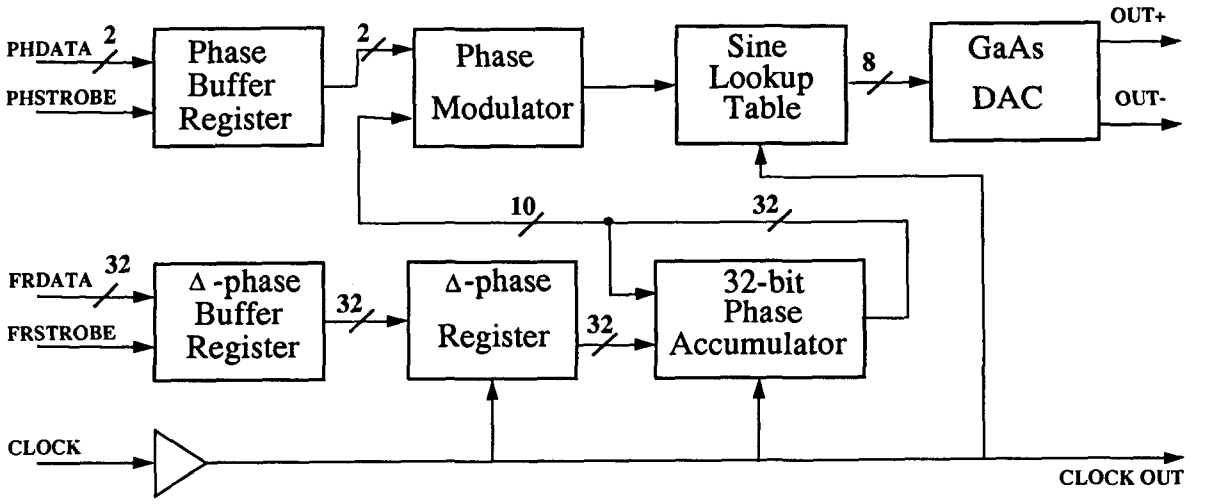
2.3 Radial Loop

The radial loop is configured similar to the booster beam control system. The radial position signal is digitized using a 12-bit ADC and is read into DSP #4. The radial position values are compared with the desired reference data inside the signal processor. Resulting data is multiplied by the time-varying gain and then converted to phase values by going through a lookup table for the phase shifter. In this way the radial loop is producing a phase modulation of the DDS signal. However, a more simplified approach is to perform frequency modulation at the input end of the DDS at a much lower sampling rate than the beam phase loop. This can be easily accommodated in the future, if needed. For preliminary beam studies, it is wise to use only the DDS-based beam phase loop and Fermilab radial loop.

3.0 EQUIPMENT DESCRIPTION

3.1 Direct Digital Synthesizer

We are using a GaAs Modulated Direct Digital Synthesizer, STEL-2173, from Stanford Telecom. This synthesizer block diagram is shown in Figure 3. We run the synthesizer with a 1-Ghz clock for a frequency sweep between 30 Mhz to 53 Mhz in 33 ms. We have done a number of tests in the Laboratory to prove that the source has no phase discontinuity. However, the best test would be to try with the beam itself. The device uses 32-bit data and has a sine wave output with better than –40 dBc spurious noise. DDS frequency resolution is 0.232 Hz. Frequency data is updated at 1.56 μs from the DSP.



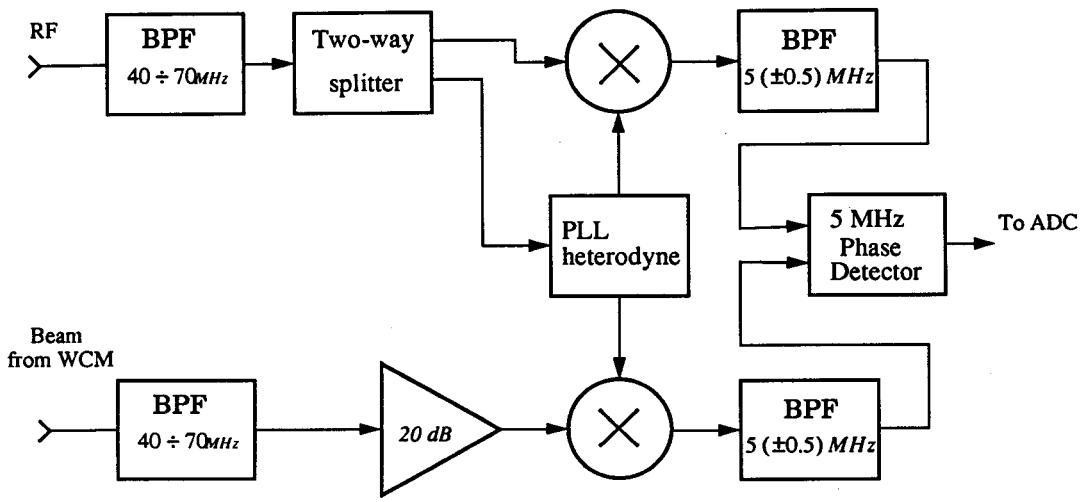
Features:

- **FREQUENCY RANGE:** 5 kHz to 400 MHz @ 1 GHz clock
- **RESOLUTION:** 0.233 Hz (32 bits) @ 1 GHz clock
- 2-bit PHASE MODULATION
- PHASE COHERENT INSTANTANEOUS FREQUENCY SWITCHING
- SWITCHING SPEED: 62.5 MHz (delay - 25 ns) @ 1 GHz clock

Figure 3. Direct Digital Synthesizer, STEL-2173.

3.2 Beam Phase Detector

Figure 4 shows the schematic layout of the beam phase detector which has two parts, the Phase-Locked Loop heterodyne circuits and a 5-Mhz phase detector. Heterodyne circuits are designed to convert the 30-Mhz to 53-Mhz-input frequency to the 5-Mhz-intermediate frequency so that the phase detector circuits will operate at a fixed frequency. A VCO is used in the Phase-Locked Loop (PLL) heterodyne circuits.



Features:

RF bandwidth ..... 30 MHz
IF bandwidth ..... 1 MHz
LF bandwidth .....30 kHz
Beam input dynamic range ..... 20 dB ($\Delta\varphi \leq 2^{\circ}$)
Bunch shape sensitivity ..... not noticeable.

Phase range ..... $0 \div 2\pi$
Nonlinearity ..... $\Delta\varphi \leq 5^{\circ}$

Figure 4. Beam Phase Detector.

3.3 Adder and Local Synchronization Circuits

Figure 5 shows the block diagram of the 32-bit adder and local synchronization circuit board which was designed and developed to work like an interface board between the DSP and DDS or DSP-ADC/TDC and DDS. There are latches, buffers, tristate logic and 32-bit adder circuits. Also, local synchronization circuits on this board will synchronize the feedback DSP data with the DDS strobe. This part is essential to make sure that the feedback data is added synchronously with the frequency ramp data just before the strobe appears on the DDS.

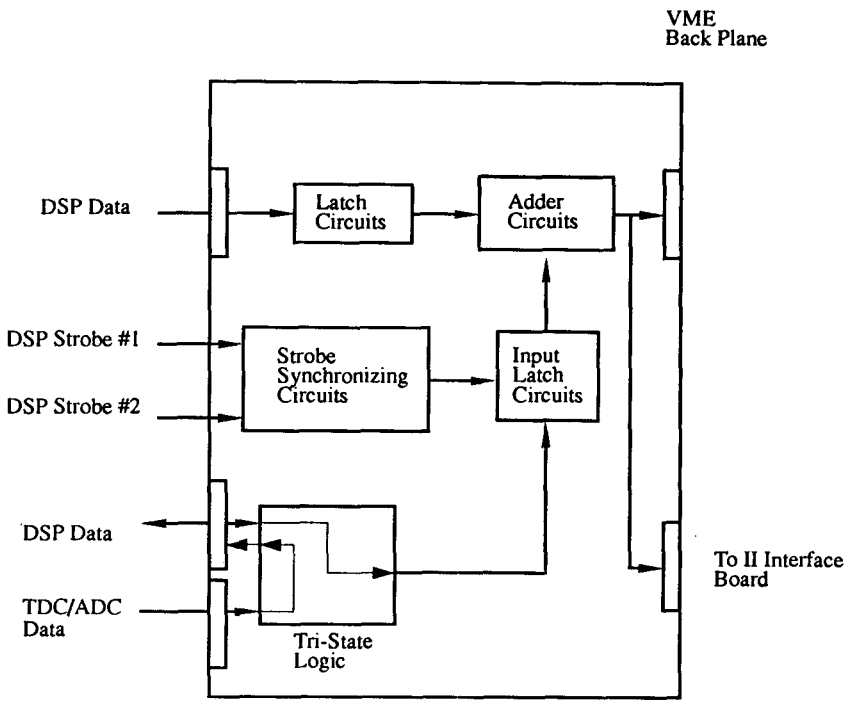


Figure 5. Adder and Local Synchronization Circuit Board (DSP-DDS Interface Board).

3.4 Digital Signal Processor

Figure 6 shows the schematic of the DSP board that is manufactured by Sky Computers. It has two 32-bit floating-point TMS320C30 signal processors from Texas Instruments. It has 2 Mbytes of global DRAM shared by both the C30 processors and the usual control registers to interface with the VME bus. There are, however, 64 Kwords of Static RAM available for each C30. When we use one C30 for ramping the frequency, the Static RAM is loaded with the frequency table. Since the static memory is linked to the processors with zero wait state we could launch data to the DDS at a rate faster than 500 Khz. A UNIX-based Sparc 1e processor is used to develop the DSP software. All the communication to the UNIX workstation is done via the VME backplane interface. More information on the DSP board is available in Reference 2.

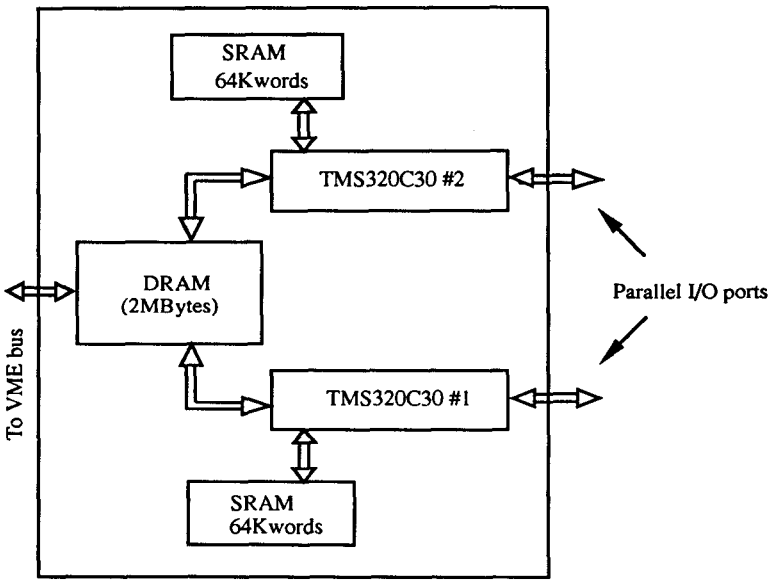


Figure 6. Digital Signal Processor Board.

3.5 Time-to-Digital Converter

A 20-ps resolution, 32-bit, TDC is used for the time interval measurement between two markers in the synchronization loop. The TDC is built by Highland Technology, Inc., on a CAMAC platform. It accepts one pulse edge as a time reference and another pulse as a 'hit' signal. The module reports the time-of-hit measured relative to the reference edge in less than 200 ns after the 'hit' edge has appeared. The theory of operation of the device is explained in Reference 3.

3.6 Bunch Selector Circuits

The primary function of the circuit is to generate the 'hit' timing signal of Figure 2 for the TDC. Figure 7 shows the block diagram of the internal functional blocks. The harmonic number is selected at 84 in our experiment. TCLK signal is used to reset the counters before the start of the next cycle. The veto delay circuit is sometimes used to prevent reading of negative time from the TDC. A veto delay of less than a nanosecond would be sufficient.

Figure 8 shows a block diagram of the synchronization and beam phase loop. The hardware components described above are shown as blocks with inputs and outputs. These lines represent the digital data lines.

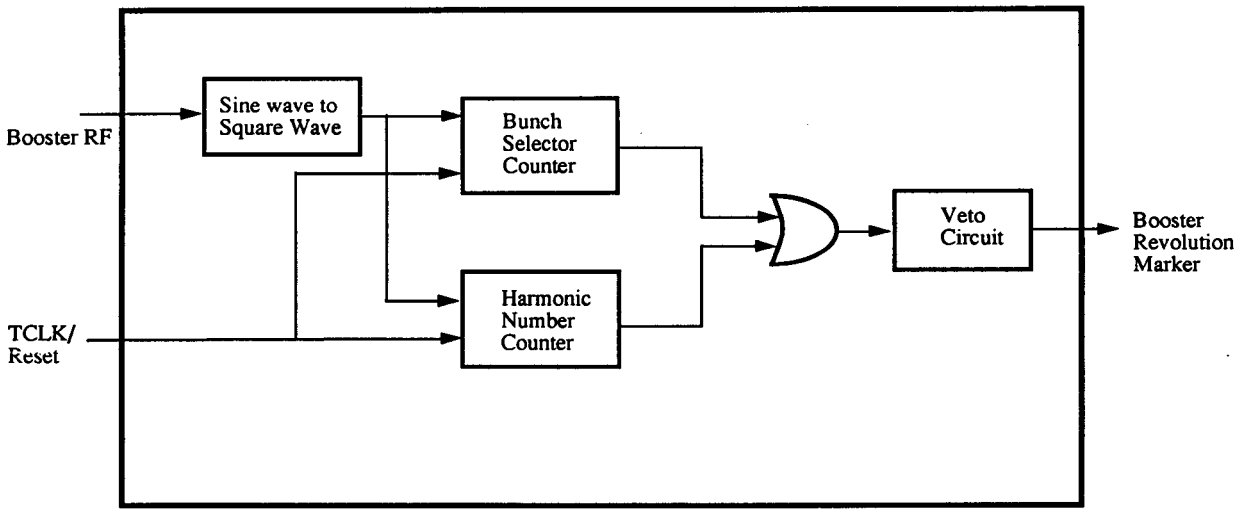


Figure 7. Bunch Selector Circuits.

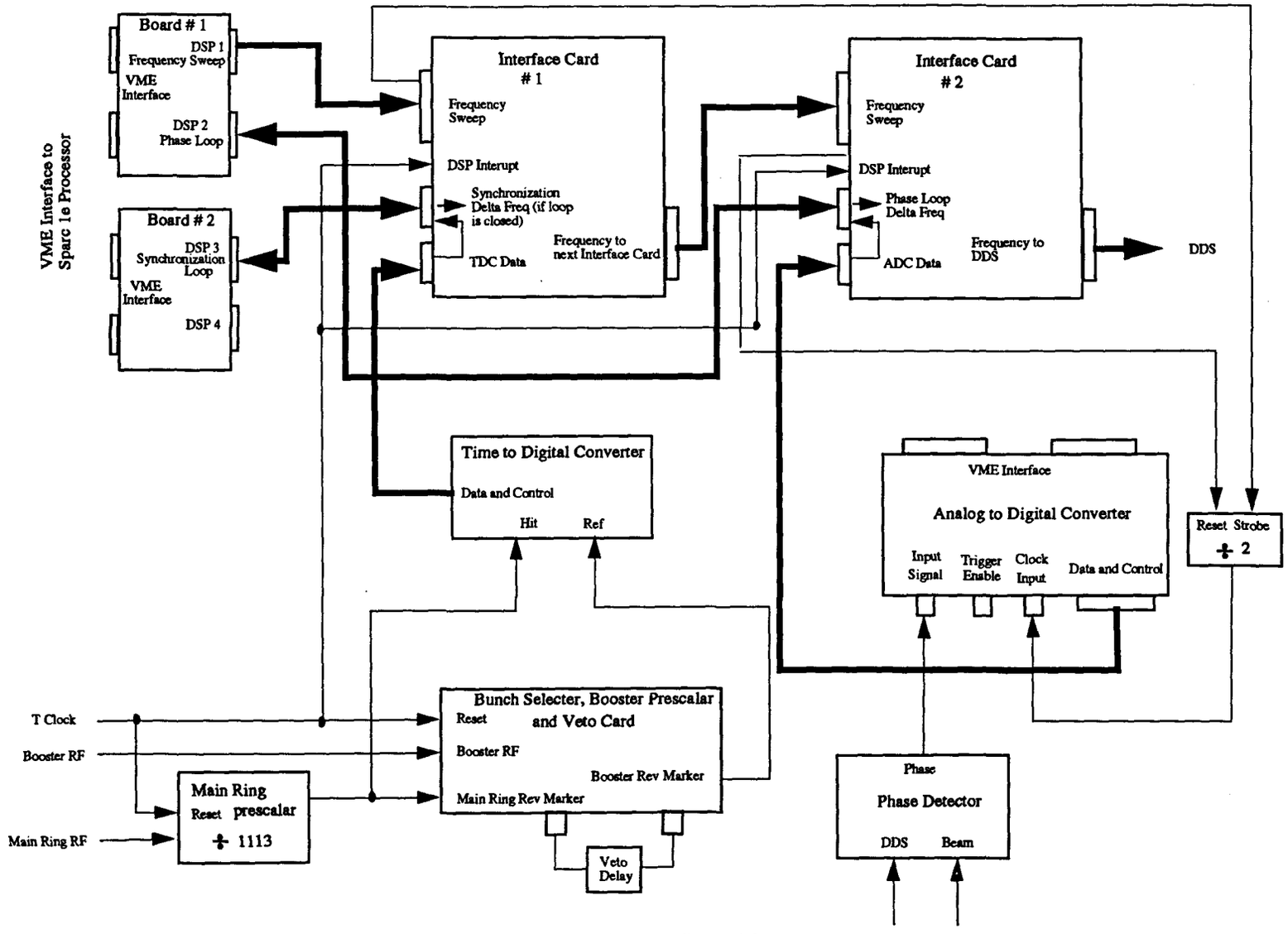


Figure 8. Integrated System Block Diagram.

4.0 DESCRIPTION OF THE SOFTWARE

There are many software routines we have written over the years while developing the system. In this document we describe the flow charts of only those programs used on real time inside the DSPs pertaining to the parasitic tests. All the real time software used in the DSP are coded in C30 assembly language. To understand the actual source, one needs familiarity with the C30 software and Sky DSP board architecture. In Reference 4 we have shown some C30 literature from Texas Instruments. In addition to the assembly codes we have several FORTRAN codes used off-line to compute the frequency curve, process trip data, track particles, *etc.*

4.1 Frequency Ramp Program

Figure 9 shows the flow chart of the frequency ramp program. As we can see in the flow chart, immediately after the TCLK appears, the internal timer in the DSP will start counting up to 1.56 μs. After this first time event the DSP will pull the first value from the frequency ramp table and down load to the adder circuit board. Again the loop will wait for another 1.56 μs and pull the second value after the event has taken place. Thus the loop continues until the end of the table. After completing all the values the DSP will wait for the next TCLK.

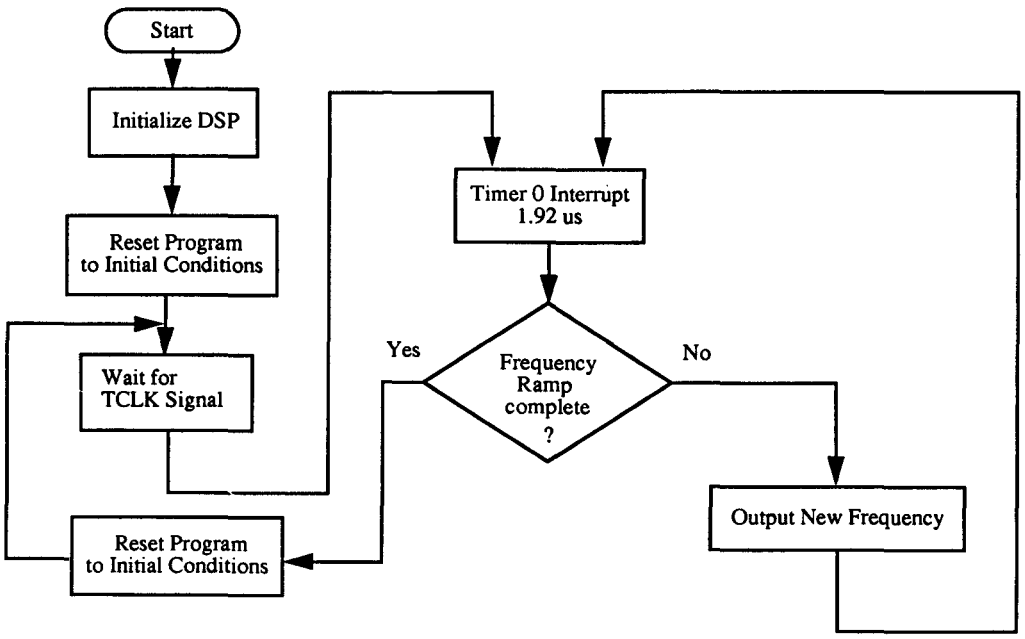


Figure 9. Flow Chart for Frequency Ramp Program.

4.2 Beam Phase Loop Program

Figure 10 shows the flow chart for the beam phase loop program. This program is quite simple and involves limited instruction cycles. Since the ADC is sampled after the TCLK, we poll inside the phase loop DSP for the first data from the ADC, read the ADC data, and provide correction to the ramp DSP data. The correction is done by multiplying the ADC data with a constant stored in the DSP or filtering (if necessary) and then launching the new data on the adder circuits. The process of taking data and adding corrections will continue. Since the ADC is supplied with an external sample clock, the DSP will count each sample take after the TCLK. After a predetermined number of counts it will output zero frequency to the adder circuits and wait for the next cycle to begin.

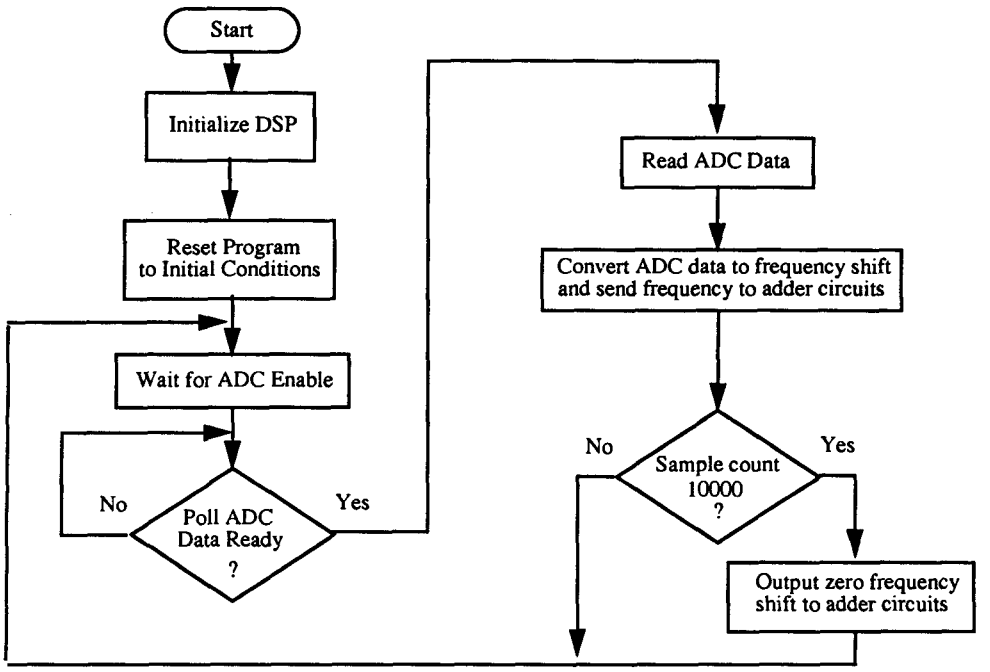


Figure 10. Flow Chart of the Phase Loop Program.

4.3 Synchronization Loop Program

We have written several programs for the synchronization loop. Figure 11 shows the flow chart of a simplified and straightforward program. This program is used for the 'trip' measurement. In the parasitic studies since the synchronization loop was not closed the flow chart of the closed-loop program is not shown. Again, the synchronization DSP will poll for the TDC data after the TCLK. The data is stored in the DSP memory on line for up to 2000 main ring revolution counts. The data is read into the Sparc 1e memory from the DSP with a separate program.

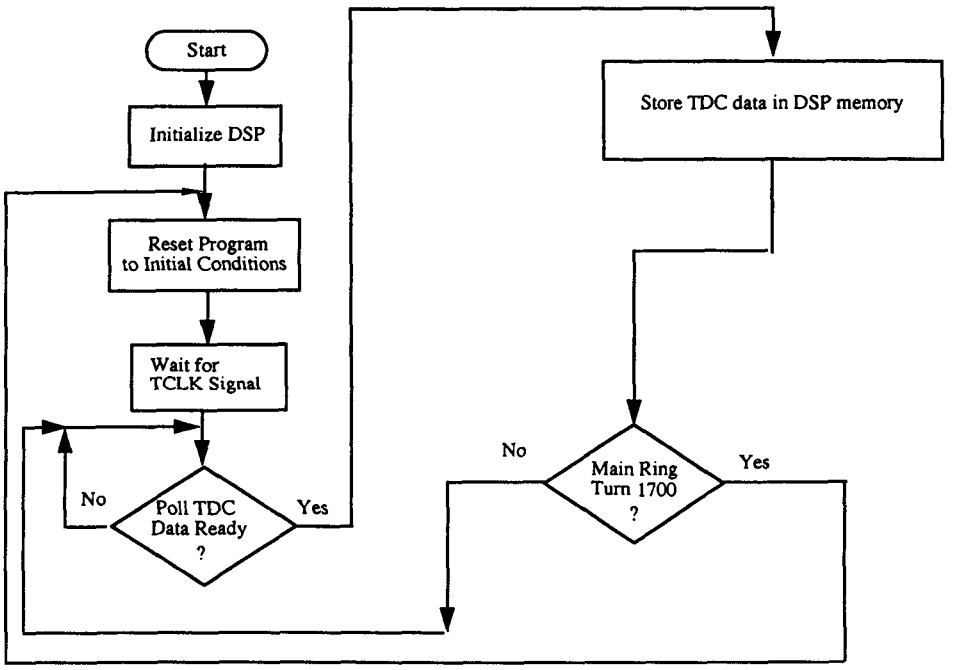


Figure 11. Flow Chart of the Program used for 'Trip' Measurement.

5.0 PARASITIC TESTS ON THE BOOSTER AND RESULTS

Several parasitic tests were conducted on the booster low-level-rf system. They were done mainly to study the capabilities of the new digital low-level-rf system. Some of the important results are reported below.

5.1 VCO Frequency Measurement

Since the DDS is required to sweep from 30 Mhz to 53 Mhz and then back to 30 Mhz in one cycle, we attempted to measure the VCO frequency ramp using the time interval (known as 'trip') obtained from the TDC. The curve is shown in Figure 12 for the 'trip' measurement of Figure 13. The X-axis represents the revolution numbers of the Main Ring markers after the TCLK. Figures 14, 15 and 16 show the frequency curves with expanded axes. Clearly, the peak-to-peak frequency error is under 1 Khz, which is effectively related to the TDC jitter combined with the VCO error. Figures 12 through 16 are shown for no beam condition. The synchronization loop locking the booster VCO with the Main Ring Synthesizer may have been disconnected at the time of recording these values.

The trip measurement with the beam in the booster is shown in Figure 17. Four lobes at the end correspond to the fraction in the ratio of the harmonic numbers (1113/84) and shows that the booster VCO was locked to the Main Ring Synthesizer.

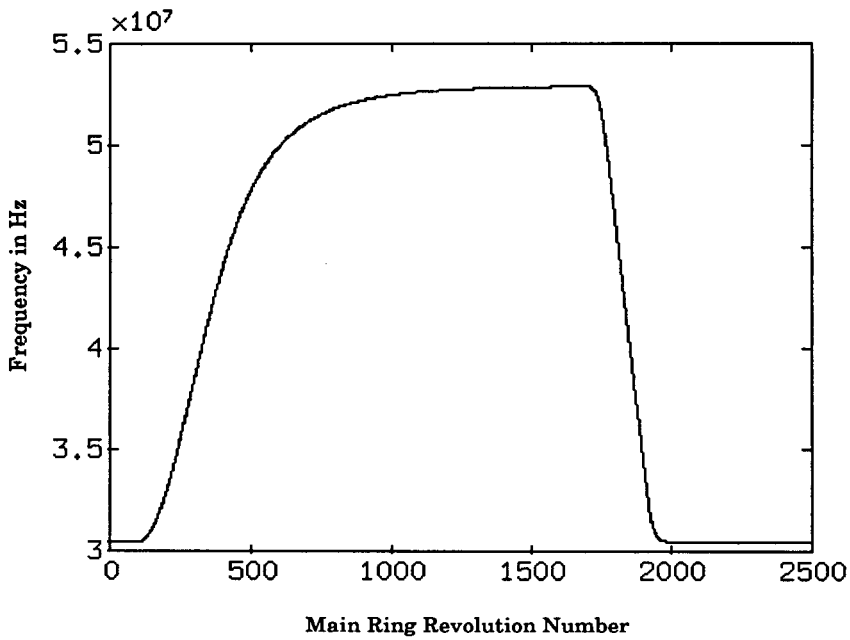


Figure 12. Frequency Ramp Calculated from the Trip Measurement of Figure 13.

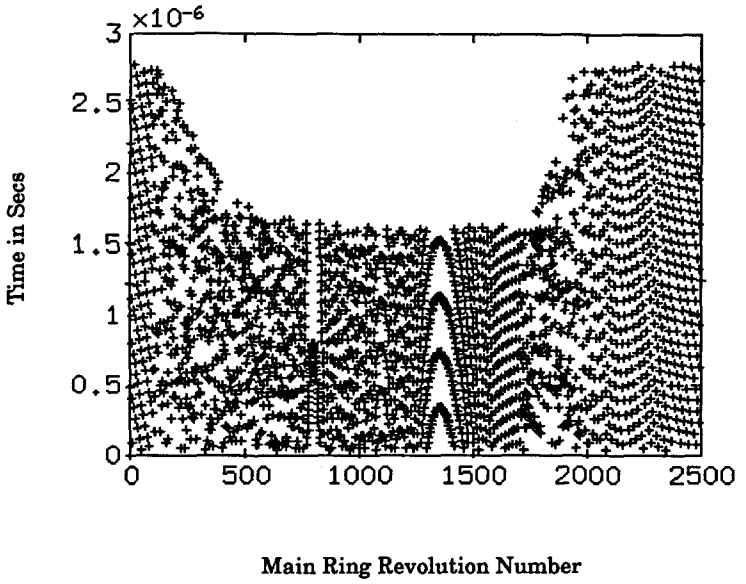


Figure 13. Booster Trip Data without Beam (and No Synchronization Loop On).

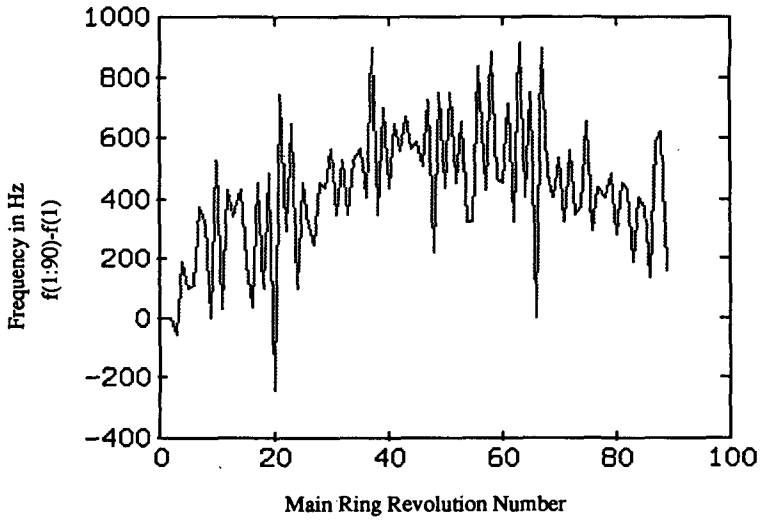


Figure 14. Frequency v/s Main Ring Revolution Count.

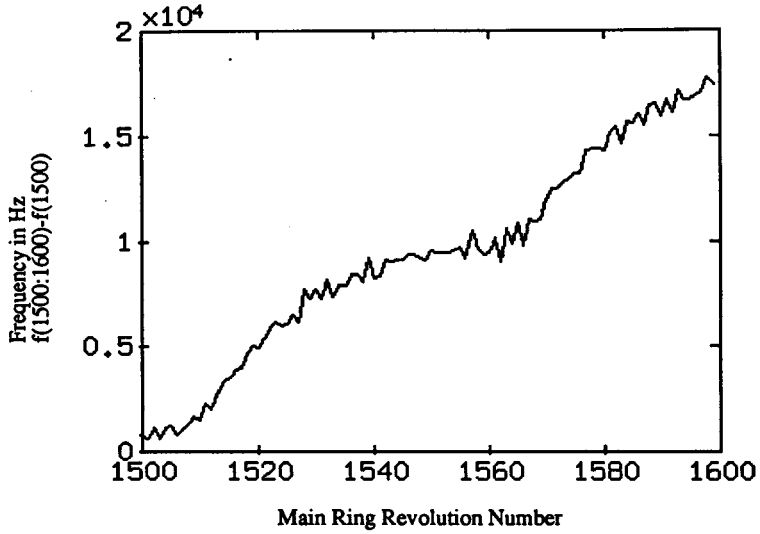


Figure 15. Frequency v/s Main Ring Revolution Count.

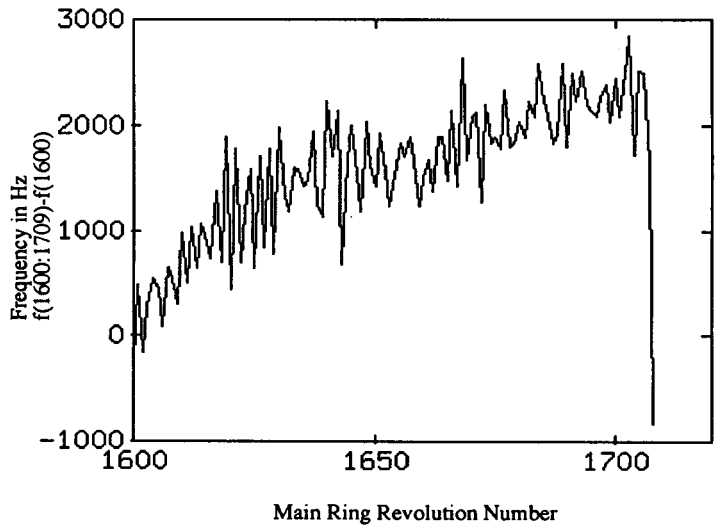


Figure 16. Frequency v/s Main Ring Revolution Count.

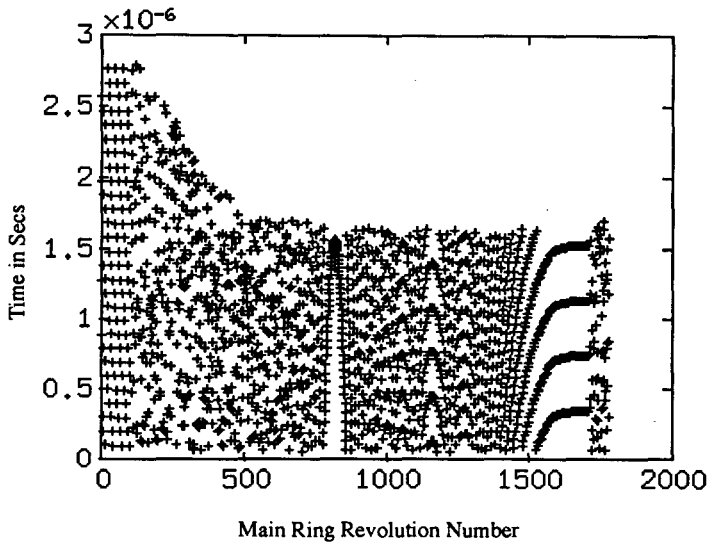


Figure 17. Trip Measurement with Beam in the Booster.

5.2 Measurement of the Cable Delay in the Beam Phase Loop

The configuration shown in Figure 18 was used to measure the cable delay in the beam phase loop. The VCO and the beam signal were used as two inputs to the beam phase detector. The output of the phase detector was compared to the booster beam phase detector signal, FPERR. The cable is trimmed until two signals appear similar. Our measurements showed the cable delay as 1.4 μs. Figure 19 shows the two signals.

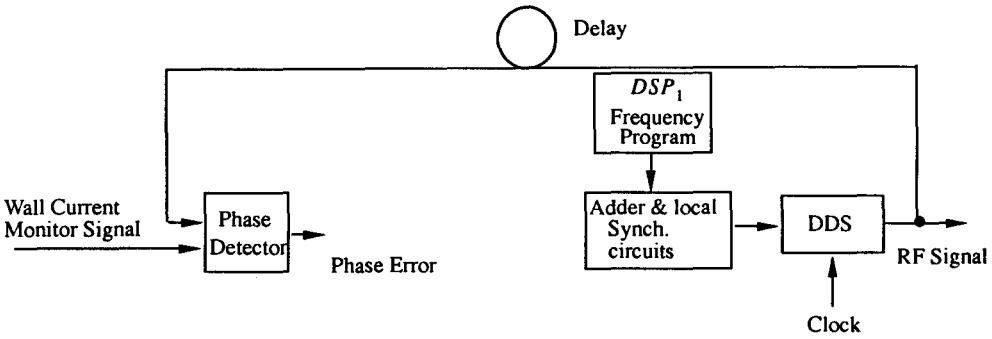


Figure 18. Cable Delay Measurement System.

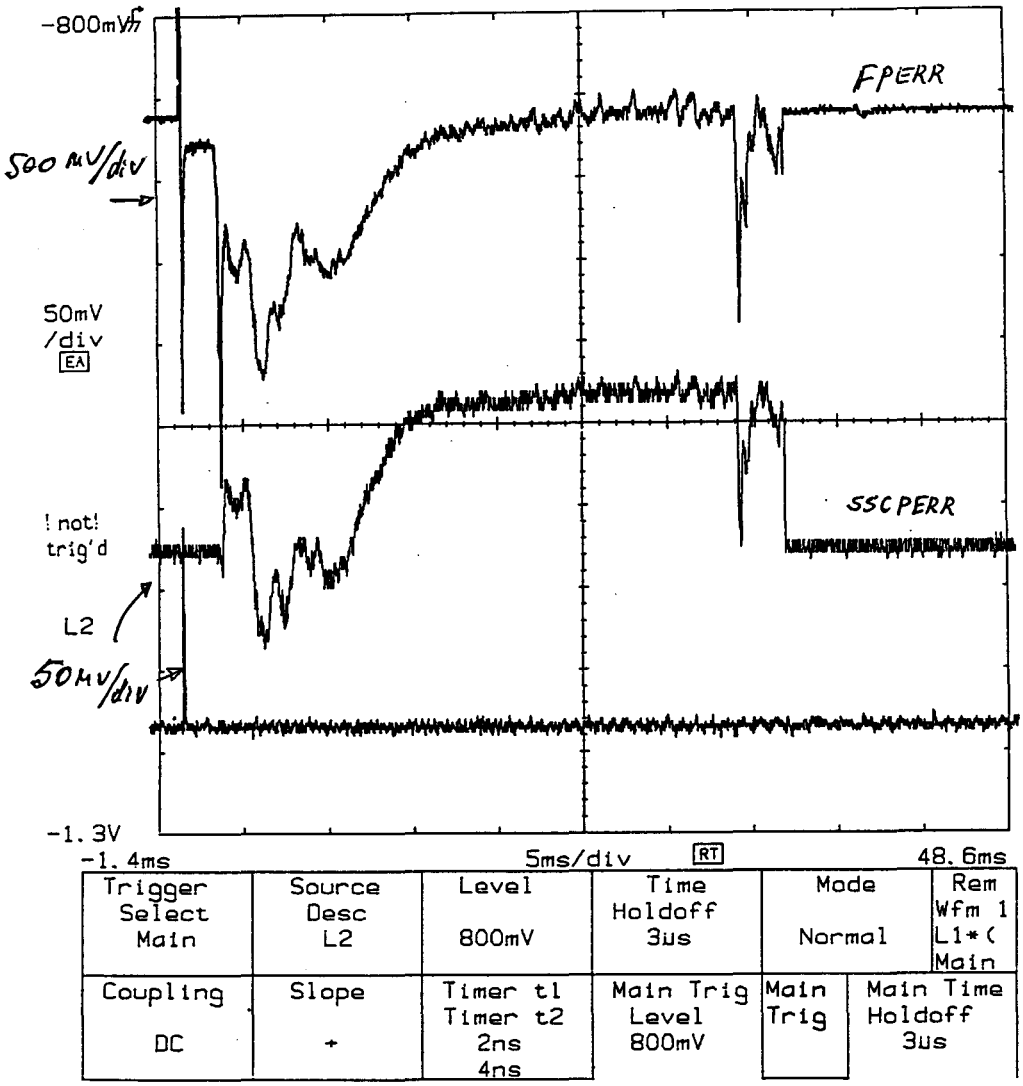


Figure 19. Phase Detector Error Signal while Measuring the Cable Delay.

5.3 Phase Loop Tests

With the synchronization loop open, the phase loop was closed to parasitically demonstrate the operation of the frequency program, phase-lock DSP, DDS, and the phase detector circuitry in parallel with the booster VCO. Figure 20 shows the output of the phase detector bottom trace. The top trace is the phase error between the VCO and the DDS signal. The data was taken with a sampling period in the phase loop equal to about 3.12 μs. We have improved the phase loop sampling to less than 3 μs since then.

5.4 Repeatability of Time-varying Phase between Booster and Main Ring Synthesizer

With several trip measurements, we calculated the integrated phase per booster cycle by tracking one bunch. In Figure 21 integrated phase for 25 consecutive cycles is shown in terms of the booster turns. Data was taken on November 17 that 1:30 p.m. Figure 22 shows the phase over a period of 24 days. The fluctuation of phase appeared to be within 8 turns. Since the fluctuations are due to the slow drift in the magnetic field, the measurements taken on different days suggest the repeatability of the time-varying phase.

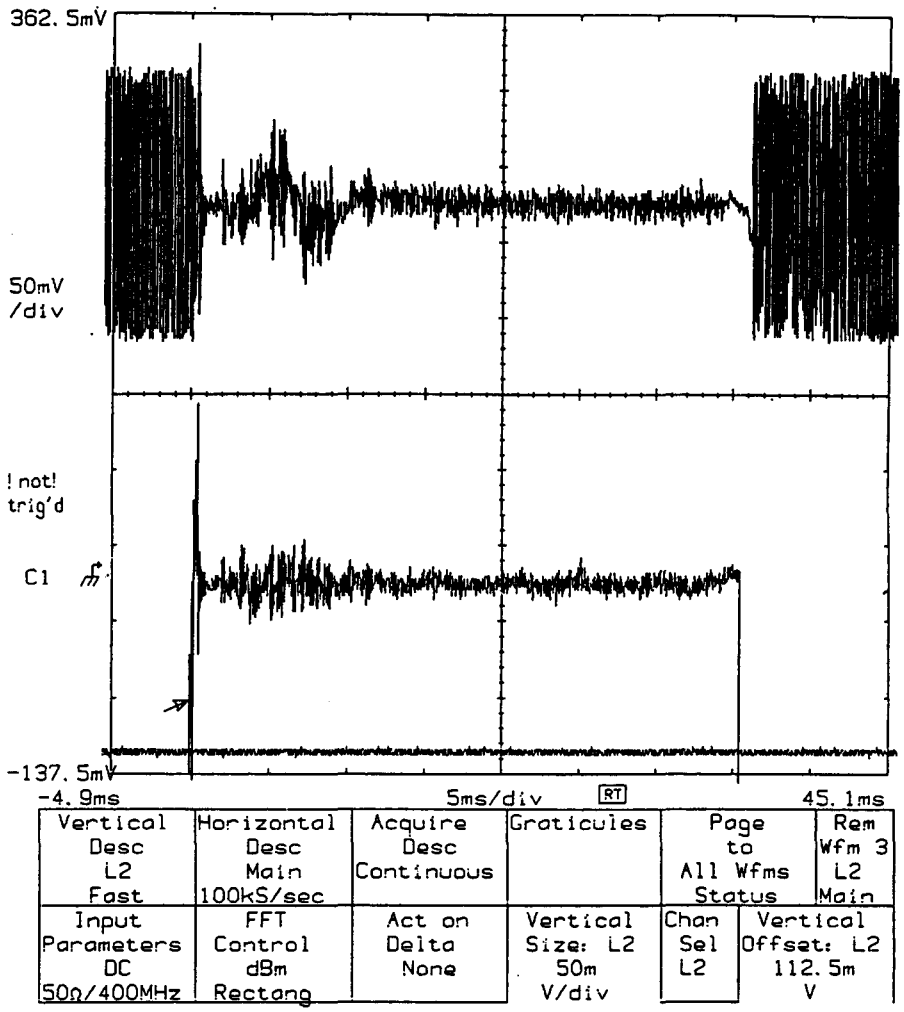


Figure 20. Phase Detector Error Signal when the DDS Was Locked to the Beam.

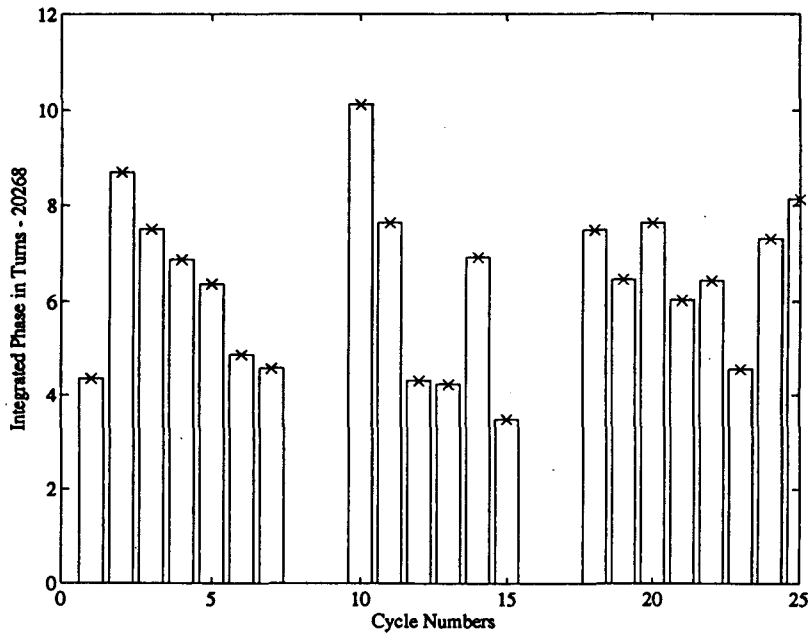


Figure 21. Integrated Phase for 25 Consecutive Cycles (Nov. 17, 1:30 pm).

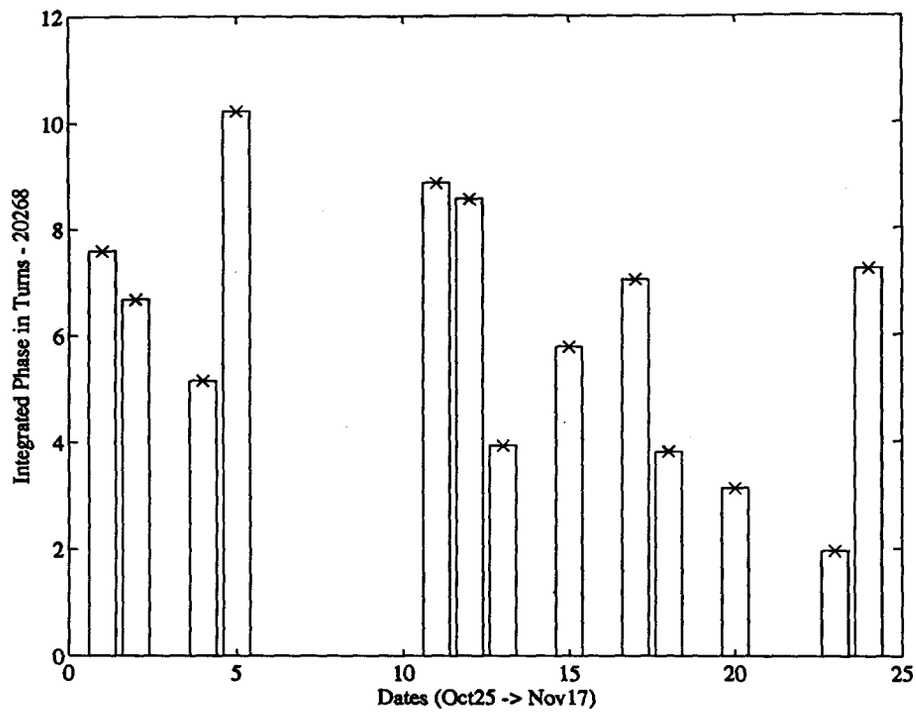


Figure 22. Integrated Phase for Data taken from Oct. 25—Nov. 17.

6.0 CONCLUSIONS

The test results shown in this report give a good indication of the hardware capabilities to phase-lock to the beam. However, the parasitic experiments do not show the effectiveness of the phase loop to damp the dipole oscillations without beam loss. Since we have a sampling period of 3 μs in the phase loop, which is about 13 times lower than the highest synchrotron period, there is hope to achieve effective damping. Our simulation results have indicated very good loop performance for such a sampling period. Also, a stepwise frequency approximation with a period of less than 2 μs in the frequency ramp DSP would no doubt produce additional parasitic frequency modulation. The fundamental of this sampling frequency can cause sidebands around the rf frequency. Our calculations show that the relative levels of these spectral components are way below the DDS noise level (–40 dBc). Hence, a sampling period of 2 μs or less for the frequency ramp shouldn't cause additional sidebands.

The frequency measurement using the TDC seems to be more accurate than any other techniques we know. Hence, the table inside the DSP producing the ramp can be made as close as we need for the beam. By adding the phase-loop-frequency shift to the ramp table, we would have greater frequency accuracy. This in itself may become very useful for machine diagnostics.

If, with the phase loop hardware we are able to operate the machine without beam loss, then testing of the synchronization loop means simply running another program in the DSP. As a precautionary step before trying the synchronization loop, we may need to conduct more trip measurements to study the effect of slow drift in the magnetic field.

ACKNOWLEDGMENTS

The author and his team at the SSC Laboratory who assisted in developing and testing the hardware are very grateful to D. McGinnis, J. Steimel, J. Lackey, R. Tomlin, B. Barnes from Fermilab for their cooperation while working on the booster. We are also grateful to many other people at Fermilab who were helpful to us during the experiment. We hope that there will be similar cooperation in future and the Fermilab team will give us, sometimes, an opportunity to test the hardware with beam.

REFERENCES

1. R.C. Webber and L.K. Mestha, "Proposal to Test a New Low Level Rf System on the Fermi National Accelerator Laboratory Booster Synchrotron," SSCL Document ADA-3120001, 14 Nov. 1991.
2. *Sky Challenger C30 Hardware Manual*, Sky Computers, 1990.
3. *M690 TDC Manual*, Highland Technology, Inc., 1992.
4. *TMS320C3x User's Guide*, Texas Instruments, SPRU031C, Revision F, July 1992.