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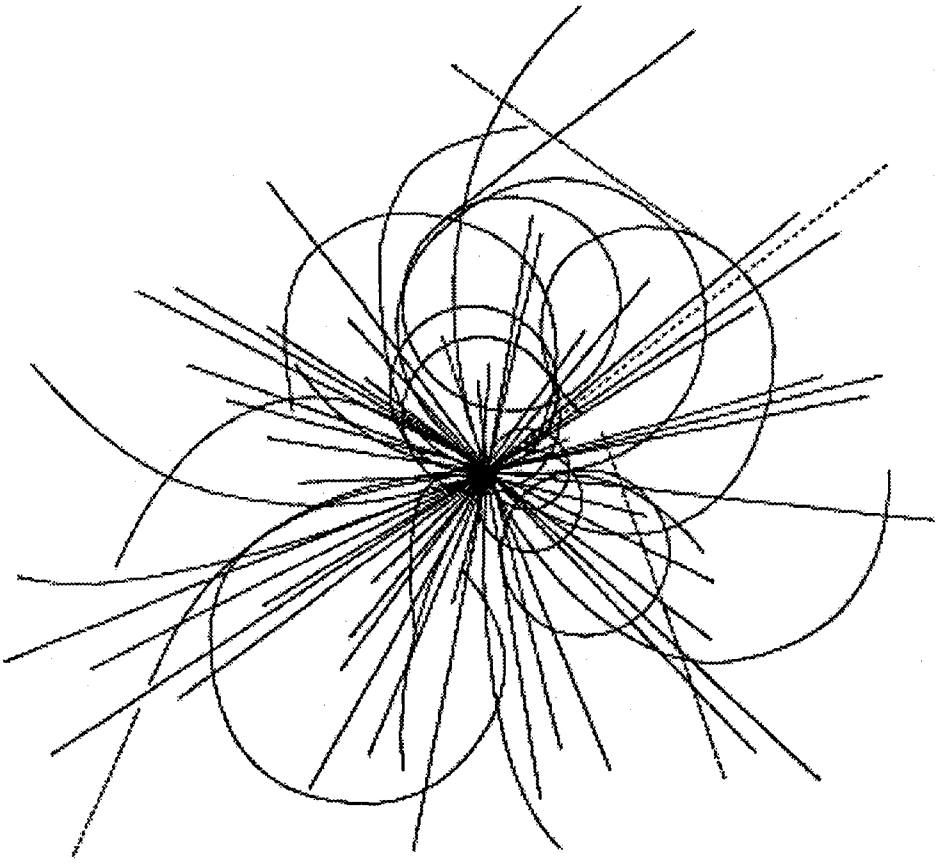

Superconducting Super Collider Laboratory

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Abstract

We report test results for the second version of the current-splitter chip for the Photo Multiplier Tube (PMT) digital readout system. The chip was designed by Fermilab and fabricated using the Orbit 2 micron BiCMOS process. Version 2 of the splitter has 10 splitting ranges compared to 9 in the previous design. Measurements were done to test the performance of the current-splitter chip at the Physics Research Division, Superconducting Super Collider Laboratory (SSCL).

1.0 INTRODUCTION

The current-splitter chip operates in such a way that the input current pulse from the photomultiplier tube is divided into 10 binary weighted current pulses that are integrated on 10 separate capacitors for a gated interval of 16 ns. The circuit is biased in such a way that the voltage on only one of the capacitors will be in the 1~2V range. The voltage on this capacitor will be digitized with a flash Analog-to-Digital Converter (ADC). The index of the capacitor is encoded. ADC output and capacitor index form a mantissa-exponent pair in a floating-point representation of the input current. Detailed operation of this chip is discussed elsewhere.[1] The measurements on the current-splitter chip are basically divided into two groups: dc characteristic and transient characteristic.

2.0 DC CHARACTERISTICS

We have measured the standby power consumption. The on-chip NPN output buffers used to drive the pads for measurement purposes were disabled during the measurement. The measured power consumption was about 26 mW, most of which was consumed by the input current amplifier.

For the second version of the current-splitter chip only 5 output ranges, I/1, I/2, I/8, I/32, and I/512 are provided externally. Each range has its own separate ground line. All ranges have an integrating capacitor and output buffers except range I/8, which only has a pad capacitor. Dc splitting accuracy for these ranges was measured through the ground line of the range. For this measurement, the dc biasing current mirror of 65 μA and the large shunt transistor were disabled so that the input current was provided through the input pin by a current source and a HP 3458A multimeter. Therefore, the input current incorporated both the normal bias current and the input current. The current flowing through the ground line of each range was then recorded as a function of input current by a HP 3457A multimeter. Figure 1 shows the result of output current as a function of input current for range I/1. The splitting deviation is the difference between measured output value and the ideal one. As shown from the graph, range I/1 or the multiplier added about 4% excess charge to the

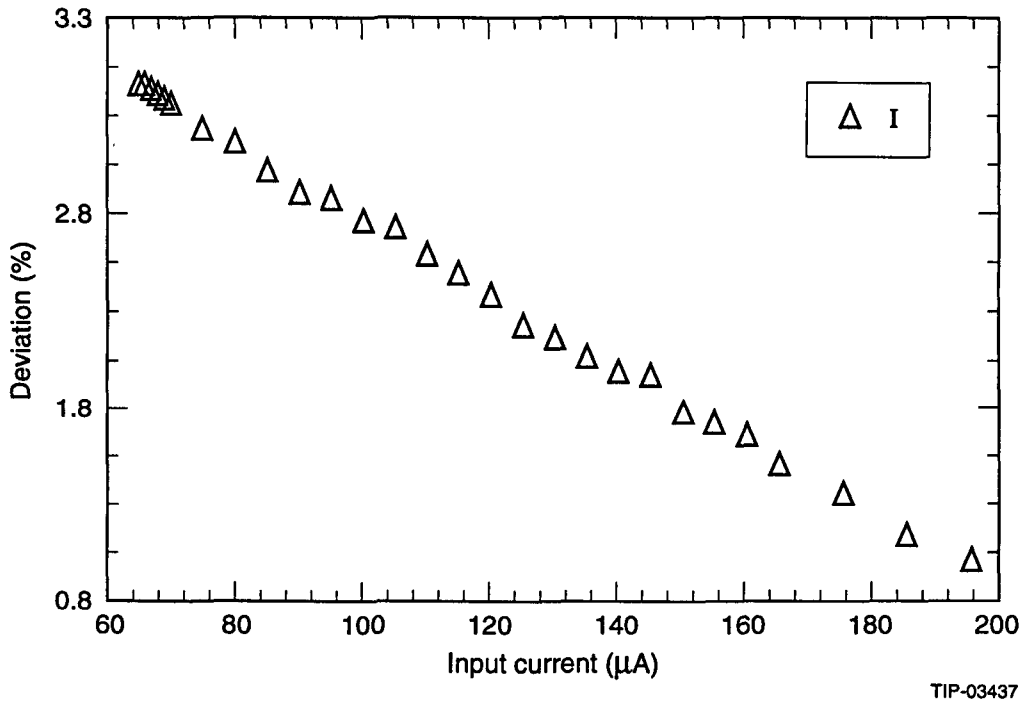


Figure 1. Dc Splitting Accuracy for Range I. Relevant input currents are between 6.5 and 130 μa.

output current. This deviation decreased with increasing input current by about 2% over the input range of interest. The designer suggests that the new design would fix these problems. Results of the remaining ranges are shown in Figure 2. The output from these ranges had a loss of charges of less than 4%. The splitting ratio of ranges I/1 : I/2 : I/8 : I/32 at a dc operating condition of 65 μA is 2.15 : 1 : 0.251 : 0.0625. Except for range I/1, the dc ratios were very good. The splitting error at dc is less than 0.4%. We were not able to measure I/512 because there was no current flow out from the pin. It is not clear what is wrong with the tested chips. Only ranges I/1 and I/2 were tested for the full range of their intended input current range because of concern that a large dc current may damage the chip.

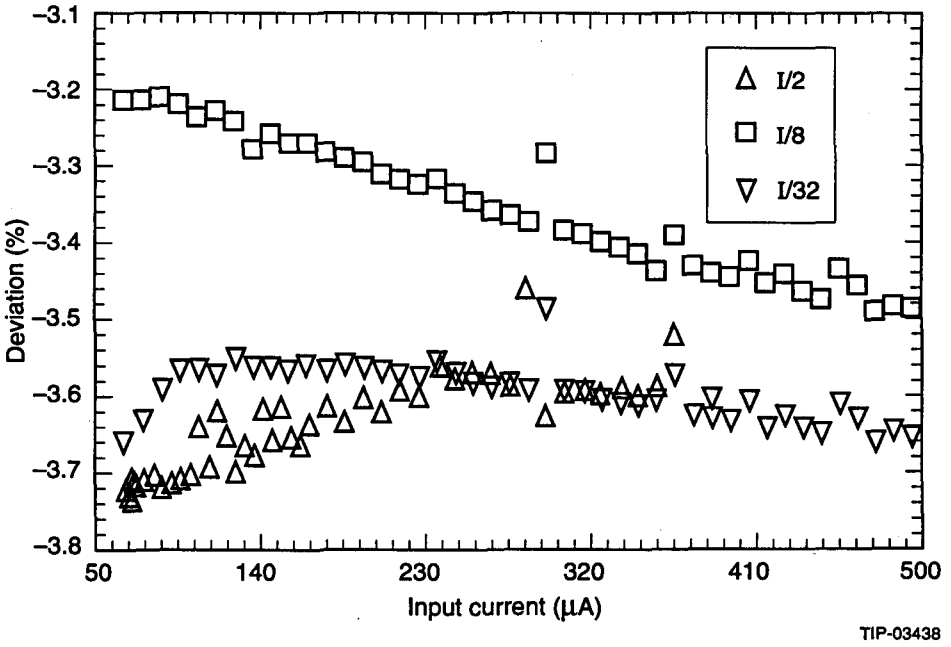
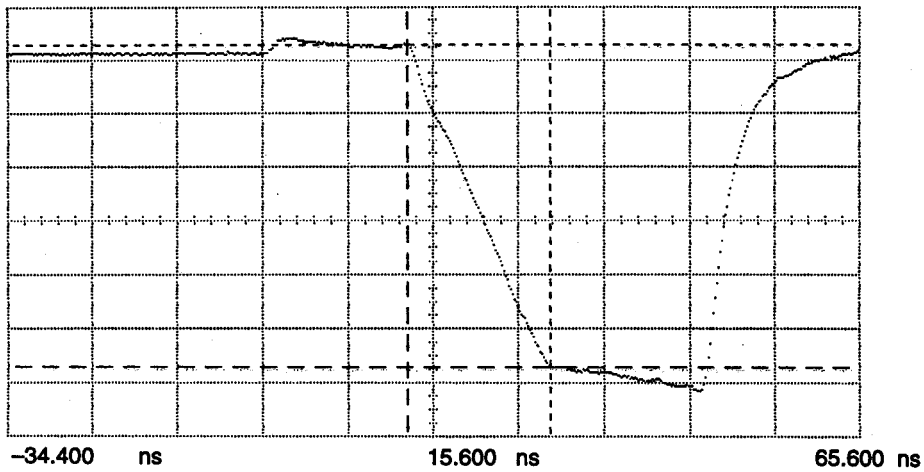


Figure 2. Dc Splitting Accuracy for Ranges I/2, I/8, and I/32. Relevant input currents for range I/2 are between 130 and 260 μa.

3.0 TRANSIENT CHARACTERISTICS

The more important characteristic is the transient response of the chip. First, we looked at the operation of charge integrating on the capacitors. Ranges I, I/2, I/32, and I/512 have on-chip buffers to drive the output pins. An additional high-speed buffer was used to drive the coax cable to the measuring equipment. We applied complementary pulses with a pulse width of 16 ns to the current switches and properly set and reset the PMOS switches. The output from the capacitor of range I/1 was measured with a HP 54111D digital oscilloscope. Figure 3 is a typical measured waveform on an integrating capacitor. By measuring the current flowing out of the ground line of that range, the size of the capacitor was estimated to be around 1.26 pF, close to the design value. To accurately measure the charge integrated on the gated capacitor, a dc current was used to provide a very accurate input current. During this measurement, the bias current mirror of 65 mA and the large shunt transistor were disabled so that we could accurately measure the current flowing through the current splitter. The base of the clamping transistor was biased at –2.35 V. Figure 4 shows the measured result of range I. The solid line is the least-squared fit to the measured data between 1 to 2 V, which is the intended operating range. The residue between the fit and the measured data is shown in Figure 5. Figures 6 and 7 show the results for range I/2. The observed nonlinearity for range I/1 is approximately 1%. For range I/2, it is less than 0.5%. As for range I/32, we were not able to measure it because the output did not change with the input current. It seems that there was a large current coupled from the reset PMOS switch to the ground line when it is operating.



Ch. 2 = 70.00 mVolts/div
Timebase = 10.0 ns/div

Offset = –271.0 mVolts
Delay = 15.600 ns

Delta V = 421.4 mVolts
Vmarker1 = –462.0 mVolts
Delta T = 16.800 ns
Start = 12.600 ns

Vmarker2 = –40.60 mVolts

Stop = 29.400 ns

Trigger mode : Edge
On pos. edge on Trig3
Trigger levels
Trig3 = 0.000 Volts
Holdoff = 70.000 ns

Figure 3. Typical Output Waveform from the Current Splitter.

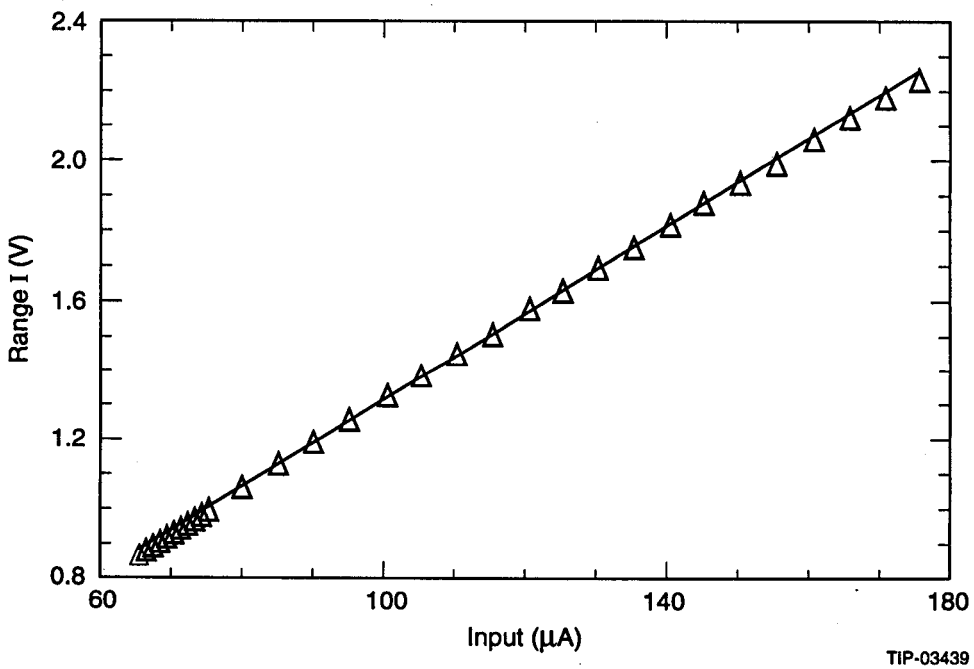


Figure 4. Output of the Range I/1 Charge Integrating Capacitor as a Function of Input Current. Solid line is the least-squared fit to the data between 1 to 2 V.

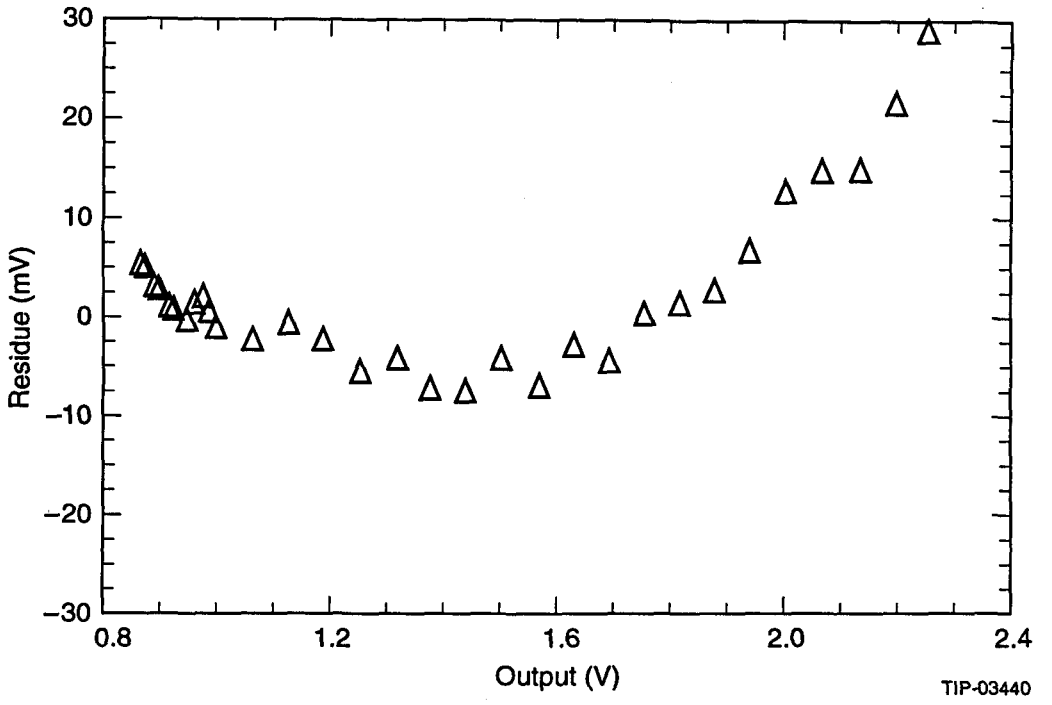


Figure 5. The Residue Between the Fit and the Measured Data for Range I.

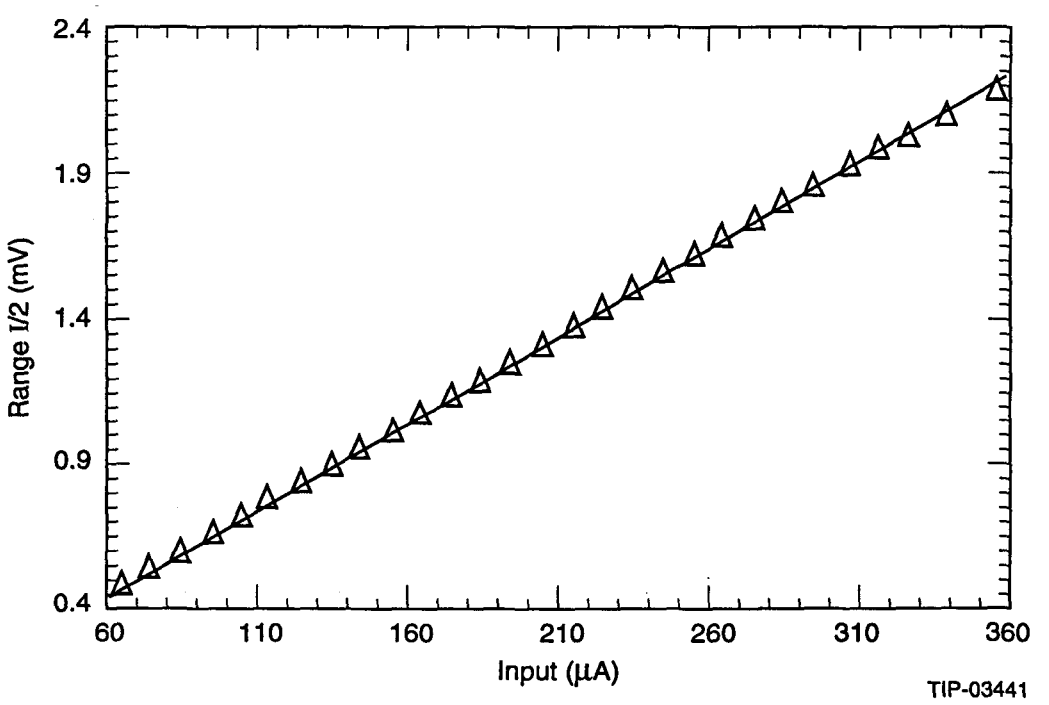


Figure 6. Output from the Integrating Capacitor as a Function of Input Current. Solid line is the least-squared fit to the measured data between 1 to 2 V.

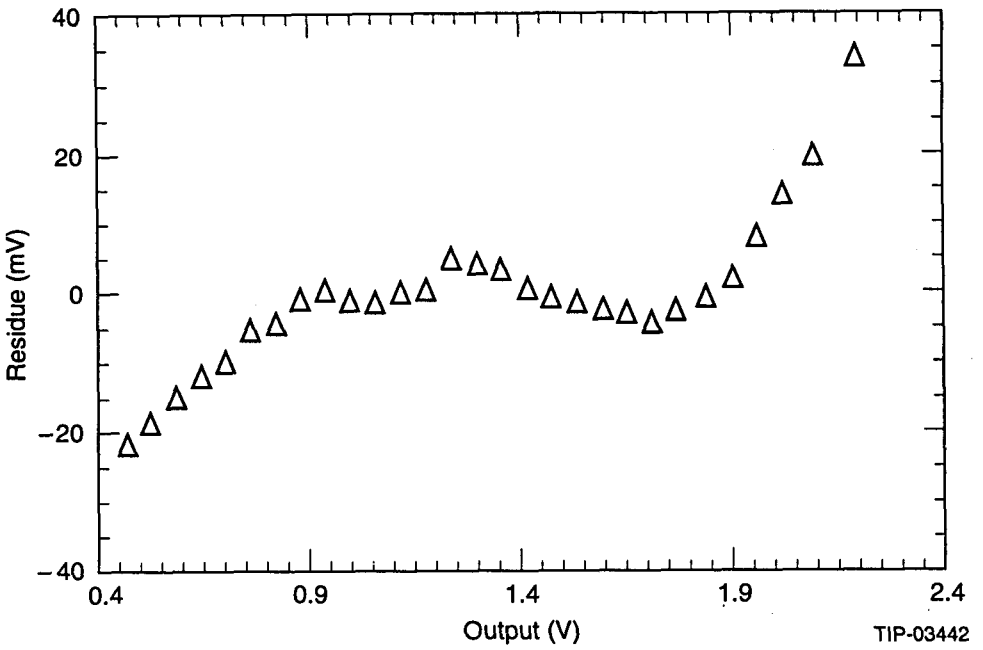


Figure 7. Residue Between the Fit and the Measured Data for Range I/2.

The above measurements only showed the operation of the charge integrating stage. To test the dynamic performance of the chip, a current pulser built using a rf transistor injected current to the input of the current splitter. By using a high-frequency Tektronix CT-2 current transformer, the current pulse from the current pulser was monitored through the oscilloscope. The input current pulse had a rise time of 2 ns, a fall time of 2 ns, and a width of 12 ns. The results of range I/1 are shown in Figures 8 and 9. The results for range I/2 are shown in Figure 10 and Figure 11. As can be seen from the graphs, the deviations are similar to the case of integrating the dc current on the capacitor.

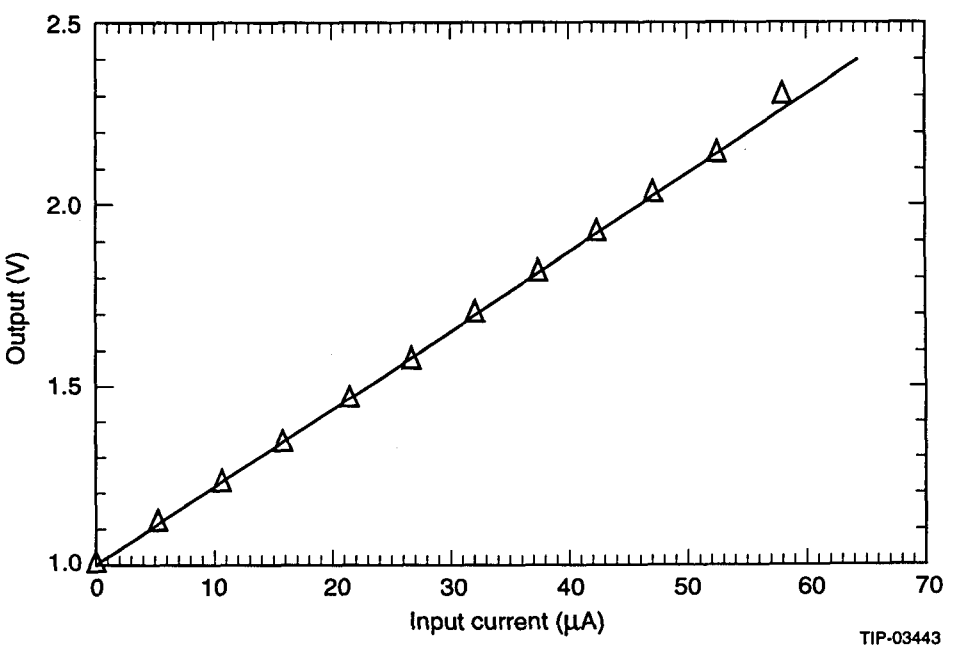


Figure 8. Dynamic Test Results for Range I. The output from the integrating capacitor is plotted as a function of the input current pulse magnitude. The solid line is the fit to the measured data between 1 and 2 V.

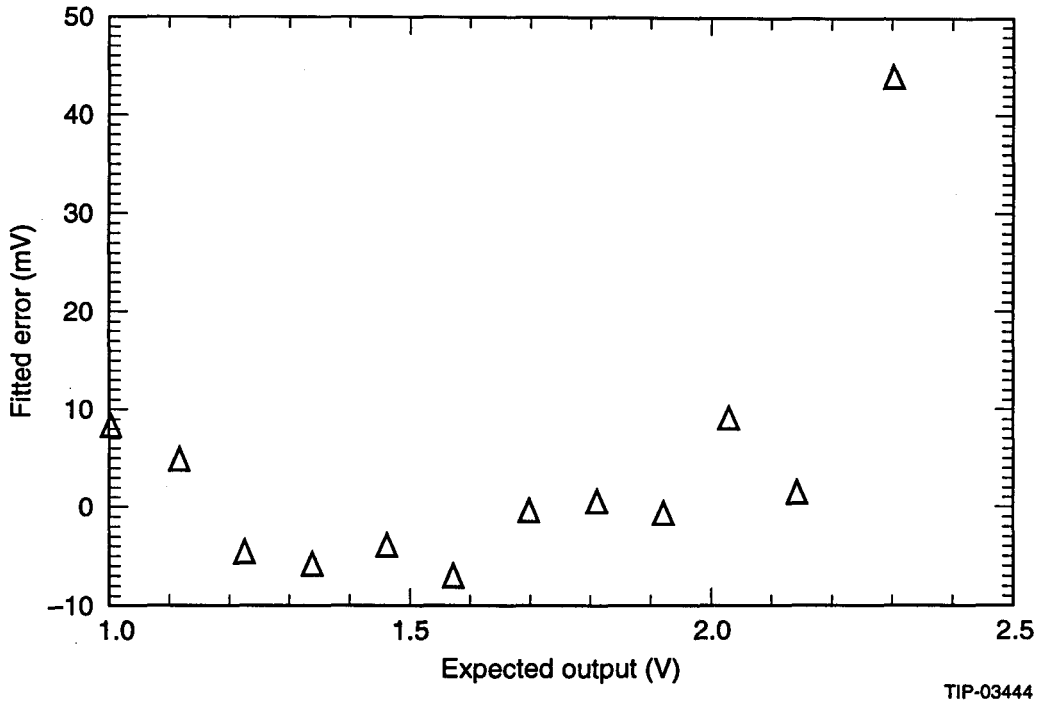


Figure 9. The Residue Between the Fit and the Measured Data for the Range I/1 for the Dynamic Test.

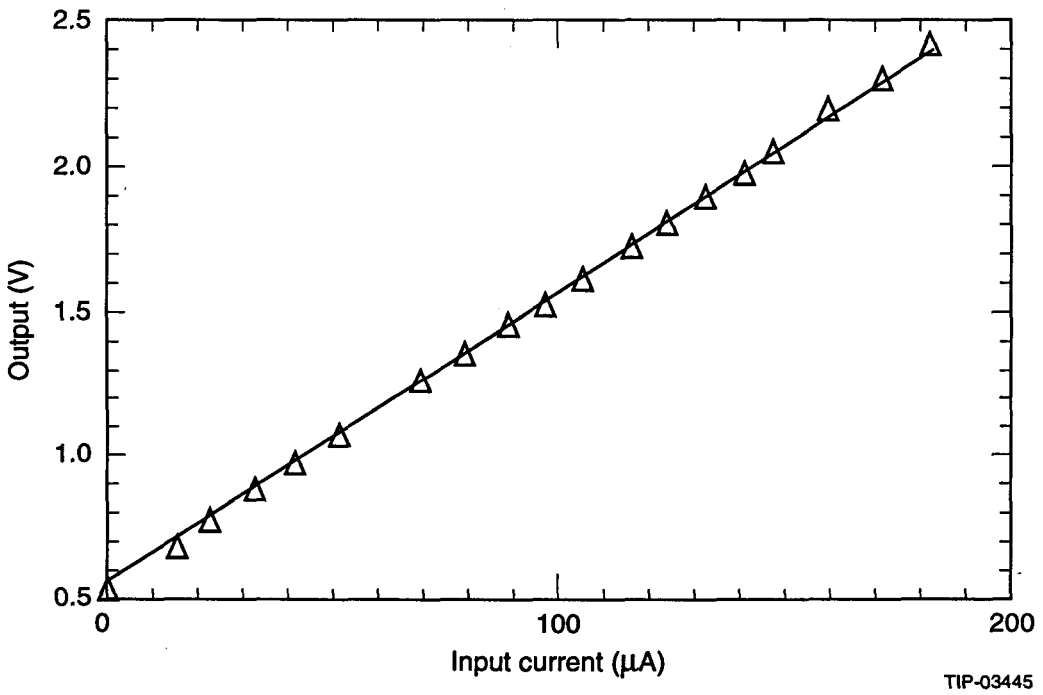


Figure 10. Output of Range I/1 as a Function of Input Current Pulse Magnitude in Dynamic Test. The solid line is the fit to the measured data from 1 to 2 V.

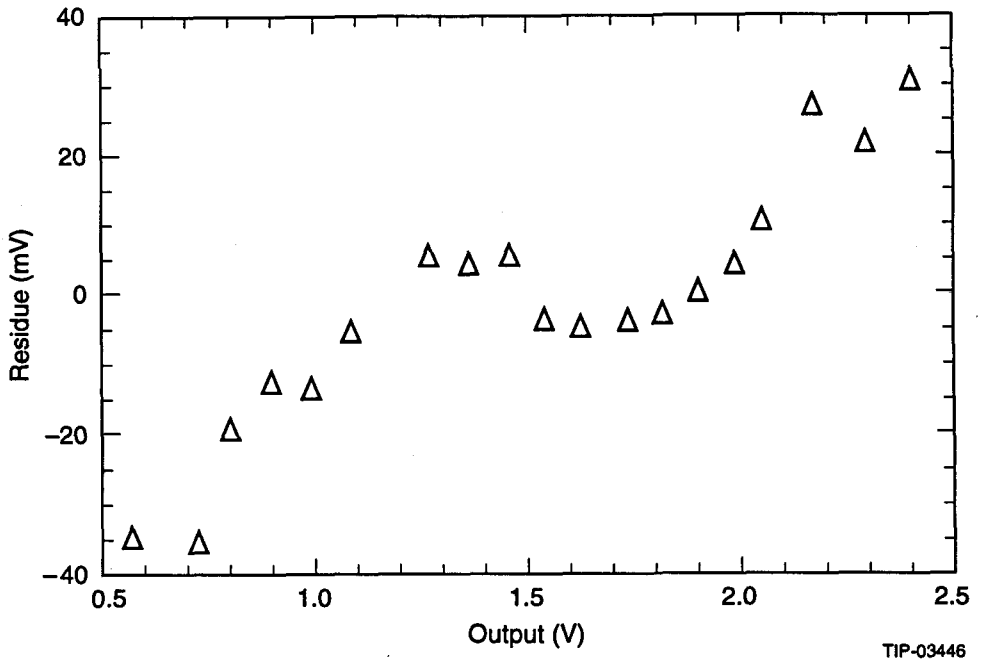


Figure 11. Residue Between the Fit and the Measured Data for Range I/2 Dynamic Test.

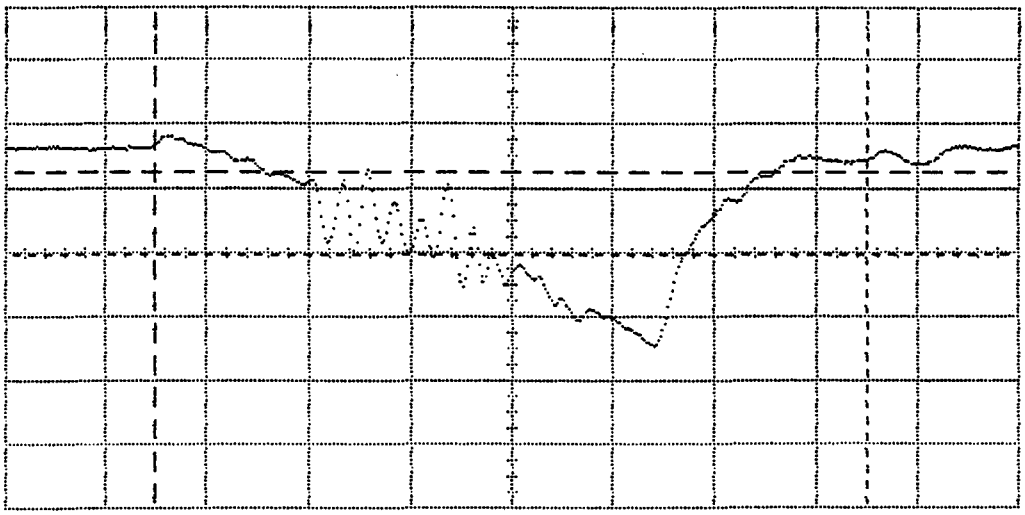
Time delay of each range was measured by comparing the output pulse from the ground line to the input pulse. The output from each ground line was fed to the oscilloscope through a 50-Ω-coax cable. There was a delay spread of about 1.3 ns from range I/2 to I/32. An additional 1.1 ns delay was observed for range I.

In the measurements, we observed some ringing in the input current (about 10% with a 100 mA input pulse). This ringing appeared on the output as well. This has been attributed by the designer to the input stage behaving inductively at high input current level.

Cross talk between ranges was also investigated. By applying a 100 mA pulse to the input of the chip, we observed a step of 26 mV and the consequent damped ringing on a hold capacitor output as shown in Figure 12. As the switches to this capacitor were open, no signal should have been observed. For example, noise on such capacitors may contribute to an error in the presample measurement used for baseline subtraction.

Noise on the chip was also investigated. The test setup was very well shielded to reduce the emi interference. A LeCroy 7200 Scope was used to histogram the noise magnitude. The rms noise due to the output buffer only was measured to be less than 450 μV. The reset switch 5 V swing and the complementary switches increased the noise level to about 1 mV. This noise was basically due to ringing at the on-chip output buffer coupled to the 5 V reset switch swing.

In conclusion, we have tested some of the important characteristics of the second version design of the current-splitter chip. The current splitting and charge integration on the capacitor worked well on the available test ranges.



18.800 ns 68.800 ns 118.800 ns

Function1 = 20.00 mVolts/div
Timebase = 10.0 ns/div

Offset = –32.81 mVolts
Delay = 68.800 ns

Delta V = –25.60 mVolts
Vmarker1 = –7.600 mVolts
Delta T = 70.000 ns
Start = 33.800 ns

Vmarker2 = –33.20 mVolts

Stop = 103.800 ns

Trigger mode : Edge
On pos. edge on Trig3
Trigger levels
Trig3 = 0.000 Volts
Holdoff = 70.000 ns

Figure 12. Effect of Cross Talk Due to a Large Input Current Pulse.

REFERENCES

1. R. J. Yarema, G. W. Foster, J. Hoff, M. Sarraj, and T. Zimmerman, "A Pipeline Multiranging, Integrator and Encoder ASIC for Fast Digitization of Photomultiplier Tube Signals," The Second Annual Conference on Electronics for Future Colliders, Chestnut Ridge, New York, May 19–21, 1992.