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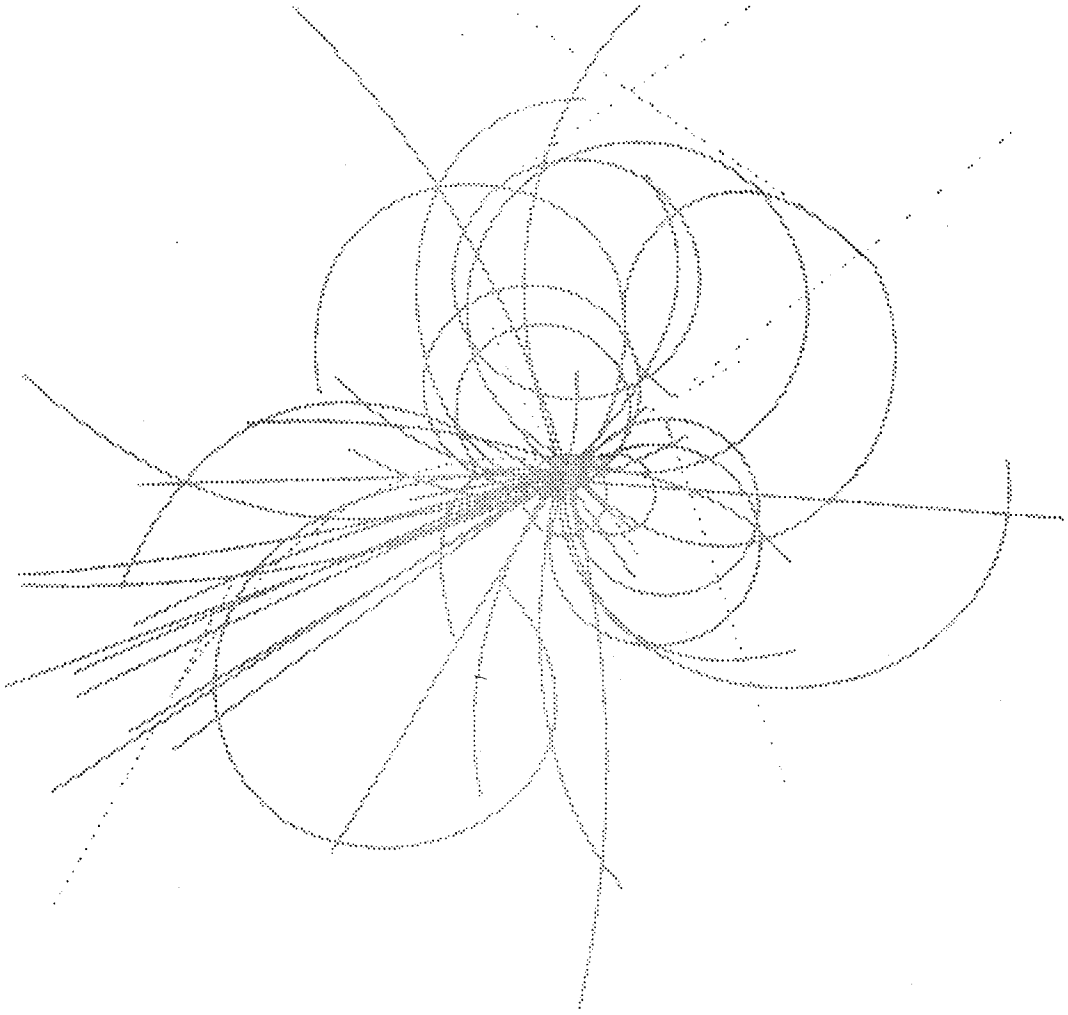

Early Stages in the Development of the Global RF Feedback for the SSC Low Energy Booster

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EARLY STAGES IN THE DEVELOPMENT OF THE GLOBAL RF FEEDBACK FOR THE SSC LOW ENERGY BOOSTER

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Abstract: A new method to generate the controlled master frequency has been designed to meet the requirements for accelerating the beam in the Low Energy Booster of the Superconducting Super Collider. This method is also designed to achieve rf synchronization for beam transfer to the Medium Energy Booster. The sweeping of the rf during acceleration complicates the programmed synchronization. The architecture discussed in this paper can be tailored to include all types of synchronization methods. Global synchronization timing for collider injection is discussed briefly. With the available hardware the frequency is updated at intervals of less than a microsecond using a TMS320C30, floating-point Digital Signal Processor. We are investigating the feasibility of generating the frequency with a Direct Digital Synthesizer as the frequency source for smooth acceleration within the LEB frequency range. Some of the problems associated with the products are discussed with a view to improve the design.

INTRODUCTION

The basic Low-Level rf system comprises several feedback control loops. Well-controlled master frequency is necessary to (1) capture the Linac beam, (2) accelerate the beam while correcting for the radial excursions due to field errors, and (3) transfer the beam to the next machine. Several feedback loops are involved to accomplish these functions. A precise control of the master frequency helps in filling the collider rings with less emittance dilution. Since the filling process is quite involved, we have attempted to set the goals by describing the timing sequence for filling cycles. There are several novel schemes in which the precise timing sequence can be generated to extract the beam. In developing the controlled master frequency, emphasis is given to the flexibility needed to incorporate any of the novel transfer schemes under investigation.

It is normal practice to use a Voltage Controlled Oscillator (VCO), or a phase-locked-loop frequency synthesizer with a VCO as the source of frequency.[1-3] An alternative way to produce frequency is by programming a Direct Digital Synthesizer (DDS), a device that generates frequencies with digital techniques. For the Low Energy Booster (LEB) at the

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from 47 MHz to 59 MHz are considered. Various feedback loops discussed in this paper to control the master frequency are centered around the DDS. Most of the digital synthesizers available in the market have serious phase discontinuity problems, with some exceptions. We highlight a test set up to observe these defects.

GLOBAL RF FEEDBACK SYSTEM

A conceptual diagram of all the feedback loops associated with the master frequency generator is shown in Figure 1. A Digital Signal Processor (DSP1) is loaded with the required frequency table to sweep the rf signal frequency between 47.518 MHz and 59.776 MHz in 50 ms. The maximum rate of change of frequency, on the order of 1036.8 MHz/sec, occurs at about 5.7 ms into the LEB cycle. The DSP1 processor is able to read a single frequency value from the onboard static memory and to update the DDS frequency at a specified interval. The DSP and DDS combination can give an update interval of as short as 180 ns. The DDS we have evaluated is capable of changing the frequency in about 25 nanoseconds with 1 GHz clock frequency. Since the technology is rapidly advancing, it would not seem unreasonable to consider a complete digital approach to close all the associated feedback loops, as in Figure 1.

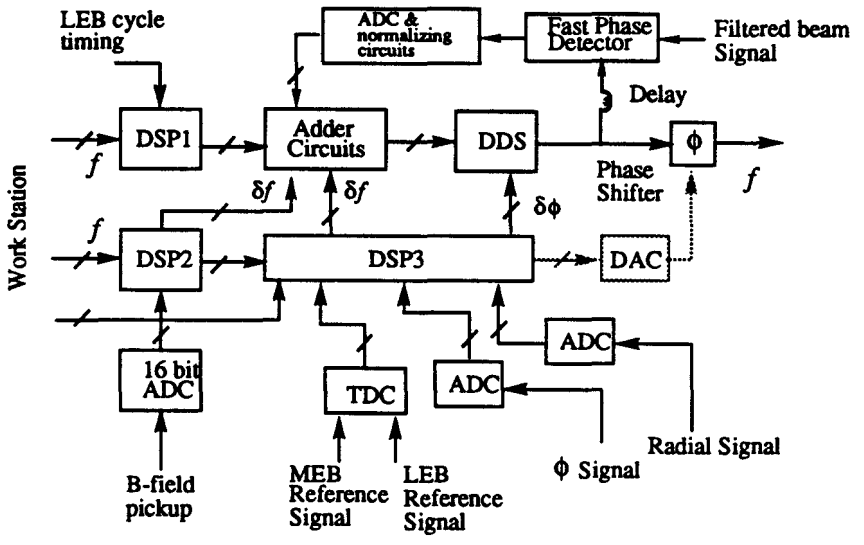

Figure 1. Schematic of the active feedback loops involved with the master frequency oscillator. (Interfacing circuits are not shown for simplicity).

Field Loop

The frequency table stored in DSP1 is corrected in real time every 2 s by using the measured B-field signal with an off-the-shelf 16-bit Analogue-to-Digital Converter (ADC) with a 2 s sample period. The processor in the B-field loop (DSP2) has a frequency table similar to that in DSP1 but with appropriate resolution which will correspond to each bit combination of the ADC. Thus these values will form a frequency look-up table with respect

to the B-field. With this we can generate a frequency shift, δf, which is equal to the difference between the ideal frequency and the frequency corresponding to the ADC value (error in the B-field). In this way we can allow the DDS to sweep the frequency even if we disable the B-field loop.

Radial Loop

In some accelerators, such as the Fermilab Booster and DESY III proton machine, a B-field loop of the type described above is not included.[1] However, in the Fermilab Booster the correction for the field error is done by measuring the radial offset of the beam and varying the phase of the rf signal driving the high-power rf system. A similar loop can be implemented here for the SSC LEB. It is desirable to have the radial beam signal sampled once every Medium Energy Booster (MEB) turn. We then process it inside a DSP by using the advanced feedback controllers (under investigation), so that a limited phase shift is applied to the rf signal. A necessary phase shift can be implemented digitally in the DDS or by means of a wideband analogue phase shifter. Since the radial position can also be corrected by modulating the ramping frequency at the input end of the DDS, the digital implementation will help to achieve optimal trade-off between the frequency shift and the phase shift. The radial feedback loop may not be needed for collider operation since the beam phase loop (explained below) and the B-field loop may be sufficient to handle the unwanted beam excursions. However, for machine studies, on some occasions we may need to steer the the beam radially. To do this a δR program may have to be loaded into DSP3 from the workstation without disturbing the real time operation. We are evaluating the hardware for such architecture. Also, when we consider the LEB-MEB synchronization using the phase-control scheme, the radial position information may be useful to implement the multi-variable feedback controller.[4] Should we encounter unexpected problems during commissioning of the accelerator, an analogue radial feedback loop could be added without major changes with the digital system described above.

ϕ Loop

This loop may be necessary for machine studies period, or while commissioning the accelerator. It includes the accurate measurement of the phase of the center of the bunch with respect to the rf wave, ϕ. A ϕ program can be loaded into the DSP. Measured values are compared with theoretical values to obtain the phase error. The phase error is then applied to the DDS or the phase shifter, thus forcing the beam to follow the new program. The B-field and the radial feedback loops are used appropriately, if necessary, to the input end of the DDS. If we need to use this loop to damp the synchrotron oscillations, then the loop bandwidth must be designed well above the highest synchrotron frequency.

Synchronization Loop

This feedback loop is configured depending on the approach one can adopt to achieve synchronization. In Figure 1, a Time-to-Digital Converter (TDC) is shown in the synchronization loop. It is used to measure the position of the LEB reference signal for each MEB revolution. This will enable us to record the arrival time of the LEB reference wave. Using this time-of-flight information, the phase of the LEB reference wave is calculated in terms of the path length for each MEB reference wave. To achieve this goal, we may need information on the average radial position offset during the arrival time measurement. This information is available from the output of the radial loop ADC. The phase error is calculated by subtracting the measured LEB phase values from those stored in the processor. (The phase values stored in the processor are for the ideal case.) This phase error is then used to compute the frequency shift required to keep the phase error zero. By coupling the radial loop with the

synchronization loop, we are in a position to compute the optimal frequency shift and the phase shift, if necessary. The frequency shift from the synchronization loop is fed to the adder circuits to control the master frequency. This feedback loop can be turned on at any time during the acceleration cycle.

If we use a phase-locking approach to synchronize the LEB with the MEB, then, as in Fermilab Booster,[1] we need to close the synchronization loop a few milliseconds before the flat B-field region. A phase detector will be used instead of the TDC to detect the phase information between the down-converted frequency from the LEB and the MEB reference waves. The phase values are compared with a table to follow a smooth program back to the extraction frequency. If the DDS is stable enough, we may not need an alternative frequency source to bring the phase difference to zero. However, an accurate matching of the frequency, phase, and rate of change of frequency is needed to accomplish the phase-locking scheme. The hardware architecture seems to be able to provide the necessary flexibility. Also, if necessary, a feedback loop to the beam can be included to smear out the noise on the frequency shift while phase-locking the two rf waves.

Beam Feedback Loop

A conceptual diagram of this loop is shown in Figure 1. The implementation may include more electronics. The loop can be closed during ramping so that the DDS can be phase-locked to the beam. The beam pickup signal may need pre-filtering through a band pass filter before it is sent to the fast phase detector,[1] depending on the hardware.[5] The fast phase detector output is digitized and normalized to integrate with the DDS. A small delay may be necessary between the DDS output and the fast phase detector as in the Fermilab Booster system. By dc coupling the beam phase loop using an additional circuitry after the ADC, we can use the loop merely to add a small frequency shift to the DDS adder circuits while ramping.[5] However, if the dc coupling is not done, the beam frequency is generated from the beam phase loop by disconnecting the ideal frequency table from DSP1. Under such a condition, the B-field loop may have to be disabled since the beam frequency would act as the reference to the DDS. Also, if we use this loop to damp synchrotron oscillations, the bandwidth must be well above the highest synchrotron frequency in the LEB. We have included this to work with a worst-case scenario.

Linac rf Signal

A few microseconds before the Linac-to-LEB injection, the LEB master frequency hardware may be required to generate the correct injection frequency to drive the Linac rf system. This is because the Linac rf system will be running at the 9th harmonic of the LEB injection frequency. Linac frequency must remain unchanged while the LEB frequency is allowed to ramp during acceleration. We have two schemes, shown in Figure 2, in which this could be achieved. In Figure 2(a), we show the design using a separate DDS for the Linac reference source. The data lines to the Linac DDS are hard-wired, and the output signal is multiplied to give nine times the LEB injection frequency. Reset lines are used to accurately start the two DDSs at zero phase. A minimum of interfacing between the two DDSs would allow significant flexibility in controlling the Linac frequency relative to the LEB injection frequency. It is not clear whether the phase discontinuity created by the DDS reset signal would have problems to the high-power rf system. Alternatively, in Figure 2(b), the Linac reference frequency is generated using a Voltage Controlled Oscillator (VCO). Here the gated track and hold circuits will be used to phase-lock the VCO to the LEB DDS at the appropriate time before and during injection. The hold circuits maintain the required frequency to the Linac rf system.

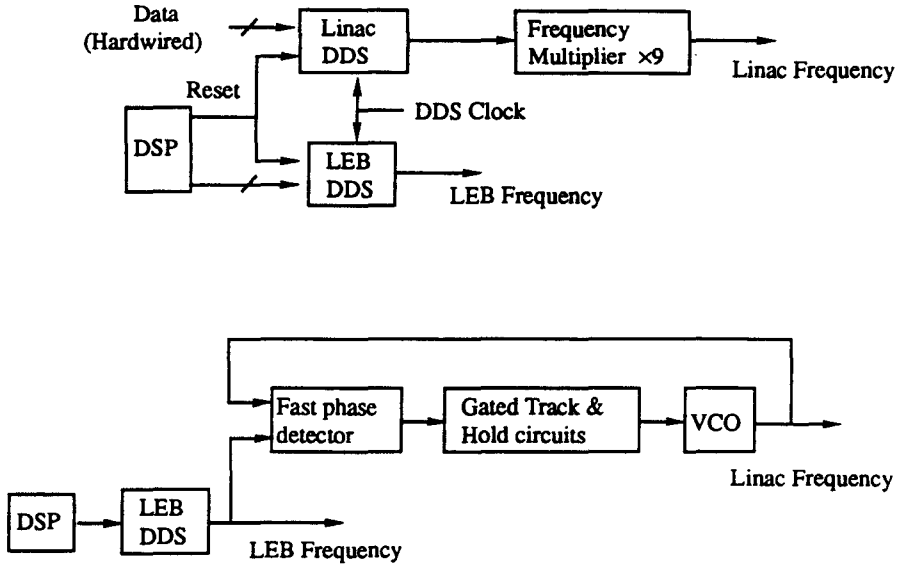

Figure 2. (a) Schematic diagram of the setup to generate Linac frequency using DDS. (b) Schematic diagram of the alternate setup to generate Linac frequency use VCO.

GLOBAL SYNCHRONIZATION TIMING

Global timing sequence for synchronization depends on the filling sequence required for the collider operation, injection, and extraction kicker rise and fall times and the cycle time of each machine. In Figure 3, the collider filling scenario is given with the number of beam bunches and gaps. Refer to the SCDR[6] for the injection and extraction kicker parameters. In Figure 4, the timing associated with each machine cycle is shown in detail. The injection time required for the Linac to the LEB is 6.819 μs due to three-turn injection. At this time we disable all the feedback loops mentioned above and hold the LEB frequency to the injection frequency. The numbers 1 to 2916 in Figure 4(a) represent the number of Linac beam bunches stacked in the LEB. Figure 4(b) shows the timing between the beam bunches just before acceleration. After acceleration to the top LEB energy (Figure 4(c)) beam pulses are separated by 16.68 ns and are extracted into the MEB. There will be two gaps in the MEB due to injection and extraction kicker rise and fall times. Figure 4(d) shows the MEB filling sequence from the LEB for the first two MEB-to-High Energy Booster (HEB) transfers. At least 24 gaps are needed in the MEB to accommodate the MEB extraction kicker and the HEB injection kicker rise times. In this cycle there are seven LEB transfers; in the third MEB-to-HEB transfer there are only four full LEB transfers and one partial transfer (Figure 4(e)). Thus we would need to include a counter module to the LEB-MEB synchronization loop shown in Figure 1. The partial transfer of only 70 bunches is made by aborting the unwanted LEB bunches at the top energy into the beam dump located somewhere in the transfer line. Furthermore, there will be eight transfers from the HEB to the top collider ring with the filled bunches and the gaps as shown in Figures 4(f) and 4(g). Effectively it takes 1752 sec to fill the top collider ring (Figure 4(g)). A similar filling sequence is followed to the bottom collider

ring (Figure 4(h)) by reversing the polarity in the HEB. From Figure 4 it is clear that the complete collider filling time is 3517 seconds with the current design.

From the synchronization chart it must be noted that while the MEB is accelerating, there will be no beam in the LEB until all the beam from the MEB is extracted to the HEB. This means the second set of injections to the MEB takes place only after completing one full MEB cycle. Thus there will be a period in which there will be no beam in many of the LEB cycles. This means the radial feedback loop and the synchronization loops in Figure 1 may need to be opened when the LEB is free-running without the beam. If needed, the timing circuits will be developed to incorporate these considerations.

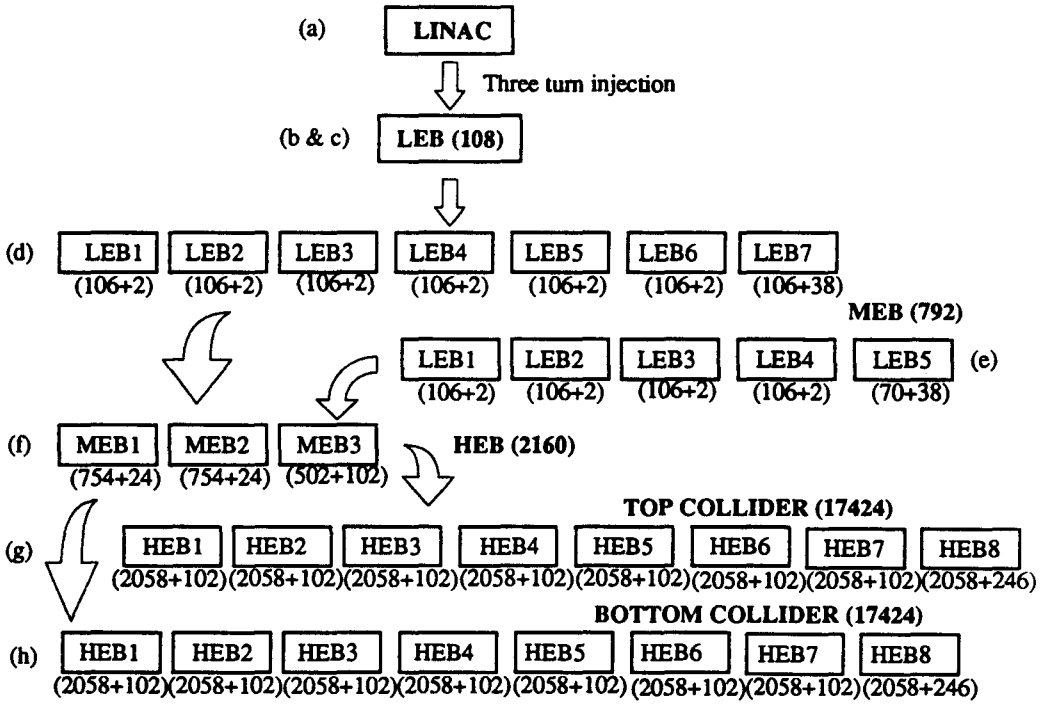

Figure 3. Filling sequency for collider operation.

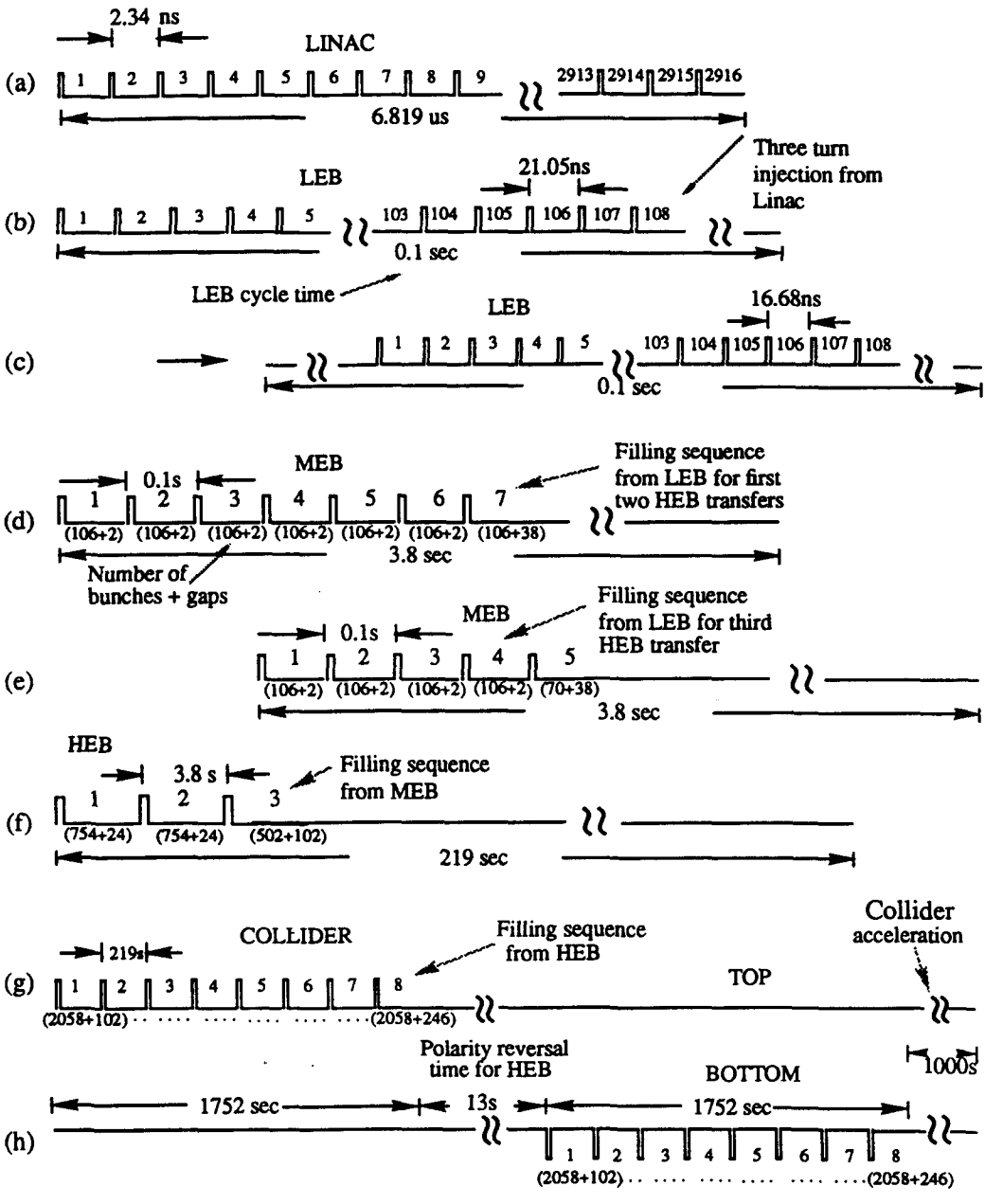

Figure 4. Filling sequence for collider operation with timing operation.

SYNCHRONIZATION SCHEMES UNDER INVESTIGATION

There are several ways to implement beam transfer synchronization. In previous proceedings of this conference we reported three schemes:[7] phase-control, phase-locking, and phase slippage. The phase-control and phase-locking schemes are very similar in principle, but they differ in their implementation. In simple terms, the phase-control approach involves measuring the phase information between the LEB and MEB reference rf waves (see Figure 5) and then estimating the error by subtracting the ideal values stored in the computer memory on a real time basis at every MEB revolution. The error is corrected by adding or subtracting a small frequency shift to the LEB DDS. Thus the LEB rf wave is forced to follow a pre-programmed trajectory. At the instant of transfer, the LEB rf wave has the same phase as the MEB rf wave with a constant phase offset. This offset is required because of the transfer line between the LEB and the MEB. With this approach we know in advance the MEB turn number at which a given LEB bunch is transferred. Since the frequencies are matched, the synchronization is expected to be smooth. In the phase-locking approach, the LEB and MEB frequencies are down-converted a few milliseconds before extraction.[1] The phase-locking throughout the acceleration, or at least half-way in the middle, is not possible with this method due to very large phase accumulation. Since the third transfer scheme involves offsetting the LEB frequency by about 1 KHz relative to the extraction frequency and waiting for phase coincidence points, we would need to have more electronics at the output end of the LEB DDS. A good phase detector between the LEB and the MEB rf signals can be considered to detect the phase coincidence points. In this particular case, we would need to keep the radial loop open. Alternatively, we can load a δR program from the workstation to the DSP to force the orbit to a desired position. This action will create a small frequency offset in the LEB frequency. Thus the global architecture outlined in Figure 1 can provide the necessary flexibility we need to try all the methods. A purely analogue approach does not give full flexibility to test the phase-control scheme.

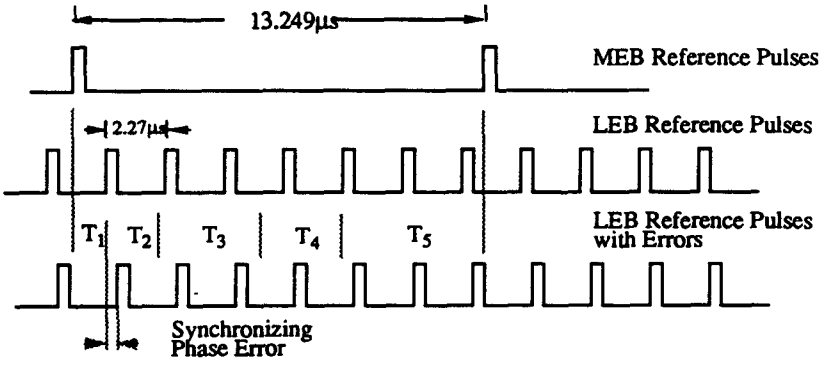

Figure 5. Basic timing diagrams of synchronization with a phase-control method.

Modelling equations for the beam synchronization loop and the radial position loop are derived in Reference 4 by assuming the cavities are well-tuned. The cavity detuning effects due to beam loading and the error due to phasing multiple cavities can be considered secondary to the multi-variable feedback loop model. Using the model, we expect to design a robust controller which would maintain the orbit shift to minimum value and also synchronize with the MEB. We expect to bench test the hardware with different feedback controllers and to simulate field errors. Recent hardware experience with such attempts is discussed below.

HARDWARE EXPERIENCE

The hardware configuration shown in Figure 6 is used to bench test the synchronization loop as a demonstration of the "proof of principle" of the phase-control approach. Later, the hardware will be extended to bench test the phase-locking and phase-slippage schemes with additional essential circuitry. In Figure 7 we show the schematics of the VME/CAMAC data acquisition system used to communicate with the DSP and other electronic modules. A SUN 4/330-based workstation is used as the mainframe computer to develop the assembly-level software for the DSP. Two 32-bit floating-point DSPs, TMS320C30, from Texas Instruments were used as the processing units. The C30 DSP board is made by SKY Computers. It has 2 MB of Dynamic RAM and the usual control registers to interface with the VME bus. All the communication to the UNIX workstation is done through the VME interface bus.

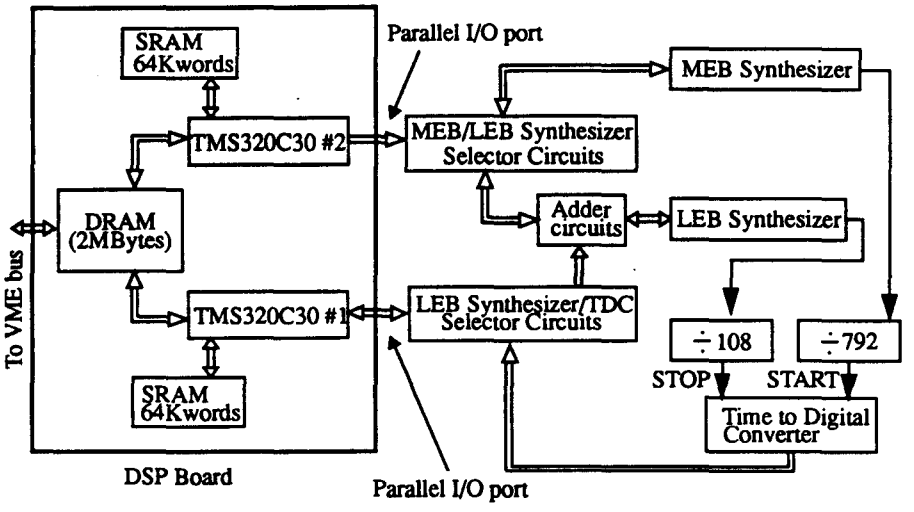

Figure 6. Schematic representation of the system diagram used to bench test the synchronization feedback loop.

The Static RAM used in the SKY board is only 64 K words long. Using C30 #2 on the SKY board, the MEB synthesizer is loaded with an appropriate number to generate the rf at the LEB extraction frequency. Then the same processor is used to generate the master frequency by reading the frequency data stored in the Static RAM and then launching it to the LEB frequency synthesizer at a specified time interval in real time. Since we have only 64 K words of static memory as a storage place for the frequency table, we set the time interval equal to 960 ns to cover 50 ms ramping time for the LEB. Even though the DSP board has 2 MB of global memory, we could not use this due to a memory refresh cycle invoked by the global RAM arbiter on a priority basis. We would like to see a DSP product which has as much as 2 MB or more Static RAM with zero wait states to further reduce the frequency updating interval to as low as 180 ns. It will be useful to ramp the frequency at small intervals so that the frequency jump required from the previous interval is small.

The counters, dividing by 108 and 792, represent the number of rf waves in one revolution of the LEB and MEB, respectively. The TDC measures the arrival time of the first LEB reference pulse after every MEB reference pulse. The data is then read into the C30 #1 and processed using the trip-plan and the feedback controllers explained in Reference 4 to

generate the frequency shift, $\delta f(t)$. The frequency shift is fed to the adder circuits on the interface board to correct the master frequency. The operation of the feedback loop is repeated every MEB turn, which is about 13.249 μs long. We expect to include a small phase error at the beginning between the LEB and the MEB reference waves. After we close the feedback loop, the loop will bring the phase error to zero. If the phase error is zero, then at a designated MEB turn we must have the phase synchronization for transfer (see Reference 4). Thus the result of this experiment is expected to demonstrate the ability to phase-lock the fixed frequency oscillator of the MEB during injection, to a variable frequency oscillator of the LEB from any given MEB turn.

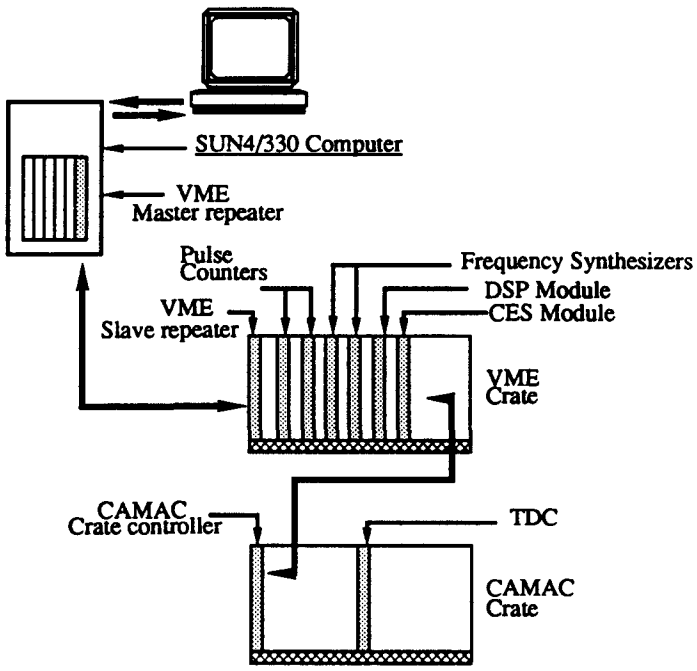

Figure 7. The hardware architecture with VME and CAMAC read-out system.

The TDC we have been using is made by Lecroy Corporation's Model 4204. In this module, the decoded time interval data does not appear instantaneously on the parallel port to read into the DSP. Also, the resolution varies from 0.156 ns to 2 ns in absolute terms. Hence there is inconsistency in the time measurement. Ideally, we would like a TDC to have a resolution of better than 30 ps with no time lapse for the conversion. The maximum time we expect to measure would not exceed 2.2 μs. The DDSs have advantages over the phase-locked loop VCOs due to the fine frequency resolution (1 part in 2^{32}). They have fast switching speed between output frequencies, and good spurious and phase noise performance. The phase discontinuity we have observed on some DDSs is the most undesirable behavior for our application. The discontinuities in the rf signal are normally due to lack of onboard synchronization of the clock and the frequency strobe signal. The best tool to test for phase discontinuity is the accelerator itself. However, we have carried out a simple test (Figure 8) in which we use two identical synthesizers. In the first approach, two DDSs are driven in parallel by the data such that the most significant bit is toggled to offset the frequency by 0.93 Hz. This test will enable us to look for the discontinuity when all the usable data lines on the DDS are fully loaded. In the second approach, they are driven in parallel by a counter. The second approach is used to test when the frequency is swept at a

certain rate. In our case we used the counter circuitry to sweep at a 1 MHz rate, although we could go much higher than this. The step size in frequency was again made to be 0.93 Hz by selecting one of the bits on DDS #2 to ground and the same bit on the other DDS high. The output of the two DDSs are then passed through a mixer. The mixer output is filtered using a low pass filter so that the original frequencies of the two DDSs, their harmonics, and their sum are removed. Only the difference frequency is recorded in Figure 9. When the two DDSs are running without the phase-discontinuity, the filtered output of the mixer must be a pure sinusoid with a frequency equal to the difference in frequency of the two DDSs. When there is phase jump in one DDS due to poor circuit layout or no synchronization, the mixer output shows discontinuities, as in Figure 9. This is undesirable for our application since the sudden phase change will lead into coherent oscillations, emittance dilution, and possible beam loss. Hence we are proposing to the DDS manufacturers to include this in their standard test procedures.

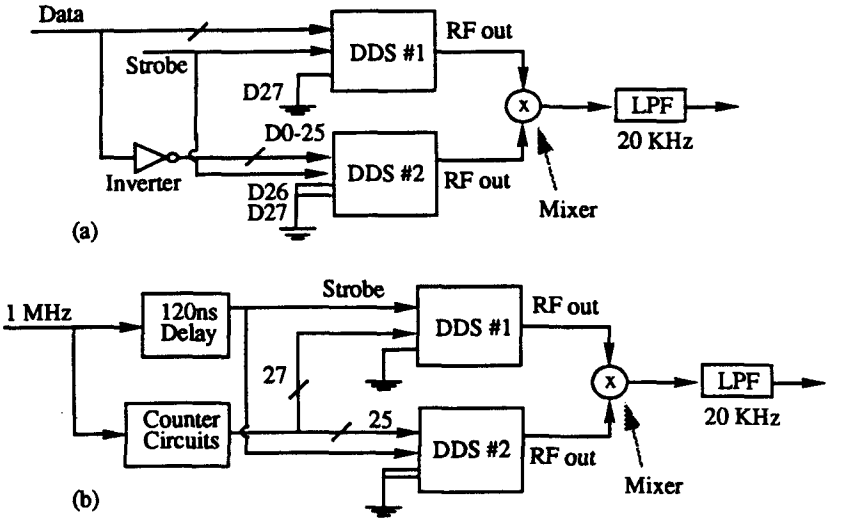

Figure 8. Test setup to observe phase discontinuities in the DDS.

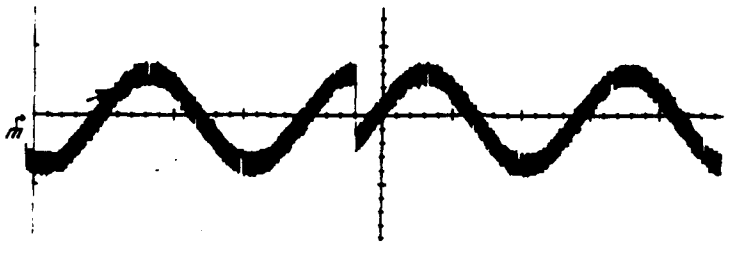

Figure 9. Output signal of the mixer (only difference frequency is retained).

CONCLUSIONS

We have shown in this paper the hardware architecture involved in producing master frequency to the SSC Low Energy Booster which is controlled during capture, ramping, and extraction. The hardware architecture we have proposed allows an environment to test all the transfer schemes under consideration. The radial feedback loop hardware is considered in the system to control the beam orbit due to field errors. The B-field loop to the master frequency

oscillator is included to bench test the synchronization loop by imposing random errors in the field signal. The heart of the system consists of Digital Signal Processors and Direct Digital Synthesizers. We would need a DDS to have a spur suppression of up to 70 dB with the possibility of phase modulation included to the rf signal. Because of its speed, the DSP executes feedback control algorithms well. With our existing DSP hardware, we would have difficulties in accessing the processor without interrupting the real time operation. By using the radial position signal and the synchronizing phase signal in a single processor, we can implement a global feedback controller which would produce an optimum frequency and the phase shift to control both parameters. Since this approach is still theoretical, we are proposing to simulate the feedback scheme under various practical limitations. However, should there be unexpected problems, the configuration can be easily tailored to include more conventional frequency and phase-control schemes used in other accelerators.

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