SSC PC-025
89 PAGES

SSC DETECTOR R&D PROPOSAL

DEVELOPMENT OF TECHNOLOGY FOR PIXEL VERTEX DETECTOR

University of California at Berkeley -
Space Sciences Laboratory,
University of California at Davis,
Hughes Aircraft Company,
University of Iowa
Iowa State University,
Lawrence Berkeley Laboratory,
University of Oklahoma
University of Pennsylvania
Princeton University
Stanford Linear Accelerator Center
Yale University

October 2, 1989

Collaboration Members

1. **UCB-SSL:** John Arens*, Garrett Jernigan
2. **UC Davis:** David Pellett
3. **Hughes Aircraft Company:** Frank Augustine, William Flaugh, Gordon Kramer, Carl Pfeiffer, Ken Reyzer, David Wiggins, John Winterberg
4. **University of Iowa:** Ed McCliment
5. **Iowa State University:** John Hauptman
6. **Lawrence Berkeley Laboratory:** Steve Holland, David Nygren*, Helmuth Spieler, Michael Wright
7. **University of Oklahoma:** Phil Gutierrez, Pat Skubic
8. **University of Pennsylvania:** Nigel Lockyer
9. **Princeton University:** Kirk MacDonald
10. **SLAC:** Stephen Shapiro
11. **Yale University:** Paul Karchin

* Contact Persons

Contents

1 Executive Summary **7**

2 Introduction **9**

3 Relevance of Pixel Vertex Technology to the SSC **11**

3.1 Overview 11

3.2 Intermediate P_t Physics and Vertex Detection 11

3.2.1 BCD Vertex Detector 13

3.3 High P_t Region and Vertex Detection 16

3.3.1 SDE Vertex Detector 16

4 Technical Discussion **20**

4.1 System Design Process 20

4.2 Design, Fabrication, and Test of a Prototype Pixel Detector 22

4.3 Design and Fabrication of the Control and Data Acquisition Electronics 23

4.4 Pixel Detector Tests 24

4.4.1 Laboratory Tests 24

4.4.2 Radiation Damage Studies 25

4.4.3 Beam Tests 26

5 Technical Progress Summary **29**

5.1 UCB/SLAC/HUGHES Generic Program 29

5.1.1 Device Summary 29

5.1.2 Device Evaluation 29

5.1.3 Device Design and Simulation 32

5.1.4 Conclusion 32

5.2 LBL Technical Progress 37

5.2.1 A Robust High-Temperature Detector Fabrication Process . . 37

5.2.2 Monolithic Integration of Circuitry and Detectors 37

5.2.3 Low-power Low-noise Analog Circuitry Optimization 38

5.2.4 Radiation Damage Studies of Detectors and Circuitry 38

5.2.5 PIXSTRIP, a design study for a smart pixel array 38

6 Statement of Work and Budget Summary **40**

6.1 **Hughes Aircraft Company** 40

6.2 **Lawrence Berkeley Laboratory** 40

6.3 **UC Berkeley - Space Sciences Laboratory** 41

6.4 **Stanford Linear Accelerator Center** 42

6.5 **University of Oklahoma, Yale University, and University of Iowa** 42

6.6 **UC Davis and Iowa State University** 43

6.7 **University of Pennsylvania, Princeton University** 43

7 Budgets and Schedules **45**

8 Appendices **50**

8.1 HUGHES AIRCRAFT COMPANY CAPABILITIES 50

8.1.1 MOSAIC ARRAY DEVELOPMENT 55

8.1.2 ORGANIZATIONAL RESOURCES 56

8.1.3 FACILITIES 56

8.1.4 KEY PERSONNEL RESUMES 63

8.2 A READOUT DESIGN FOR HIGH FLUX ENVIRONMENTS . . . 66

8.3 SILICON PIN ARRAY PAPER 67

8.4 A SET OF POSSIBLE READOUT DESIGNS 68

1 Executive Summary

- **Proposal Objectives:**

  This proposal covers the 12 month first phase of a 36 month program to demonstrate key technical performance requirements for silicon pixel vertex detectors for the SSC. The effort addresses differing needs for high P_t and intermediate P_t experiments such as those studied by two different groups, the Solenoidal Detector Experiment (SDE), and the Bottom Collider Detector (BCD).

  During the first year, system design concepts will be developed, a preliminary system cost analysis will be performed, and prototype hybrid detectors will be designed and fabricated. Beam tests on the pixel detectors will be performed, and special test equipment will be designed and built to operate the prototype arrays. The principal objective of this first phase is to demonstrate the technical and cost feasibility of pixel detector systems for the BCD and the SDE. After the full 36 month term, final design verification and key hardware elements will be demonstrated; beam tests of detector arrays will demonstrate readiness for full scale engineering development.

- **Team Description:**

  The SSC places severe performance requirements upon detector technology, requiring new and imaginative solutions in many areas such as tracking and vertex detection. A team approach coupling the high energy physics community and industry is essential to establish realistic technical requirements, develop an appropriate systems architecture, provide rapid evaluation and test beam results, and optimize the overall system performance for an acceptable cost.

  The industrial partner, Hughes Aircraft Company, is a recognized leader in both pixel array design and sophisticated electronic system fabrication. Pixel detector arrays in a 10×64 format and in a 256×256 format have already been built and initial test data is presented in this proposal. The physics research members of the team combine technical expertise in semiconductor devices and extensive and varied experience in high energy physics research. BCD and SDE, the major SSC initiatives reflecting this experience, are well-represented in this collaboration.

- **Key Elements of the Proposed Program:**
  - Early appraisal of system feasibility and cost issues reduces risk;
  - Early involvement of industry will increase rate of progress toward a final system and introduce sophisticated management practices;
  - First year effort addresses wide range of physics requirements;
  - Coordinated effort by all key members of physics community eliminates duplication of effort and ensures good communications.
  - Prototype pixel arrays with sparse readout circuitry will be designed and built for testing and evaluation.
- **Total Phase One Cost for Proposed Program : $1,190,000**

2 Introduction

For the SSC, silicon pixel detectors offer the attractive prospect of highly unambiguous pattern recognition, high spatial resolution, high radiation tolerance, and fast time response, which are essential qualities for vertex detection and tracking close to the beam pipe. The extremely challenging physics and background environment of the SSC would appear to make all other known detector concepts inferior to a pixel detector for this purpose. Much of the basic semiconductor technology needed to realize pixel detectors suitable for the SSC already exists, and significant advances in pixel detector designs have been achieved during the current SSC Generic R&D program. Nevertheless, to meet projected SSC schedules for detector construction, a substantial effort is needed now to realize the progress needed to achieve the required technical performance and to establish budgetary requirements for these detector systems.

Within the broadest context of SSC physics, there are perhaps three or four distinct categories for pixel detector applications. High P_t physics, with a wide variety of physics signatures, requires a complex two-level trigger structure, that has substantial impact on the pixel array architecture. Intermediate P_t physics, on the other hand, places emphasis on very rapid readout of detector information after a single relatively short trigger decision interval. A third category includes more specialized physics goals such as exotic particle searches where high quality ionization density information as well as spatial resolution is required. Finally, it has been recognized that the pixel arrays we intend to develop are very well matched to a possible solution (in conjunction with an image intensifier) for the rather daunting readout system requirements for a scintillating fiber detector at the SSC. While the pixel array characteristics needed for all four categories may overlap substantially, only the first two categories are addressed directly in this proposal.

To facilitate rapid progress in the development of silicon pixel vertex detectors, a sizable collaboration including an experienced industrial partner has been formed. In large part, the proponents are associated with the BCD and SDE groups, which have undertaken substantial efforts to evaluate the detector requirements for the intermediate and high P_t SSC physics contexts respectively. Through these associations, the technical goals of this collaboration will maintain the closest possible relationship to the requirements associated with the high and intermediate P_t physics of the

SSC. The collaboration is entering into a teaming agreement expressing our collective intention to work together through the construction phase of SSC detector systems.

The current proposal presents in detail our plan for the first year of what is foreseen as a three year program to reach a rather complete engineering demonstration. The development program for the following two years, including an approximate estimate of budgetary requirements, is given in broad outline.

3 Relevance of Pixel Vertex Technology to the SSC

3.1 Overview

The SSC will provide a window into an entirely new and uncharted physics domain. In order to best exploit the discovery potential of this instrument, interactions must be studied in sufficient detail to separate rare or unexpected processes from the ferocious backgrounds characteristic of the SSC. New physics processes are expected to generate heavy quarks and leptons as decay products much more frequently than known QCD processes. Heavy quarks will be copiously produced, offering an opportunity for the study of the mechanism of CP violation and rare decays. On a more mundane level, a consequence of the high design luminosity is a high probability of more than one interaction per beam crossing. It is clear that the ability to measure vertex structure is an essential although extremely difficult technical challenge.

There exists to date no silicon vertex detector in an e^+e^- machine or hadron collider, though efforts are underway to install such devices in several experiments, like CDF at Fermilab, MarkII at SLAC, and Delphi and Aleph at CERN. These first generation detectors all use silicon strip technology and newly developed VLSI circuits mounted on the detector for amplification and readout processing. The SLD vertex detector at SLAC will be a CCD device with very a slow readout.

3.2 Intermediate P_t Physics and Vertex Detection

The BCD experiment is a program of physics that will study intermediate and low P_t physics at the SSC. It is hoped that the BCD can begin taking data at Fermilab in the mid 1990's with some of the detector systems. The complete experiment will be a first round detector at the SSC. The physics goal of this experiment is the complete and thorough study of the CP violating decay modes of the B meson. Only B mesons that decay to all charged states are considered. CP violation has great importance within the standard model and is a subject of much interest for

theorists and experimentalists. The following is a list of some of the interesting physics questions that can be addressed with a detector at the SSC that has a powerful vertex detector.

1. Cosmological models invoke CP to help explain the matter-antimatter asymmetry in the universe. Thus the existence of the universe is thought to be related to CP in some way.

2. Multiple Higgs bosons can lead to relative complex phases that in turn have CP violating effects. Thus the understanding of mass generation and CP is related.

3. CP violation is important to the generation puzzle. With two families there is no CP violation in the Standard Model. All existing data is consistent with three families or one complex phase. If there are four families, then there are three complex phases and new CP phenomena are expected.

4. Measurements of CP violation in the B system can overconstrain the C-K-M matrix.

5. Left-right symmetric models predict small CP violating effects in the B system.

6. There is some hope that if the C-K-M elements are well determined it will be possible to observe symmetries in the mass matrices of the quarks and therefore Yukawa couplings.

7. The Standard Model is a parametrization of experimental data. It provides no insight into the origin of CP violation. Further study of CP violation in the K system and information from a new system may provide valuable information far beyond the standard model.

8. The search for Higgs particles that decay into $\bar{b}b$ is made possible with a vertex detector. Technicolor mesons can decay to $\bar{b}b$ as well.

9. In summary, many fundamentally important physics topics are within reach of study at the SSC if a vertex detector of sufficient performance can help extract the B signal.

3.2.1 BCD Vertex Detector

Introduction The emerging opportunities to study B physics at the SSC are primarily a result of the advancement of silicon vertex detector technology. It has been understood for some time that the SSC could produce of order 10^{12} $\bar{b}b$ pairs per year. The experimental challenge is to fully reconstruct the B meson invariant mass from its decay products. There are 2-6 charged tracks from the B meson and typically over 100 charged tracks in the event. Fortunately the B lifetime is sufficiently long that the decay vertex can be separated from the beam collision point using a precision vertex detector. The invariant mass is then calculated using only tracks coming from a secondary vertex. Techniques like this have given rejection factors of up to 10^6 in some decay channels in low rate fixed target experiments.

The most relevant work for BCD is that of the CDF group. However, in order to reconstruct fully the B meson mass with high efficiency over a large solid angle, the BCD vertex detector design is significantly more complex. The requirements are described in the following sections.

Vertex Detector Requirements The BCD must build the best vertex detector possible if it is to achieve success at the SSC. If the vertex detector does not work well, the experiment will be severely compromised. The BCD vertex detector should determine the impact parameter of charged tracks with respect to the decay vertex to less than $10\mu m$ rms error. The multiple scattering error on the track is proportional to $R/P_t\sqrt{L/L_0}$, where R is the radius to the first detector plane, P_t is the transverse momentum and L/L_0 is the percent radiation length. To meet the required resolution goals, the vertex detector inner layer must be placed at R$\sim$ 1.25 cm. This short distance is necessary because the average P_T of tracks from B decay at the SSC is less than 1 GeV/c. Furthermore, there is much incentive to minimize the amount of material and the Z of the material. Beryllium is therefore a common choice for the support material.

The radiation damage tolerance for gamma rays must be greater than or equal to 10Mrads. If luminosities above $10^{32}cm^{-2}sec^{-1}$ are required to study smaller than expected CP asymmetries, a higher radiation resistance will be important. The neutron flux in BCD may be less than detectors with 4π steradian hadron calorimetry

coverage, but BCD has substantial iron in the magnet yokes and muon detection system. A better estimate of the neutron flux in BCD is needed.

An important design factor will be the hit occupancy. This may ultimately determine the pixel readout system and the highest luminosity possible in the vertex detector. A sophisticated simulation of the silicon vertex detector is underway by the BCD group and will contribute to design considerations in the next couple of months. The pattern recognition strengths of a small pixel device must be traded against the difficulty in manufacturing the electronics for each pixel as the size decreases below $100 \times 100\ \mu m^2$.

The following is a list of mechanical issues that the BCD vertex detector group must address in the coming months with simulation and tests. This overall system mechanical design specification is underway. We list issues and raise questions that require examination during the performance period of this proposal.

1. The vertex detector is envisioned as being constructed with self-supporting modules. The silicon detectors would be glued into a polygon matrix. The modules would then be mounted to an externally supported structure called a "gutter". It is the gutter philosophy and alternatives that require examination as part of the work of this proposal. Ref. Fermilab TM-1616 Jostlein et al.

2. The alignment accuracy can be considered in two parts. The initial alignment of detectors with respect to each other and the support structure (the gutter) during and after assembly must be specified. The long and short term drifts due to heating from the amplifiers must be simulated in order to understand the limits of an acceptable tolerance specification. It is estimated the x-y accuracy must be $\leq 4\mu m$, while the accuracy in Z may be $\leq 200\mu m$ over the length of the gutter.

3. The assembly procedure needs to be studied.

4. The cooling requirements may feed back into the electronics design. An efficient cooling system, capable of extracting 2-5 kW of power will permit a lower noise amplifier design. The cooling will be gas and liquid.

5. The issue of operating below room temperature, *e.g.* zero degrees, must be studied. This will reduce leakage currents in the detector.

6. Material from connectors and cables are a major source of scattering. Fiber optics should be studied as an alternative signal transfer technique even if power dissipation is higher.

The electronics issues for BCD are similar but perhaps more severe than those for SDE, primarily because of two reasons. First, the required resolution for BCD must be $\leq 10\mu m$. This suggests a pixel size of $\sim 30 \times 30\mu m^2$. The subsequent area available for electronics is roughly an order of magnitude less for BCD than SDE. Secondly, the noise level required is driven by the dipped track problem, ie. small deposition of charge for high angle of incidence tracks. A high efficiency for detecting tracks that deposit ≤ 6000 electrons is necessary. Even so, this places a 45° track cutoff angle of incidence. The remaining issues and questions are listed.

1. A further consideration driving the low noise goals of the electronics, ~ 50 electrons rms noise per pixel, is the very large number of noise hits in a system of $\geq 10^7$ pixels.

2. The radiation damage effects are similar for BCD and SDE, but if BCD runs at higher luminosity, this changes. The higher luminosity running will be determined by the magnitude of the CP asymmetries. Also, the proximity of the silicon to the beam during injection may give large damage, as experienced with UA2.

3. The BCD wishes to read out the vertex detector every few microseconds, in contrast to SDE. The readout designs may be different.

4. The resetting philosophy of the pixels for the two experiments may be different. If the reset frequency is too small, pixel occupancy becomes excessive. This may be more severe for SDE if the level 2 wait time is $\geq 50\mu$sec.

5. The bunch crossing tagging procedure must be defined.

6. The advantages of driving analog versus digital signals needs investigation.

7. Centroid finding techniques are of great interest to BCD because the dipped tracks give up to 60 hit pixels.

3.3 High P_t Region and Vertex Detection

For a complete tracking detector, a high resolution, radiation hard detector array is needed near the SSC beam to tag b's and τ's and to allow lifetime measurements of new long-lived particles[1]. Such detectors are needed for track reconstruction and accurate dE/dx measurements to search for free quarks in the cores of jets[2]. In addition, the detector provides accurate separation of tracks coming from different primary interaction vertices in a single beam bunch crossing.

The following are some representative physics goals for the vertex detector in the central rapidity region:

(a) Tagging of secondary vertices in the search for an intermediate-mass Higgs boson decaying via the $b\bar{b}$ or $\tau\bar{\tau}$ channels. The detector is also valuable for reducing backgrounds by anti-tagging in other Higgs mass regimes.

(b) Tagging isolated leptons from W decays to reduce background from QCD jets and photon conversions to e^+e^- pairs. This is needed, for example, to study WW scattering or heavy Higgs decay via the channel $W(\rightarrow l\nu) + W(\rightarrow jets)$.

(c) Improvement in the signal to noise ratio in high-mass top quark searches. Possible decay chains of interest are, *e.g.*, $t\bar{t} \rightarrow be\nu\bar{b}q\bar{q}$ or $t\bar{t} \rightarrow e\nu\mu\nu b\bar{b}$. The b's may be fairly soft, so the pixel tracker can help here.

(d) Accurate measurements of the physics processes involving the copiously produced b quarks.

3.3.1 SDE Vertex Detector

Introduction In large part the general characteristics of the BCD vertex detector also apply to the SDE vertex detector. Rather than repeat those, we elaborate on the specific characteristics needed for the SDE.

A major difference is that the SDE vertex detector must coexist with and be integrated with a much larger and very complex tracker, which we presume here to be a silicon-based system. As such, it may be expected that systems engineering considerations will play the dominant role in the ultimate physical configuration and general electronic architecture.

A useful definition of a pixel detector is that the subdivision of detection elements has been increased to the maximum practical extent consistent with the intrinsic spatial resolution. A consequence of this extreme subdivision is that the hit rate of individual pixel cells is typically a few hundred Hz. This is true even for rather large pixels such as 100 x 100 μm^2 close to the beam line at full design luminosity. In turn, this low hit rate allows the pixel to be used as its own buffer for either analog or digital information. This powerful but paradoxical fact is the central concept for the systems architecture of the pixel detectors considered in this proposal. At the same time, this feature places stringent limitations on the length of time data can be maintained without compromise from pileup effects; it also introduces complexity in the relationships among deadtime, pixel reset, and circuit design.

A "smart pixel" concept has been developed by D. R. Nygren and H. Spieler to match the SDE requirements; a further elaboration of this concept and other issues can be found in appendix 8.2, which is a reprint of a report given at the Snowmass 1988 meeting.

Vertex Detector Requirements The SDE vertex detector is envisaged to provide tracking within a range of $\pm$ 2.5 units of rapidity, matching the general range of tracking for the detector systems at larger radii. Physically, this translates into an extent along the beamline of about $\pm$ 50cm for a 10 cm outer radius for the pixel vertex detector. The inner radius may well be constrained by background and rate limitations to a radius not less than 4 cm.

The minimum number of layers needed is generally regarded as three; this number in principle provides some constraints for elementary track finding. As more realistic simulations are performed, adding backgrounds, delta rays, deadtime, and other real-life effects, it can be expected that the minimum number of layers increases to four. Detailed and carefully executed simulations are an essential part of the process leading to a stable system architecture.

The rather long luminous region ($\sim$ 7 cm) along the beam direction has an impact on pixel geometry. Particularly in the very central region, a large range of track angles through a given pixel will exist, on the order of $\pm 45°$. Given a standard detector thickness of 250-300 μm, this range translates into a similar "natural length" for deposited energy in the beam direction. Ionization fluctuations will be substantial along the projected track length. The consequence is that a pixel cell substantially smaller than 200 μm will receive relatively small

fluctuating signals that cannot be used to improve the resolution. From this perspective, a pixel cell has a similar natural length that can be used for needed circuit functionality.

On the other hand, resolutions of 4-5 μm are desired in the spatial dimensions transverse to the beam. Experience with strip detector systems has indicated that this level is achievable with widths on the order of 50 μm. For detector sizes of this scale, diffusion and ionization processes contribute to an intrinsic spreading of charge that can be used to improve resolution using analog information. Therefore, a rectangular pixel on the order of 40 x 200 μm is an attractive possibility.

The orientation of the pixel array can be chosen to be normal to the center of the luminous region to minimize track obliquity. This leads to another beneficial result for the distribution of the pixel arrays along the beam direction. For progressively larger values of rapidity, the pixel arrays are increasingly angled, leading to a kind of "Fresnel cylinder" configuration that permits a considerable gap between one ring of arrays and its neighbors without loss of efficiency for all but the very lowest momenta. This significantly reduces the number of arrays needed to provide coverage as compared with a configuration in which the arrays are not angled. Unfortunately, an adequate drawing illustrating this Fresnel concept is not yet available.

Calculated power dissipation for each layer of this pixel array is on the order of 100W. Removal of this heat with a reliable low-mass technique is a very serious mechanical engineering challenge. At the same time, the low-mass support structure must incorporate complete power distribution, trigger, timing, data bus, etc. connectivity. Probably the successful realization of needed functionality within the severe physical constraints will be the most challenging aspect of a complete SSC vertex detector.

The trigger for the SDE will be a two-level hierarchy as far as detectors are concerned. Level one may occur on average every 100 crossings with a synchronous accept/reject occurring about one or two microseconds after the crossing. The greater the delay in forming this trigger, the more silicon must be devoted to storing pattern information. It is imperative that this time interval be kept to a realistic and stable minimum, and made immune to gradual increases due to "improvements". Level two is expected to provide another factor of about 100 in rejection, but the latency is variable, perhaps even greater than 30 μsec. Given current uncertainties in knowledge of background rates, there is a danger

that pixel information could be contaminated for very long level two trigger latency. Simulation of this will be an important part of the information needed to choose sensible system architectures and pixel cell designs.

If pixels can store information, they must also have the means to clear information at appropriate intervals. A system-wide reset can be easily envisaged, but this must occur more frequently than the level two accept, as the arrays will likely become too heavily "occupied". A system-wide reset occurring after level one accepts (keeping the needed information) will introduce excessive deadtime. It appears possible to selectively reset only those pixels falling out of the accept time window. Clearly, the reset question will be an important issue.

The issue of radiation damage has two main branches, one for the detectors and the other for the readout IC's, which have quite different aspects.

After SSC operation is underway, the leakage current generated by the detectors will become hundreds of times greater than at first. One concern is stability against breakdown, which will benefit from a robust process such as that developed at LBL. Another concern is that the dark current will contribute integrated charge comparable to or greater than that of charged particle tracks. This indicates the need for detectors with AC coupling to the preamps. LBL is developing the means to provide robust high resistance polysilicon resistors to bleed off the pixel leakage current to ground and the capacitors needed to isolate preamp voltage offset. At the extremely high fluences corresponding to years of SSC operation, there is little information about charge collection and trapping effects. LBL, in collaboration with others, is pursuing a systematic radiation damage evaluation program.

References

[1] Report of Large Solenoid Detector Group in Proceedings of the Workshop on Experiments, Detectors, and Experimental Areas for the Supercollider, p. 340 (1987).

[2] Exotics Group Summary Report in Proceedings of the Workshop on Experiments, Detectors, and Experimental Areas for the Supercollider, p. 853 (1987).

4 Technical Discussion

4.1 System Design Process

To determine the feasibility of a pixel vertex detector for the SSC several basic questions must be answered:

(a) What are the radiation background characteristics in which the vertex detector must operate and how do these background fields determine radiation hardness requirements?

(b) What are the physical constraints (*e.g.* multiple coulomb scattering and photon conversion limits, ...) that a vertex detector must match?

(c) What are the spatial resolution and track-pair requirements?

(d) What are the timing resolution requirements for track tagging?

(e) What are the trigger requirements and how do they affect system architecture?

(f) What are the data readout requirements and how do they affect system architecture?

The answers to these questions are at least partially known; given this much, then the questions resolve to technical issues:

(a) Are high speed, low power, radiation hardened detector and readout assemblies practical with current technology?

(b) Can an efficient data collection and processing system be devised which can accommodate these assemblies?

(c) Can a stable low-mass mechanical and cooling system be built?

The proposed work addresses these questions from both a technical and a cost viewpoint.

The proposed program will consist of three main activities: the design, simulation, and fabrication of a prototype detector and readout array, the simulation and development of a signal and data processing architecture, and a conceptual design for the entire system. The efforts for the pixel array development are discussed in detail elsewhere, but the prototype design and simulation will influence and be impacted by the work done in the other parts of the proposed

effort. For example, the functions and features which will be incorporated into the initial prototype will be those which are necessary to validate the prototype as a proof of concept. These features will be determined by a review of the existing concepts by the team. This task is complicated by the diversity of physical processes investigated by the different collaborators. These concepts will be examined to distill the essential technical features which are common to the various concepts and which will enable a decision to be made as to the feasibility of the pixel array vertex detectors.

With an initial pixel array architecture determined, the question of system feasibility can be addressed. In order to perform this evaluation a candidate system design must be used. Representative quantities will be used to arrive at one or more system configurations, from which a design may proceed. The first step in developing a system design is determining a data collection plan. This plan will detail how the data collected by the pixel arrays will be used to accomplish the track reconstruction. This plan will be the roadmap for the signal and data processing design. The data collection plan will address the various trigger configurations so that such quantities as data rates and buffer sizes may be determined. In addition, the data collection plan must address the track reconstruction algorithms. The reconstruction algorithms will influence such system level components as pixel size, number of pixels, signal to noise ratio, and digitization accuracy. By developing such a data collection plan, system architectures may be developed which take advantage of signal preprocessing, thereby reducing subsequent data acquisition and storage requirements. After the data collection plan is defined a simulation model will be developed which will allow design tradeoff studies to be conducted. The goal of such analysis will be to determine the minimal system configuration necessary to achieve the physics goals.

Finally, a complete system design will be performed to assess cost and lifetime considerations. The system design will cover mechanical packaging, detector layout, cabling, cooling, shielding, and other matters that need to be studied to identify technology and cost drivers.

The first phase 12 month program proposed herein is shown in Figure 2. Provision is made for regular technical interchange meetings at 2 and 3 month intervals with all principal members of the team involved in pixel detector development. The proposed readout design will be thoroughly reviewed at a concept design review, preliminary design review and final design review before initiat-

ing wafer fabrication. This review process will assure that the critical readout requirements necessary to demonstrate technical feasibility for both the BCD and SDE experiments are being addressed.

A number of readout designs have been proposed and these will be thoroughly analyzed so that feasibility can be assessed:

4.2 Design, Fabrication, and Test of a Prototype Pixel Detector

The objective of the fabrication task is to fabricate prototype detector arrays whose performance can be measured and compared against SSC goals. Experience gained in the prototype development will then be utilized in the development of the full scale system.

Following the development of the conceptual design described in the previous section, a detailed design must be produced. The detailed design development comprises two broad areas of activity, technology selection and circuit development. There are several device technology candidates which could be used in the development of a prototype array. Silicon MOS technology offers very low power and reasonably high speed. It is inherently hard against neutron radiation, and can be hardened against total dose radiation. Bipolar technology offers speed advantages over MOS, but at the expense of somewhat higher power. Bipolar devices are extremely hard to total dose but suffer some degradation in neutron environments. Unipolar devices, such as JFETS and MESFETS, offer further speed enhancements when fabricated in high mobility material such as gallium arsenide. Their radiation hardness is similar to that of bipolar transistors. Finally, it may be desirable to employ a BICMOS process, which is a merger of MOS and bipolar technologies on the same chip.

This allows the use of low power MOS circuitry in power critical areas, while having bipolar transistors available for portions of the circuit which require high drive capability.

The following requirements were agreed upon for the first prototype hybrid pixel readout. These requirements were considered generic to both the SDE and BCD experiments. They are appropriate for a first year demonstration to demonstration to demonstrate the technical feasibility of pixel detector arrays;

(a) Power from 100 mW per square centimeter to 1000 mW per square centimeter.

(b) Readout time of approximately 1 μs per hit

(c) Tag time about 10 ns

(d) Radiation hardness in excess of 1/2 megarad

(e) Noise level of 200 electrons rms

These specifications are believed to be a reasonable and conservative set of first year goals. Substantially better performance is expected over a longer time period as progress is achieved.

The completed prototype arrays will be subjected to a variety of tests in order to verify their performance. Initially, the readout ICs, are tested at the wafer level in order to determine whether the design is functioning correctly as well as to identify candidate parts for dicing, packaging and performance testing. Following wafer level testing, candidate parts will be hybridized to detectors and packaged for performance testing. The devices will be operated at speed using a pulsed laser as an excitation source. Such a setup will enable a full range of diagnostic and performance testing to be performed.

Following the diagnostic testing and performance verification, parts will be delivered to the appropriate university and laboratory researchers for further testing and initial tracking experiments.

4.3 Design and Fabrication of the Control and Data Acquisition Electronics

Electronics to power and clock the existing 10×64 arrays will be built for long duration radiation tests. These tests will be performed at UC Davis and one or more of the following institutions: SLAC, Los Alamos, University of Tennessee at Knoxville, and Hughes Aircraft as described in the *Pixel Detector Tests* section. It is too costly to assign the complex data acquisition system to this task as it must be available for beam tests.

Electronics will also be designed and built to operate the new detector arrays that will be built as part of the work described in this proposal. The sparse readout scheme of the new detectors will be quite different from the random access readout schemes used in the existing 10×64 and 256×256 arrays. Work

on designing this control and data acquisition electronics must proceed simultaneously with the pixel array readout electronics. The electronics will be based as much as possible on the electronics design that is used to operate the existing detectors. The existing system matches a set of computers and processors to the several tasks. Calculation speed and real time capability are the most important features of the processors. Custom built circuits using state machines, shift registers, and other digital components will be built if speed requirements make them necessary. The software for the system will be written in parallel with the hardware design and fabrication work to more fully ensure the system will work and to complete the system rapidly.

4.4 Pixel Detector Tests

The testing program for pixel detectors will involve

- laboratory tests,
- radiation tests, and
- beam tests.

We propose to combine relevant ongoing individual generic R&D programs in order to bring a coherent and efficient effort to bear on the problems. Beam tests using pixel detectors and silicon microstrips will allow us to evaluate the performance of the pixel detectors themselves as well as that of a combined system of pixels and microstrips in an accelerator environment.

4.4.1 Laboratory Tests

Testing in the laboratory is aimed primarily at characterizing the performance of the devices and optimizing them for high energy physics applications. Typical issues here are:

- signal to noise ratio
- stability of performance characteristics
- spatial and time resolution
- effectiveness of readout architecture.

Continued testing of the existing devices from Hughes, a radiation hard 10×64 array with 120 μm square pixels, and a 256×256 array with 30 μm square pixels, is an essential preliminary step in this effort. This will be funded in part by the existing generic R&D program.

The new pixel device must be tested to insure that the presence of data is signaled sufficiently rapidly (within $\sim 10ns$) and that data is capable of being read out at speeds consistent with SSC requirements. A new data acquisition and control system is required for these tests in order to run the device at design speed. Funding for the development of this system (including both the hardware and the extensive software) is contained in the SSL budget.

4.4.2 Radiation Damage Studies

Radiation testing of the devices is necessary to insure that they will be capable of enduring the high neutron and charged particle fluences expected in the SSC environment. The charged particle dose rate at a radius of 10 cm from an SSC high luminosity intersection point is estimated to be $\sim 3 \times 10^3$ Gy/year. The flux of neutrons back-scattered from the surrounding calorimeter is estimated to be comparable in magnitude and more serious in terms of radiation damage. Hence the performance of the the detectors and the hybrid readout circuitry must be reliably characterized with respect to both displacement damage and long term ionization effects. These tests would proceed most rapidly and efficiently if they utilized the device test beams at the 68 MeV UCD cyclotron and proposed radiation testing facilities at SLAC. The latter would provide a ^{60}Co source and a ^{252}Cf neutron source plus personnel for management of dosimetry[1]. If this does not materialize, then an alternative such as Los Alamos may be needed for long-term neutron exposures and facilities at the University of Tennessee at Knoxville (UTK) or Hughes for ^{60}Co sources or X-rays.

Irradiation by neutrons and by gamma rays can be viewed as the two extreme tests. Irradiation by fairly ionizing protons is useful in that it produces a mix of ionization and displacement effects, as will be the case at the SSC. Furthermore, recent studies of displacement damage as a function of energy with a variety of incident particles indicate that in many situations, the resulting effects can be accurately scaled from one energy and particle type to another[2]. Hence a program of testing at the UCD cyclotron is proposed. This facility is regularly employed for tests of radiation damage to semiconductor devices by a variety

of users. Proton energies are available up to 68 MeV with a maximum flux of 2.5×10^{14} protons/s. Typical dose rates in actual tests are of the order of 20 Gy/s spread uniformly over a 40 cm^2 area. Well-calibrated instrumentation exists for dosimetry and monitoring the areal uniformity of the beam. Readout and control electronics can be placed in the radiation cave behind shielding blocks near the equipment under test. Remote control systems can be located within range of a 30 m cable run. A further potentially useful diagnostic tool is the *proton microprobe*—a 4.5 MeV beam 5 μm in diameter with a flux of up to 1.3×10^{10} protons/s. Work is taking place at present to extend the microprobe energy to 40 MeV although with an increased diameter of 30 μm. Such a beam could be used to test specific areas on a chip for sensitivity to radiation. Various neutron beams are also available.

The existing radiation hard 10×64 array will be the principal subject of these tests during the first year of this program.

The funding for these tests is contained in the budget requests of UCD, SLAC and OU. It should be mentioned here that if long-duration radiation tests are to be performed, dedicated electronics to power and clock the devices must be fabricated. It is too costly to assign the complete data acquisition system to this task, as it must be available for the beam tests described below.

Radiation testing of the new SSC devices resulting from the present proposal will follow a similar path. Additional power and clocking circuits may be necessary, however. These tests will be scheduled for the second year of the proposal.

4.4.3 Beam Tests

Testing of the pixel arrays in particle beams is required to demonstrate the functionality of the readout system, to study algorithms relating to the ultimate spatial resolution achievable with these devices, to measure charge sharing and its effects, and to study the response to particles which strike the device at non-normal incidence.

Tests of Existing Arrays Three separate tests of the existing pixel arrays are proposed: one at the UCD cyclotron, one at the Hyperon Beam at Fermilab and one at the Fermilab MTest Beam.

The UCD cyclotron can be used for initial charged particle beam tests of the 10×64 array. Response of the detector would be measured in a parallel beam of 68 MeV protons. This would also facilitate the study of detector performance as a function of radiation dose. These tests could be further refined if the location of each track were accurately known as it enters the array. OU expects to assemble double-sided microstrip detectors with SVX-D readouts which would be well suited to such a test, since they provide correlated (x, y) position measurements with a minimum of scattering material and in a compact geometrical arrangement. A portable test setup would access the SVX CAMAC modules and other diagnostic equipment using a Macintosh computer, a National Instruments GPIB interface and a GPIB/CAMAC crate controller. This apparatus with the required software would be provided jointly by OU and UCD. A Sun workstation will be required at UCD to control the data acquisition system for the 10×64 pixel array itself. OU is requesting funds in the present proposal for travel money to conduct the tests, for mechanical supports and interface PC cards for the microstrip detectors and for support of a graduate student during the next fiscal year.

Tests of the (non- radiation hard) 256×256 arrays as part of more sophisticated tracking systems in beams of minimum ionizing particles will be done at Fermilab.

The first of two such studies will take place in the E781 test beam during May and June of 1990. The apparatus will occupy a 350 GeV/c Σ^- beam of intensity $\sim 10^6$ particles/s (12% hyperons). Two pixel arrays will be used, followed by a number of silicon strip detectors. Though this is primarily a test run, we are hopeful of recording a number of charmed cascades and lambdas, and producing a publishable piece of physics. The funding for this test will come primarily from generic R&D funds which have come to SSL and SLAC as well as funds from E781 sources.

Immediately following the E781 test, we propose to move the 256×256 pixel arrays to the Meson Lab at Fermilab where the BCD collaboration will be performing tests of microstrip detectors in the MTest beam during the 1990 fixed target run. Here, one can obtain a 5 cm square beam spot of $1 - 3 \times 10^6$ particles per spill at energies between 75 and 250 GeV. The OU microstrip system will be read out with CAMAC–interfaced SRS and SDA modules controlled by a VAX3100 computer workstation. Detector arrays will be used to measure position resolutions and noise for a variety of detector types. We plan to take

advantage of this setup to further evaluate the performance of the 256 × 256 array and to measure the improvement in vertex resolution brought about by the use of pixel detectors. Funding for the microstrip tests has already been obtained and the computer data acquisition system has been installed. In this proposal, we request only those additional funds required for testing of the pixel detectors themselves.

System Test of New Array As indicated above, the new array, which will be designed and built as part of the work proposed here, will be subjected initially to a series of laboratory and radiation tests similar to those of the original radiation-hard 10 × 64 array. Following this, OU proposes to use it in a vertex detector system combining microstrip and pixel devices. The goal of these tests is to measure the position resolution for reconstructing vertices with a detector system similar to that required for an actual SSC experiment. This will allow a direct evaluation of the capabilities of such a combined pixel/microstrip system in an accelerator environment.

Funds for the microstrip tests will be requested in a separate subsystems proposal. Time will be requested in the C0 interaction region at Fermilab during the 1992-93 colliding beam run. OU requests additional funds in this proposal for a Sun-4 computer system and associated software to be stationed at Fermilab, for mechanical supports for the pixel detectors and for incremental operating and travel expenses involving the pixel tests at Fermilab.

References

[1] D.E. Groom, private communication.

[2] G.P. Summers, *et al*, Correlation of Particle-Induced Displacement Damage in Silicon, IEEE Trans. Nuc. Sci. **NS-34**, 1134 (1987).

5 Technical Progress Summary

5.1 UCB/SLAC/HUGHES Generic Program

Development of hybrid vertex detectors has been the goal of the team comprised of Eric Arens and Garrett Jernigan of the Space Sciences Laboratory at UCB (SSL) and Stephen Shapiro of SLAC for the past three years. In collaboration with the Hughes Aircraft Company, we have designed and fabricated two hybrid pixel arrays. The sensor portion of the hybrid arrays were fabricated by Micron Semiconductor Limited.

5.1.1 Device Summary

The properties of these two arrays are described in Table I.

TABLE 1

Summary of Device Parameters		
Array Dimension	10×64	256×256
Pixel Size	120 μm	30 μm
Detector Material	Silicon	Silicon
Number of Readout channels	10	2
Power During "Write" Cycle	0 mW	0 mW
Power During Read Cycle	10 mW	2 mW
Clock Speed	1 MHz	1 MHz
Readout Mode	Random Access	Random Access
Radiation Hardness	1 MRad	?
Noise at Room Temperature	$\leq$ 300 e- rms	?

5.1.2 Device Evaluation

To evaluate these devices, two separate data acquisition systems to clock and read out the arrays were developed. The one for the 10×64 array was developed first, while the second, more sophisticated system for the 256×256 array was completed only recently. The 10×64 system is described in our first publication [1] while the second is discussed briefly in a paper given by Steve Gaalema at the

1989 International Industrial Symposium on the Super Collider in New Orleans earlier this year, and which is appended to this proposal. Figure 1 is a block diagram of this system. At New Orleans, the hybrid concept was discussed, and its application to SSC highlighted. At that time we had just taken some preliminary data with the 10×64 array, and it was presented.

Testing of these devices with radioactive sources started in mid-september, 1989. This additional data, taken with the 10×64 array, will be briefly presented here. A ^{106}Ru beta source and an ^{241}Am alpha source were used to irradiate the device. The pixel capacitance is 80 x 10^{-15} F. The pixel is 120 μm square. Spectra for both the alphas and the betas were obtained.

The data are presented in Figure 2. They have been cast in a fashion which allows, from an analysis of these spectra only, the calculation of four quantities; signal to noise, noise, size of the charge cloud, and spatial resolution.

In our geometry, particles enter the device on the cathode of the PIN diode, the side farthest from the bump bonds. Thus, much of the charge collected must drift across the entire depletion distance of 300 μm. The charge cloud, spread by scattering of the initial radiation and by diffusion, will have a finite lateral size. If the particle were closer to the edge of a pixel than to the center, one would expect charge to be shared by adjacent pixels. On average, we see charge spread over nine pixels; a 3×3 array. If this spreading is correlated to the inital position of the particle within the pixel then a well defined locus of points will be evident in Figure 2 rather than a random distribution. The axes in Figure 2 represent the ratio of the charge in the center-top (labeled *early*) pixel and the center-bottom (labeled *late*) pixel divided by the charge in the center column of the 3×3 array.

The cluster of points near the origin represent events which have no charge deposition in the off-center or adjacent pixels. Therefore, the variance of this cluster is a measure of the fluctuation of the ratio of the signal of a typical non-hit pixel and the total signal from the three pixels in a hit column. This variance is the inverse of the average signal to noise ratio. The signal to noise ratio for betas determined from this variance of 0.029 ± 0.007 is 34 ± 8. The average signal size for this data set is roughly 6300 electrons. Thus, the noise is about 185 electrons (rms). A similar calculation for the alpha data presented in Figure 2 yields a variance of 0.008 ± 0.001, a signal to noise of 125 ± 15, and a noise level of 287 electrons (rms).

These noise measurements are consistent with a calculation of KTC noise and

dark current noise, which are the dominant sources of noise at room temperature. For our devices these are 110 electrons (rms) and 120 electrons (rms) respectively yielding a combined noise of 165 electrons (rms).

From the ratio of the number of data points which lie near the axes and the number of data points in the cluster near the origin, one can determine the average size of the charge cloud produced by an incident charged particle. For betas this size is 19 μm (1 σ) and for alphas this size is 28 μm (1 σ).

To determine spatial resolution one uses the fact that the cluster of data points near the origin corresponds to events which deposit nearly all of their charge in the central pixel. Thus, within this region, no interpolation is possible. For those events which are near the edge of a pixel one can use the variance noted earlier to estimate the error in the position within the pixel. For the betas which strike within 30 μm of an edge, the centroid of the 19 μm (1 σ) distribution can be located to within about 2 μm. A similar results for alphas is 2-3 μm across the entire 120 μ pixel, due to the larger size of the alpha induced charge cloud.

These measurements, though preliminary, are the first measurements demonstrating good performance of a pixel array at room temperature.

The major effort of the last six months was the completion of the readout system for the 256×256 array. Late in September, the last bugs were removed, and the 256×256 devices in our possession could be characterized. We have run a curve of cathodes voltage against charge collected, and convinced ourselves that we fully deplete the detector. We also were able to measure the dark current in our device for one setting of readout speed (48 ms to read out the entire chip). At this speed, the dark current was within a factor of two of that measured by Micron Semiconductor for the high purity silicon wafer used in producing these devices. We have not yet had the opportunity to calibrate the capacitance of each pixel so in the calculation we used that of the 10×64 device. Figure 3 shows the operation of the 256×256 PIN array. The device is operated by the generation of clock pulses to drive row and column shift registers which scan the full array. The electronics that control this operation is diagramed in Figure 1. The upper panel of Figure 3 is a display of a portion of the full readout consisting of two 128 row samples. The operation is shown for three different settings of the detector bias voltage and clearly indicates the increase in dark current in response to increases in PIN bias voltage. The lower panel is an expanded view of a 19 pixel segment of a row. The clock trace shows the time of pixel reset which occurs every 2.7 μs in the example shown.

5.1.3 Device Design and Simulation

Last year, in anticipation of this proposal, we proposed [2] the creation of a prototype array by the Hughes Aircraft Co. which met some of the SSC specifications. Though this proposal was premature, its preparation, and the design work and simulation which followed have provided useful ideas for the present effort. Figure 4 is a schematic of our proposed design for a device which was to be radiation hard, responsive to charged particles in 15 ns and which had a readout scheme which allowed the complete analog information to be read out in several hundred microseconds. An alternative array architecture is being studied which requires more electronics on chip and less software for readout. Such a design can be readout faster than simpler alternatives. A description of this design is included as an appendix and represents work in progress. A preliminary study of the interaction of these devices with a digital signal processor was carried out during the last year. The study revealed that some architectures would require several hundred microseconds for the readout and calculation of the centriod of charge clusters induced by particle hits. The parallel design will operate significantly faster that the simplier serial design shown in Figure 4 since it presents the data to the digital signal processor in a form ready for analysis.

5.1.4 Conclusion

The UCB/SLAC/HUGHES generic program has reached the primary objective of fabricating and demonstrating the operation of hybrid PIN diode arrays with a room temperature noise of less than 300 electrons (rms). Such devices can be used for some high energy physics experiments today and are a significant step towards the development of devices which meet SSC requirements. We have also developed a prototype system including both hardware and software necessary for the operation of these devices. This system serves as guide for the development of a SSC control system as well as providing the capability to evaluate devices both in the laboratory and in the field. We have also developed some preliminary concepts for new devices which approach SSC requirements and have carried out a modest program of simulations. More work is necessary to properly calibrate and characterize these devices.

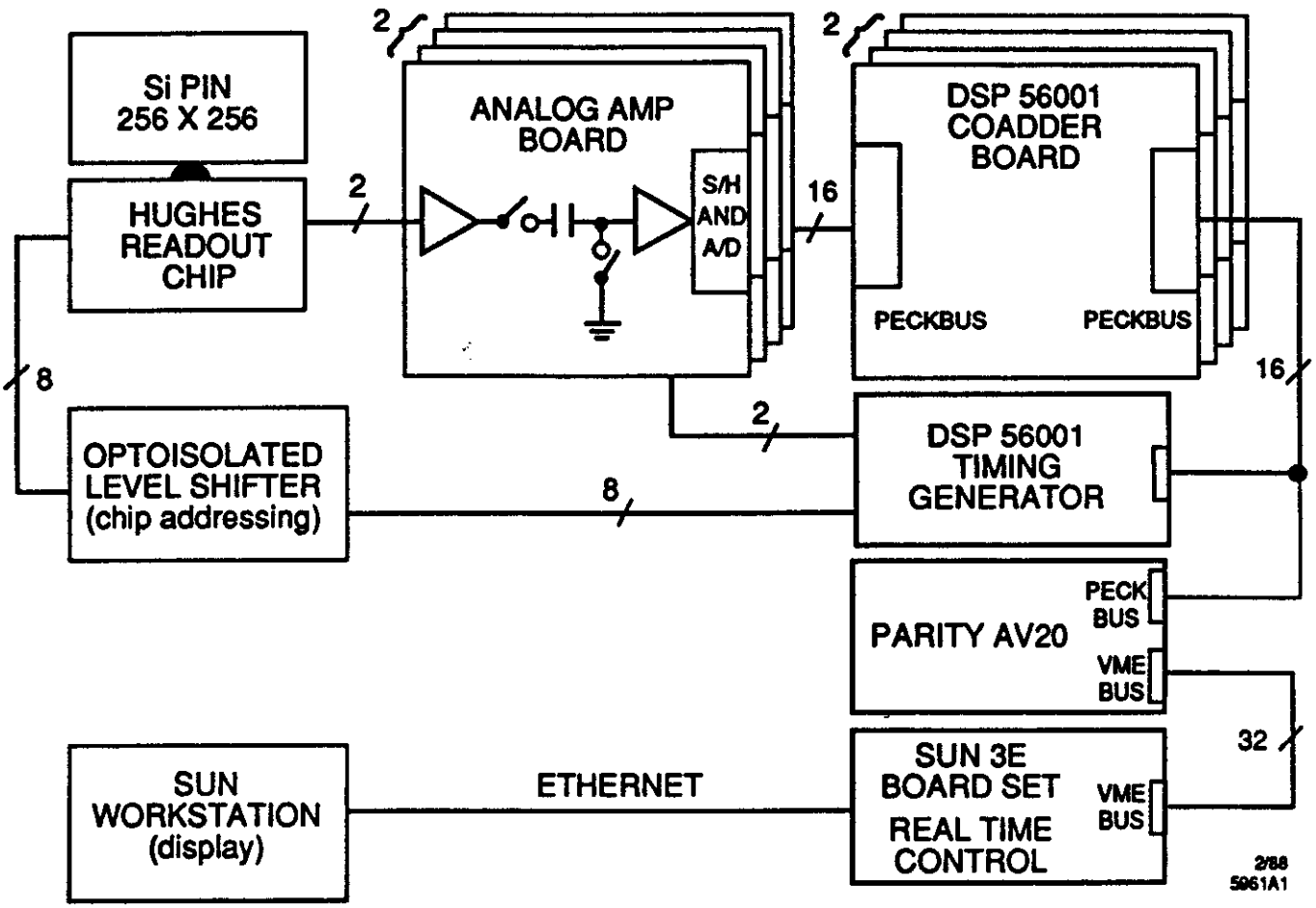
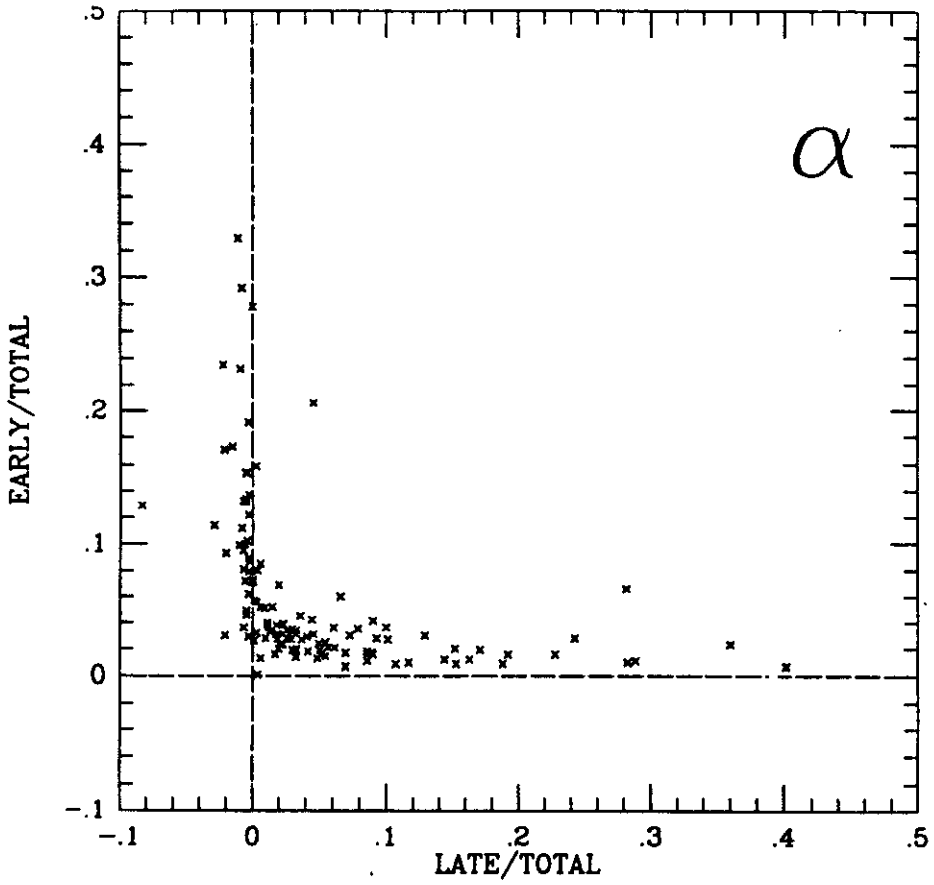


Figure 1: Block diagram of the control and data acquisition systems



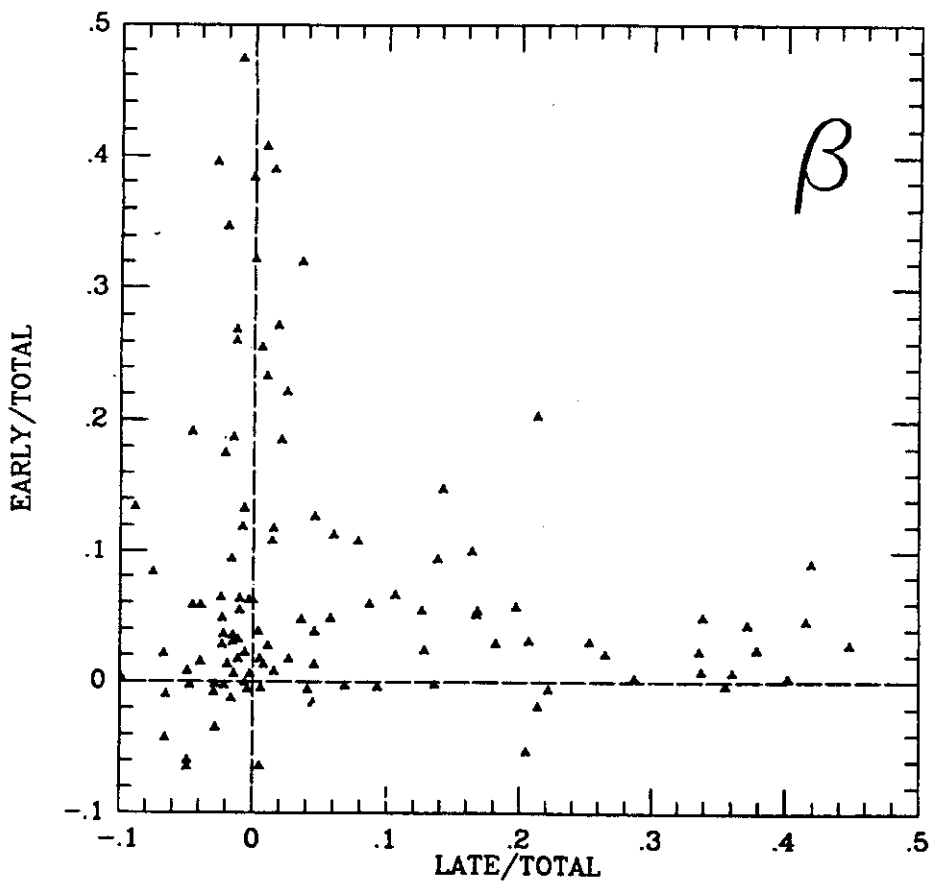


Figure 2: Scatter plots of charge sharing for α and β particles

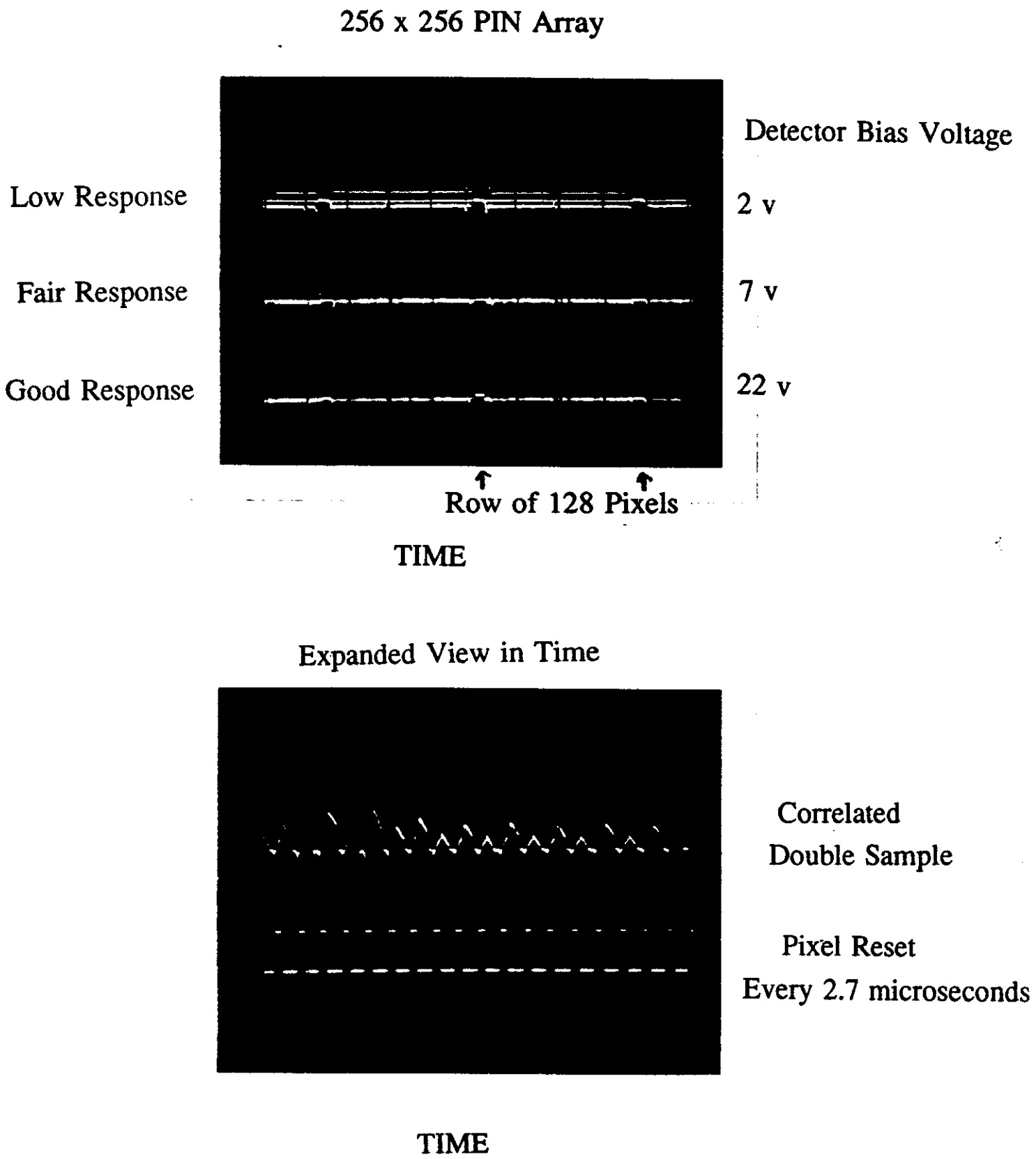


Figure 3: Oscilloscope traces of clocks and output of 256×256 array

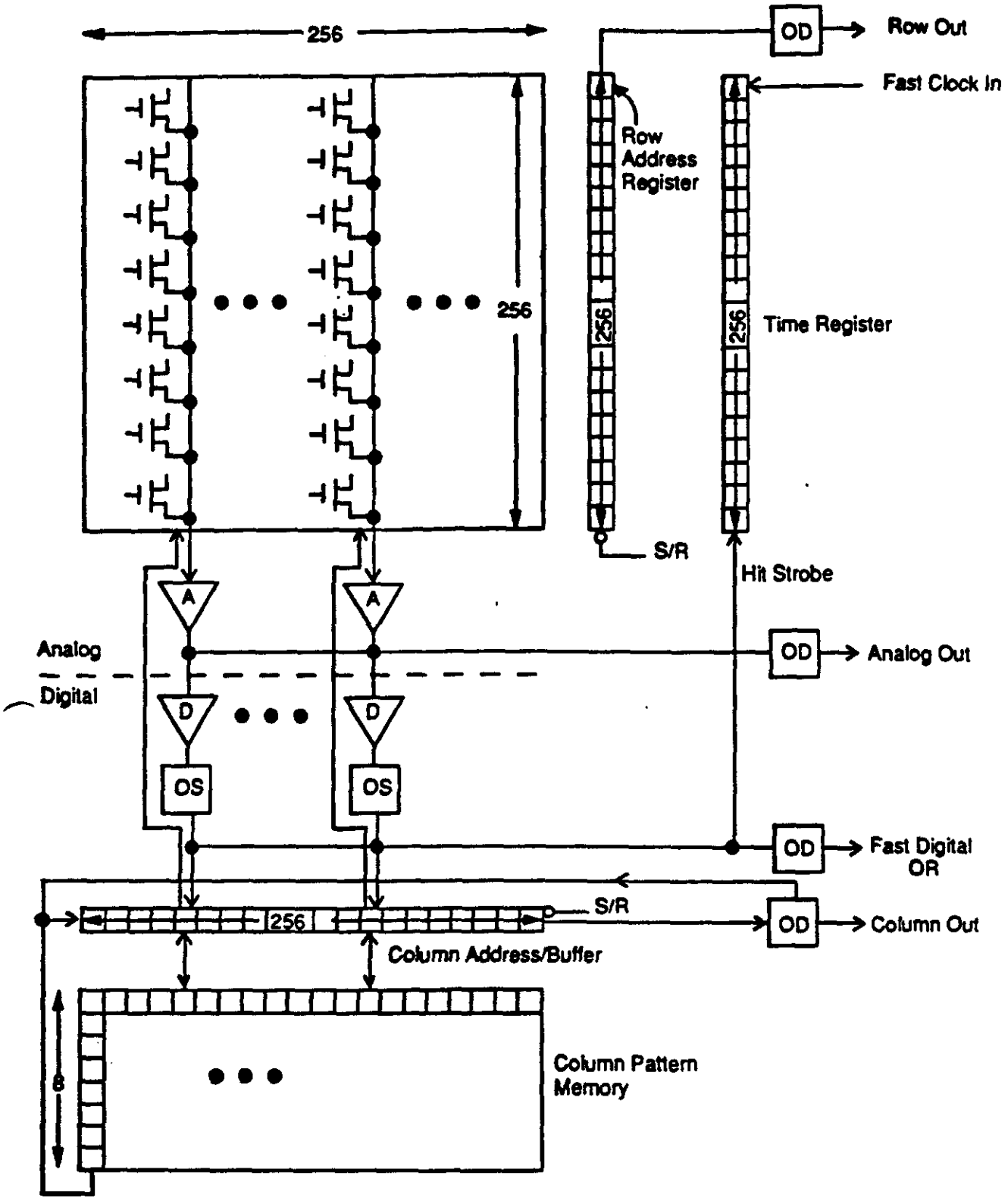


Figure 4: One of the proposed readout architectures

5.2 LBL Technical Progress

In this section, a very brief outline of relevant current activities and progress is given. Effort has been directed in five areas:

(a) A Robust High-Temperature Detector Fabrication Process;

(b) Monolithic Integration of Circuitry and Detectors;

(c) Low-power low-noise Analog Circuitry Optimization;

(d) Radiation Damage Studies of Detectors and Circuitry;

(e) PIXSTRIP, a design study for a smart pixel array.

These topics are described in greater detail in Appendix 8.2, a report presented at the 1988 Snowmass Meeting. References are included there.

5.2.1 A Robust High-Temperature Detector Fabrication Process

In this work, a backside phosphorus-doped polysilicon layer has been postulated by S. Holland of LBL to offer excellent gettering characteristics for heavy metal contaminants that cause excessive leakage currents and/or early breakdown behavior in detectors. The technique has been found to work extremely well in practice, producing very uniform and reproducible devices with high performance. This gettering technique actually turns the high temperature steps used in conventional IC fabrication to advantage, as the diffusive mobility of the contaminants is high enough at those temperatures to capture essentially all contaminants within the electrically inert back layer. Strip detectors have been produced with high yields, and exceptional performance. These are being utilized in the activities discussed below, as well as in a related effort aimed at a silicon tracker with optimized power dissipation.

5.2.2 Monolithic Integration of Circuitry and Detectors

Building on the results mentioned above, PMOS transistors have been integrated on high-resistivity silicon with high-quality detectors. These devices have both channelstop and threshold implants, and compare favorably with better commercial transistors. A complete CMOS process is regarded as a straightforward extension of this work, but effort will be needed to fully optimize the

P-well characteristics. A novel JFET structure has been analyzed, and would appear to offer low-noise rad-hard performance. All processing steps are conventional, permitting commercial foundries to fabricate devices with low risk. This is the first clear example of a technique that eliminates the traditional incompatibility of detector fabrication and integrated circuitry. A strip detector with an integrated PMOS amplifier/MPX has been fabricated.

5.2.3 Low-power Low-noise Analog Circuitry Optimization

In this task, an intimate knowledge of device physics, circuit design principles, radiation damage effects, and measurements to define scaling behavior are combined to synthesize guidelines and principles for optimized low-power low-noise analog circuitry. Both CMOS and bipolar technologies have been included in these analyses. These have application to both pixel detectors and strip detectors, and lead to novel configurations with greatly reduced power dissipation relative to extensions of current design practice. The impact of these studies on overall feasibility for a silicon tracker is quite substantial. For pixel cells, designs have been evolved that are expected to demonstrate less than 100 electrons rms noise, with power dissipations less than 10 μW per pixel. The use of CR-RC shaping with peak detection has been developed to minimize shot noise under conditions of heavy radiation damage to the detector. A pixel cell design with optimized analog performance is scheduled for implementation in silicon this winter.

5.2.4 Radiation Damage Studies of Detectors and Circuitry

In collaboration with UCSC and Los Alamos, a set of exposures has been made under conditions that will allow the determination of damage constants for differing resistivity, crystal orientation, and process steps. The exposures correspond roughly to one week and one year of SSC operation. The preliminary results do not support the prevailing mythology that the damage constants depend sensitively on the resistivity. Other aspects of this work are systematic noise measurements of commercial radhard MOSFETs, an area of great interest and little systematic information. A theoretical analysis of the relationship between detector size (area and thickness), signal/noise ratio, electronic integration time, damage constant and fluence has been made, which permits the straightforward evaluation of system performance.

5.2.5 PIXSTRIP, a design study for a smart pixel array

This device is a linear 128 channel array implemented in silicon to test some of the logic and sparse data readout features of the smart pixel array concept. The sparse data feature efficiently scans large address fields to find true hits belonging to the time-slice of interest. A major result of this study is that the sparse data scan proceeds to find a column (or row) with hit data at an extraordinary scan speed of 660 MHz. On average, a column with a valid hit is found in about 100 nanoseconds. In a two-dimensional version, logic is included for the interrogation of row elements to identify only true hits. Ambiguities are thus suppressed at the chip level. This built-in logic is capable of expressing the two-dimensional address of a hit pixel in about two hundred nanoseconds. Much of the circuit design concept is an evolution of the successful LBL SVX silicon strip readout IC.

References

[1] Stephen L. Shapiro, William M. Dunwoodie, John F. Arens, J. Garrett Jernigan, Stephen Gaalema, Silicon PIN Diode Array Hybrids for Charged Particle Detection, NIM, **A275**, 580 (1989).

[2] Stephen L. Shapiro, John F. Arens, J. Garrett Jernigan, Stephen Gaalema, A Vertex Detector System for the Superconducting Super Collider, submitted to Department of Energy, September, 1988.

6 Statement of Work and Budget Summary

The following statements of work and budgets for the various team activities are proposed.

6.1 Hughes Aircraft Company

(a) Hughes Aircraft Company budget request -$487K

(b) Perform system level architecture and design studies for pixel detector systems, for vertex tracking for both SDE and BCD pixel experiments;

(c) Perform a preliminary cost analysis of the proposed pixel detector systems;

(d) Design fab and test pixel array addressing the critical requirements for technical feasibility.

(e) Personnel

   i. See resumes in appendix 8.1.4

6.2 Lawrence Berkeley Laboratory

(a) Lawrence Berkeley Laboratory budget request - $280K

(b) Provide design support and system analysis to Hughes Aircraft Company including a review of proposed designs;

(c) Continue development work on LBL detector process to provide appropriate pixel detector arrays for Hughes Aircraft Company;

(d) Perform analysis of radiation damage studies on detectors, circuitry, and hybrid arrays with other collaboration members.

(e) Personnel

   i. Steve Holland will devote 40% of his time to the task of detector development and fabrication, using the new LBL high temperature detector process. These detectors will be matched to the pixel cell geometry, (to be defined) and will incorporate AC coupling using built-in capacitors and polysilicon resistors. As a variety of detector geometries are needed, this effort level represents a minimum.

ii. David Nygren will devote 80% of his time to physics direction and coordination of this entire proposed activity. His salary is supported by the LBL HEP budget.

iii. Helmuth Spieler will devote 40% of his time to the tasks of pixel array architecture development, circuit and system analysis for prototype smart pixels, and detector process development. These activities will have a close relationship to the effort described in a SSC major subsystems proposal for a silicon tracking system, which will require a 50% effort. The remaining 10% is devoted to a generic R&D program emphasizing radiation damage studies.

iv. Michael Wright will devote 40% of his time to the task of CMOS pixel cell circuit design and analysis, under the guidance of Helmuth Spieler. Pixel cell designs will be laid out, and prototypes fabricated and tested. These designs will support the effort undertaken at HAC, and are also intended to provide an avenue to understand alternate concept performance. Another 50% of his time will be dedicated to the work for a silicon tracking system. The remaining 10% is allocated to a variety of CMOS design projects.

6.3 UC Berkeley - Space Sciences Laboratory

(a) UC Berkeley - SSL budget request - $211 K

(b) Continue testing of the current pixel arrays that have been prepared;

(c) State machine or digital signal processor design;

(d) Assist in detector readout design

(e) Test system development.

(f) Personnel

i. John Arens will devote 50% of his time to helping design a readout architecture and testing detectors, mainly in the SSL lab. He will participate in designing the electronics for operating the detectors that will be designed and built as part of this proposal. He will coordinate activities between the physics groups and Hughes.

ii. Garrett Jernigan will devote 50% of his time to helping design the data acquisition and data storage system and to designing and building the

electronics for operating the detectors that will be designed and built as part of this proposal. The design work for the electronics cannot begin until the architecture of the readout chip is completed.

6.4 Stanford Linear Accelerator Center

(a) Stanford Linear Accelerator budget request - $61K

(b) Perform laboratory, radiation, and beam tests with the current pixel arrays and those being developed;

(c) Perform mechanical and cooling studies of proposed vertex detector systems.

(d) Assist in detector readout and pixel architecture design

(e) Personnel

i. Steve Shapiro will devote 100% of his time to testing detectors and investigating mechanical and cooling systems. The testing will be performed in two or three areas:

A. Testing the 10×64 and 256×256 pixel arrays that were recently produced by Hughes Aircraft and Micron Semiconductor at SSL, at accelerators, and in high radiation flux facilities.

B. Using the 256×256 array in the test setup of Jim Russ' E781 experiment at Fermilab. This work will be funded by Russ.

C. Testing the detector arrays that will be designed and built as part of the work of this proposal.

6.5 University of Oklahoma, Yale University, and University of Iowa

(a) Budget request - $85K

(b) Radiation Damage Studies;

(c) Beam tests at Fermilab;

(d) Preparation for Beam Tests of a Vertex Detector Subsystem.

(e) Personnel

i. Phil Gutierrez will devote 33% of his research time to testing strip and pixel detectors. He will test both the existing 10×64 and 256×256 arrays and also the detector arrays that will be designed and built as part of the work described in this proposal. He will have no teaching responsibilities in the spring of 1990.

ii. Pat Skubic will devote 33% of his research time to testing strip an pixel detectors. He will test both the existing 10×64 and 256×256 arrays and also the detector arrays that will be designed and built as part of the work described in this proposal. He will have no teaching responsibilities in the spring of 1990. He will coordinate activities at Oak Ridge if radiation sources there are used. He will also handle the travel accounts for the University of Pennsylvania, Princeton, Yale, and the University of Iowa if the SSC chooses to consolidate small financial grants.

iii. Paul Karchin will devote 5% of his time to reviewing designs and test results.

iv. Ed McCliment will devote 10% of his time to participation in beam testing at FNAL.

6.6 UC Davis and Iowa State University

(a) Budget request - $66K

(b) Physics simulations of system performance in SSC environment;

(c) Proton beam testing of pixel detector arrays.

(d) Personnel

i. David Pellett (UC Davis) will devote 20% of his research effort to testing the existing 10×64 array and the arrays that will be designed and built as part of the work proposed here. He will coordinate tests at the U.C. Davis 68 MeV cyclotron.
Altogether, half of Pellett's research effort will be devoted to SSC studies under the existing UC Davis generic R&D program plus a major subsystems proposal on silicon tracking, if the latter is approved. In addition to pixel device testing, this program includes simulation and design studies of a pixel vertex detector for the central rapidity region. These efforts, which involve additional personnel, complement the work of the present proposal.

ii. John Hauptman (Iowa State University) will devote 25% of his time to detector simulations and will participate in detector tests. Funding is requested for travel only.

6.7 University of Pennsylvania, Princeton University

(a) No funding requested;

(b) Provide design analysis and simulation for BCD experiment.

(c) Personnel

i. Nigel Lockyer will devote 40% of his research time to the design and simulation of the BCD detector. About 1/3 of this time is used for studying mechanical and electrical issues related to the vertex detector. He will install the pixel geometry and gutter support structure into the Geant simulation program. He will provide Monte Carlo event analyses to Hughes in order to study readout schemes. Raw data rates per tile and clusters of tiles will be provided. He will simulate alignment effects on B reconstruction efficiencies and on background rejection. He will ensure good communication between this project and the BCD data acquisition system being designed by Ed Barsotti of Fermilab.

Nigel Lockyer assumes the computing resources of this project will be provided by the Farm proposal of Lockyer, McDonald, et al submitteed to the SSC laboratory. The overlap in the software development for the pixel project and the Farm studies are nearly 100%. Funds for this work are requested in the Farm proposal.

ii. Kirk McDonald will devote 10% of his time to simulating events and reviewing designs and test results.

Total Cost: $1190K

7 Budgets and Schedules

The budgets for the proposed work are given below for each institution. A schedule for a five year program to produce a complete prototype vertex detector for the SSC is given in Figure 1. The schedule for the work proposed here covers one year and is shown in Figure 2.

Hughes Aircraft Company Budget Summary

Total Material			$ 23,600
Direct Labor Elements—Hours			
Member technical staff	1,234		
Associate engineer	156		
Research assistant	48		
Senior member of technical staff	1,776		
Senior technical engineer	98		
Total Direct Labor (hours):	**3,310**		
Other Direct Costs—Dollars			
Wafer processing		$ 60,708	
Data processing		3,000	
Travel		6,954	
Total Other			$ 70,662
Total Estimated Cost:			**$ 425,870**
Total Cost of Money:			$ 18,414
Total Estimated Cost Plus COM:			444,284
Fee or Profit:			42,601
TOTAL PRICE:			**$ 486,885**

Lawrence Berkeley Laboratory Budget Summary

Scientific/Engineering Personnel ($ 150,000/FTE):

Helmuth Spieler	0.4 FTE		
Steve Holland	0.4 FTE		
Michael Wright	0.4 FTE		
Total	1.2 FTE		$ 180,000

Technical Personnel ($ 100,000/FTE):

Distributed effort	0.5 FTE		$ 50,000

Equipment: none requested

Supplies and Expenses:

MOSIS submissions	$ 15,000	
Travel	12,000	
Shops	6,000	
Supplies	6,000	
Noncapital equipment	11,000	
Total Supplies and Expenses:		$ 50,000

Total Support Request:	**$ 280,000**

University of California–Space Sciences Laboratory Budget Summary

Labor			
Arens	25%	$ 22,000	
Jernigan	25%	16,000	
Engineer	50%	30,000	
Technical	25%	12,000	
Programmer	50%	22,000	
Total Labor			$ 101,000
Travel			10,000
Capital Equipment			18,000
Overhead			57,000
Total Support Request:			**$ 211,000**

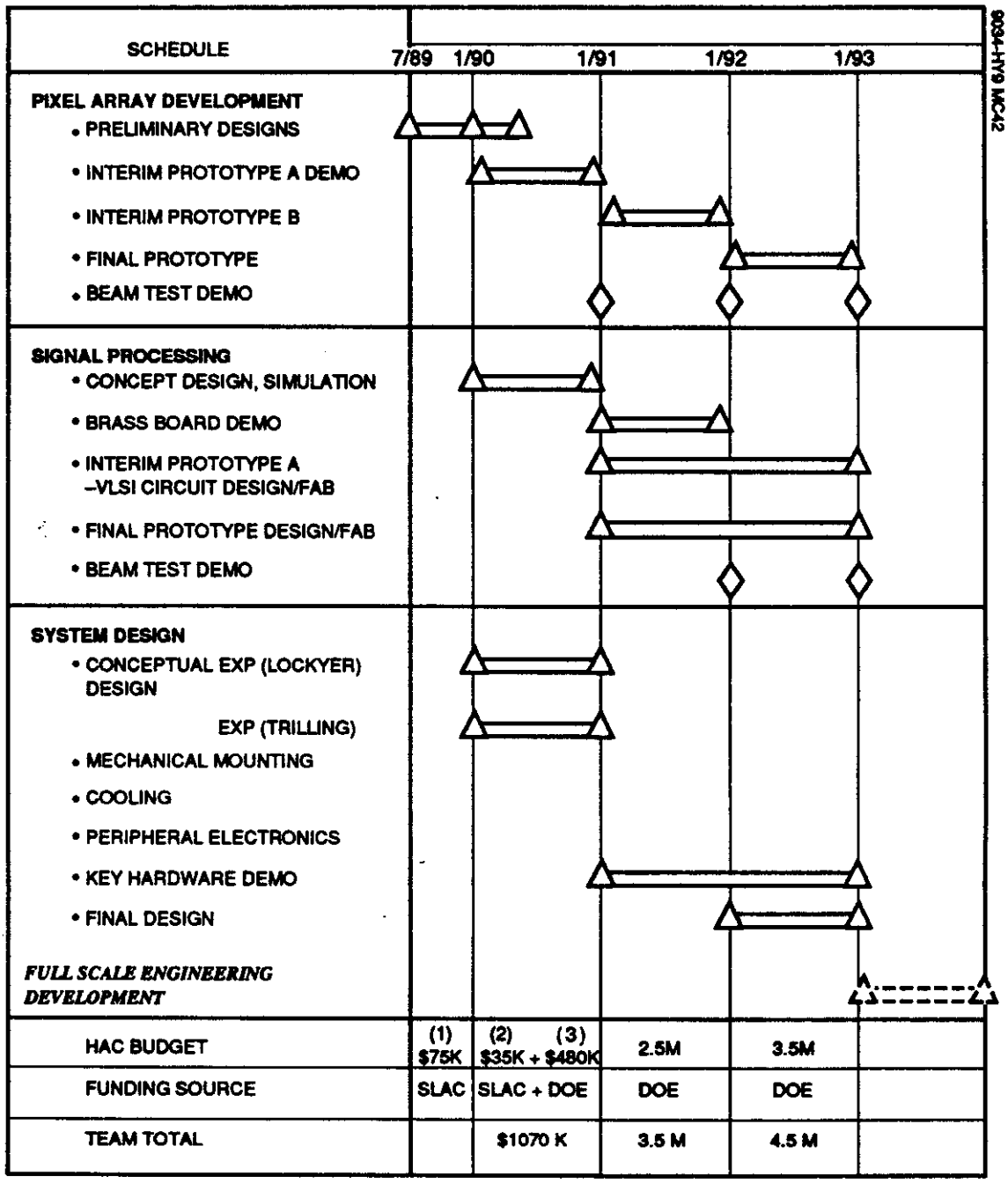
SLAC Budget Summary

Material		
Mounting hardware for 256 × 256 device		$ 1,850
Power supplies and clock drivers for radiation tests		3,000
Labor		
	hours	
Mount for 256 × 256 device	160	$ 4,000
Power supplies and clock drivers	125	3,000
Software support–simulation of mounting, cooling	500	15,000
Software development	250	7,500
Travel		8,000
Overhead		18,150
Total Support Request:		**$ 60,500**

UC Davis Budget Summary

Student Labor	$ 10,000
Equipment–SUN workstation etc. for radiation tests	15,000
Supplies	2,000
Beam time for radiation damage studies	10,000
Travel (including budget for J. Hauptman)	14,000
Overhead	15,000
Total Support Request:	**$ 66,000**

SSC – LONG RANGE PIXEL DETECTOR DEVELOPMENT PLAN



(1) EXISTING FUNDING

(2) ANTICIPATED FUNDING

(3) THIS PROPOSAL

Figure 1. SSC long range pixel detector development plan.

University of Oklahoma Budget Summary

Material	
Mechanical supports and cables	$ 6,000
Mechanical supports, interface cards, cables	3,000
Irradiation charges and instrumentation (pixel tests at UTK or Hughes)	5,000
Pixel detector mechanical supports and cables ("C0" tests)	13,000
Labor	
Graduate Research Assistant, 1/2 year	12,000
Capital equipment	
SUN-4 computer and support hardware	18,000
Travel	7,400
Overhead	5,044
Total Support Request:	**$ 69,444**

University of Iowa Budget Summary

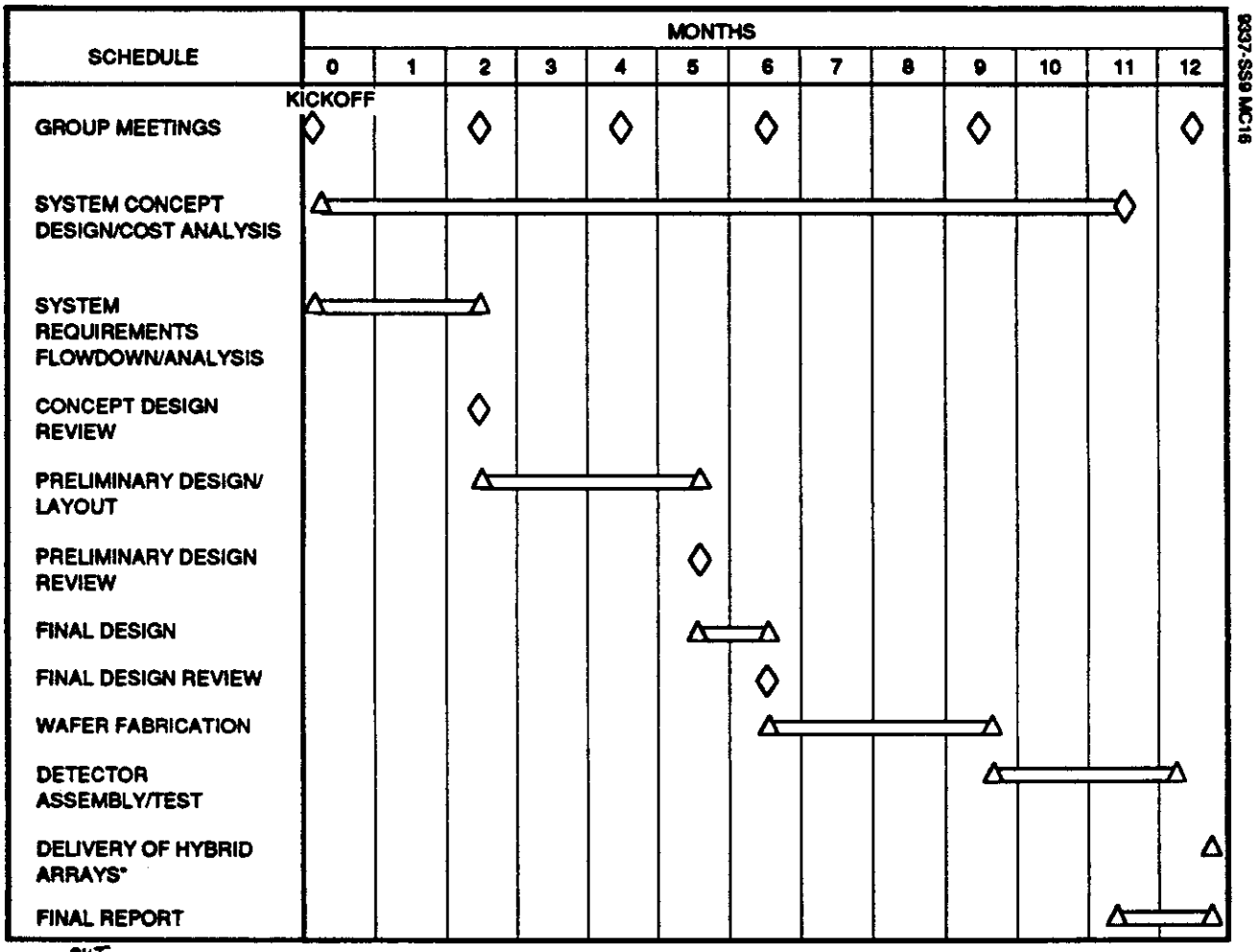
Travel	7,500
Total Support Request:	**$ 7,500**

Yale University Budget Summary

Travel	7,500
Total Support Request:	**$ 7,500**

The milestone schedule for the Hughes effort is shown in Figure 2. Regular meetings will be held at 2 and 3 month intervals among all team members to ensure accurate and up to date communication and technical interchange. A Concept Design Review, Preliminary Design Review, and Final Design Review will be held to ensure that the readout design will satisfy the appropriate system requirements.

SSC PROGRAM – PIXEL DEVELOPMENT – HUGHES AIRCRAFT COMPANY



◇ INPUT FROM TEAM COLLABORATORS

* MIN OF SIX HYBRID ARRAYS DELIVERED TO TEAM COLLABORATORS

Figure 2. Hughes Pixel Vertex Detector System Development for SCC program—milestone schedule.

8 Appendices

8.1 HUGHES AIRCRAFT COMPANY CAPABILITIES

The electronic readout and hybrid technology, which are critical to the development of hybrid pixel detector arrays for the SSC, exist at Hughes as a result of the work in long wave infrared (LWIR) sensor technology. The SSC similarly requires sensitive, radiation hardened, high speed pixel detector arrays. Readout arrays and their hybridization have already been made available to SLAC and UCB on an existing SSC detector development project ("Silicon Pin Diode Hybrid Arrays for Charged Particle Detection: Building Blocks for Vertex Detectors at the SSC." G. Kramer et al., presented at the 1989 International Industrial Symposium on the Super Collider, New Orleans, LA, February 8-10, 1989).

Some of the key technology requirements for the SSC detector are:

(a) Thin substrate detectors to minimize multiple scattering effects;

(b) High speed operation to match beam crossing and particle rates;

(c) Radiation hardness.

Our capability to "thin" detector chips is demonstrated in Figure 1, which shows detector chips thinned to 50 m and hybridized to a readout chip. Likewise, readout chips can be thinned.

Hughes technology can meet the high speed operation needs for the SSC as shown by the performance of shift registers. The latest Hughes high speed silicon integrated circuit was recently tested. It uses the lowest risk silicon on sapphire (SOS) process (Figure 2) technology at Hughes. The chip is a digital fully pipelined 6x6 bit multiplier that operates at speeds greater than 132 MHz. The chip has 8340 metal oxide semiconductor field effect transistors (MOSFETs), and the latest lot has an 85 percent operational yield. Using this exact technology, one could expect a digital shift register circuit to operate at speeds between 300 and 500 MHz. The circuit uses 1.5 μm gates and 5-V supplies. Figure 3 shows the scope photos of the chip operation. The clock is running the chip at 125 MHz, and the chip response is at 100 MHz. From the photo, it is clear that, if the clock rate could be increased, the chip could respond at 250 MHz. The SOS technology is radiation hard to greater than 1 Mrad(Si) of total dose.

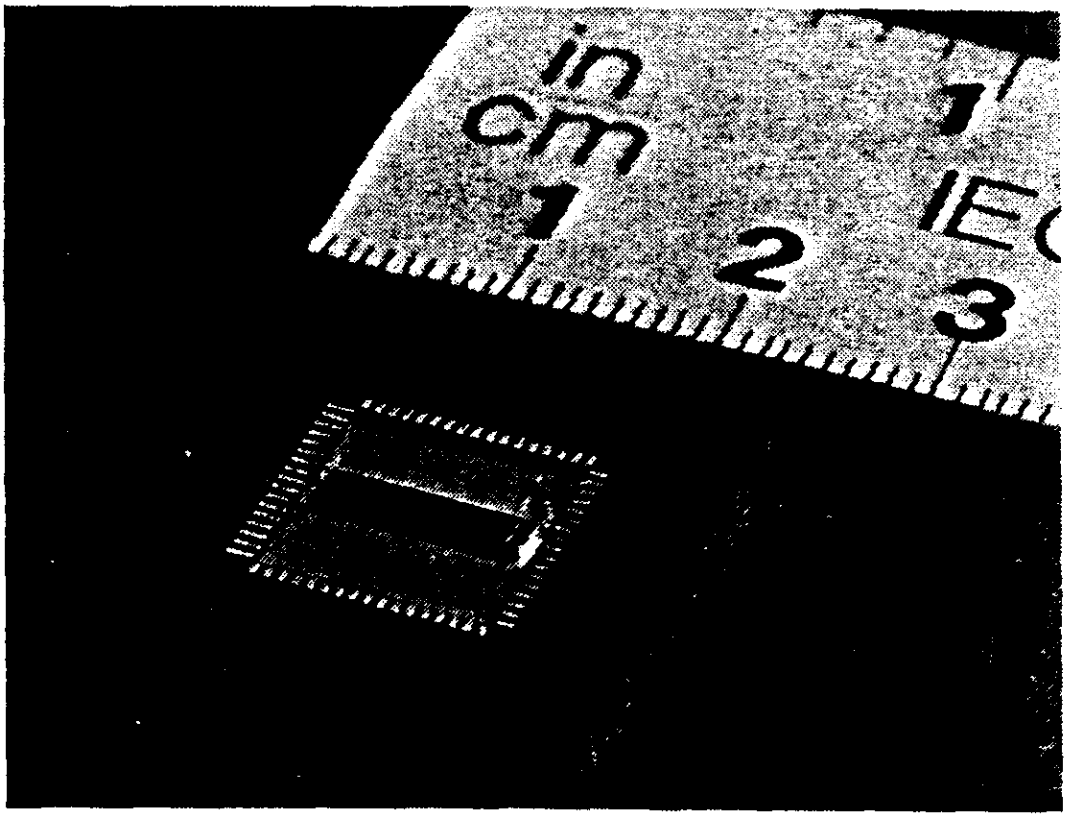


Figure 1: Thinned chip technology. Top chip on hybrid array is thinned to 50 μm.

In the past 4 years, more than $50M of contract funds for hybrid detector array technology has been received by Hughes. The experience gained from these efforts, in addition to company funded IR&D, will ensure the success of the proposed SSC detector development program.

Hughes is a leader in the development of LWIR sensor technology for the Department of Defense, having compiled more than 95 percent of all LWIR space background flight data and performed more that 70 percent of all successful target measurement flights using Company sensors. In 1964, Hughes developed the far infrared search track sensor, the first LWIR sensor to be twice flown successfully in space (1967), followed in 1970 by the first ballistic missile defense fly along infrared (FAIR I) sensors. These sensors successfully gathered the first comprehensive LWIR radiometric measurements of ballistic missile targets in flight. Hughes provided the first mosaic surveillance focal plane to be flight tested, HICAMP I in 1978, and the largest mosaic surveillance infrared focal plane chip to be flight tested, HICAMP II in 1983.

The HI-STAR sensor, designed and developed by Hughes in 1971, completed 11 flights on Aerobee sounding rockets, gathering the LWIR stellar background data that today remains the definitive comprehensive data reference base in this country. The Hughes Celestial Mapping Program saw the first orbital flight of an LWIR sensor cooled by a closed cycle refrigerator; many orbits and many stellar background maps were completed. The PII sensor, developed in 1971, was successfully operated in the field from 1974 through 1978 to obtain LWIR signature measurements from an airborne platform.

The Hughes designating optical tracker sensors, with five successful flights to date, provide the basic instruments for the only continuing low background LWIR exoatmospheric target radiometric signature measurement program in existence. The Hughes miniature vehicle sensor is the first planned operational LWIR sensor, and the space infrared experiment represents the only advanced satellite-based LWIR measurement sensor cooled by a closed cycle refrigerator. The Airborne Optical Adjunct (AOA) sensor program, which has developed the most advanced IR sensor ever built, is in final test. Delivery to system integration was completed in July 1988.

Each year Hughes invests heavily in independent research and development (IR&D) programs and is strongly committed to advancements in the field of sensor technology. Special emphasis is given to space related focal plane development, including detectors, readouts, and signal processing. Much of this

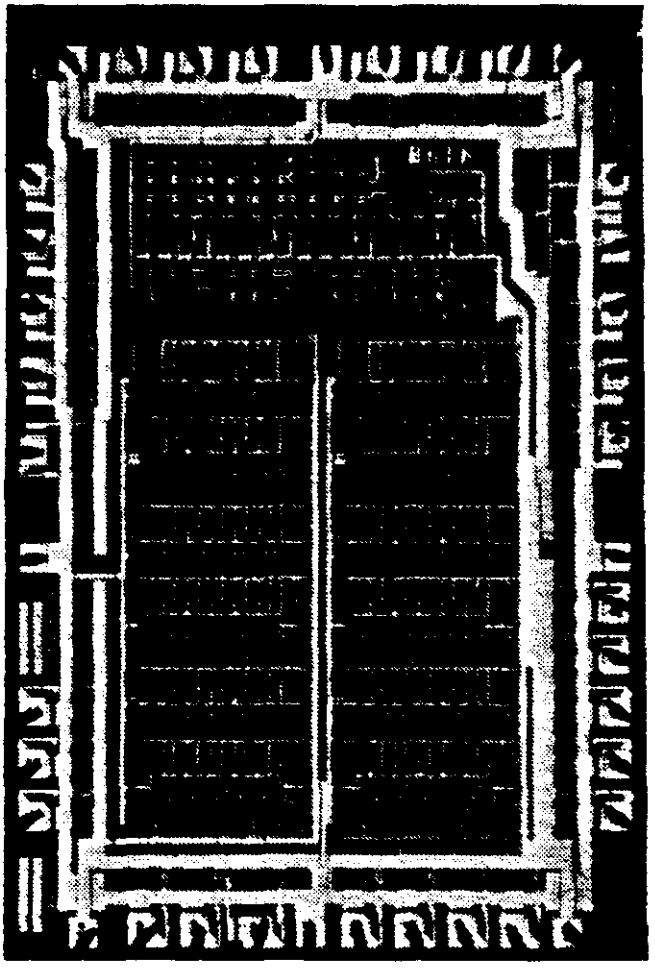
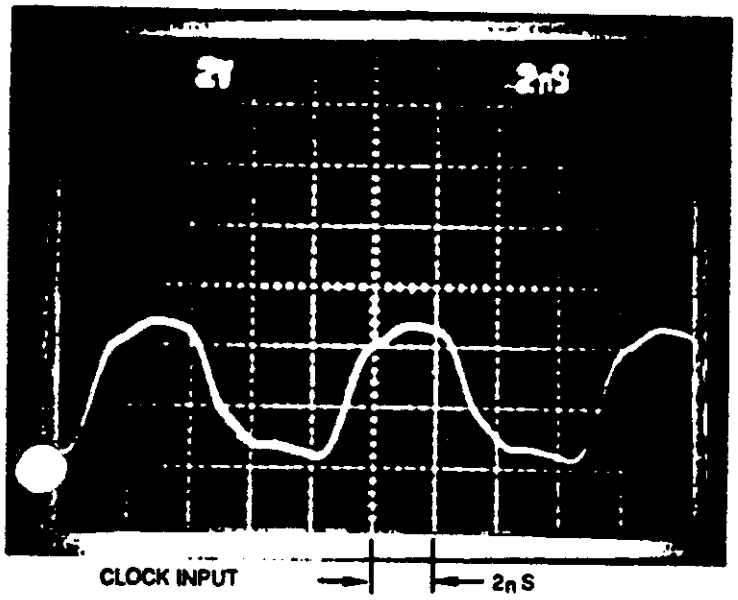
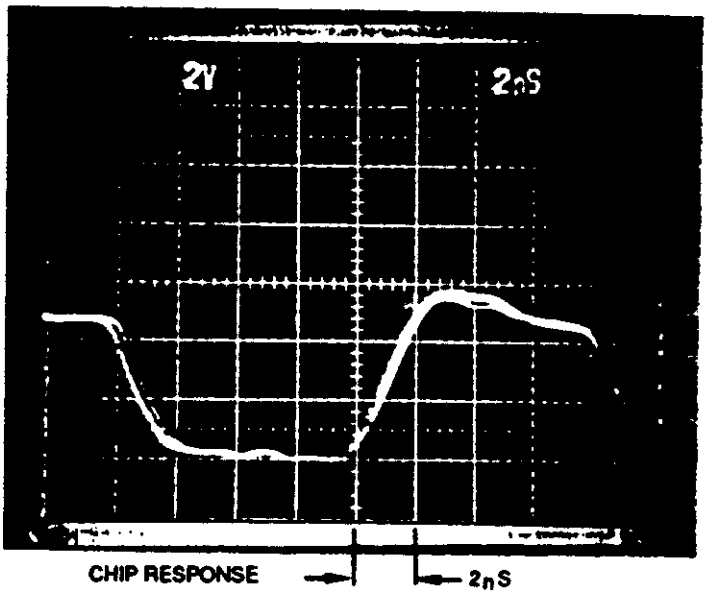


Figure 2: SOS 6x6 bit multiplier, composed of 8340 MOSFETs, operates at 132 MHz.



CLOCK IN ≅ 125 MHz



OPERATING AT ~ 100 MHz

UPPER LIMIT = ~ 250 MHz
WITH FASTER CLOCK

Figure 3: SOS digital multiplier demonstrates ability to operate at 250 MHz.

IR&D will directly benefit SSC programs.

8.1.1 MOSAIC ARRAY DEVELOPMENT

The mosaic infrared sensor technology (MIST) and forward acquisition sensor (FAS) optical sensor programs required intensive efforts to develop high density mosaic focal plane arrays. Hughes has led in the development of state-of-the-art technologies necessary to support major improvements required in next generation infrared sensor performance; the monolithic focal plane array (MFPA) was demonstrated in 1973, the first monolithic extrinsic silicon infrared sensitive chip in 1974, and the first incorporation and flight of a many thousand element MFPA in 1976. These advances have paced the industry. The Defense Advanced Research Projects Agency Charge Coupled Device program, the Mini-HALO program, the Air Force's Forward Looking Infrared Technology Development program, and the Army's Tank Breaker missile seeker all use Hughes mosaic technology. The USAF space based surveillance system detector technology program and the Ballistic Missile Defense Advanced Technology Center's MIST and FAS programs have led to the design evolution of the high performance source follower per detector (SFD) concept, which is the key to the low noise integration and readout of the tens of thousands of low noise, background limited detectors required for space surveillance and tracking system development.

The AOA program developed and manufactured a focal plane with 15 modules, each consisting of 2,560 Si:Ga detector elements and devices that measure contamination level and sensor optical image quality. In addition, the Sensor Experimental Evaluation and Review (SEER) program has successfully demonstrated the feasibility of producing hardened sensor chip assembly (SCA) hybrids with LWIR Si:As detector arrays and SFD multiplexer readouts. The Precursor Above the Horizon Sensor (PATHS) program has not only demonstrated reproducibility by fabricating Si:As impurity band conduction hybrids with high yield but has also developed high performance silicon capacitive feedback transimpedance amplifier and germanium SFD multiplexer readouts. This program is also establishing a documented pre-pilot process capability for IBC detectors and silicon readouts. The experience and capability established from the SEER and PATHS programs will be directly applicable to the technology development of the SSC Detector System.

In addition, development efforts on GaAs integrated circuits for both digital and radiation hardened analog readout circuits are being pursued at Hughes.

8.1.2 ORGANIZATIONAL RESOURCES

Hughes has the organizational depth and commitment to successfully conduct the Pixel Vertex Detector System Development for SSC program. The corporate structure of Hughes is shown in Figure 4. Management of the Company is vested in M.R. Currie, Chairman and Chief Executive Officer, and D. H. White, President and Chief Operating Officer. The Electro-Optical and Data Systems Group (EDSG), which employs over 10,000 personnel, is responsible for the overall management of research, development, test, manufacture, and evaluation of tactical, laser, and space electro-optical systems. EDSG, headed by R. D. Brandes, Senior Vice President and Group President, will be responsible for the overall management and coordination of the Pixel Vertex Detector System Development for SCC program.

The Hughes Microelectronics Center (HMC) has extensive experience in advanced silicon detectors and on-focal-plane signal processing electronics. Thus, it can develop and manufacture advanced hybrid arrays to meet SSC system requirements. Hughes has developed and demonstrated the advanced analog radiation hard CMOS process for readouts.

The Hughes Research Laboratories (HRL) directly support the fundamental technology refinement and process optimization with their extensive analysis and mensuration capabilities.

Hughes is strongly committed to the design and development of superconducting supercollider detector systems. A highly skilled team has already been formed as the nucleus of the proposed program and is organized as shown in Figure 5. Hughes is fully committed to providing the personnel and facility resources to ensure the success of this program.

8.1.3 FACILITIES

Electro-Optical and Data Systems Group Complete facilities for the Pixel Vertex Detector System Development for SSC program are available at EDSG's modern engineering and manufacturing facility. This 1,750,000-square-foot facility, located in El Segundo, CA, is specifically designed and equipped

to facilitate all aspects of electro-optical production and technological development.

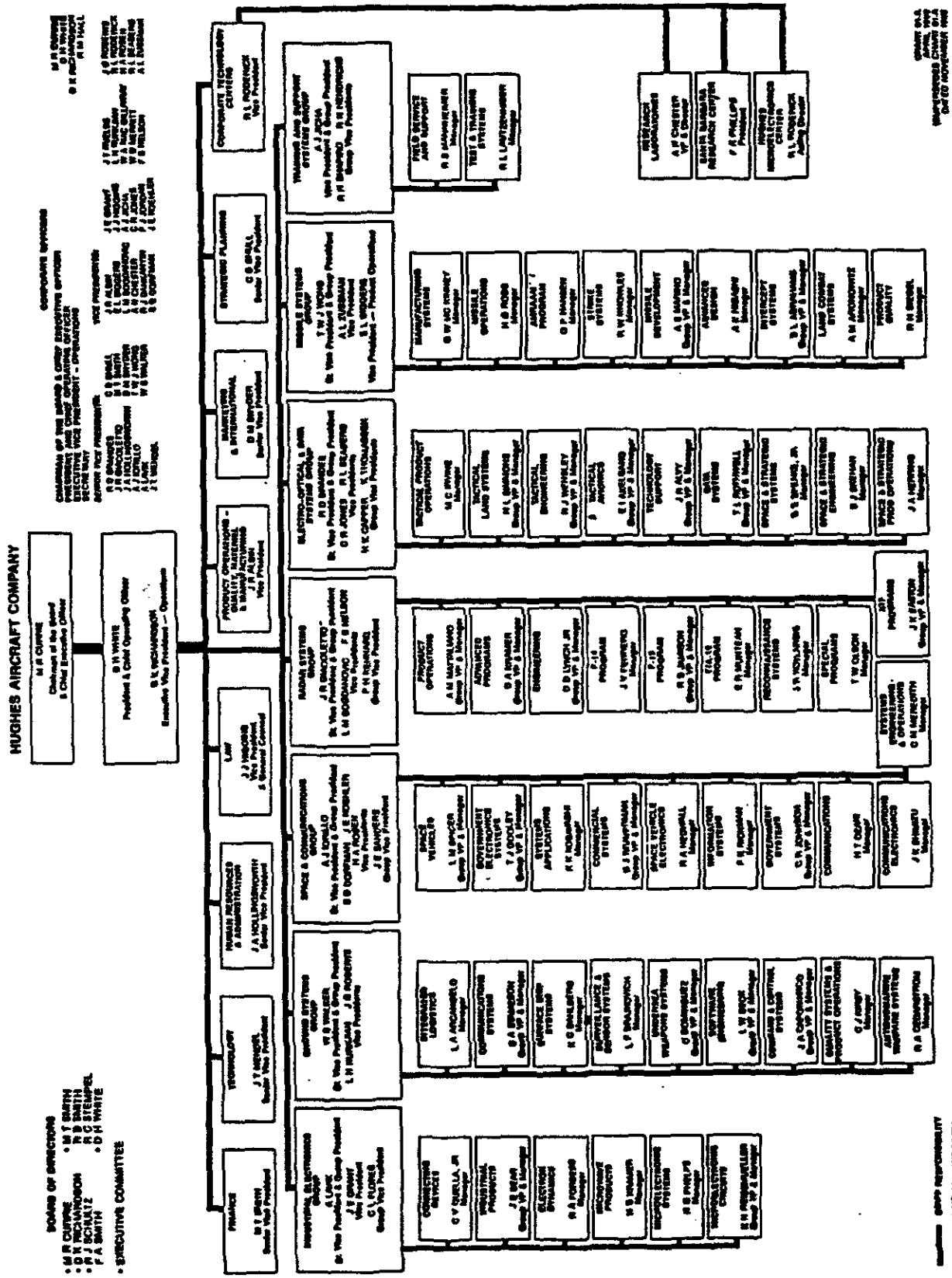


Figure 4: Hughes corporate organization.

Integrated testing laboratories, computer and processing facilities, and engineering personnel offices are available to support hybrid array development. Facilities and equipment are available to measure and evaluate all the critical performance parameters of integrated detector assemblies. Cobalt radiation test equipment for radiation hardness verification is also available. Some of the key facilities and equipment are located in the Space and Strategic Engineering Division's Integrated Focal Plane Array (IFPA) Laboratory. This laboratory includes a dedicated computer- aided facility for testing and evaluating the performance of detectors, readouts, and signal processing electronics. It has four permanent, fully equipped test consoles. Flying spot infrared scanners measure detector/readout infrared performance over a wide range of dwell times and signal and background photon fluxes in the sensor systems being simulated. This facility has been further enhanced by the addition of a computer and laboratory interface system that can be connected to the test instrumentation to log data and control test sequence.

Hughes Microelectronics Center HMC, with a staff of approximately 600 people, is located in a 150,000 square-foot facility in Carlsbad, CA. Various semiconductor devices are produced here, including silicon infrared detector arrays, advanced readouts, SOS/CMOS, germanium, and bipolar CMOS mixed technology chips. Facilities exist to design, process, test, and package very complex analog and digital integrated circuits. The programs supported range from low volume prototype parts for systems in the early stages of development to parts fabricated according to appropriate military standard procedures for space/flight programs. The facility contains the VHSIC 1 pilot line.

HMC delivers approximately 4000 parts per year for development and flight programs. In the digital SOS/CMOS area, the following programs are representative of this capability: the Miniature Vehicle Sensor, Thornton Secure Communication, MILSTAR signal processing, M-1 Abrams tank, forward looking infrared multiplexers, USASDC VLSI radiation hardening, and very high speed integrated circuits. For the analog command and control electronics and silicon focal plane arrays (FPAs), successful technology demonstrations have been achieved in the Advanced Anti- tank Weapon System-Medium, Fiber Optic Guided Missile, High Endoatmospheric Defense Interceptor, Highly Calibrated Airborne Measurements program module using doped silicon area arrays, Trident program using a visible imaging array, and a variety of other programs such as Advanced Sensor Demonstration, FAS Joint Services Seeker, PATHS,

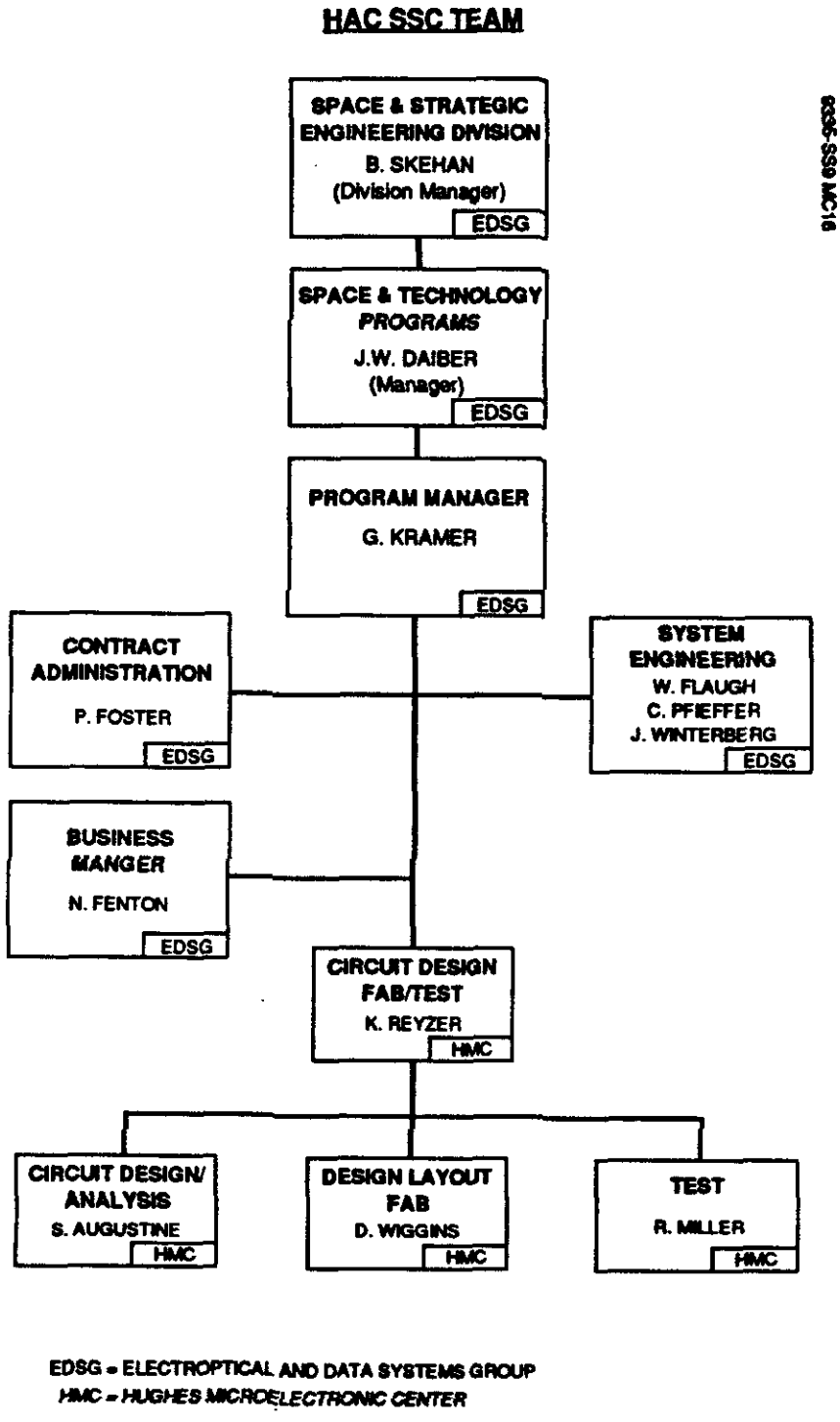


Figure 5: Hughes organization for the Pixel Vertex Detector System Development for SSC program.

and AOA. These efforts demonstrate a unique ability to design and fabricate state-of-the-art hardware.

Processing: The HMC processing laboratory is responsible for the fabrication of prototype linear integrated circuit devices, as well as the development of state-of-the-art processing technology in support of Hughes' numerous MFPA programs. High quality workmanship and stringent process control are emphasized. The 12 furnace tubes are assigned to oxidation (both dry and pyrogenic), diffusion drives, and low pressure chemical vapor deposition of silox and polysilicon. The implementation of Bruce microprocessor control to the furnaces has greatly extended the range of processes and the degree of process control. The use of Canon 2X and 4X projection aligners enables high quality photolithography for dimensions down to 1.0 m. Two Varian sputtering systems are operational; one has three S-gun targets (two dc and one rf) for developmental work; the other, with two (dc) S-guns, is used for standard pure Al depositions. Additional capabilities include a two-chamber AMT 1200 epitaxial reactor and an ion implanter.

FPA Assembly: Facilities include an evaporation system dedicated to the deposition of indium for point interconnect bonding (PIB). The indium PIB approach is used for both device-to- substrate or multilayer electrical interconnect substrates bonding, and for bonding together hybrids of detector chips directly mounted on readout chips. A flip-chip bonding tool was specifically designed and built to accommodate PIB. Using infrared optics and precision mechanical controls, devices with 100,000 interconnects can be made with uniformity, excellent alignment and planarity, and high yields. State-of-the-art photolithographic and evaporative processes enable the precision definitions of a variety of materials for conduction on any required substrate surface. An inverse optics FPA alignment tool was developed and built at HMC for the precision mounting and alignment of the FPA devices to a substrate.

Hybrid Array Testing: More than 90 engineers and technicians support the FPA test department, including engineering, production testing, and custom test equipment and software fabrication. Six general purpose FPA test stations are capable of FPA cryogenic/optical measurements. Each system has a real-time data acquisition and display capable of acquiring data up to 10 MHz with 12-bit resolution and displaying corrected FPA images up to 1024x1024 arrays at a 30-Hz rate. All test systems are computer controlled with programmable bias supplies, pulse generators, word generators, data acquisition and display,

dewar temperature control, blackbody and modulator, and X-Y table for focus spot measurements. One wafer parametric test system, four portable semiconductor parameter analyzers, and two detector test stations are available for measuring individual components. All test systems have a low current (¡10 pA) capability. Software packages are available to extract parameters and support the development of new models.

Three radiation sources are used to characterize FPA devices. An ARACOR x-ray source produces variable radiation dose rates from 2 to 200,000 rad/min in silicon over a 0.3 to 0.9 cm2 area. X-ray energy is variable from 10 to 60 KeV. The unit is equipped with a wafer prober, package part holder, and custom 68-pin liquid nitrogen dewar. A 50-milliCurie cobalt60 source is used to measure transient effects up to 108 photon/cm2-sec, and a 2400-Curie cobalt60 source is used to measure total dose effects up to 2x105 rads(Si)/hour. Each source has a custom 68-pin liquid helium dewar within the radiation chamber.

Three analog test stations are available to test radiation hard analog-to-digital converters, digital-to-analog converters, and variable gain amplifiers that are part of the FPA pre- and postprocessing electronics. All the test stations have 12-bit resolution on all input bias supples, pulse drivers, and function generators. The data acquisition uses a logic analyzer (16 channel, 8K memory) or a digitizer (10 bits at 30 MHz, 4K memory).

In addition, 20 dedicated test stations support major programs, and six detector test stations measure spectral response from 2 to 18 mm, pulse responsivity, and spectral noise.

Readout wafer testing includes operability, output gain and offset over the output amplifier operating range, input source follower input gain and linearity, and power dissipation. Each test is automatically graded, and a wafer summary is printed with yield statistics.

The SCA test station optically tests the SCA (a detector array indium bonded to an amplifier/multiplexer array). After the detector bias is optimized, the SCA is tested for pulse response, noise, noise equivalent power, and linearity over the systems operating background and signal levels. A crosstalk test is performed by focusing a spot onto a single detector measuring the response in the surrounding detectors.

Hughes Research Laboratories HRL leads in fundamental research and development. With over 500 personnel, this facility is one of the world's most advanced laboratories dedicated to basic research and early technology development. This facility has produced literally thousands of technology breakthroughs which have resulted in the giant strides necessary to convert concepts into operational systems. HRL is a pioneer in the materials, evaluation techniques, detector design, and process development for focal plane technology. They have been and currently are directly involved in the rapid advancement of bulk silicon, blocked impurity band silicon, mercury cadmium telluride, and numerous other infrared detectors. In addition, radiation hardened GaAs electronic circuits are being developed.

8.1.4 KEY PERSONNEL RESUMES

GORDON KRAMER, Manager, Technical Staff, EDSG. BSME, The Cooper Union, 1959; MS (Engineering Science), California Institute of Technology, 1960. Mr. Kramer rejoined Hughes in 1985 and is coordinating technology programs between EDSG and HMC. He has an extensive background in the research and development of solid state and thin film electronics, radiation detectors, and electro-optic devices. Mr. Kramer spent 8 years at Aerojet Electro Systems Company in the development of integrated focal plane arrays. He was previously employed at HRL. Mr. Kramer was the associate program manager in the PATHS/SEER Programs Office. He is currently the program manager on the SDIO sponsored program, HYWAYS (Hybrids With Advanced Years for Surveillance).

K.C. REYZER, Head, Strategic Engineering Development, HMC. BS (Engineering Science), Purdue University; MS (Engineering Science), California Institute of Technology; PhD (Electrical Engineering), UCLA. Dr. Reyzer has worked with electro-optical devices for the generation, detection, and postdetection processing of both visible and IR radiation. His experience includes engineering and technical management for research, development, engineering prototype, and flight hardware programs. His organization is responsible for readouts, detector array hybrids, and FPM development for strategic applications.

FRANK L. AUGUSTINE, Senior Staff Engineer, HMC. BS, MS, and PhD (Electrical Engineering), Purdue University. Dr. Augustine has been with

Hughes since 1984. During that time, he has been involved in bulk and IBC detector modeling, advanced radiation hard readout development, and advanced low power FPA module development. He was co-designer of the CRC-310 SFD readout used on the SEER program, directed the design and fabrication of the CRC-333 SFD readout used on the PATHS program, designed the CRC-334 CTIA readout used on the PATHS program, and was the responsible engineer for the virtually biased impurity band integrating transducer subtask on the Advanced LWIR Concepts program. He is the IR&D project manager for FPA readout development in the Focal Plane Laboratory. Prior to joining Hughes, Dr. Augustine was a VLSI process engineer for Hewlett-Packard Company.

CARL PFEIFFER, Laboratory Chief Scientist, EDSG. BME (Mechanical Engineering), Cornell University. Mr. Pfeiffer has been with Hughes since 1979. He was designer and technical director of electro-optical signal processor development for the Forward Acquisition System and Airborne Optical Adjunct. He is now extending this work to the "third generation" design, to be used for the Ground-Based and Space-Based Surveillance Systems (GSTS and SSTS) and the Midcourse Surveillance Experiment (MSX). He holds patents on the Extremely- High-Speed, Real-Time Background Filter for Radiation Detector and on the Array Correlation System for Radiation Detector. He also invented the Folded Dynamic Range Detector Readout and the Coherent Delay and Integration of detector arrays, which are now being developed for use on GSTS and SSTS. Prior to joining Hughes, he was a senior staff engineer at TRW Systems Group and Supervisor of the Space Guidance Theory Group at Jet Propulsion Laboratory.

DAVID G. WIGGINS, Project Engineer, HMC. BS (EET), Brigham Young University; MS (EE), San Diego State University (to be completed December 1990). Mr. Wiggins joined Hughes in September 1985. He is currently acting as a project engineer for high density, low noise CMOS readout circuits for focal plane arrays. Previously Mr. Wiggins designed analog radiation hard signal processing components and clock/bias generation circuits. Prior to joining Hughes, he worked at AMI where he designed and tested standard cell and gate array products. While pursuing his BS degree he worked at Hughes in Fullerton as a student engineer performing analog design and first article testing.

WILLIAM H. FLAUGH, Chief Systems Engineer on Airborne Optical Adjunct Program, EDSG. BS (Physics), California State University, Long Beach. Mr. Flaugh is responsible for all AOA system engineering activities, including

requirements allocation and flowdown, signal processor algorithm development, simulation subsystem performance estimation and monitoring, subsystem specifications, subsystem test planning and data evaluation, specification compliance verification, and customer liaison. Previously he was chief system engineer for SBSS payload activities, including requirements flowdown and subsystem design coordination, at Rockwell International. Prior to rejoining Hughes in 1984 he was manager of the Sensor Systems Engineering Group with responsibility for all system engineering activities associated with strategic electro-optical sensors. These activities included sensor performance characterization, generation of system and subsystem specifications, configuration trade studies, and system interface definition.

JOHN WINTERBERG, Systems Engineer, EDSG, B.A. Physics, University of Pennsylvania. Mr. Winterberg has been with Hughes since 1985. He is systems engineer responsible for the design, integration, and test of a signal processor that processes data from large IR focal plane consisting of 38,000+ detectors, using parallel pipelined signal processor operating on all detectors in real time as well as distributed data processor for array-to-array correlation and state vector estimation. He is also responsible for the design and development of signal processing algorithms as well as the detailed simulation of the IR system, and for ensuring and determining system compliance to requirements. Prior to joining Hughes, Mr. Winterberg developed 3-D non- contact coordinate measurement system at Ball Aerospace and Electronic Systems Division. Previously at the University of Pennsylvania, he participated in Fermilab collaboration E395 and E609 and participated in the a-a collaboration at ISR.

8.2 A READOUT DESIGN FOR HIGH FLUX ENVIRONMENTS

The following paper was given at the Snowmass conference in 1988.

SILICON TRACKING DEVICES FOR THE SSC

David R. Nygren
Lawrence Berkeley Laboratory
Berkeley, CA 94720

Abstract

The desirable properties of pixelized silicon charged particle detectors in the SSC context are discussed and compared with silicon strip detectors. A device architecture matched to the SSC environment, the "smart pixel array," is presented in some detail. Pattern recognition experience and Monte Carlo studies with QCD jet events are discussed. The radiation hardness advantage of pixelized detectors is developed quantitatively. A new high temperature process developed at LBL, permitting simultaneous fabrication of high quality transistors and detectors on high-resistivitiy material is presented. The current status of pixel and strip detector development at LBL is briefly reviewed.

1 INTRODUCTION

Tracking requirements at the SSC can be broadly characterized by the challenges of resolving many closely-spaced tracks within high multiplicity jet-like events, of measuring high momentum tracks accurately, of achieving efficient coverage of a large solid angle, of detecting secondary vertices, and of maintaining effective rejection of enormous instantaneous background rates. Together, these requirements drive the physical segmentation of tracking systems under consideration to an unprecedented level. In the case of silicon strips, tracking systems approaching a million addressable elements have been under study.[1-2] Systems with pixelized detectors involve at least an order of magnitude more.

Although the segmentation of a pixelised tracking system is very large, the advantages are compelling: track detection essentially free from overlap and complete absence of ambiguity in event reconstruction. Despite the expected complexity of SSC events, a non-projective tracking system with high resolution can reduce the necessary number of tracking layers to less than six. Additional advantages of pixelized detectors are a very large intrinsic signal/noise ratio and an effective radiation hardness that can easily tolerate decades of full luminosity SSC operations.

Despite large system segmentation, the quantity of primary tracking data that must be read out for even a rather complex event will be quite modest, on the order of 10 kilobytes. From the standpoint of system design, therefore, it is essential that the readout scheme be able to skip very efficiently over empty elements. In other words, the system architecture must be matched to the ultra-sparse nature of the data field.

With regard to random backgrounds, it is also clear that SSC detector systems must provide local time-slice buffering of information, at least until level I triggering decisions can be made. For example a detector without buffering will have contributions from about 100 events/microsecond at the design luminosity, adding perhaps 3600 extra background tracks (for ±3 in pseudorapidity coverage) to any event of interest. Given the complexity anticipated for most SSC events of interest, any unnecessary addition of out-of-time tracks to the reconstruction task will be a heavy and perhaps overwhelming burden. Therefore, the architectural concept must include time-slice buffering associated with pattern information.

Strip detector readout systems can be equipped with time-slice buffering in a relatively straightforward way. The design of VLSI electronics for this purpose has been undertaken already by several groups.[2-5] For pixel devices, the situation is more complicated, and an architecture that capitalizes on the ultra-sparse character of the data seems appropriate. To provide some background for discussion, it is useful to review briefly the characteristics of some existing pixel devices. The suitability for the SSC of another interesting device, the silicon drift chamber, is treated elsewhere in these proceedings.[6]

The most familiar pixel device, and the only type to be used thus far as charged particle detectors for high energy physics research, is the optical CCD.[7] Optical CCD's are designed with the presumption that all pixels carry wanted information, and the devices are organized to read out every pixel. Readout times are in the millisecond range. In short, these devices have an architecture diametrically opposed to the needs of the SSC. In addition, the depletion depths are on the order of only 10 - 20 μm, resulting in relatively small signals for charged particles. Operation at cryogenic temperatures is required to eliminate substantial dark current levels associated with the long readout time. Finally, rather husky high-speed charge transport clock drivers must be located nearby, requiring careful system design to minimize induced noise. Nevertheless, impressive spatial resolutions have been obtained: ±5 μm rms in x and y, and ~40 μm double track resolution.[8]

To ameliorate the serious limitations of the CCD in this context, various concepts have been considered, such as fast gat-

ing, fast clearing, and simultaneous sensing of an entire row for presence of hits. However, none of these provides a really fundamental solution to the limitations of the CCD concept for the SSC. It would appear that conventional CCD's will play no significant role in tracking at the SSC.

There also are less familiar pixel devices organized around a row-column intersect, random-access principle, such as those developed by Hughes Aircraft Company.[9] These elegant hybrid devices have addressible amplifiers on each pixel, and have also been used for scientific applications ranging from IR astronomy to x-ray detection. The amplifiers are unpowered until readout, and hence these devices lack altogether the capability to provide time-slice buffering with pattern information, an essential feature for the SSC. Because the pixels are normally quiescent and produce no prompt signals, there is no straightforward way to add the time-slice buffering capability. In addition, the random access feature by itself does not provide the means to search efficiently for struck pixels; a complete scan is still necessary. A random access architecture by itself is not a solution.

What is needed for the SSC is an architecture that provides unambiguous, direct registration and efficient readout of pixels which have been struck in the particular time slice of interest. The Smart Pixel array concept developed at LBL is intended to provide a solution matched to the challenge of the SSC environment.[10]

2 SMART PIXEL ARRAY

2.1 Concept

The basic concept of the Smart Pixel Array is that each pixel shall be equipped with continuously sensitive circuitry, so that prompt signals will be generated at the instant charged particles pass through a given pixel. These prompt signals are propagated directly to x-y pattern registers at the periphery of the chip. The pattern registers store the occurrence of these signals as fast time-sliced pattern information. The buffers within the pattern register are made deep enough to accommodate the time neccesary to generate a level I trigger. An event trigger will initiate pixel charge interrogation, directed efficiently by the stored pattern information for the time slice of interest. The direct interrogation of pixel charge content eliminates nearly all ambiguities at this stage, an especially important feature. The primary data are space points essentially free of pile-up and ambiguity. The device thus operates in two distinct modes, a pattern acquisition mode, and a random-access pattern-controlled readout mode. This functionality is illustrated schematically in figure 1.

The smart pixel array has been developed at LBL by D. Nygren and H. Spieler. In this concept, a smart pixel requires considerable circuitry to realize the needed functionality. A low-noise low-power amplifier, shaping element, and discriminator are needed to detect the occurrence of a hit. In addition, an analog memory element is required to provide hit verification during readout and interpolation information during reconstruction. Digital logic to propagate the "hit" signal to the pattern registers, to respond to interrogation, and to provide reset is also needed. Analog to digital conversion is done off-chip.

Nevertheless, for a standard 2 μm feature size CMOS foundry process, this circuitry fits into an area of about 100 × 100 μm^2. The circuitry can just as easily be packed into an equivalent

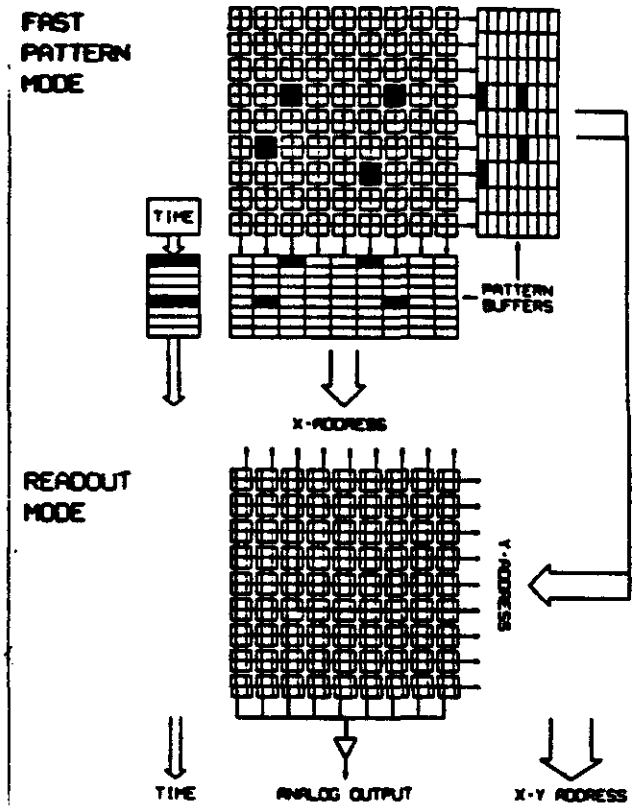


Figure 1: A schematic depiction of the smart pixel array concept modes of operation. During data acquisition, pattern and time information are stored in the buffers on the chip edge, while analog information is retained in pixels. For readout, row information for the time slice of interest efficiently directs interrogation of column information, including verification of hits by analog readout of struck pixels.

rectangular area of about 40 × 250 μm^2, a more natural choice from the standpoint of circuit layout. The elongated rectangular shape can be used to provide higher resolution in phi using the narrow dimension, while the longer dimension along the z direction is a natural match of typical detector thickness ($\simeq$280μm) to the range of track angles associated with a long luminous region. This area requirement, though substantially larger than non-smart pixels, is still small enough to provide excellent pattern recognition, as discussed later. At a 10 cm radius the hit rate per pixel is just 100 Hz at full SSC luminosity. This allows plenty of time to retrieve the analog information during readout.

As is well-known, charge sharing among neighboring detector elements provides analog information that can be used to reduce the spatial resolution to a small fraction of the element size. It should be sufficient here simply to note that the pixel size in one dimension at least can be made as small as that of strip detector systems (with much poorer signal/noise) that have provided resolutions smaller than 5 μm.[11]

The implementation will be as a hybrid array, in which the detector wafer and readout integrated circuit (IC) are separately fabricated and are joined together using the well-established "indium bump bonding" technique. This allows separate optimization of the detector and readout IC, using standard technologies.

For the SSC in particular, this permits the use of available commercial rad-hard IC foundry processes for the readout IC. For the indium bump interconnection of detector and readout IC, a bonding pad of about 40 x 40 μm^2 will be needed; however, it is possible that some of the circuitry can be placed under the bonding pad aluminization to save some space. The trend toward smaller feature size, now at 1.0 μm for advanced commercial processes, offers the prospect both of improved performance and significantly smaller pixel area requirements.

Eventually, a monolithic implementation with the readout circuitry integrated onto the detector surface may be possible. As discussed briefly below, significant advances toward this goal have been made recently at LBL.

2.2 Pixel Performance

The principal issues here are signal/noise ratio, speed of response, power dissipation, and radiation hardness. In addition to this list of concerns for device design, there is a formidable set of problems associated with the implementation of a large system. A detailed discussion of these vital issues is outside of the scope of this paper. A more complete technical discussion can be found in our 1987 LBL DOE proposal.[10]

The signal/noise ratio for smart pixel arrays can be very high, primarily because the electronic noise in this case can be made very small. The capacitance presented to the amplifier by a pixel of 100 x 100 μm^2 is $\simeq$100 fF, dominated by edge effects. Coupled to a well matched amplifier, this miniscule capacitance leads to extremely low predicted noise levels, *e.g.* $\leq$ 100 electrons rms for our designs. It is worth mentioning that similar noise levels have been regularly observed for various MOS circuits with similarly low input capacitance. Furthermore, it is important to note that an architecture that would gang a pixel amplifier outputs to individual row/column discriminators will increase the noise by $\sqrt{n}$, compromising the signal/noise ratio by at least a factor of 10.

With regard to signal, a fully depleted detector of 280 μm thickness will on average provide a signal corresponding to 22,500 electrons. The calculated signal/noise ratio thus exceeds 200. This favorable situation provides several circuit and system design advantages:

1. **Simplicity** The design of front-end circuitry can be significantly simpler than that for strip systems. This leads to smaller area requirements for the pixels. Alternatively, some signal/noise can be traded for a reduction in power dissipation.

2. **Threshold** The impact of unavoidable manufacturing variations on amplifier and discriminator threshold characteristics of a large-scale system should be negligible; in other words, it should be easy to find an operating point for a pixel array that rejects all electronic noise, while providing essentially 100% efficiency for minimum ionizing particle tracks. Recalling the ultra-sparse nature of the data, it is clear that the ability to reject all electronic noise is an important attribute for any system with a very large number of discrete detection elements such as the strip or pixel systems envisaged for the SSC. This may not be as easy to achieve for large-scale strip systems, which may be expected to have a signal/ noise ratio of $\simeq$ 10-20. For example, setting the threshold at 3.5 σ on an otherwise ideal system with 10^6 strips, 10 nsec RC-CR shaping time, and gaussian noise will introduce 900 extra noise hits. To accommodate the inevitable circuit variations and noise conditions of a real system, the thresholds may have to be set considerably higher than this, with possible loss of efficiency for real tracks.

3. **Radiation Damage** A signal/noise ratio of several hundred provides considerable headroom for the accommodation of deterioration due to radiation damage. This deterioration can occur in both the detector and the readout circuitry. In detectors, the initial effect caused by radiation damage is an increase in shot noise due to increased dark current. A quantitative treatment of the noise problem due to radiation damage to the detector is given in a subsequent section. After irradiation, MOS transistors also display degraded noise characteristics although the sensitivity to damage depends upon the manufacturing process. There is some evidence that JFETs, which do not employ an oxide layer for their functionality, show very little deterioration in noise characteristics at the few Mrad level.[12] The relationships among noise characteristics, process, and radiation damage are not well-documented; more study is clearly warranted.

4. **Time Resolution** Another benefit of the very large intrinsic signal/noise ratio is that the risetimes of the pixel amplifier/discriminator can be long relative to the 16 nsec interbunch period of the SSC and still tag the correct time slice. The time resolution is determined by the amplifier integration time t_i and the signal/noise ratio (S/N = R):

$$\delta t = t_i / R$$

An integration time of 100 nsec is possible within the power dissipation constraint; the calculated time resolution is thus a small fraction of the SSC bunch period. Alternatively, longer peaking times can offer reduced power dissipation without loss of time resolution.

Speed of response, power dissipation, and electronic noise are strongly interrelated circuit design issues. A natural constraint is the maximum allowed power dissipation. Hefty power distribution busses and cooling mechanisms would add undesirable mass close to the vertex. A reasonable limit would appear to be 100 mW/cm^2, or 10 μW per pixel.

2.3 Discussion

Unlike other pixel concepts, the smart pixel array concept contains an inherent *economy of action* principle. During data acquisition, the smart pixel array is quiet until traversed by ionizing radiation. There are no strobes or clock signals continuously scanning the amplifier array. System power dissipation and induced noise are minimized. In the design we prefer, the SSC bunch crossing signal is continuously scaled by a single counter. Prompt pixel signals cause both the timing counter status and the pattern information to be strobed into augmented pattern+time registers, thereby linking the two kinds of information. The strobe pointer is then incremented to await the next hit. This signal-driven design avoids unnecessary activity, and very substantially reduces the depth requirement for the

pattern+time registers. For example, a 4 cm^2 device (a size we hope can eventually be manufactured) at 10 cm radius will experience, on average, 4 hits in one microsecond, a likely level I trigger interval. Unless secondary backgrounds are dominant, 16 time slices should be more than sufficient to accomodate natural rate fluctuations. This may be compared with the depth of 64 time-slices needed to span one microsecond in a continuously clocked design.

3 PATTERN RECOGNITION

Pixel devices have the self-evident virtue of providing nonprojective spatial data. However, the actual level of performance will depend upon several factors such as pixel size, proximity to the beamline, the underlying physics of an event (*e.g.*, QCD jets vis-a-vis Higgs production), and ability to reject background.

Thus far the only example of the use of pixel devices in an experiment is with CCD's in CERN NA32.[13] NA32 also employed a silicon strip system, which permits a limited comparison of strip and pixel information quality. Monte Carlo studies at LBL have also provided useful information about pattern recognition.

3.1 NA32 Experience

NA32 is a fixed target experiment which had the goal, among others, to identify charm particles and measure their lifetimes. In essence, a short target was followed by an array of 7 planes of silicon strips positioned from 5 to 12 cm after the target. The experiment was operated at first without the CCD's. Under these conditions, two independent reconstruction efforts found charm events with low efficiency, and with an overlap of only 15%. The dominant problem was merged tracks in the early planes. Only about 60% of all clusters were distinct .

Two GEC P8600 CCD devices were subsequently added, at distances of 1 and 2 cm from the target. The pixel size of these 385 x 580 arrays was 22 x 22, μm^2, leading to ~5.0 μm rms spatial resolution and ~40 μm two-track resolution. With the information from the CCD's, efficiencies for identifying charm events increased very substantially, and the overlap rose immediately to more than 85%. The CCD's in combination with clean microstrip hits and the downstream drift chambers were sufficient to resolve a large sample of charm events without background. Both the spatial resolution and the two-track resolution contributed to the effectiveness of the CCD's. It should be noted that this experiment pioneered the utilization of both strip and pixel devices for physics; however, later experiments such as FNAL E691, using finer resolution microstrip planes, have also found large, clean charm event samples.[14]

3.2 Monte Carlo Studies

Monte Carlo studies of some aspects of pixel performance have been made at LBL in collaboration with Ed Wang. The questions that these Monte Carlo studies addressed include the following:

- For QCD jets of 0.3 and 1.0 TeV/c, aimed normally at the center of a pixel array from a distance of 10 cm, what fraction F of events are registered with no more than 1 track per pixel?
- How does the fraction F depend on pixel area and shape?
- What is the relative performance of other kinds of pixel arrays that lack some capabilities of the smart pixel array?

The benchmark physics process chosen for these studies is the QCD jet, generated with the code Pythia 4.8. At the SSC high $P_\perp$ QCD jets will be tightly collimated, dense and frequent. Their study will contribute much to a more fundamental understanding of hadronic processes at high energy. These jets therefore would appear to provide a rather stringent yet straightforward test for pattern recognition efficiency. The detection of secondary vertices from heavy quark decays is another vitally important topic, but the software needed for a careful study of these processes was not yet available.

The geometry developed for this study typically consisted of a pixel array of area 1 x 1 cm^2, with options for variable pixel size and shape. The known axis of the QCD jet was aimed normally at the center of the array from a distance of 10 cm. Figure 2 shows a Lego plot of particle frequency for 1000 events; for clarity, large pixel sizes were chosen for this figure. The densely populated central peak riding on a broad background illustrates the inherent reconstruction difficulty. For the 1 TeV/c jets, the average charged particle multiplicity within this 1 cm^2 area is 12, with fluctuations up to 30.

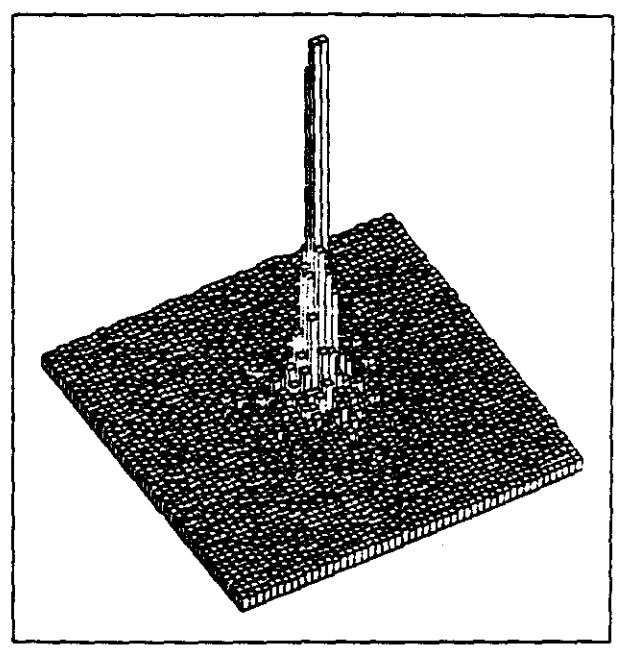


Figure 2: The density of tracks normally incident on a 1 cm^2 pixel array 10 cm from the point of production of 1 TeV/c QCD jets. A densely populated central region riding on a broader background makes this a particularly challenging class of events to reconstruct.

The fraction F of fully resolved events, *i.e.*, the fraction of events that are registered with no more than one track per pixel, versus pixel dimension (for square pixels) is given in Figure 3 for 1 TeV/c jets. It is noteworthy that even for rather large pixel dimensions such as 100 x 100 μm^2 the fraction F is still as high as 0.9. Most of the remaining events have just one pixel with two tracks. The lower energy 0.3 TeV/c jets gave somewhat higher

F values due to the lower multiplicities.

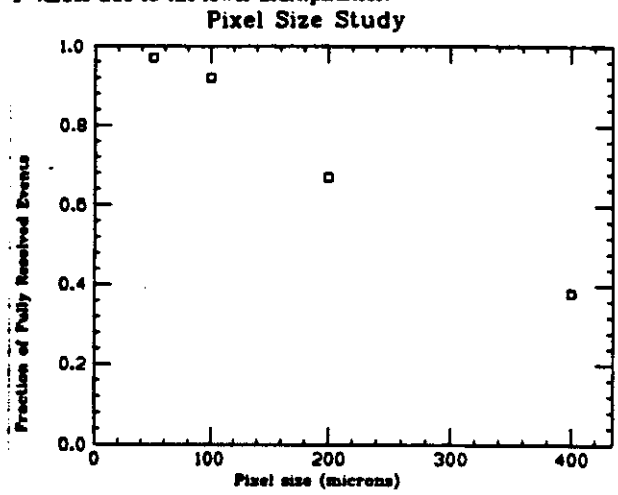


Figure 3: For 1 TeV/c QCD jets normally incident on a 1 cm^2 pixel array 10 cm from the production point, the fraction F of events with all tracks fully resolved is shown versus pixel dimension. Although this plot is for square pixels, equivalent results were found for rectangular pixels of equal area.

Rectangular shapes, such as 40 × 250 μm^2, were also studied with the conclusion that the F values depend only on the pixel area. While much work remains to be done, it seems clear from these studies that pixel devices with pixel areas on the order of 10^4 μm^2 can provide excellent pattern recognition capability even for very challenging processes such as QCD jets.

The smart pixel architecture retains analog information on the pixel for subsequent readout and pattern verification. Another architecture studied employed a three-axis pattern registration (x-y-u), but with no analog sample and hold. Pattern identification would be accomplished by an off-line 3-axis coincidence match. The motivation for this study was to see if the potential advantage of circuit simplification would be offset by difficulties in pattern identification due to chance coincidences. The results indicated, however, that the number of chance 3-fold coincidences was rather high: a 50% increase in apparent "hits" for a 50 × 50 μm^2, rising to 80% for 100 × 100 μm^2, for the 1 TeV/c QCD jets. For this reason and because this architecture has an intrinsic resemblance to a strip geometry, we chose not to study this particular architecture further.

4 RADIATION HARDNESS AND DETECTOR ELEMENT SIZE

4.1 Theoretical Background

In addition to basic material properties, the radiation hardness of semiconductor detectors depends on design parameters of the detector and the readout electronics system. Substantial gains in the ability of a silicon detector to tolerate radiation damage can be achieved through a high level of segmentation, such as is naturally achieved in a pixel array. This section summarizes the treatment presented by D. Nygren and H. Spieler in the *Report of the SSC Task Force on Radiation Effects at the SSC*.[15] Two basic mechanisms are responsible for radiation damage in silicon detectors:

1. Displacement of atoms from their lattice sites (bulk damage).
2. Electron-hole pair generation in isolation layers, with trapping.

Displacement damage seems to be dominant in high energy physics applications of semiconductor detectors. These effects are easier to predict than the ionization mechanisms in dielectrics because they are much less sensitive to processing variations. Displacement damage manifests itself primarily through three phenomena:

1. Increased leakage current (shot noise).
2. Change in the resistivity of the material (depletion voltage effects).
3. Increased recombination or trapping of signal charge.

Increased leakage current is the most prominent initial effect. More work is needed for a quantitative assessment of the other two. The discussion here deals only with the impact of the leakage current.

The leakage current increase is due to the generation of carriers by radiation-induced lattice defects, which create intermediate energy levels in the band gap. This leakage current contributes shot noise Q_n

$$Q_n = (I_L \cdot t_i/q_e)^{1/2} \tag{1}$$

where Q_n is expressed in electrons, q_e is the electron charge, I_L is the leakage current, and t_i is the effective integration time of the circuitry. The signal Q_s obtained from the detector is

$$Q_s = n_s \cdot W \tag{2}$$

where n_s is the number of electrons per unit length created by the particle traversing the detector, and W is the thickness of the sensitive layer. It is useful to cast the discussion in terms of the signal-to-noise ratio $R = Q_s/Q_n$. From equations 1 and 2, the maximum current that can be tolerated is then

$$I_L = (n_s^2 \cdot W^2 \cdot q_e)/(R^2 \cdot t_i) \tag{3}$$

For a silicon detector n_S = 80 electrons/μm for minimum ionizing particles; this yields the numerical equation

$$I_L = (100nA \cdot \sec \cdot cm^{-2})W^2/(R^2 t_i) \tag{4}$$

A typical case might be W = 300 μm and t_i = 100 ns, which allows a maximum current of 90 nA if we require a signal to noise ratio of R = 100, or a current of 9 μA for R = 10.

The detector leakage current is directly dependent on the generation lifetime t_g through the relation

$$I_L = q_e \cdot n_i A \cdot W/(2 \cdot t_g) \tag{5}$$

where n_i is the intrinsic free carrier concentration (thereby introducing an implicit temperature dependence) and A is the area of the detector.[16] The effect of displacement damage on ti_g is given by[17]

$$1/t_g = 1/t_{go} + K \cdot F \tag{6}$$

where t_{go} is the pre-irradiation geseration lifetime, F is the particle fluence and K is the damage coefficent associated with the specific type of radiation and detector material. In a system designed to sustain substantial radiation damage $t_{go} \gg t_g$, and this expression may be simplified to

$$1/t_g = K \cdot F \tag{7}$$

Inserting (7) in (5) yields the detector leakage current as a function of radiation type and dose:

$$IL = q_e \cdot n_i \cdot A \cdot W \cdot K \cdot F/2 \tag{8}$$

Combining this expression with (3) defines the interdependence between signal-to-noise ratio R, radiation type and dose (K, F) and detector/readout parameters (n_s, A, W, t_i). The allowable fluence, for example, is

$$F = (2 \cdot n_s^2 \cdot W)/(K \cdot n_i \cdot A \cdot R^2 \cdot t_i) \tag{9}$$

For a silicon diode detecting minimum ionizing particles, n_s = 80 electrons/μm and $n_i = 1.5 \cdot 10^{10}\text{cm}^{-3}$ at 300° K. Inserting these values provides a numerical relationship for the allowable fluence

$$F = (85\text{cm}) \cdot W/(K \cdot A \cdot R^2 \cdot t_i) \tag{10}$$

for a given detector/readout design. This equation provides a very instructive relationship for the evaluation of bulk effects in silicon detectors.

4.2 Discussion

Equation 9 shows that radiation hardness, in the practical sense of a system performance requirement R, is determined by several factors:

- Detector material (through n_s, n_i and the damage constant K)
- Detector geometry (through the thickness W and area A)
- Integration time of the electronics t_i

Radiation resistance can be enhanced by decreasing the area or increasing the thickness of the detector elements, or by reducing the integration time of the electronics. While all of these are design choices, detector area and integration time have the greatest flexibility; smaller elements of course bring greater electronic complexity, whereas reduced integration time leads to increased power dissipation.

For the evaluation of tracking devices at the SSC one can use equation 10 to calculate the maximum allowable area of a detecting element for a given lifetime under typical operating conditions:

$$A = (85\text{cm}) \cdot W/(K \cdot F \cdot R^2 \cdot t_i) \tag{11}$$

At distances greater than about 10 cm for the beam axis the background is expected to be dominated by neutrons from calorimeter albedo. At full luminosity the neutron fluence is roughly 10^{13} cm^{-2}yr^{-1} or 10^{14}cm^{-2} for a 10 year period. It is worth noting that the uncertainties on this value of the neutron fluence are probably quite substantial in either direction. For the following examples the values $K = 1.4 \cdot 10^{-7}\text{cm}^2 s^{-1}$ for the damage constant,[17] $W = 300\ \mu$m for the detector thickness, and an integration time t_i of 100 nsec have been adopted.

1. **Silicon Strips** In this example, the system is assumed (idealistically) to display an initial signal-to-noise ratio $R \gg 20$, where the noise is determined by the strip capacitance at the preamplifier input. How large can the strip size be and still provide $R = 20$ after 10 years of operation? For a strip pitch of 50 μm, the calculated length using equation 11 is about 1 cm. This would be the case if there were no room temperature annealing; however, preliminary results presented at this conference by Kondo *et al.* indicate for their devices an anneal time constant of about 160 days.[3] This interesting result may, however, depend on processing choices. If this anneal time constant is a general result, then the corresponding length for $R = 20$ would be at least 10 cm. As noted above, faster electronic integration times can provide additional margin to preserve overall sytem performance. From the above discussion, and assuming both the generality of the annealing results and that no additional backgrounds exist, it appears possible that silicon strip detectors of $\simeq$10 cm length in a carefully designed system should survive the shot noise effect of radiation damage. Long strips near the beam pipe may not survive.

2. **Pixel Arrays** Clearly, a pixelized detector will be less prone to shot noise effects than a strip detector by the ratio of element area, all other factors assumed identical. The smart pixel element, with an area of *e.g.* 40 × 250 μm^2, is 500 times smaller than a 10 cm × 50 μm strip. The shot noise is essentially negligible after ten years, even without annealing.

5 A NEW ROBUST PROCESS FOR DETECTOR FABRICATION WITH INTEGRATED CIRCUITRY

5.1 Background

Silicon p-i-n detectors for high energy charged particles utilize high-resistivity silicon to obtain low leakage currents and large depletion depths at moderate applied voltage. Ideally, a modern detector process should offer minimum sensitivity to process-induced contaminants and would also be compatible with contemporary IC fabrication techniques. Such a process would allow the integration of front end circuitry with the detector, providing improved performance, reliability, and system design flexibility.

Until now, this has not been the case. Conventional detector processes have been found to be incompatible with the sequence of high temperature steps characteristic of IC fabrication. Very large leakage currents have been consistently observed if high temperature steps are included after the initial oxide growth. The reason is that the detector leakage current is extremely sensitive to impurities such as iron, nickel, copper, gold, etc., that introduce energy levels near the band gap center. For example, the presence of gold at a level of $1 \cdot 10^{-9}$ will increase leakage current density by three orders of magnitude. At typical IC fabrication temperatures of 1000° C, gold will migrate millimeters/hour through silicon, whereas at 600° C, the diffusion is very small.

5.2 The New High-Temperature Process

At LBL, Steve Holland has recently developed a new high-temperature process that turns the diffusion of impurities at high

temperatures to advantage.[18] In his process, impurities are effectively removed from the active region by capture on the backside of the wafer, an electrically inert region. This technique is an example of "gettering," a concept which has a long history in vacuum tube and semiconductor electronics, but until now has not been applied with such success to the problem of detector fabrication. The LBL process appears to be fully compatible with high-quality transistor and IC fabrication steps.

Briefly, the LBL process utilizes a layer of polysilicon on the wafer backside, in-situ doped with phosphorus, and formed by chemical vapor deposition at 650° C. This 1 μm thick layer serves both as the gettering layer and backside contact. The gettering properties of this layer are due to the presence of both the polysilicon and the phosphorus. Detectors and transistors were simultaneously fabricated on the same wafer along with control devices that lacked the gettering layer.

5.3 Results

Figure 4 shows the leakage current versus bias voltage for both gettered and ungettered diodes; the current is reduced by a factor of 400 at low voltages and even more at higher voltages. The leakage current at 100V, which corresponds to a fully depleted detector, is on the order of 1-2 nA/cm^2. This compares very favorably with the results of Kemmer.[19] However, the Kemmer process limits processing temperatures to 600° C after the initial oxidation, whereas devices made by the LBL process have experienced approximately three hours at 900° C. The low-temperature Kemmer process leads to incomplete activation and high sheet resistance of the implanted layers; in turn this prevents monolithic integration of high performance circuitry.

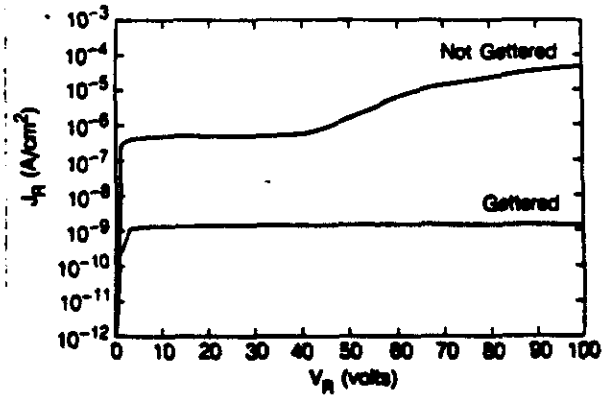


Figure 4: The detector diode reverse-leakage current for a device with backside gettering compared to one without. Both devices were fabricated on the same wafer.

The p-channel MOSFET transistors made by the LBL process were found to display good output current-voltage and frequency response characteristics. The application to the substrate of a 30V bias (sufficient for full depletion) causes only small deviations from the unbiased curves, as shown in figure 5. Diodes fabricated on the same wafer were tested up to 1000V bias, again with leakage currents on the order of 1-3 nA/cm^2.

An LBL-process detector was exposed to an Americium 241 source, demonstrating excellent energy resolution. The FWHM for the 59.4 keV gamma ray is approximately 1.8 keV, limited

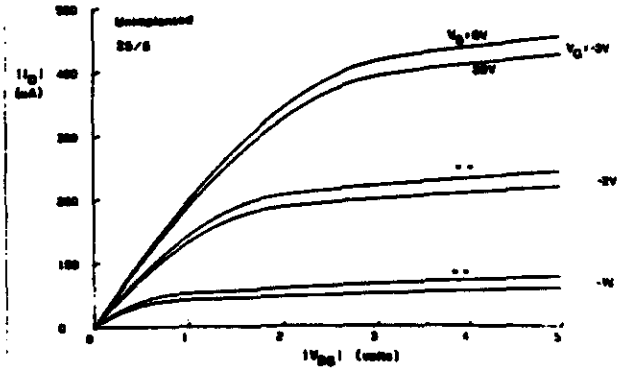


Figure 5: Current-voltage characteristics of a p-channel MOSFET fabricated on 10KΩ-cm silicon. The channel width to length ratio is 25μm/5μm. The effect of the substrate bias is seen to be small; 30V is sufficient to deplete this material.

in this instance by the noise of the signal-processing electronics. A short detector with 128 strips has also been fabricated; preliminary results indicate low ($\leq$ 10 nA/cm^{-2}) and extremely uniform ($\leq$ 3% rms) strip leakage currents .

5.4 Conclusion

An extrinsic gettering technique has been developed that provides both a robust process for the fabrication of high-quality p-i-n diodes and the prospect of monolithic integration of these detectors with high performance CMOS and/or JFET circuitry.

6 SMART PIXEL ARRAY DEVELOPMENT STATUS

6.1 Device Analysis

CMOS technology offers a combination of speed, low power dissipation, and industrial maturity that makes it the clear choice for short term readout IC goals. However, nearly all commercial effort has been focussed on digital applications. The design of CMOS devices for unconventional and demanding applications such as detectors for high energy physics requires careful evaluation of device characteristics under a range of unusual operating conditions. Modeling of circuit response is quite likely to be seriously at variance with reality if standard parametrizations of device performance are employed.

Accordingly, significant effort has been spent in performing these measurements on a variety of custom devices. These include nmos and pmos transistors of various W/L ratios and elementary amplifiers, fabricated by the MOSIS organization. In addition to the DC characteristics for a family of drain – source curves and the gain-bandwidth response, a range of channel geometries has been evaluated to provide reliable scaling relationships.

6.2 SVX IC

In addition to its basic purpose as the readout device for the CDF silicon strip vertex detector, the SVX IC [20] project serves as an important stepping-stone in the realization of the smart

pixel array. The SVX, designed mainly by Stuart Kleinfelder, offers similar noise performance to the pioneering Stanford μplex NMOS IC,[21] but dissipates a factor of 10 less power, and has a built-in sparse data readout feature that substantially reduces readout time by eliminating unhit channels. The sparse readout mode scans past empty channels at about 400 MHz. This same circuitry will be employed in the pattern readout of the smart pixel array. The input amplifier envisaged for the smart pixel array shares concepts with the SVX amplifiers.

6.3 Circuit Design Studies

A number of low-power low-noise amplifier designs have been modeled, with the aim of reducing power dissipation to the minimum compatible with response time and noise goals. Comparator designs, again building on the experience with the SVX IC have also been studied. The digital logic carried on each pixel has reached a fairly complete state. A one-dimensional array of pixel amplifiers and comparators has been submitted for fabrication through MOSIS. A two-dimensional version is planned for submission after a satisfactory evaluation of the one-dimensional chip has been completed.

6.4 Microsystems Laboratory

Considerable effort has been expended to bring into existence a new modern facility at LBL for the further development of detector process ideas and device fabrication. This new facility, the Microsystems Laboratory, provides four contiguous clean rooms offering $\simeq$700 ft^2 of Class 10 workspace. In addition to other novel detectors and devices, pixelized detector arrays will be fabricated here, possibly with integrated JFET's to provide a low-noise radiation-hard input stage for a pixel readout IC made by a standard rad-hard CMOS foundry process.

7 SUMMARY

Pixelized detectors offer several significant potential advantages relative to strip detectors in pattern recognition, systems engineering, and effective radiation hardness. A smart pixel architecture concept matched to the SSC environment has been developed, and pixel circuitry has been designed and implemented. A robust process for fabricating detectors with integrated circuitry has also been developed. With appropriate levels of effort devoted to device and system engineering, a powerful tracking system employing pixelized detectors can be realized.

8 ACKNOWLEDGEMENTS

This paper is largely concerned with the efforts and accomplishments of the LBL Advanced Detector Development Group. In addition to the explicit references to individuals within the text, I wish to acknowledge the seminal contributions made by Helmuth Spieler to the conceptual development and engineering advances of this program.

9 REFERENCES

1. *Report of the Task Force on Detector R&D for the SSC*, M. G. D. Gilchriese, ed., p. 74, June, 1986.

2. Seiden, A., "Tracking Requirements for the SSC and Silicon Strip Development," these proceedings.

3. Kondo, T., "Radiation Damage of Silicon Devices and R&D for JCCD Readout of Microstrips," these proceedings.

4. Heijne, E., "Future Silicon Detector Development in Europe," these proceedings.

5. Watase, Y., "Integrated Circuit Development in Japan for Future Experiments," these proceedings.

6. Rehak, P., "Silicon Detector and Readout Development at BNL," these proceedings.

7. Damerell, C. J., *et al.*, "Charge-Coupled Devices for Particle Detection with High Spatial Resolution," Nuc. Inst. and Meth. **185**, pp. 33-42 (1981).

8. Bailey, R., *et al.*, "First Measurement of Efficiency and Precision of CCD Detectors for High Energy Physics," Nuc. Inst. and Meth. **213**, pp. 201-215 (1983).

9. Gaalema, S., "Low-Noise Random-Access Readout Technique for Large PIN Detector Arrays," IEEE Trans. Nuclear Science **NS-32** pp. 417-418 (1985).

10. Nygren, D. R., and Spieler, H., "Semiconductor Detector and Integrated Electronics Development," LBL proposal to the DOE, July 1987.

11. England, J. B. A., *et al.*, "Capacitive Charge Division Readout with a Silicon Strip Detector," Nuc. Inst. and Meth. **185**, pp. 43-47 (1981).

12. Binkley, D. M., "A Radiation-Hardened Accelerometer Preamplifier for $2 \cdot 10^6$ rad(si) Total Dose," IEEE Trans. Nuclear Science **NS-29**, pp. 1500-1507 (1982).

13. Barlag, S., *et al.*, "Lifetimes of Charged and Neutral D Mesons," Z. Phys, C, **37-1**, 17-23 (1987).

14. Raab, J. R., *et al.*, "Measurement of the $D^0, D^+, and D_s^+$ Lifetimes," Phys. Rev. D, **37**, 2391-2402 (1988).

15. *Report of the Task Force on Radiation Effects at the SSC*, M. G. D. Gilchriese, ed., p. 74, June, 1988.

16. Sah, C-T., Noyce, R. N., and Shockley, W., "Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics," Proc. IRE **45**, 1228 (1957).

17. van Lint, V. A. J., *et al.*, *Mechanisms of Radiation Damage on Electronic Materials*, Vol. 1, (Wiley, New York, 1980).

18. S. Holland, "Fabrication of Detectors and Transistors on High-Resistivity Silicon," presented at the Workshop on Pixel Detectors, Leuven, Belgium, May 31-June 2,1988; LBL preprint LBL-25520, June (1988).

19. Kemmer. J., "Improvement of Detector Fabrication by the Planar Process," Nucl. Inst. and Meth. **226**, pp. 89-93 (1984).

20. Kleinfelder, S., *et al.*, "A Flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout," IEEE Trans. Nuclear Science **35**, pp. 171-175 (1988).

21. Walker, J. T., *et al.*, "Development of High-Density Readout for Silicon Strip Detectors", Nucl. Inst. and Meth. **226**, pp. 200-203 (1984).

8.3 SILICON PIN ARRAY PAPER

This paper was given at the SSC industrial symposium in New Orleans in February, 1989.

SLAC–PUB–4942
May 1989
(I)

SILICON PIN DIODE HYBRID ARRAYS FOR CHARGED PARTICLE DETECTION: BUILDING BLOCKS FOR VERTEX DETECTORS AT THE SSC*

GORDON KRAMER** AND STEPHEN GAALEMA
Hughes Aircraft Company, Carlsbad, CA 92009

STEPHEN L. SHAPIRO AND WILLIAM M. DUNWOODIE
Stanford Linear Accelerator Center, Stanford University, Stanford, CA 94309

JOHN F. ARENS AND J. GARRETT JERNIGAN
Space Sciences Laboratory, University of California, Berkeley, CA 94720

ABSTRACT

Two-dimensional arrays of solid state detectors have long been used in visible and infrared systems. Hybrid arrays with separately optimized detector and readout substrates have been extensively developed for infrared sensors. The characteristics and use of these infrared readout chips with silicon PIN diode arrays produced by MICRON SEMICONDUCTOR for detecting high-energy particles are reported. Some of these arrays have been produced in formats as large as 512 × 512 pixels; others have been radiation hardened to total dose levels beyond 1 Mrad. Data generation rates of 380 megasamples/second have been achieved. Analog and digital signal transmission and processing techniques have also been developed to accept and reduce these high data rat s.

INTRODUCTION

High-resolution vertex and tracking devices at the SSC will be important for the reconstruction of complex events, including secondary vertices close to the primary interaction point. The main properties required of these devices are: fast response time, fine spatial resolution, multiple particle resolution, and radiation hardness.

A resolution of better than 10 μm and the ability to distinguish the many particles of a jet can be achieved with two-dimensional pixel devices. Due to the three-dimensional nature of the coordinate information provided, these provide efficient track finding with a minimum number of layers in the high-multiplicity environment of the SSC.

The SSC beam crossing period will be 15 ns, and interesting events will occur every 100 to 10,000 crossings. Hit times must be recorded to an accuracy of one crossing period, and the readout time of the detectors must be less than the mean interval between interesting events to avoid large dead time losses.

*Work supported by the Department of Energy, contract DE–AC03–76SF00515.
**Permanent address: Electro-Optical & Data Systems Group, Hughes Aircraft Company, El Segundo, CA 90245.

Presented at the 1989 International Industrial Symposium on the Super Collider, New Orleans, LA, February 8–10, 1989.

The expected combination of high luminosity and large particle multiplicity will produce a high-radiation environment in the vicinity of the collision point. For a proton-proton total cross section of approximately 100 mbarn, the SSC will yield approximately 10^8 interactions per second when operating at its design luminosity of $10^{33}/\text{cm}^2/\text{sec}$. At a distance of 5 cm from the beam, the absorbed radiation dose will be approximately 1 Mrad per year.

New electronic detector systems usually require at least several years for development. Examples are CCDs, infrared detector arrays and x-ray bolometers. The schedule for the SSC construction is commensurate with the schedule for new vertex detector development if the latest existing technology is used as a base.

DEVICE CANDIDATES

Candidates for vertex/tracking devices at the SSC include: wire chambers, scintillating fiber detectors, silicon microstrip detectors, double-sided microstrip detectors, silicon drift chambers; and pixel devices in the form of CCD arrays, monolithic silicon arrays and hybrid microdiode arrays. It is generally recognized that in terms of space, momentum and two-track resolution, wire chambers at present are inferior to silicon devices. It is also generally recognized that pixel devices are preferable to strip devices or drift devices, as far as two-track resolution is concerned.

Pixel devices—in particular, silicon diode arrays—are a natural choice for vertex detectors. These devices provide three-dimensional coordinate information with a spatial resolution of a few microns. However, as we move farther from the collision point to the tracking detector, many of the other devices mentioned above become attractive candidates for a variety of reasons.

A vertex detector based on the use of a pixel device would provide efficient track-finding with a minimum number of layers in the high-multiplicity environment of the SSC due to the three-dimensional nature of the coordinate information provided. The absence of ambiguities in coordinate matching which are always present in nonpixel devices allows the number of detector layers to be minimized, thereby reducing the size and cost of the vertex detector.

The only pixel devices presently in use in high energy physics experiments today are CCDs.[1] These devices are inappropriate to the SSC environment for a variety of reasons, including: (i) a small signal size of about 1000 electrons, which necessitates their being cooled, renders them extremely susceptible to degradation caused by radiation damage, and requires costly and delicate readout electronics; (ii) a varying transfer efficiency across their faces; (iii) no off gate during readout, resulting in a time/space ambiguity; and (iv) a serial readout resulting in a readout time of about 10 msec for a device with 10^5 pixels.

A number of researchers are presently working on the problem of fully integrated pixel detectors in monolithic arrays.[2,3] The goal is to fabricate the readout electronics on the same high-resistivity silicon as the detector diodes. Success in these efforts will result in detectors having the minimum thickness possible. However, there will be a loss of flexibility. A change in either the detector specification or the readout specification will result in not only a circuit change, but also a re-analysis of the production process, since they are now intimately coupled. There will be difficulty in production, since both the detector and the readout electronics must be fabricated in high-resistivity facilities which can handle this new process. There are far fewer of these facilities worldwide than there are those which can produce more conventional circuits.

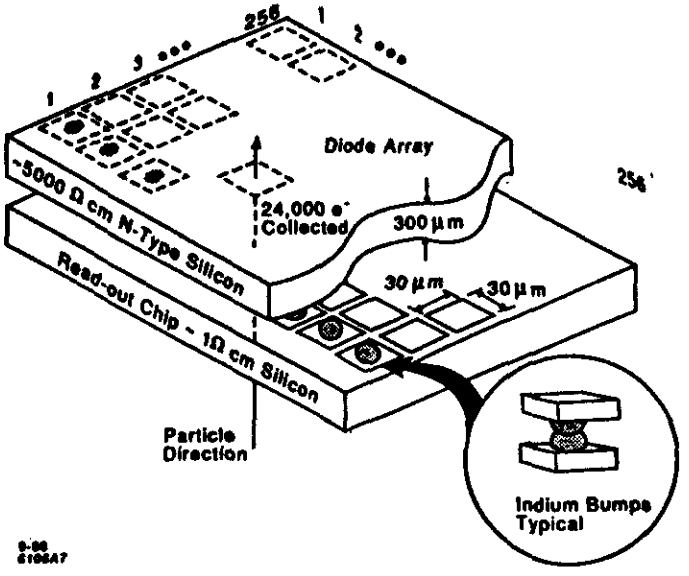


Fig. 1 : Schematic representation of a Silicon PIN Diode hybrid detector.

The architecture which we find to be well suited for charged particle detection at the SSC is that of a hybrid.[4] The charged particle detector and the readout electronics are constructed as two separate silicon chips, each optimized for its specific function. The two chips, indium bump bonded together, then provide the basic building block for the construction of a detector array.

SILICON HYBRID ARRAY EXPERIENCE

The choice of the hybrid design (*viz., one in which each diode of the detector* array is bonded to an independent amplifier readout circuit on a mating VLSI chip via an array of aligned indium metal bumps that cold weld under pressure to form ohmic contact), allows for additional flexibility in the selection of detector and readout electronics.[5] For instance, a change in the leakage current specification of the detector array will not affect the readout electronics, nor will a change in the VLSI chip oxide thickness to accommodate a radiation hardness specification affect the detector array. Figure 1 is a schematic representation of a silicon PIN diode array hybrid. Figure 2 is a microphotograph of an array of indium bumps prior to the bonding process. The bumps shown are approximately 15 μm in diameter. A small (10 × 64 pixel) hybrid mounted in a 68-pin leadless carrier is shown in Fig. 3. The readout chip in this device, the Hughes CRC–198, was originally designed to mate with a long-wave infrared detector chip which for optical reasons required 120 μm square pixels. The success of this chip lead to a series of larger arrays with smaller pixels (for 3–4 μm infrared platinum silicide Schottky barrier detectors) as shown in Table I. A photograph of the 256 × 256 pixel CRC–365 hybrid, which has become fairly mature, is shown in Fig. 4. Figure 5 is a histogram of the infrared sensitivity of each pixel of a 256 × 256 hybrid array. Of note is the nearly identical electronic response of the 65,536 pixels of the array and the notation that only three pixels in the array are dead. Currently being developed are 512 × 512 (see Fig. 6) and larger arrays. The circuit used in the array unit cell of all of the chips listed in

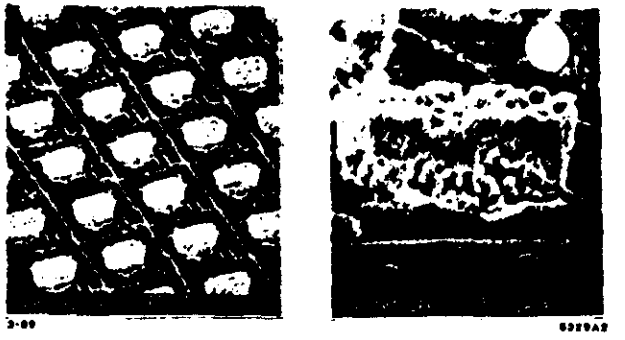


Fig. 2 : A microphotograph of an array of indium bumps prior to the bonding process.

Table I is called a source follower per detector (pixel) or SFD with direct readout (DRO) multiplexing as opposed to CCD multiplexing.

Figure 7 is a schematic diagram of the MOSFET circuit of the 10×64 readout array. The diagram has been divided into its several functional portions. The section replicated for each pixel contains four MOSFETs. Signal charge is generated by the detector diode, and is fed to the gate of the signal MOSFET, where it stays until a readout is made. The pixel selection circuit indicates how a sequence of address lines can select an individual pixel by turning on the gates of the V_{DD} bias MOSFET and the enable gate of the reset MOSFET. The U_{reset} signal allows the gate of the signal MOSFET to be reset to the V_{reset} level for any pixel that is enabled by the reset MOSFET. All of the signal MOSFETs in a column of the array are connected to a readout MOSFET in a source follower configuration which provides power for driving an external circuit.

PIN DIODE HYBRID ARRAYS

The existing infrared readout chips can be mated to PIN diode arrays to produce hybrids with a number of advantages as high-energy particle detectors.

The present readout chips allow random access to any pixel, which then operates as an independent detector. By virtue of its geometry alone, each pixel detector (PIN diode)

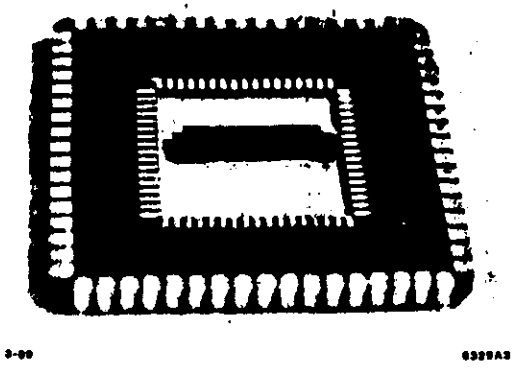


Fig. 3 : A photograph of a 10 × 64 readout chip bump bonded to a Silicon PIN diode array.

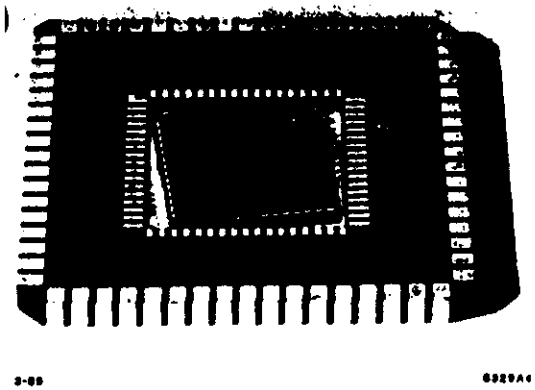


Fig. 4 : A photograph of a 256 × 256 silicon hybrid.

provides about 3,000 times less sensitivity to diode leakage current than a microstrip detector, which will increase the radiation hardness to neutrons. To complement this increase in the radiation hardness of the detector diode, one of the present readout chips (the 10×64 array) has been fabricated in a technology which is radiation hard at cryogenic temperatures to 1 Mrad of Cobalt 60 gamma rays.

The hybrid operates at room temperature, eliminating the need for a cryostat and easing the problems of installation, alignment and accessibility for power and control cabling.

The detector thickness itself can now be optimized. The PIN diode array can be fabricated to give the requisite signal (80 $e/\mu m$ of silicon), while the VLSI chip can be thinned to less than 100 μm if necessary. This feature is important for minimizing multiple-scattering effects and also for limiting the number of adjacent pixels turned on by tracks incident at large angles to the surface.

It should be noted that the diode anodes are indium bump bonded to the silicon readout chip, leaving the cathode available to be etched into a pattern of pads or strips. Signals picked up on the cathode pads would be available for fast triggering or for reducing

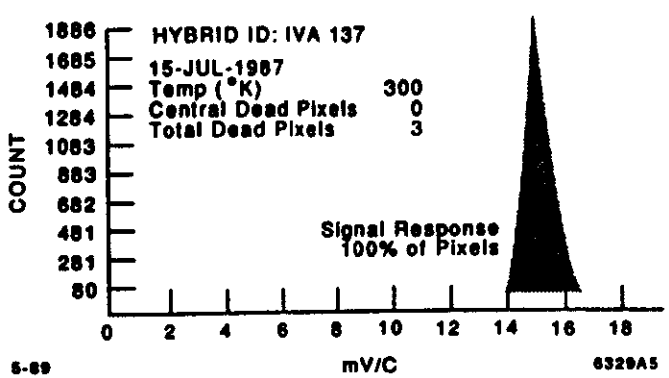


Fig. 5 : A histogram of the infrared sensitivity of each pixel of a 256 × 256 hybrid array.

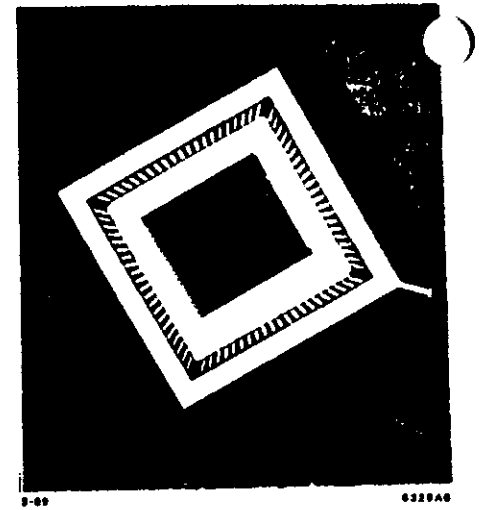


Fig. 6 : A photograph of a 512 × 512 silicon infrared hybrid.

the readout time by using the random access nature of the readout electronics. System considerations will determine if the cathode signals are useful.

To address the problem of data which may accumulate during the readout cycle, gating circuitry can be designed to inhibit the flow of charge between the detector and the readout chip after an event is tagged. Alternatively, an input buffer can be added which leaves the detector alive but which does not alter the data being read out. These features do not exist on the present readout chips.

To address the problem of data being recorded from various beam crossings, a design must be adopted which allows the data and the time of arrival to be correlated. Present chips do not have this feature. They do appear to have the ability to provide a "fast indication that a particle has been recorded by the detector. However, we have not yet explicitly studied this feature in the laboratory. This ability, important if confirmed, can

Table I.

Design	Array Size	Pixel Size (μm)	Year
CRC-171	10 × 32	120 × 120	1980
CRC-198	10 × 64	120 × 120	1981
CRC-228	58 × 62	75 × 75	1983
CRC-234	128 × 128	50 × 50	1984
CRC-304	256 × 256	30 × 30	1985
CRC-350	256 × 256	30 × 30	1986
CRC-352	244 × 400	24 × 24	1986
CRC-365	256 × 256	30 × 30	1986
CRC-389A	244 × 400	24 × 24	1987
CRC-389B	512 × 512	20 × 20	1987
CRC-412	488 × 640	20 × 20	1988

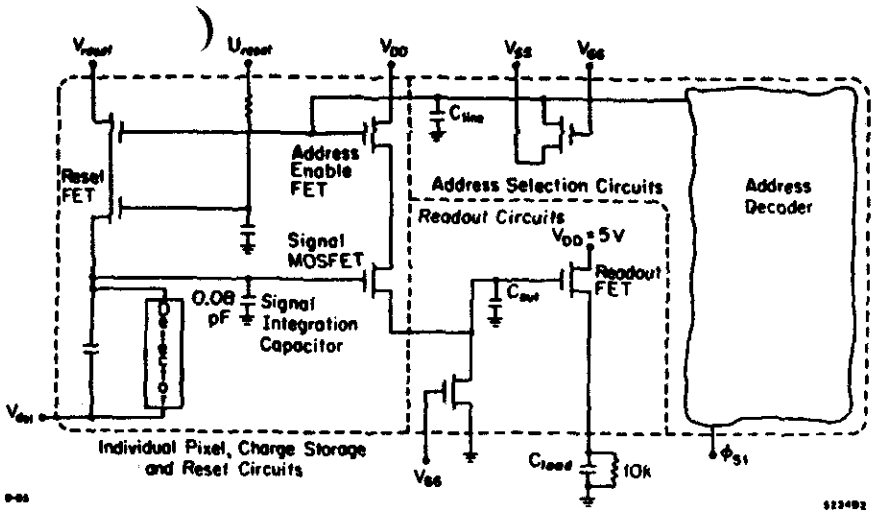


Fig. 7 : Schematic drawing of the readout electronics of the 10 × 64 readout array.

be used in designs to strobe shift registers which record time information while retaining the small pixel size of our present chips.

In the present generation of readout chips, it should be noted that the power used during the write cycle is essentially zero. Power is used only when reading, and cooling needs thus are lessened.

DESCRIPTION OF PRESENT HARDWARE

There are two readout chip geometries currently being built into detector arrays. Figure 8 is a photograph of the two mating PIN diode arrays on a production wafer.[6] Shown are a number of 10×64 arrays with 120 μm square pixels and a number of 256×256 arrays with 30 μm square pixels. The diode arrays are identically processed and differ only in that they must mate with their respective readout chips. The readout chips are

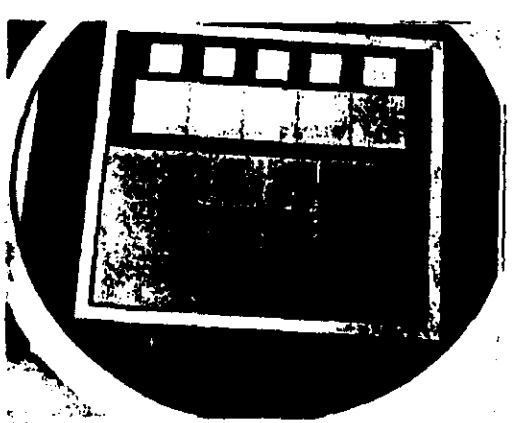


Fig. 8 : A photograph of 256 × 256 and 10 × 64 PIN detectors on a wafer. The five square structures at the top of the wafer are test diodes. The wafers have been manufactured by MICRON SEMICONDUCTOR, LTD., Sussex, England.

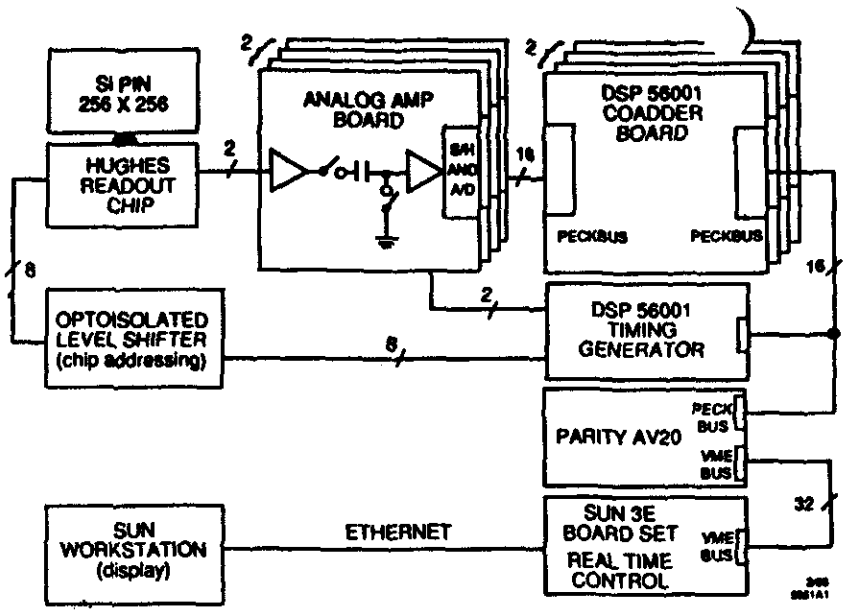


Fig. 9 : A block diagram of the high energy physics data acquisition electronics.

similar, but have some differences. For instance, the 10 × 64 array has been optimized to be radiation hard to 1 Mrad at 10° K. It has a random access architecture in that a unique setting of its address lines will select one and only one row of pixels. The 256 × 256 array, on the other hand, is random access in that the pixels are addressed via row and column shift registers. This feature makes addressing a given pixel more complicated but allows easy implementation of a sparse scan algorithm. This particular readout chip has been optimized to collect electrons but is bipolar at the signal levels we expect.

Figure 9 is a block diagram of the high energy physics data acquisition system. A Sun Microsystems Sun-3/110LC-4 workstation controls a system housing a Sun 3/E CPU, a Motorola 68020 bus converter board, amplifiers, ADCs, digital signal processors and a clock generator. The digital signal processor is the Motorola DSP56001. This device acquires data at a rate of 10 MIPS, processes it and passes it via the MC68020 to the Sun 3/E. The bus converter board, a Parity systems AV20 dual-port processor, interfaces the local analog bus (PECKBUS) to the VME bus.

The noise performance of the 10 × 64 readout chip at 10° K has been measured to be 45 electrons rms referred back to the input. This is within a factor of two of the expected Johnson noise of the gate of the input signal MOSFET. At room temperature, the expected noise signal should be about 200 electrons rms, taking into account the square root of the temperature ratio in the Johnson noise component. However, the measurement has not yet been made. If the noise performance is as expected, detectors thinner than the traditional 300-μm-thick devices currently being fabricated would offer more than adequate signal-to-noise performance.

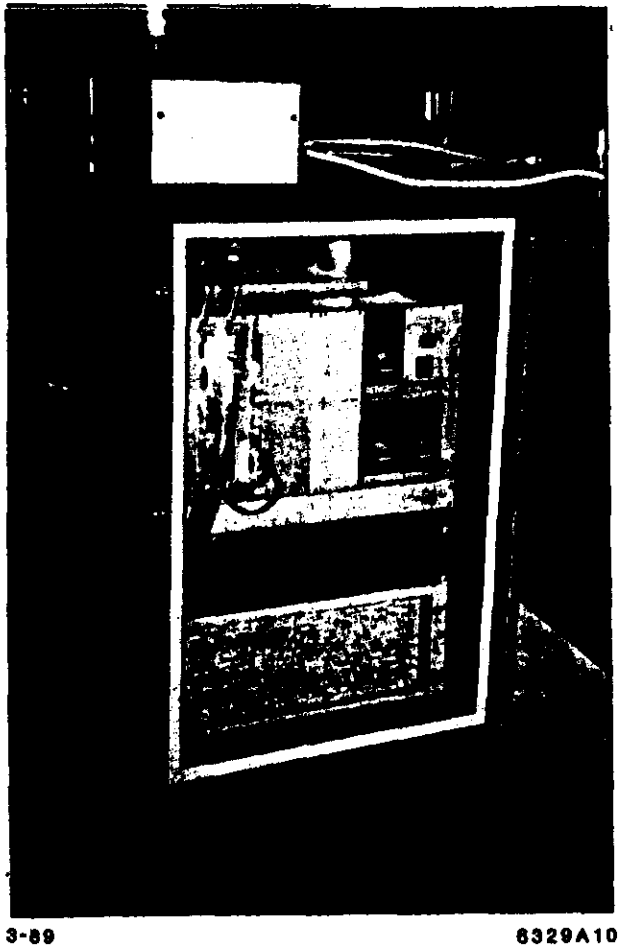
RESEARCH PROGRESS

Using Detector Development funds from the Department of Energy, a contract was made with Micron Semiconductor to design and fabricate two silicon PIN diode arrays.

The array specifications were chosen to allow the detector chips to mate with two Hughes Aircraft Co. readout chips. The arrays fabricated are a 10×64 array with 120 μm square pixels and a 256×256 array with 30 μm square pixels. The first silicon 10×64 hybrid arrays were completed in December 1988, and the silicon 256×256 hybrid arrays are being built. The data discussed in this paper were taken with the 10×64 array.

Additional Detector Development funds were used to begin the fabrication of the dedicated high energy physics data acquisition system described above. The amplifier/ADC/DSP56001 boards and the clock generator in the present system, however, are circuits remaining from the infrared data acquisition system.[7] These need to be redesigned to high energy physics criteria. Figure 10 is a photograph of the data acquisition electronics for the 256×256 array.

A data acquisition and display software package based on the infrared system has been written. The operating system is UNIX, the DSP has been programmed in assembly language, and various control functions are written in Magic/L, an interactive language



3-89 6329A10

Fig. 10 : A photograph of our present data acquisition system for the 256×256 array.

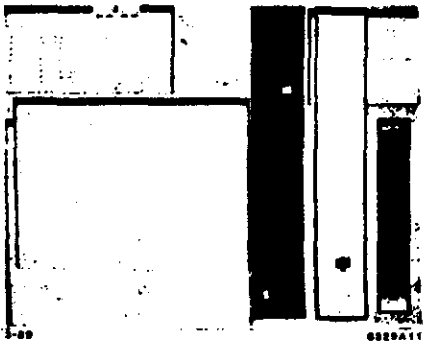


Fig. 11 : A photograph of the SUN display screen. Included is a display of the timing and control pattern, the pulse height scale, and two event windows each showing a 10×64 representation of the hybrid.

derived from Forth. The Parity AV20 dual port processor has been programmed in C, and the DSP will be reprogrammed in C. Figure 11 is a photograph of a SUN display during data acquisition. The large window on the left displays the timing pattern used to read out the hybrid. The small window on the right shows the pulse height scale, which is a color scale from blue at the top to white at the bottom. The two rectangular windows just right of the center represent the pixel array and contain two events; the one on the right has detected an alpha particle, while the event on the left has two alphas and a 59.5 KeV x-ray.

Figure 12 is a photo of the hybrid placed under an Americium 241 alpha source. Americium 241 is also a source of 59.5 KeV and 26.3 KeV x-rays. The mounting fixture is a low temperature Dewar for tests to be performed later, which will characterize the hybrid's performance as a function of temperature.

Figure 13 is a scope trace of an output channel. The faint traces are the signals from the detected alpha particles. Correlated double-sampling electronics described

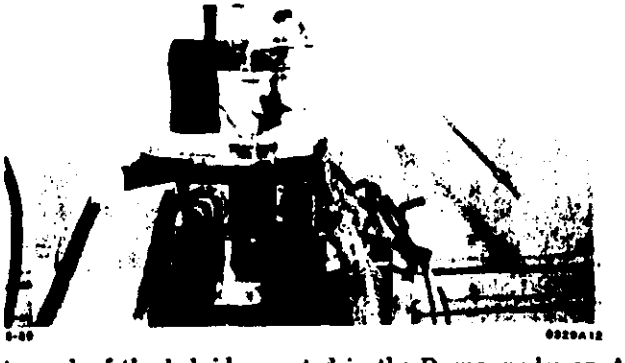


Fig. 12 : A photograph of the hybrid mounted in the Dewar, under an Americium source.

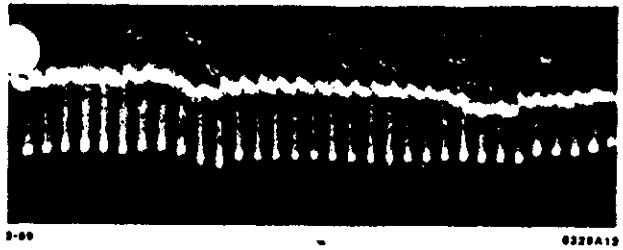


Fig. 13 : A photograph of a scope trace of an output channel (one row) of the 10 × 64 detector.

elsewhere[8] is needed to reduce the 1/f noise and provide the excellent signal-to-noise ratio performance observed.

At the present time, a system exists which can read with either of two detector geometries: 10 × 64 or 256 × 256. The program of testing and characterizing these devices has just begun. The first hybrid arrays have just been manufactured. Preliminary data demonstrate the detection of alpha particles and 60 KeV x-rays with a high signal-to-noise ratio. However, the readout system has not been optimized. The timing pattern and bias voltages have not been swept through their respective ranges, and environmental noise has not yet been removed. The preliminary data are encouraging. The detection of a 60 KeV x-ray means that we have detected a signal having approximately 16,700 electrons. This is less than the 24,000 electrons generated by a minimum ionizing particle traversing 300 μm of silicon.

Table II is a summary of current device characteristics.

LOW-MASS, HIGH-DATA-RATE PACKAGING

Packaging techniques have also been developed for the infrared application of these chips that should be very useful for the SSC. A beryllium module pedestal is shown in Fig. 14 that holds several 10 × 64 hybrids used on the Airborn Optical Adjunct (AOA) Program.[9] The beryllium structure that holds up to 48 of these modules in a focal plane (Fig. 15) is over 16 inches long. This focal plane generates over 380 million analog data

Table II: Summary of Device Parameters.

Array dimension	10 × 64	256 × 256
Pixel size	120 μm	30 μm
Detector material	Germanium Silicon	Silicon
Number of readout channels	10	2
Power during "write" cycle	0 mW	0 mW
Power during read cycle	10 mW	2 mW
Present clock speed	1 MHz	2 MHz
Theoretical clock speed	10 MHz	10 MHz
Readout mode	Random Access	Random Access
Processing power	20 MIPS/channel	20 MIPS/channel
Radiation hardness	1 Mrad	?
Noise at room temperature	< 300 e^- rms	< 300 e^- rms

Fig. 14 : A photograph of a beryllium module pedestal holding several 10 × 64 hybrid arrays.

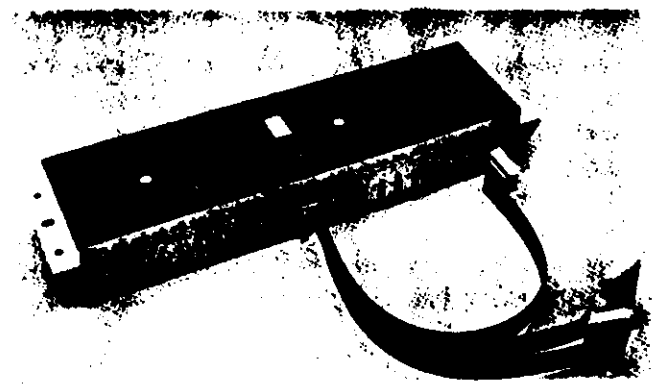


Fig. 15 : A photograph of the AOA focal plane.

samples per second. The data is then converted from analog to digital information and processed at a rate of 15 billion operations per second by the data processor shown in Fig. 16.

CONCLUSION

Silicon PIN diode pixel detectors appear to be the prime candidate for an SSC vertex detector. Pixel detectors should have the best performance in terms of resolution, signal-to-noise ratio, radiation hardness and unambiguous high-speed response. An architecture to achieve correlation between the pixel containing the data and the time of the beam crossing using a combination of on-chip and off-chip signal processing appears feasible to implement advanced radiation-hardened silicon CMOS technology. More study is required to ensure that the power that must be dissipated to achieve full operating speed is compatible with the maintenance of PIN diode operating temperatures. The produciblity of large hybrid diode array/readout chips of up to 512 × 512 pixels has been demonstrated.

Very preliminary data from our present 10 × 64 silicon hybrid arrays demonstrate the detection of alpha particles and 60 KeV x-rays.

3-89 6329A16

Fig. 16 : Sensor signal processor for the AOA program.

REFERENCES

1. C. Damerell; *Experiment* NA32 at the CERN SPS; Vertex Detectors; Rutherford Appleton Laboratory Report RAL 86-077 (July 1986).
2. S. Parker, "A Proposed VLSI Pixel Device for Particle Detection," submitted to the International Workshop on Silicon Pixel Detectors for Particles and X-rays, Leuvan, Belgium (June 1988).
3. G. Vanstraelen, I. Debusschere, C. Claeys, and G. Declerck, "Fully Integrated CMOS Pixel Detector for High Energy Particles," submitted to the International Workshop on Silicon Pixel Detectors for Particles and X-Rays, Leuvan, Belgium (June 1988).
4. S. Shapiro and T. Walker, "The Microdiode Array—A New Hybrid Detector," SLD-New Detector Note No. 122 (October 15, 1984).
5. S. Gaalema, "Low Noise Random-Access Readout Technique for Large PIN Detector Arrays," *IEEE Trans. on Nucl. Sci.* NS-32 1:417 (February 1985).
6. Fabricated by MICRON Semiconductor Ltd., Sussex, England.
7. J. F. Arens, J. G. Jernigan, M. Peck, C. A. Dobson, E. Kilk, J. Lacy, and S. Gaalema, "10 Micrometer Infrared Camera" *Applied Optics*, 26:18 (1987).
8. S. Shapiro, W. Dunwoodie, J. Arens, J. Gernigan, and S. Gaalema, "Silicon PIN Diode Array Hybrids for Charged Particle Detection," SLAC-PUB-4701 (December 1988), submitted to *Nucl. Inst. and Meth.*
9. The Airborn Optical Adjunct Program, *Aviation Week and Space Tech.* (November 1988).

DESIGNS FOR A HIGH ENERGY PHYSICS DETECTOR ARRAY

Introduction

A vertex detector for a high energy physics experiment supplies the information needed to determine the trajectories of particles coming from the collision or interaction region. Several layers of thin detectors are often sufficient to reconstruct the tracks. The accuracy of locating the tracks is determined by the sizes of the detector elements and by the accuracy of the interpolation procedure, if one is used. The design and the speed of the readout electronics must be high enough to accommodate the event rate. The readout system in general consists of electronics associated with each detector element, electronics associated with groups of detector elements, and a state machine or a digital signal processor (DSP).

Solid state detectors have fast response times, can be divided into narrow strips or into small pixels, and can be compactly mated to readout electronics. Table 1 describes detectors suitable in various settings.

Table 1 - Hit multiplicity and resolution of detectors

Detector elements and quick-look information	Interpolation	Maximum number of hits per beam crossing	Resolution
Wide strips	No	Few	Low
Wide strips	Yes	Few	High
Narrow strips	No	Few	High
Pixels; Xs independent of Ys	No	Few	Low
Pixels; Xs independent of Ys	Yes	Few	High
Pixels; X, Y pairs	No	Many	Low
Pixels; X, Y pairs	Yes	Many	High

Design Approach

A detector array having pixels is needed for some high energy physics experiments, and the remainder of this paper is devoted to describing some possible designs. The detector array is used to determine a point on the trajectory of an ionizing particle as shown, for example, by the two clusters of hit pixels with their neighbors in Figure 1. The cluster on the right would be produced by an ionizing particle perpendicularly incident on the face of the detector array and passing roughly through the center of a pixel. The cluster on the left would be produced by ionizing particles passing obliquely through the array. If the pixels are tall and narrow, the particle will pass through several pixels as shown.

The readout electronics consists of some circuits in the pixels, other circuits connected to the columns and to the rows of the array, and circuits in a controller. One approach among several approaches to designing a vertex detector for the SSC is to incorporate complicated analog and digital electronics on the readout chip and to thereby only need a simple controller for the readout process. A readout chip that will supply the addresses and stored charges of hit pixels and their neighbors would

8.4 A SET OF POSSIBLE READOUT DESIGNS

A set of detector array designs was begun during the generic R & D progam in the last year, and the designs to date are described in a long writeup. A few pages of this writeup follow. This work is in progress, and the writeup has not been published.

only require a simple state machine or a simple DSP for readout control. Also, if fast analog electronics in the readout chip can be substituted for digital processing electronics, speed gains are possible.

High readout speed is important to keep the number of hits on the array low during the readout. If the number of hits during the readout is large, provision in the design must be made to exclude these later, unwanted hits. A fast readout, in general, allows for a simpler readout chip than a slow readout does.

Compression of data is useful if the interesting event rate is high because the link between the pixellated detectors and the the region outside all the detector systems is constrained by a small space for cable routes. A DSP can be used to convert the coordinates and stored charge on the pixels in a cluster of pixels to a set of parameters describing the cluster. If the set of parameters is smaller than the set of coordinates and charges, the data transmission rate can be reduced.

A design that uses a complex readout chip and a simple controller instead of a simple readout chip and a complex controller is presented in this paper. The readout is fast. The readout chip performs six functions:

A) When the array is hit by an ionizing particle

1) Store the charge from an ionizing particle.

2) Store the clock time of the ionizing particle hit

B) When a level 1 trigger, signaling that a possibly ineresting event occurred, accompanied by a time window is received

1) Reset all pixels except the hit pixels and their neighbors of the possibly interesting event

C) When a level 1 trigger is not followed by a level 2 trigger and a level 1 cancellation is received

1) Reset all pixels and their neighbors of the level 1 triggered event

D) When a level 2 trigger, signaling that an interesting event occurred, accompanied by a time window is received

1) Transmit the addresses of hit pixels

2) Transmit the addresses of the neighbors of hit pixels

3) Transmit a signal from each hit pixel and its neighbors representative of the stored charge

The DSP takes the data from the array and calculates three quantities

1) Centroid of the cluster

2) Total stored charge

3) Shape of the cluster

The DSPs can be located in proximity to the readout chips or can be located outside the vertex detector volume which closely surrounds the interaction region. The latter option requires a higher data transmission rate between the vertex detector and the distant electronics.

Family of Arrays

A family of arrays with pixels will be described, beginning with simple arrays and ending with an array having the functions listed above. Because each successive array is a modification of its predecessor, understanding the components of the readout circuitry can be facilitated by studying each array in turn.

Each array is numbered, with the PS I array being the simplest. The PS I array produces one X and one Y output from one pixel immediately after being hit. Each pixel has two output lines, one to the X address memory and one to the Y address memory. The PS II array is the same as the PS I array except for having an analog to digital converter (ADC). It produces one immediate set of X, Y, and ADC outputs.

For many high energy physics experiments the array must record the time and the location of several hits, and the readout circuitry needs to be more complicated. A typical time sequence of events is shown in Figure 2. If the array can be read out before it is hit again, one time register is needed for the array. However, if the readout is too slow to read each event, only a subset of the events can be read out. The selection of each member of this subset of events might occur long after the event, and then time registers on the array would be needed to distinguish selected events from uninteresting events. Each PS array has a finite capability, and Table 2 lists the features of these arrays.

Table 2 - Readout array features

Design	Maximum number of pixels hit	Read X,Y out before next hit, BH, or after trigger, AT	Read ADC out before next hit, BH, or after trigger, AT	Read hit pixels, H, or hit pixels and neighbors, H&N
PS I	1	BH	No ADC	H
PS II	1	BH	BH	H
PS III	≥1	BH	No ADC	H
PS IV	≥1	BH	AT	H
PS IVN	≥1	BH	AT	H&N
PS V	≥1	AT	No ADC	H
PS VI	≥1	AT	AT	H&N

Sequence of Steps in Priority Selection

For a rapid readout of multiple hits, a priority selection design is used in the PS family of arrays. *PS* stands for priority selection, which means that a set of selectable items is addressed in sequence. The selectable items are the columns or the rows that contain the hit pixels. The priority selection logic quickly generates the addresses of these columns or rows. The hit columns or rows in the PS designs open some switches that are normally closed. The switches are lined up serially, and the priority selector voltage passes through the closed switches and reads the addresses of the open switches one at a time in sequence. Priority selection by using analog electronics provides faster access than by using a digital search processor.

For example, the sequence of steps followed in finding the addresses of two hit columns of an array follows. The components of the priority selection logic on each column are a switch, a flip flop, and two AND gates as shown in the PS III array. The sequence of steps followed for finding the addresses of hit columns is listed:

1) Reset the flip flops so the outputs are positive with the RFFCOL line.

2) Wait for the columns to be hit. The AND gates on the outputs of the flip flops on the hit columns will turn on, and the normally closed (nc) switches will open.

3) Begin the process to read the addresses of the hit columns by applying a voltage PSCOL to the end of the line of switches.

4) The second AND gate on the nearest hit column will turn on and the address of this column will appear on the column address lines. Read the address. The flip flop on this column will be enabled for turn off.

5) Turn off the flip flop on the nearest hit column with TOFFCOL, and the switch will close.

6) As in step (4) the second AND gate on the next hit column will turn on, and the address of this column will appear on the address lines. The flip flop will be enabled for turn off.

7) As in step (5) turn off the flip flop with TOFFCOL, and the switch will close.

8) The PSCOL voltage will appear on the end of the line of switches, making the signal ENDCOLS, signifying that all hit columns have been read.

The priority selection scheme for reading the addresses of the hit rows is the same as that for hit columns.

Arrays Using Priority Selection

The PS III-T array produces sets of X, Y outputs caused by multiple hits, and the PS IV-T array produces sets of X, Y, ADC outputs. The suffix *T* denotes that there is a transimpedance amplifier in each pixel. The transimpedance amplifier boosts the signal to reduce the effects of noise in the downstream electronics.

The X, Y coordinate pairs of hit pixels in the PS III and PS IV arrays are read out and stored immediately after being hit by adhering to the following procedure. The discriminators on the hit columns will turn on and the switches will open. For the PS IV array ALLROWS is turned on. Then priority selection is used to read the addresses of the hit columns. When reading the address of a hit column to obtain the X address of a hit pixel, the Y outputs of the pixels in the column will be enabled because the AND gates in the pixels will be on. The hit pixels in the column will turn on the discriminators on their rows. The switches on these rows will open. Priority selection is now used to find the Y addresses associated with the X address already found. The ADC values can be obtained later, such as after a trigger, by addressing the pixels with the stored addresses. The PS IV-T array would be useful if the X, Y pairs could be read out before the array is hit again. The ADC could be slow, with the array being hit a few times during the digitization. Note that the PS IV-T array has registers that can both read and write. Figure 3 is a timing diagram of the signals into and out of the array when two columns are read out. A program for a state machine or for a DSP to read the PS IV-T array is listed in Appendix A.

Reading Neighbors of Hit Pixels

Information about the neighbors of pixels hit hard enough to trigger the discriminators is also recorded in some array designs. The stored charges on these pixels must be measured in order to obtain accurate interpolations or centroids of the charge distributions. The suffix *N* denotes that information about the neighbors of hit pixels is recorded. For example, the PS IV-TN array finds X, Y, and ADC for all pixels hit and their rectilinear and diagonal neighbors as shown in Figure 4. The scheme used for finding the neighbors of hit pixels uses

1) Fanouts to 3 columns or 3 rows from each discriminator

2) Fanouts to 3 columns from each column enable line

The discriminator on a column opens the switches on its and the neighboring columns. Likewise a discriminator on a row opens the switches on its and the neighboring rows. Later, when a column is enabled to set the discriminators on the rows, the neighboring columns are enabled simultaneously when the FNDNBR signal is on. FNDNBR and ALLROWS should be turned on and off together in normal operation.

This procedure will cause discriminators to be fired on all hit and neighboring columns. When each one of these columns is enabled, the discriminators on all rows with hit and neighboring pixels fire. The neighbors include both the rectilinear and the diagonal neighbors.

Note that if a control line on the cross links between rows corresponding to the FNDNBR line were installed, it would be possible to only find the rectilinear neighbors. The ALLROWS circuit would not be needed. If neither FNDNBRX nor FNDNBRY were turned on no neighbors would be found, where FNDNBRX controls the cross links between the columns and FNDNBRY controls the cross links between the rows. If only FNDNBRX were turned on, only the neighbors in a row would be found. If only FNDNBRY were turned on, only neighbors in a column would be found. If one of these control lines were turned on and off before the other were turned on and off, the rectilinear neighbors would be found. If both control lines were turned on at the same time, the rectilinear and diagonal neighbors would be found.

Time Window Accompanying the Trigger

The trigger will occur after the interesting event occurs. The detector array will probably have been hit during several uninteresting, or background, events in addition to the interesting event while waiting for the trigger. In order to distinguish the events, the time of each hit is recorded in registers on the array. Later, the trigger will be accompanied by a time word, TTRIG, giving the time of the interesting event. However, the time resolution will be poor because the trigger will come from the calorimeters, which surround the vertex detector with large scintillators and proportional counters. Scintillators and proportional counters are slow and also have poor time resolution. The interesting event could have occurred at any one of several beam crossing, or clock, times around TTRIG. All hits within a time window around TTRIG should be accepted as being the interesting event.

The PS VI design for recording time uses time registers on the columns instead of on the pixels. This arrangement allows the pixels to be small, and it works if the event rate is low enough that a column has a low probability of being hit by both a particle in the interesting event and also a particle in an uninteresting event. The time registers serve two purposes, which are 1) recording the event time, T, and 2) comparing the recorded time, T, with the time, TTRIG, supplied with the trigger. If T equals TTRIG, the register produces an output. This output is fed into a flip flop which in turn feeds the priority selection circuit. The flip flop allows several TTRIG times in a time window to be compared with T in the time register.

The PS VII design allows a column to be hit several times because each column and each row has several time markers. There is one set of time registers for the whole array.

Event pileup

If the detector array is hit more than once during the waiting and readout periods, the system must be able to select the correct event. As the number of hits during the waiting and readout periods increases, the system becomes more complicated. Hence a fast readout scheme is important for keeping the readout chip simple. Figures 5 to 7 show the timing and charge storage features that are necessary to accommodate various event rates. Figure 5 shows the features needed as a function of mean time between hits relative to the trigger delay. Figure 6 shows the features as a function of mean time between hits relative to the readout time. Figure 7 is a superposition of Figures 3 and 4 and shows the features as a function of mean time between hits relative to a typical SSC trigger time and the PS array readout time. The features noted in these figures are described below in a list that begins with a low event rate and ends in a high event rate:

1) If a array has a reasonable probability of being hit at most once before the trigger and not during the readout, one time register for the whole array is sufficient.

2) If a column has a reasonable probability of being hit at most once before the trigger and not during the readout, one time register on each column is sufficient.

3) If a column has a reasonable probability of being hit at most once before the trigger and at most a few times after the trigger, one time register on each column and one on each row would

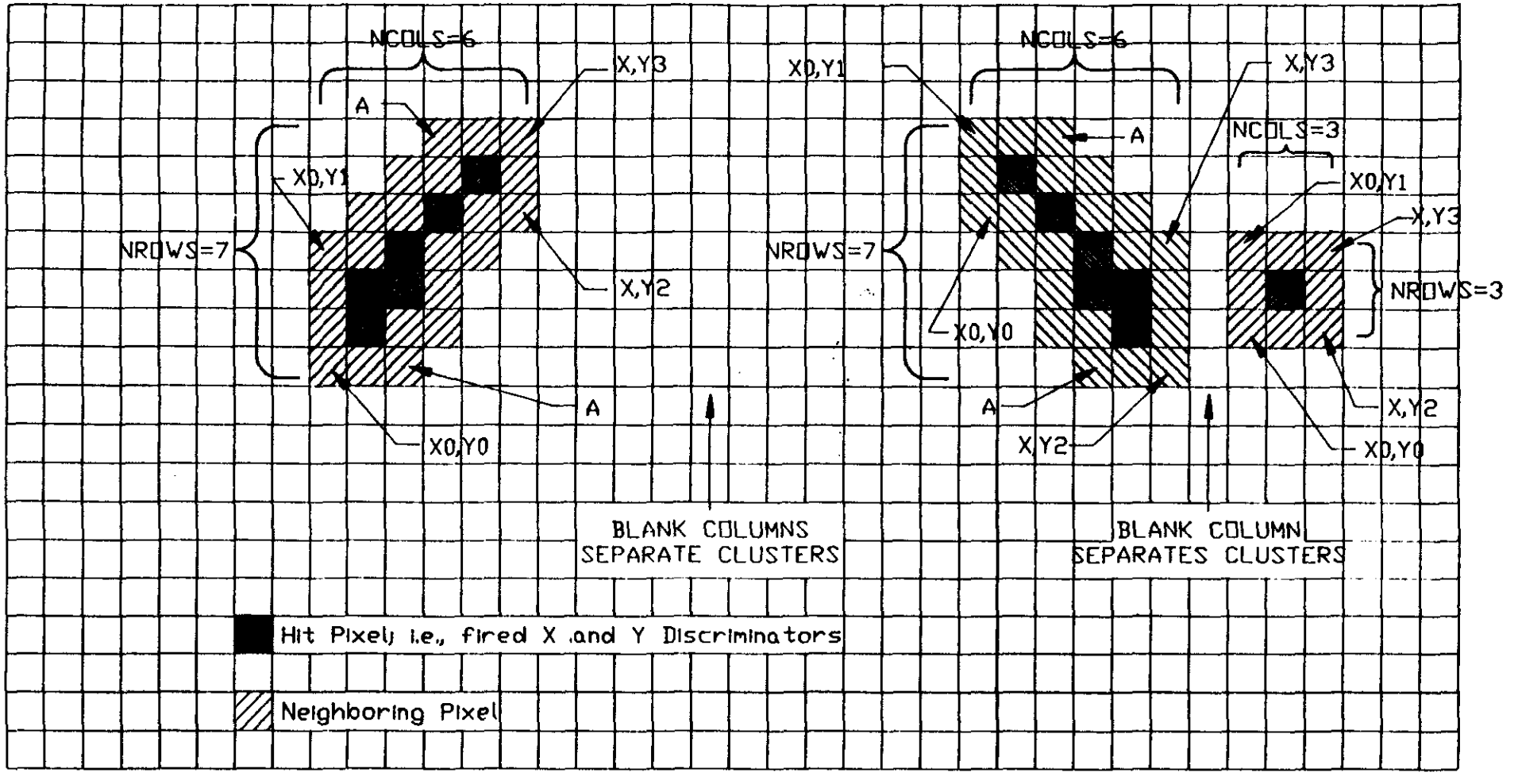
Note that if a control line on the cross links between rows corresponding to the FNDNBR line were installed, it would be possible to only find the rectilinear neighbors. The ALLROWS circuit would not be needed. If neither FNDNBRX nor FNDNBRY were turned on no neighbors would be found, where FNDNBRX controls the cross links between the columns and FNDNBRY controls the cross links between the rows. If only FNDNBRX were turned on, only the neighbors in a row would be found. If only FNDNBRY were turned on, only neighbors in a column would be found. If one of these control lines were turned on and off before the other were turned on and off, the rectilinear neighbors would be found. If both control lines were turned on at the same time, the rectilinear and diagonal neighbors would be found.

Time Window Accompanying the Trigger

The trigger will occur after the interesting event occurs. The detector array will probably have been hit during several uninteresting, or background, events in addition to the interesting event while waiting for the trigger. In order to distinguish the events, the time of each hit is recorded in registers on the array. Later, the trigger will be accompanied by a time word, TTRIG, giving the time of the interesting event. However, the time resolution will be poor because the trigger will come from the calorimeters, which surround the vertex detector with large scintillators and proportional counters. Scintillators and proportional counters are slow and also have poor time resolution. The interesting event could have occurred at any one of several beam crossing, or clock, times around TTRIG. All hits within a time window around TTRIG should be accepted as being the interesting event.

The PS VI design for recording time uses time registers on the columns instead of on the pixels. This arrangement allows the pixels to be small, and it works if the event rate is low enough that a column has a low probability of being hit by both a particle in the interesting event and also a particle in an uninteresting event. The time registers serve two purposes, which are 1) recording the event time, T, and 2) comparing the recorded time, T, with the time, TTRIG, supplied with the trigger. If T equals TTRIG, the register produces an output. This output is fed into a flip flop which in turn feeds the priority selection circuit. The flip flop allows several TTRIG times in a time window to be compared with T in the time register.

The PS VII design allows a column to be hit several times because each column and each row has several time markers. There is one set of time registers for the whole array.



Coordinates found in the sample DSP program are X0, Y0, Y1, Y2, Y3, X, NCOLS, NROWS, but coordinates of pixels labeled 'A' can also easily be found.

Other quantities calculated by DSP for determing centroid are XW, YW, W.

CLUSTERS OF PIXELS
&
QUANTITIES FOUND BY THE DSP PROGRAM

FIGURE 4

CAD FILENAME: CLUSTERS