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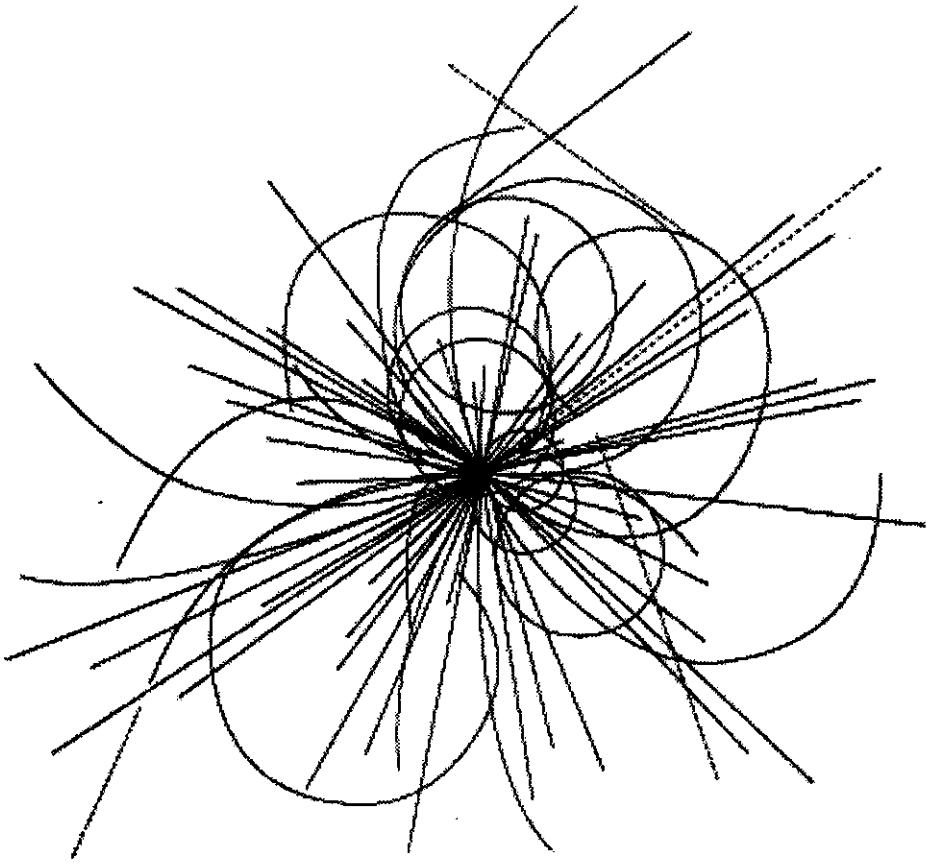
VME
Message Broadcast Systems



Superconducting Super Collider
Laboratory

SSCL-N-858

VME Message Broadcast Systems*

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Content Description

This is the design of a unified message broadcast system to handle the SSC site-wide distribution of all control system messages. The messages are assembled in the control room area and encapsulated for transmission via a fiber optic link system to devices distributed throughout the 70 miles of tunnel.

Remarks

Schematic design was captured on Racal-Redac ECAD software. All files are stored at bear.ssc.gov.

Specification for a VME Message Broadcast Receiver.

Rev 0: July 1 1992
Rev 1: Sept 15 1992
Rev 2: Nov 19 1992
Rev 3: Feb 22 1993

A Message broadcast receiver interface shall be built with the following salient characteristics.

Shall be a single height Industry Pack conforming to the Greenspring Industry Pack (IP) Logic Interface Specification.

Shall use 16 Bit data path option including ID, Memory, I/O and interrupt acknowledge cycles.

Shall be Hardware and Software compatible with the MVME-162 IP carrier PCB.

Shall handle 16 bit read data transfers only. (rev3)

Shall handle 16 bit write data transfers only. (rev3)

8-bit registers occupy the lower 8 bits of the 16 bit data path. (rev3)

Shall occupy less than or equal to 1 Kbyte of address space.

The card type and version number is contained in the ID PROM. (MBRXV1.0).

Shall receive data on a T1 (DSX-1) interface.

The interface shall receive messages over the T1 link.

The messages will have a 2 byte 'type' field followed by from zero to 13 'parameter' bytes. Encapsulation to be as in the MBS paper.

The 'type' of each message shall be compared with the contents of eight event registers

The event registers shall be writable and readable from the IP interface.

When the type of an incoming message matches the contents of one of the event registers, an interrupt will be generated.

The Message that caused the interrupt will be readable from the IP interface. The message will be contained in a 16 byte block, type field first followed by parameters.

14 messages will be stored in a buffer in the interface.

A fixed location shall contain a 16-bit word that points to the start of the block containing the message that caused the last interrupt. Eg. location 00 will contain 10 when the first interrupt is generated, and 18 when the second is generated. (rev3)

Observations:

Interrupt servicing software must service the interrupt and read the 16-bit pointer within 20uS to keep up with worst case message rate, it must also read messages within 14*(1/worst-message-rate) to avoid loss of message

because of over-writing.

Software can deduce how 'full' the 14 message buffer is by counting the number of un-serviced pointers it has.

Note that the IP standard required an interrupt mask bit that the software must set to enable interrupts after power-up. (rev3)

Address Map

I/O space: Not used.

Pack ID: Read only, Addresses 0-31 access a 32 byte prom which contains the standard IP ID format. User space is available for the ID 'MBRXV1.0'. Date is byte-wide in the lower 8 bits of the 16-bit data field.

Memory space: The lowest 7 bits of the memory address are used and mapped as shown below. Data accessed is always 16-bits wide. Upper address bits are ignored.

Address	Use	Read	Write
00	Pointer to current message buffer	Yes	No
01	Interrupt vector	Yes	Yes
02	Interrupt mask (bit 0 only)	Yes	Yes
03 - 07	Not used		
08	First event register	Yes	Yes
..	.....		
0F	Eighth event register	Yes	Yes
10-17	Message Buffer #1	Yes	No
18-1F	Message Buffer #2	Yes	No
..	.....		
78-7F	Message Buffer #14	Yes	No

Carrier Emulator

Protocol Generator

Sheet 1 of this section shows the protocol generator. This is a simulation tool, never intended for actual construction.

U5 is a 256 x 24 ROM which can be loaded with simple program instructions. It is addressed by counters U61 and U62. The contents of the ROM are address and data to the IP connector, and protocol controls: read/write and strobes. A 'HALT' instruction will suspend IP operations until an interrupt is received.

A simple state machine (U10, U15, U18, U79 etc) controls the IP protocol with exact timing.

This simulation responds to IP interrupts which vector the ROM address (U76, U77) to the value set in the low byte of the ROM (after HALT op) for IntReq0 (Message received) or to 80h for IntReq1 (Error interrupt).

During read operations data from the IP connector is compared (U13, U20, U25, U28, U66, U70) with data set in the ROM. If it differs an error is flagged (U68,3)

If no response is received from the IP, a time out circuit (U27, U34 etc.) enables the continuation of the program. This allows non-response testing.

T1 Message Generator

Sheet 2 shows the T1 stream generator.

The message sequences are stored as bytes in U42. U14, U40 address the ROM and U58 converts the bytes to bit-serial format.

This design does not generate true T1 signalling. Because simulation models for the T1 decoder chips used in the MBS receiver were not available (and it was not considered necessary to verify the operation of these commercial chips) the T1 signalling used in this simulation used a simple format. A T1 clock (1.544MHz) was passed on one of the 'balanced T1' wires, and time-multiplexed data on the other wire.

The time-multiplexed data has 4 intervals(6.176Mb/s). The first is th T1 data, the second bit is '1' if the byte the last (24th) in the frame (and it has 9 bits, the extra one being the framing bit), the third bit is a '1' for the last bit of each bite. The 4th bit is always '0'. A sync pattern is not produced for the framing bit, it is always '0'.

A model was made for the T1 decoder chip which converted this format to a T1 data stream, a 1.544MHz clock and word and frame clocks, which are the signals used by the MBS receiver system.

U56 counts the 4 multiplex periods which are encoded by the following and/or logic. U43 count the 8 bits in each bite (9 for #24), and U50, U52 count the 24 bytes/frame (channels).

```
/* Set events */

/* Set the following to load the ROM in the simulator */
INIT U15(U1) 8 x 32 = 0:
/* Bit significances are as follows:                    */
/* SEL: IO=8; Int=4; Mem=2; ID=1.                       */
/* R/W: Halt=9; Read8bits=3; Read=1;  Write=0.          */
/* After Halt, any IntReq0 restarts the program         */
/* at mem address set in low byte (ADR) of Halt op.     */

/* SEL R/W DATA ADR */
   '2   0  A001 08' H,  /* Event 1 */
   '2   0  A002 09' H,  /* Event 2 */
   '2   0  A003 0A' H,  /* Event 3 */
   '2   0  A004 0B' H,  /* Event 4 */
   '2   0  A005 0C' H,  /* Event 5 */
   '2   0  A006 0D' H,  /* Event 6 */
   '2   0  A007 0E' H,  /* Event 7 */
   '2   0  6789 02' H,  /* Int. vect. 0 */
   '2   0  5432 03' H,  /* Int. vect. 1 */
   '2   1  A001 08' H,  /* Read back event 1 */
   '2   1  A002 09' H,  /* Read back event 2 */
   '2   1  A003 0A' H,  /* Read back event 3 */
   '2   1  A004 0B' H,  /* Read back event 4 */
   '2   1  A005 0C' H,  /* Read back event 5 */
   '2   1  A006 0D' H,  /* Read back event 6 */
   '2   1  A007 0E' H,  /* Read back event 7 */
   '2   0  0003 01' H,  /* En interrupt */
   '1   9  0000 20' H;  /* HALT (will restart at 20H) */

INIT U5(U1) 8 x 32 = 32:  /* = 20H */
   '4   1  6789 00' H,  /* 20   Msg Int Ack */
   '2   1  0010 00' H,  /* Read ptr */
   '2   1  A001 10' H,  /* Read Msg ... */
   '1   9  0000 24' H;  /* Halt */
INIT U5(U1) 8 x 32 = 36:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0018 00' H,  /* Read ptr */
   '2   1  A002 18' H,  /* Read Msg ... */
   '1   9  0000 28' H;  /* Halt */
INIT U5(U1) 8 x 32 = 40:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0020 00' H,  /* Read ptr */
   '2   1  A003 20' H,  /* Read Msg ... */
   '1   9  0000 2C' H;  /* Halt */
INIT U5(U1) 8 x 32 = 44:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0028 00' H,  /* Read ptr */
   '2   1  A004 28' H,  /* Read Msg ... */
   '1   9  0000 30' H;  /* Halt */
INIT U5(U1) 8 x 32 = 48:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0030 00' H,  /* Read ptr */
   '2   1  A005 30' H,  /* Read Msg ... */
   '1   9  0000 34' H;  /* Halt */
INIT U5(U1) 8 x 32 = 52:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0038 00' H,  /* Read ptr */
   '2   1  A006 38' H,  /* Read Msg ... */
   '1   9  0000 38' H;  /* Halt */
INIT U5(U1) 8 x 32 = 56:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0040 00' H,  /* Read ptr */
   '2   1  A007 40' H,  /* Read Msg buffer 7  */
   '1   9  0000 3C' H;  /* Halt */
INIT U5(U1) 8 x 32 = 60:
   '4   1  6789 00' H,  /* Msg Int Ack */
```

```
   '2   1  0048 00' H,  /* Read ptr */
   '2   1  A006 48' H,  /* Read Msg buffer 8*/
   '1   9  0000 40' H;  /* Halt */
INIT U5(U1) 8 x 32 = 64:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0050 00' H,  /* Read ptr */
   '2   1  A005 50' H,  /* Read Msg buffer 9*/
   '1   9  0000 44' H;  /* Halt */
INIT U5(U1) 8 x 32 = 68:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0058 00' H,  /* Read ptr */
   '2   1  A004 58' H,  /* Read Msg buffer 10*/
   '1   9  0000 48' H;  /* Halt */
INIT U5(U1) 8 x 32 = 72:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0060 00' H,  /* Read ptr */
   '2   1  A003 60' H,  /* Read Msg buffer 11*/
   '1   9  0000 4C' H;  /* Halt */
INIT U5(U1) 8 x 32 = 76:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0068 00' H,  /* Read ptr */
   '2   1  A002 68' H,  /* Read Msg buffer 12*/
   '1   9  0000 50' H;  /* Halt */
INIT U5(U1) 8 x 32 = 80:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0070 00' H,  /* Read ptr */
   '2   1  A001 70' H,  /* Read Msg buffer 13*/
   '1   9  0000 54' H;  /* Halt */
INIT U5(U1) 8 x 32 = 84:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0078 00' H,  /* Read ptr */
   '2   1  A002 78' H,  /* Read Msg buffer 14*/
   '1   9  0000 58' H;  /* Halt */
INIT U5(U1) 8 x 32 = 88:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0010 00' H,  /* Read ptr */
   '2   1  A003 10' H,  /* Read Msg buffer 1 */
   '1   9  0000 5C' H;  /* Halt */
INIT U5(U1) 8 x 32 = 88:
   '4   1  6789 00' H,  /* Msg Int Ack */
   '2   1  0018 00' H,  /* Read ptr */
   '2   1  A004 18' H,  /* Read Msg buffer 1 */
   '1   9  0000 80' H;  /* Halt */


INIT U5(U1) 8 x 32 = 128:
   '4   1  5432 01' H,  /* 30   Err Int Ack */
   '2   3  0002 04' H,  /* Read Err */
   '2   3  0000 04' H,  /* Read Err */
   '1   9  0000 80' H;  /* Halt */
```

```
/* Broadcast message stream */

/* Set the following to load the ROM in the simulator */
INIT U42(U1) 8 x 32 = 0:

/* Only the lower byte is used */
/* Note: Idle changed to FF because software driver in  */
/* transmitter emulator could not produce CC as idle. */

'000000 00' H,
'000000 FF' H,
'000000 FF' H,
'000000 FF' H,
'000000 08' H, /* start */
'000000 A0' H, /* h1 */
'000000 01' H, /* h2 */
'000000 FF' H,
'000000 08' H, /* start */
'000000 A0' H,
'000000 02' H,
'000000 FF' H, /* etc */
'000000 FF' H,
'000000 FF' H,
'000000 FF' H,
'000000 FF' H;
```

Industry Pack MBRX Card

PCB Components

The schematic shows the components on the PCB.

T1, U1 (Dallas Semiconductor DS2180) and U3 (Dallas Semiconductor DS2187) receive and decode the incoming T1 data stream. Output is RCLK (1.544MHz clock), RSER (1.544Mb/s data), RCHCLK (192kHz T1 channel clock), RFSYNC (8kHz framing bit marker), RLOS (T1 data lost error) and RFER (T1 framing error). The clocks and data are fed to the MBRX FPGA for serial–to–parallel conversion, and the errors to the IPC FPGA for interrupt/error generation.

U4 (74ACT16245) is a 16–bit wide bi–directional buffer used to connect the 16 IP data bits to the internal data bus. Tri–state and direction are controlled by IPC FPGA.

U2, U5 (CY7C128) form a 16–bit wide by 2k r/w ram which us used for control registers, pointers and message buffering. Access is controlled by the IPC FPGA. This ram is 'dual ported' by circuitry in the IPC which arbitrates access by the message receiver in the MBRX and the IP interface in the IPC.

U6 (74LS14) is a hex schmidt inverter which is used to buffer some signals and to provide a delayed clock to IPC.

For information on the use and contents of the buses click here.

MBRX FPGA is an Actel A1020 FPGA containing T1 serial > parallel converter, message stream decoding, message identification and control of message storage.

IPC FPGA is an Actel A1020 FPGA containing IP protocol decoder and controller, and ram dual–porting controller.

MBRX PCB Busses

ID

Internal Data. 16-bit wide data, buffered version of IP data bus. Used for data communications between IP interface, ram, MBRX and IPC.

IA

Internal Address. 7-bit wide address for device being written/read. Addresses ram and MBRX. Is driven by IPC or MBRX depending on operation.

CTRL

Main Control bus, driven by IPC.

Contents:

- rpga Read MBRX. While 1, pass data from memory in MBRX to ID bus
- wpga Write MBRX. While 1, load data into memory in MBRX from ID bus
- wrah- Active-low write strobe to high byte Ram
- wral- Active-low write strobe to low byte Ram
- rram- Active-low read Ram word to ID.
- endio- While 0 turn on '16245 data buffer, direction depends on txrx-.
- txrx- While 0, enable D to ID buffer. While 1, enable ID to D buffer.

MBRX FPGA

This is an Actel A1020 Field Programmable Gate Array which contains 7 words of 16–bit event memory, a serial data to byte–parallel converter, MBS encapsulation decoder, header extractor, parameter counter and memory address generator, and message validation. The header is stored internally and compared with the event memory. Any match is indicated. A data multiplexer selects output to the 16–bit parallel data I/O port, either one of the event memories, the current T1 byte (duplicated on high and low bytes) or the current store address (used to save the last–message–pointer.)

Schematics For The MBRX FPGA

A top level schematic shows the block diagram of this FPGA. Bus connections are fanned out at an interface level.

Event Memory (7 words)

See schematic.

Each of the 7 event memories has 16 gated latches, buffered gate drive for upper and lower bytes, and 16–bit data busses for read and write. A third 16–bit bus carrying the current header value is compared with the latch contents in 16 ex–ors. The result is ANDed to indicate a match.

Write address buffer.

See schematic.

This decodes write operations to for load strobes for the event memories.

Read Mux.

See schematic

This selects the 16–bit data to be output from the MBRX.

msel 4	msel 3	msel 3	msel 1	msel 0	Data Source
0	0	n	n	n	Event Register n
0	1	x	x	x	Not used
1	0	x	x	x	Itdat (duplicated)
1	1	x	x	x	mcount (low 7, high 9 = 0s)

ITDAT is selected for writing T1 data into the RAM. The 8 bits of T1 data are duplicated onto the 16 bit internal (to the chip) data bus and its is turned on (rdpgal from the CONTROL chip) so that the data flows to ID and thus to the ram inputs. CONTROLLER then strobe writes either the hi or lo ram depending on if the byte is odd or even numbered (MCOUNTE.)

Serial to parallel converter

See schematic.

The 1.544Mb/s data is clocked into an 8–bit shift register, and each word is then clocked into a parallel latch. A second 8–bit parallel latch is used to hold the other byte of a header for comparison in the event memories.

Message Sync

See schematic.

This contains the Idle byte detector, checksum checker, encapsulation decoder, length down–counter and address and block up–counters.

The block counter is initialized at 2 and the address counter at 0, indicating the first storage address, 20h in RAM. When a change from Idle to Valid Start is detected, the down counter is loaded with the length value from the Start byte. For succeeding bytes the down counter is decremented and the address counter is incremented while the data is stored in ram at the address/block location.

An Idle byte is looked for at the end of message. If it is not present an error is flagged and the address counter set to zero. If it is present a valid message is flagged, the address counter set to zero and the block counter incremented.

IPC FPGA

This is an Actel A1020 Field Programmable Gate Array which handles the IP Protocol. It responds to IDsel, producing 16 bytes of data which is programmed inside the IPC, and Memsel, allowing read or write to various registers. It produces two interrupts, Intreq0 for messages received and Intreq1 for errors. It also handles arbitration for access to the ram. It does not respond to ByteSelect; data is always 8-bit wide for ID and 16-bit wide for Memory. It does not request DMA operations or assert IP Error.

Schematics For The IPC FPGA

A top level schematic shows the block diagram of this FPGA. Bus connections are fanned out at an interface level.

Alatch

See schematic.

Address latch. A 7-bit wide edge triggered latch used to hold the IP address. Inputs are 6 bits from A1-A6 and 7th bit from D00. Output is IBA0-6.

Iamux

See schematic<.p> The IAMUX selects the internal address used by the MBRX. Sources are controlled by inputs S0 and S1.

S0	S1	IIA value	Operation
0	0	IBA	IP address, RAM/ROM/Event Register etc.
0	1	IMCOUNT	MBRX is writing message to RAM @ IMCOUNT
1	0	00	MBRX is writing pointer to RAM @ 00
1	1	02 (IBA0=0)	RAM producing interrupt vector 0
1	1	03 (IBA0=1)	RAM producing interrupt vector 1

Note that during an Interrupt operation the IP address is set by the Carrier to select which Interrupt is being serviced. This value of A0 is ORed in the mux with '2' to produce the address in the ram where the vector is held.

Id_error

See schematic.

This is an 8-bit wide by 16 word mux used to produce the ID and also to read the error register. The output drives the internal data bus via tri-state buffers. The mux is addressed mostly by the internal address bus, however values E and F both read location E. The ID sequence is programmed on the inputs of the mux. See table below.

When RERR is asserted the mux address is forced to F, reading the error latch contents. The bits of the error latch are set on the PRE input by pulses and cleared at power-up on the CLR input. On the falling edge of RERR all the bits are clocked with D=0, clearing them. CLRE4 is used to clear the write-request latch. See errors.

ID string

Address (hex)	Value (hex)	Significance
0	49	ASCII I
1	50	ASCII P
2	41	ASCII A
3	43	ASCII C
4	01	Mfg ID (un-registered)
5	01	Model Number
6	01	Revision
7	00	Reserved
8	00	Driver Hi (unused)
9	00	Driver Lo (unused)
A	0C	Number of bytes used
B	CE	CRC
C	00	Not used
D	00	Not used
E	00	Not used

F	00	Not used

The CRC data is obtained from program /home/redfox/klow/ma/crc/crc* 14 Apr 93

Logic

See schematic.

U194 and U192) define the operation being performed. For every valid operation U192 is set, generating Ack*, and at least one other latch is set, indicating the type of operation: Mem Write, Mem Read, ID, Interrupt. For memory operations Mem Adr Cycle is also set. These latches are clocked by the CLK edge and D inputs are decoded from the Sel signals, and R/W*. Only Address bit 0 is used to set the Interrupt latch if the IPC is asserting the appropriate interrupt request.

Errors

See schematic.

The error latch is located on the same schematic as the ID rom, and consists of three D latches. They are set by error pulses on the PRE input and cleared by CLRN on the CLR input. They are read by RERR=1, which is generated by address decoding logic (elsewhere) when reading address 04. On the falling edge of RERR the error latches are cleared.

Data from the error latches is multiplexed into the IDROM mux at 'real' location 15decimal. When IDROM location 15 is addressed, location 14 is actually read out. (Note that locations 12, 13, 14 and 15 are 'not used' and are therefore all 00.)

Arbitration

See schematic.

The RAM used by the receiver is single–port. Because both the message receiver and the IP interface must access the RAM an arbitration system is necessary. Requests from the receiver are either for word (16 bit) or byte (8 bit) access. These are synchronized to the IP 8MHz clock and stored in U51 or U58. The requests are arbitrated in U8 and U6, setting either U66 or U7. If RAM is already being accessed, the request is queued. IP access has priority if requests are simultaneous as the IP operation is very fast compared to receiver operations.

If the receiver is accessing the RAM when IP access is requested the IP interface produces a few wait cycles. Receiver access (to write one byte or word) is very fast, so IP access is delayed only a short time.

If IP holds access for a long time (perhaps due to bad programming in the carrier board) it is possible that a queued receiver access is not processed before another receiver byte arrives. In this case U46 on the top level schematic is set, indicating an error.

Interrupts

See schematic.

The interrupt system is conventional. U41 and U81 are mask bit latches set or cleared via the IP interface. A RAM location is set in parallel with these registers, and it is the RAM contents that is read out when the mask is read via IP.

Interrupt 0 is produced when a message of interest has been received and interrupt 1 is produced when an error occurs. The interrupt request latches U22 and U39 are cleared when the appropriate IP interrupt cycle is performed.

THE PROTOTYPE MESSAGE BROADCAST SYSTEM FOR THE SUPERCONDUCTING SUPER COLLIDER

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Abstract

A prototype unified message broadcast system to handle the site-wide distribution of all control system messages for the Superconducting Super Collider is presented. The messages are assembled in the control room area and encapsulated for transmission via a general fiber-optic link system to devices distributed throughout 70 miles of tunnels. An embedded timing signal is used by the distribution system to ensure that messages arrive at all devices simultaneously. Devices receive messages using a special receiver sub-system. A simple version of this system is to be used in the Accelerator Systems String Test (ASST) at the SSC site in 1991.

I. INTRODUCTION

The Superconducting Super Collider (SSC) is a 20 TeV + 20 TeV proton collider proposed for construction in the area of Waxahachie, Texas during the next 10 years. The SSC consists of six accelerators: a linac, three booster synchrotrons and two intersecting, contra-rotating synchrotrons that make up the collider itself. The complex will occupy approximately 70 miles (112 km) of underground tunnels and is illustrated diagrammatically in Fig 1. There are estimated to be about 20,000 devices requiring remote control and interrogation in order to operate the accelerator and diagnose its condition. Tools that are being investigated to perform these tasks are time-division multiplex (TDM) transport of digital data by fiber-optic cable, reflective memory techniques for point-to-point data transmission, and a message broadcast system (MBS) for distribution of medium-time-critical commands and data.

In large accelerator control systems, general data and commands have to be sent to many devices and a broadcast system is an efficient way to do this. Such systems have been used successfully at FNAL [1] and CERN [2]. The MBS proposed for use at the SSC will carry only commands, brief data and rough timing. Precision timing is to be handled by a dedicated system [3], and voluminous operating data is to be transported by local area networks or by a reflective memory system in which data written to one memory is automatically copied via the TDM system to a remote memory, where it may be read.

*Operated by the Universities Research Association, Inc., for the U.S. Department of Energy under Contract No. DE-AC02-89ER40486.

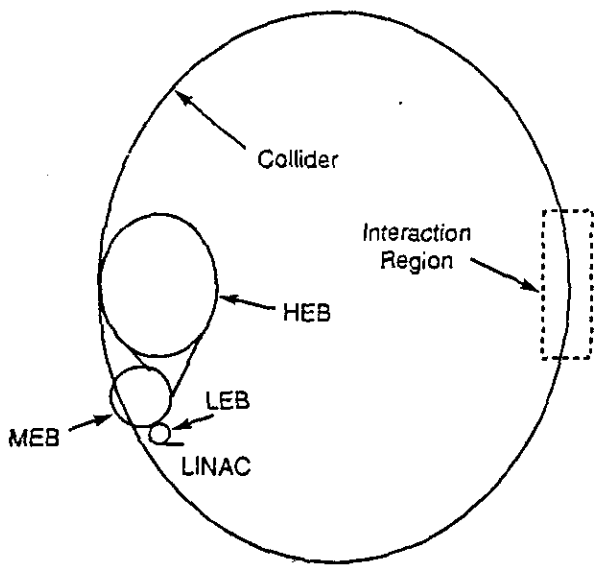


Figure 1: The Superconducting Super Collider (not to scale)

II. MESSAGE BROADCAST SYSTEM

The MBS is shown in Fig 2. and consists of one central message generation system, a transport network, timing correctors and many receivers attached to controlled devices. The transport network contains no intelligent routing mechanisms, messages are simply broadcast to all receivers. Every broadcast message has a *message type* or *identifier* header together with some trailing bytes, the number of which is indicated in the message header. Each receiver is pre-programmed to recognize a set of one or more such messages. When a receiver identifies such a message it passes the complete message to the device for execution.

Initial design plans call for separate broadcast systems for each of the six machines since the machines have vastly differing cycle times, ranging from 0.1 s to many hours. Site-wide broadcast, when required, is achieved by commanding each message generator of all six broadcast systems to send the same message.

Messages are structured using 8-bit bytes. Each message consists of a two byte header indicating the message type followed by from zero to thirteen bytes of parameters. The messages are prefixed by a start byte and suffixed by an idle byte to enable transportation by a general time division multiplex system. The format of a typical message is shown in Table 1.

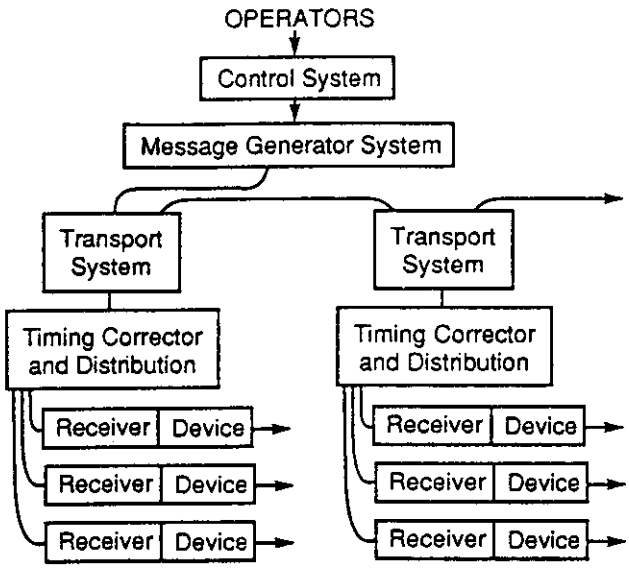


Figure 2: The Message Broadcast System

Table 1. Message Format

	msb							lsb
Start	0	0	0	1	0	1	0	1
Header	0	1	1	0	0	0	1	1
Header	0	0	0	1	1	0	0	0
Parameter	0	1	0	0	1	0	0	1
Parameter	0	1	0	0	1	0	1	0
Parameter	0	1	0	0	1	0	1	1
Idle	1	1	0	0	1	1	0	0

The format of the start and idle bytes are shown in Table 2. The two most significant bits in the start byte are set to zero to assist in identifying the start of a message, the next four bits indicate the message length and the final two bits are the byte check-sum. The message length includes the two byte header, allowing up to 13 parameter bytes, which is judged to be sufficient for all applications. The message length is thus the number of bytes before the terminating idle byte. The idle byte is binary 1100 1100, follows every message and is also transmitted as fill when there are no messages.

Table 2. Characteristics of Start and Idle Bytes

	msb							lsb
Idle Byte	1	1	0	0	1	1	0	0
Start Byte	0	0	n	n	n	n	c	c

nnnn = number of following bytes in message, cc = checksum

This format allows for easy identification and integrity checking of messages. A message starts when an idle byte is followed by a byte containing '00' in the two most significant bits. This is the start byte, and can be checked for integrity using the checksum. The message le extracted and decremented as the following head parameter bytes are received. When the message l has been decremented to zero an idle byte is exp otherwise a framing error has occurred. Data contai the optional parameters may be checked for integri embedding check bits.

III. MESSAGE GENERATION

Messages are generated by a central system consist a single message sequence generator and six messag matters, one for each broadcast network. This syst shown in Figure 3. Sequences of messages to opera various accelerator systems in tandem are predefi physicists and are contained in a database. To achi required operational state, the master sequence gen uses this database to translate high level requests fro erators to suitable sequences of low-level messages. T sequences are automatically transmitted by the me formatters to the accelerators.

Asynchronous requests and feedback control mes can also be handled by this system. Such requests include luminosity measurements on demand, turn by chromaticity values for magnet ramp feedback contr agnosis and 'beam dump' requests.

The sequence generator transfers the messages t formatter using a common random access memory (R. Each message formatter is assigned a separate blo this RAM, accessible only by itself and the messag quence generator. Messages are placed in RAM block signed to the appropriate message formatter. The for ters read their blocks of RAM continuously, encapsul and transmitting messages found there. Any asynchr message sequences earmarked for a specific accelerato transferred to special locations in RAM by the messag quence generator to be read by the appropriate form and transmitted over the broadcast network.

Every message table contains embedded instru codes specifically for the message formatter. These ins tion codes precedes each message in the table. The sage formatter recognizes these special instructions it then uses to control the transmission of the messa

The master sequence generator is a standard single puter board with a Motorola 68030 cpu. The me formatters each contain a special-purpose micro-cont which reads the common ram, executes the embedd structions and encapsulates messages for transmissio

An out of sequence message for immediate transmi may be placed by the master sequence generator in a cial location in the common RAM. This message w sent by the message formatter as soon as it finishes se the current message.

At a higher priority, special messages may be gene by a hardware signal. A transition on a line to the me formatter causes it to send a special pre-defined me

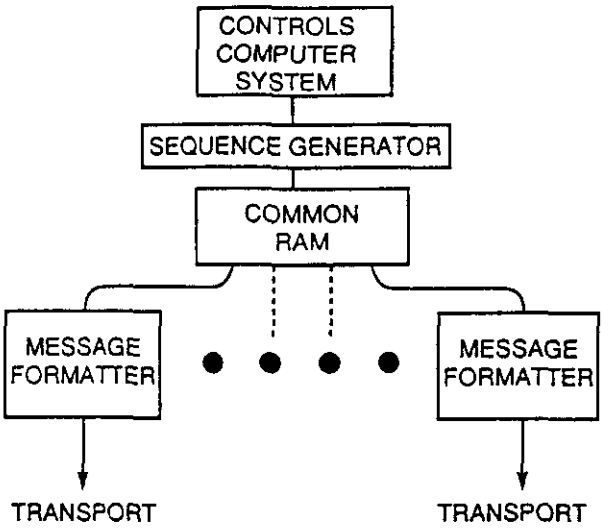


Figure 3: The Message Generation System

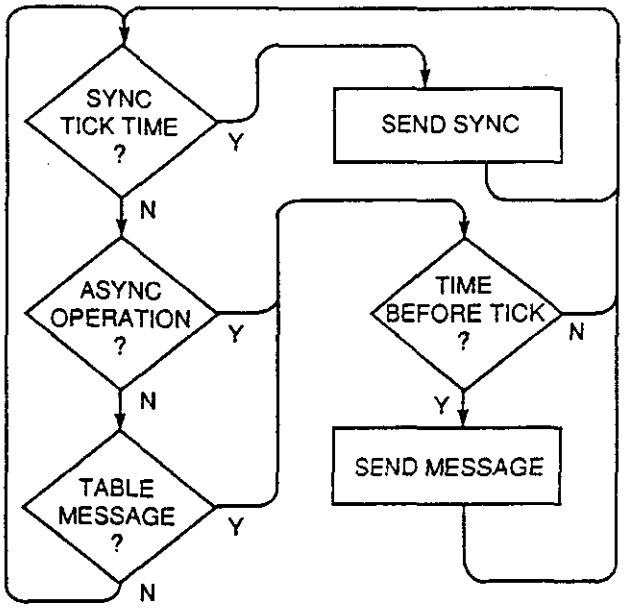


Figure 4: Flow Diagram for the Message formatter

from common RAM as soon as it reaches the end of its current message.

The message formatter also automatically produces a regular *sync tick* message. This is transmitted at a regular 1440 Hz rate (694.44 us period.) with an accuracy of a few micro-seconds, and is locked to the global precision timing system of the SSC [3]. It has two parameter bytes which contain the sync tick number. This message is used by the broadcast message distribution system for compensation of transmission delays, and may also be used as a medium precision timing signal by devices in the field. Devices requiring more accurate timing will use the global timing system of the SSC.

The sync ticks must be transmitted at the correct interval, therefore the message formatter must be aware of the time left before the next sync tick each time it has a message to send. If there is insufficient time remaining to send the next message before the next sync tick is due, then the message must be deferred until after the sync tick. A flow diagram of the tasks performed by the message formatter is shown in Fig. 4.

IV. MESSAGE DISTRIBUTION AND RECEPTION

A. Message Transport

The broadcast messages are designed to be transported by time-division multiplexing on fiber optic links, as used by the telecommunications industry. It is expected that one T1 (1.544 Mb/s) channel will be used, providing a capacity of about 26,000 messages per second, where an average message consists of a start byte, two header bytes, three parameter bytes and an idle byte.

Due to the large area covered by the SSC and delays caused by the many repeaters in the transport system, a time-skew of several milli-seconds will occur in the arrival of messages at local and remote points. To ensure that broadcast messages arrive at all devices simultaneously, a timing corrector is located at each message broadcast system distribution point. (See Figure 2)

The timing corrector compares timing signals (sync ticks) embedded in the broadcast message stream with the local precision timing system signals and inserts a correcting delay so that any broadcast message will arrive at all locations with a skew of only a few micro-seconds. Messages are prepared and transmitted from the control room ahead of the required execution time to allow for this delay. Actions which require more accurate timing than the message broadcast system can provide will use trigger signals from the global precision timing system.

B. Broadcast Message Receivers

Devices which are to receive messages via the message broadcast system do so using a broadcast message receiver (BMR.) This sub-system is connected to the transportation system and monitors all broadcast messages. It recognizes those messages which are of interest to the device, stores the message header and any associated parameters, and sends a signal to the device indicating that a message has been received. The device then interprets the message header and associated parameters, and performs the required action.

The BMR may be used as a micro-processor peripheral or as a simple stand-alone interface. As an intelligent peripheral it connects to the address and data bus, sharing access to RAM (See Fig. 5). A table of the types of messages that the device wishes to receive is placed in the RAM by the micro-processor and accessed by the BMR. Parameters associated with received messages are placed in RAM by the BMR for use by the micro-processor. The

BMR produces an interrupt to the micro-processor when a message of interest has been received. Several messages may be buffered in the RAM for eventual processing.

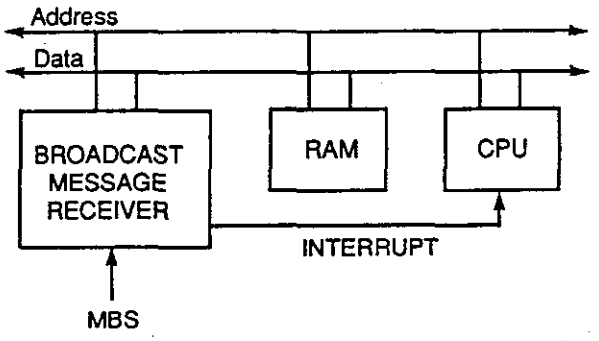


Figure 5: Broadcast message receiver with micro-processor

In simple applications the BMR may be used without a micro-processor. In this case either a switch or jumper system may be used to indicate one or two valid message types or a PROM may be used for more complex recognition. Parameters may be stored in external byte-wide D-latches. (See Fig. 6)

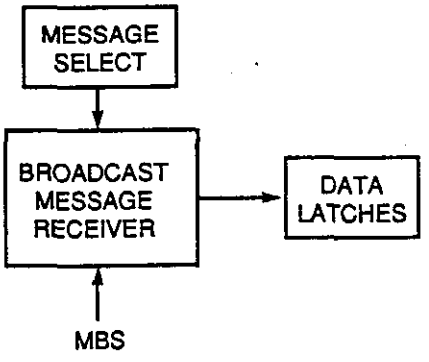


Figure 6: Simple Broadcast message receiver

V. CURRENT STATUS

Detailed design work is under way for a simple version of the message broadcast system to be used in the Accelerator Systems String Test at the SSC site in 1991. The ASST is a feasibility study of a set of cryogenically cooled super-conducting magnets. The messages will be of fixed-format containing two parameter bytes. Receivers will recognize one programmable message type, and output eight binary control signals. The system will comprise one message generator and several message receivers, interconnected by a shielded twisted-pair cable, with transformer isolation. Signalling will be T1 format at 1.544 Mb/s.

The proposed hardware configuration will consist of a Mizar 8130 (MZ8130) single board computer with a 68030 cpu functioning as the central message generator and a custom micro-controller for the message formatter.

VxWorks has been chosen as the software development environment since it provides for a real time, high performance operating system for the MZ8130 while allowing for a rich software development under Unix since VxWorks is a cross-development system.

V. ACKNOWLEDGMENTS

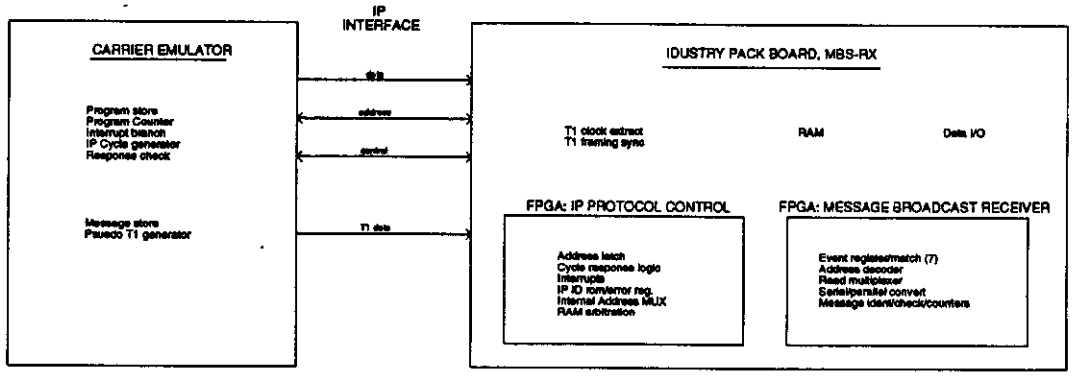
We thank H. Lue and C. Saltmarsh for their contributions to the design and development of this system.

References

[1] R. J. Ducar et al., "FNAL Booster Intensity, Extraction, and Synchronization Control For Collider Operation", 1987 Particle Accelerator Conference, Washington D.C.

[2] C. G. Beetham et al., "Overview of the SPS/LEP Fast Broadcast Message Timing System", 1987 Particle Accelerator Conference, Washington D.C.

[3] D. J. Martin et al., Early Instrumentation Projects at the SSC, SSC Laboratory Report SSCL-272 (April 1990).



REVISIONS

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	APPLICATION	

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TOLERANCE OF DECIMALS

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3. MAX. TO AVOID FILM GRAIN
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SI-METRIC

THIRD ANGLE PROJECTION

MBS-RX
SIMULATION ENVIRONMENT

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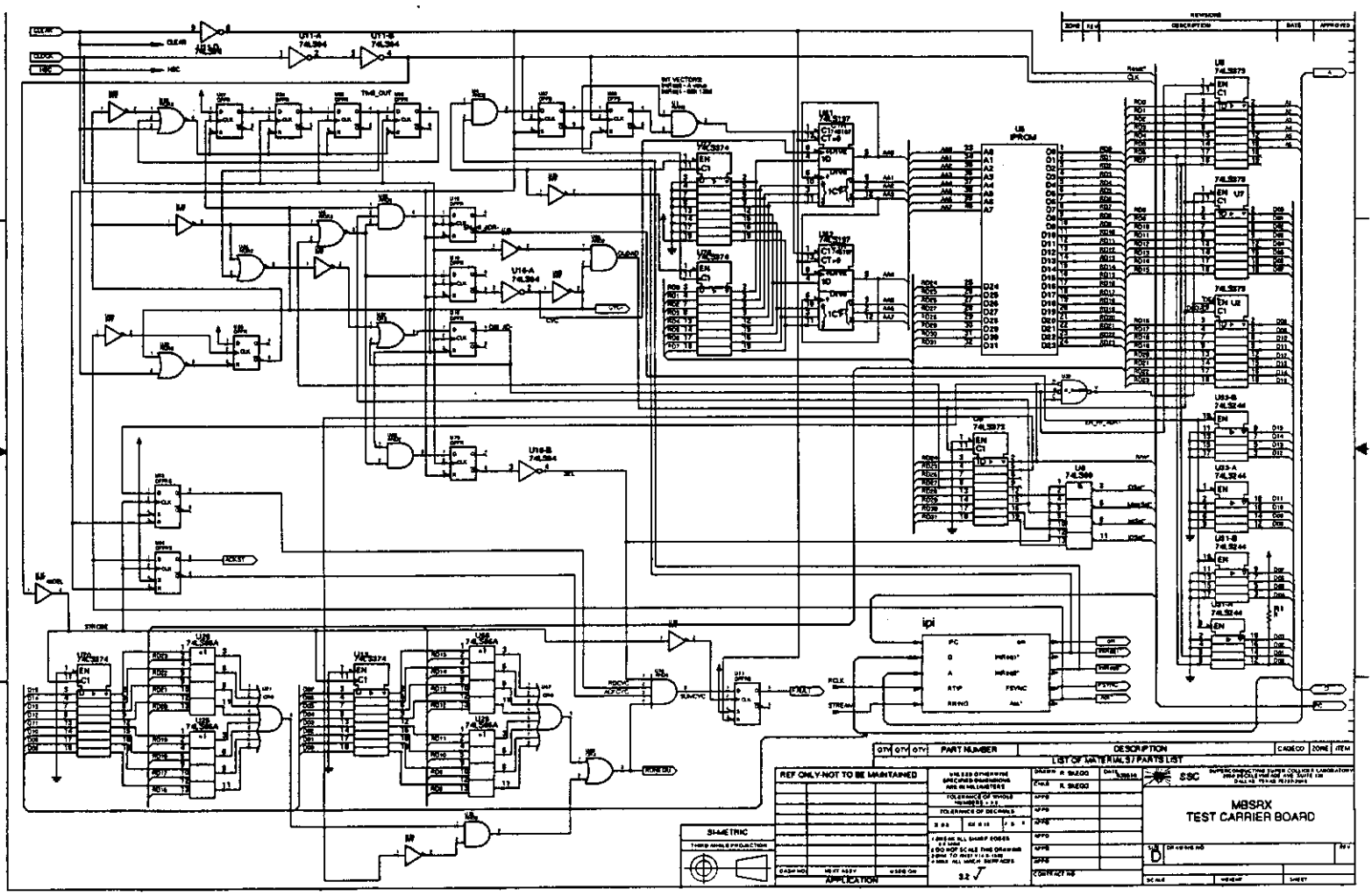
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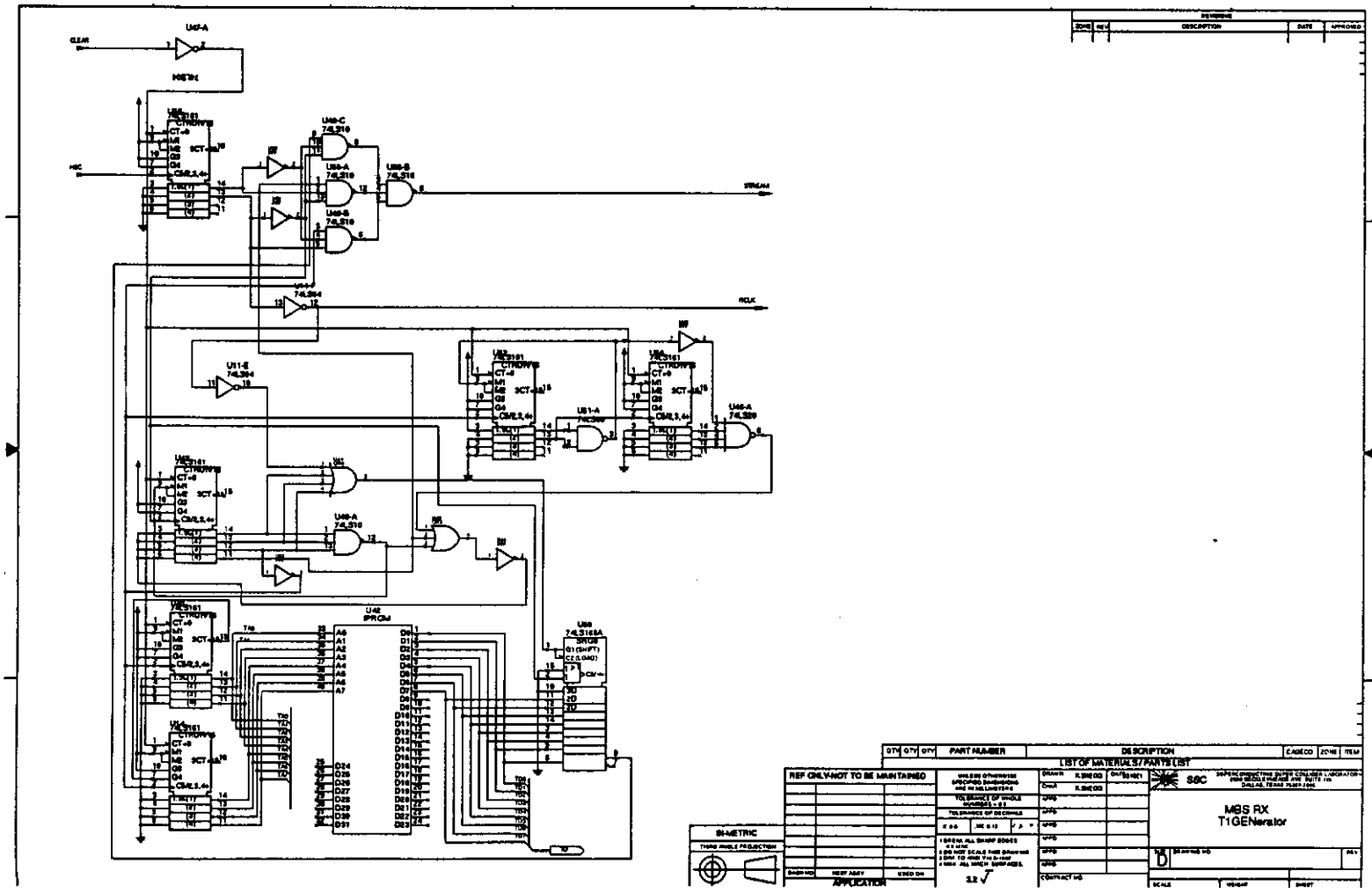

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REF ONLY-NOT TO BE MAINTAINED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
TOLERANCE OF WHOLE NUMBERS ± 0.5
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1 BREAK ALL SHARP EDGES 0.5 MAX
2 DO NOT SCALE THIS DRAWING
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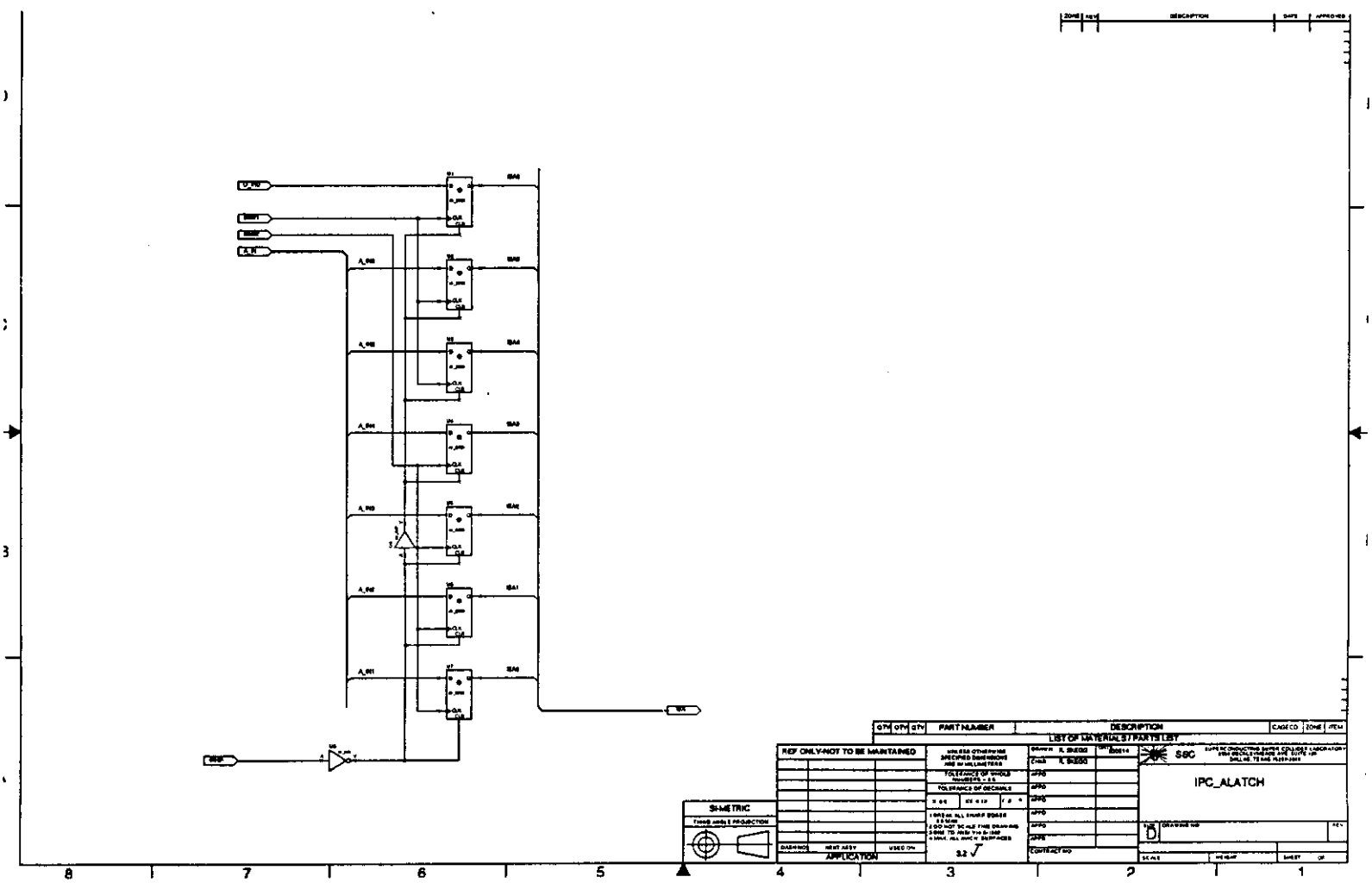

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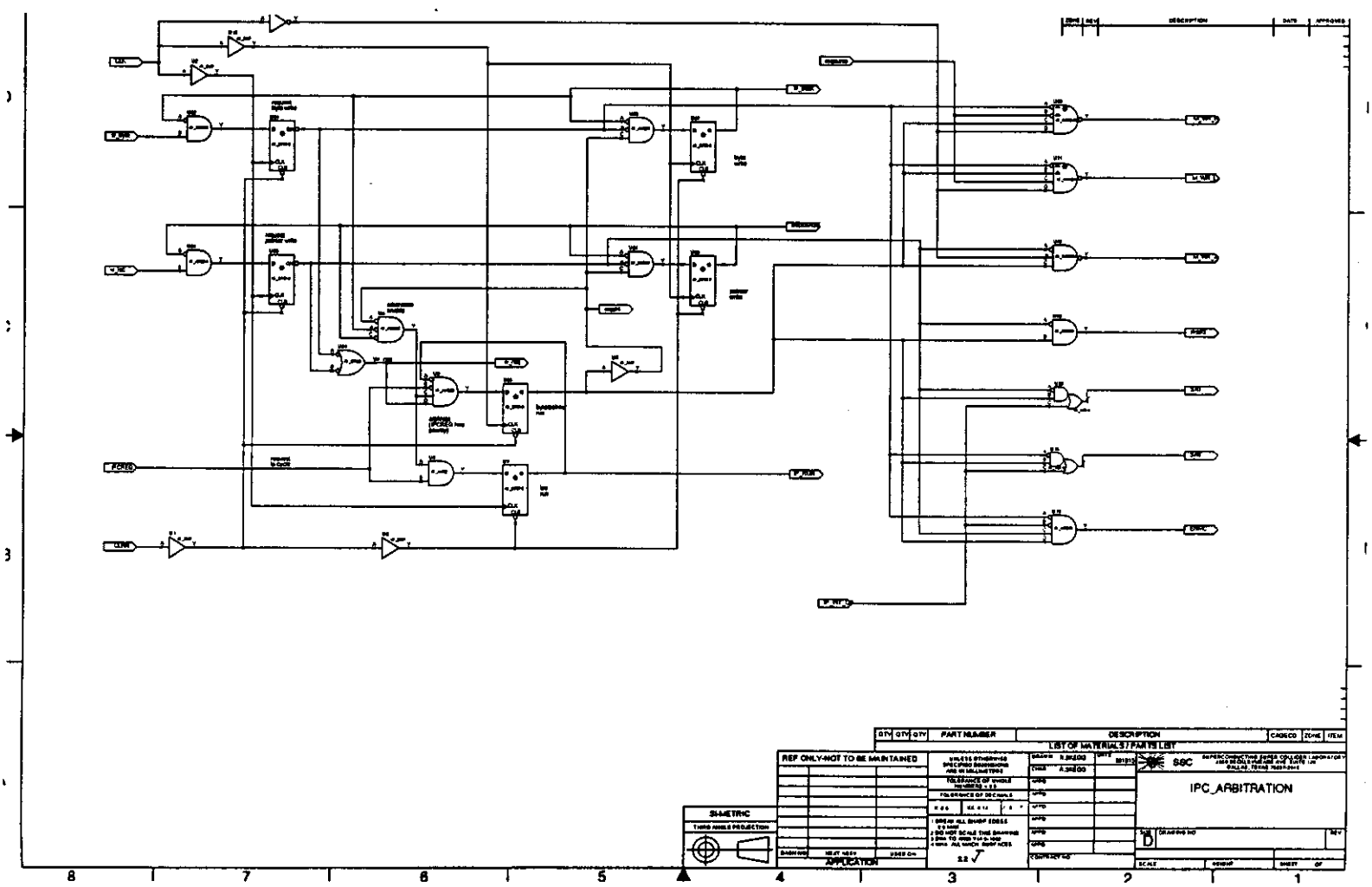

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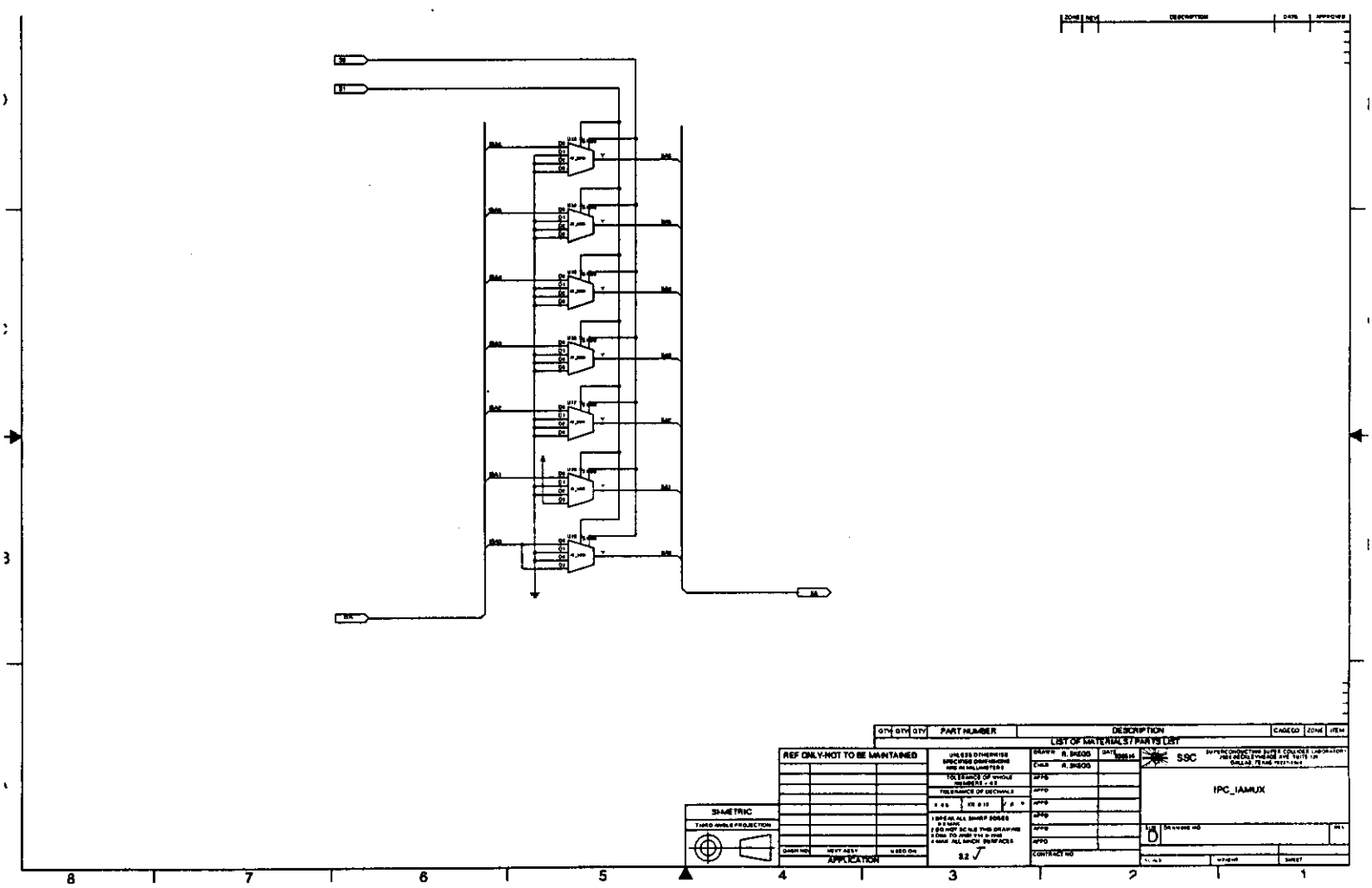

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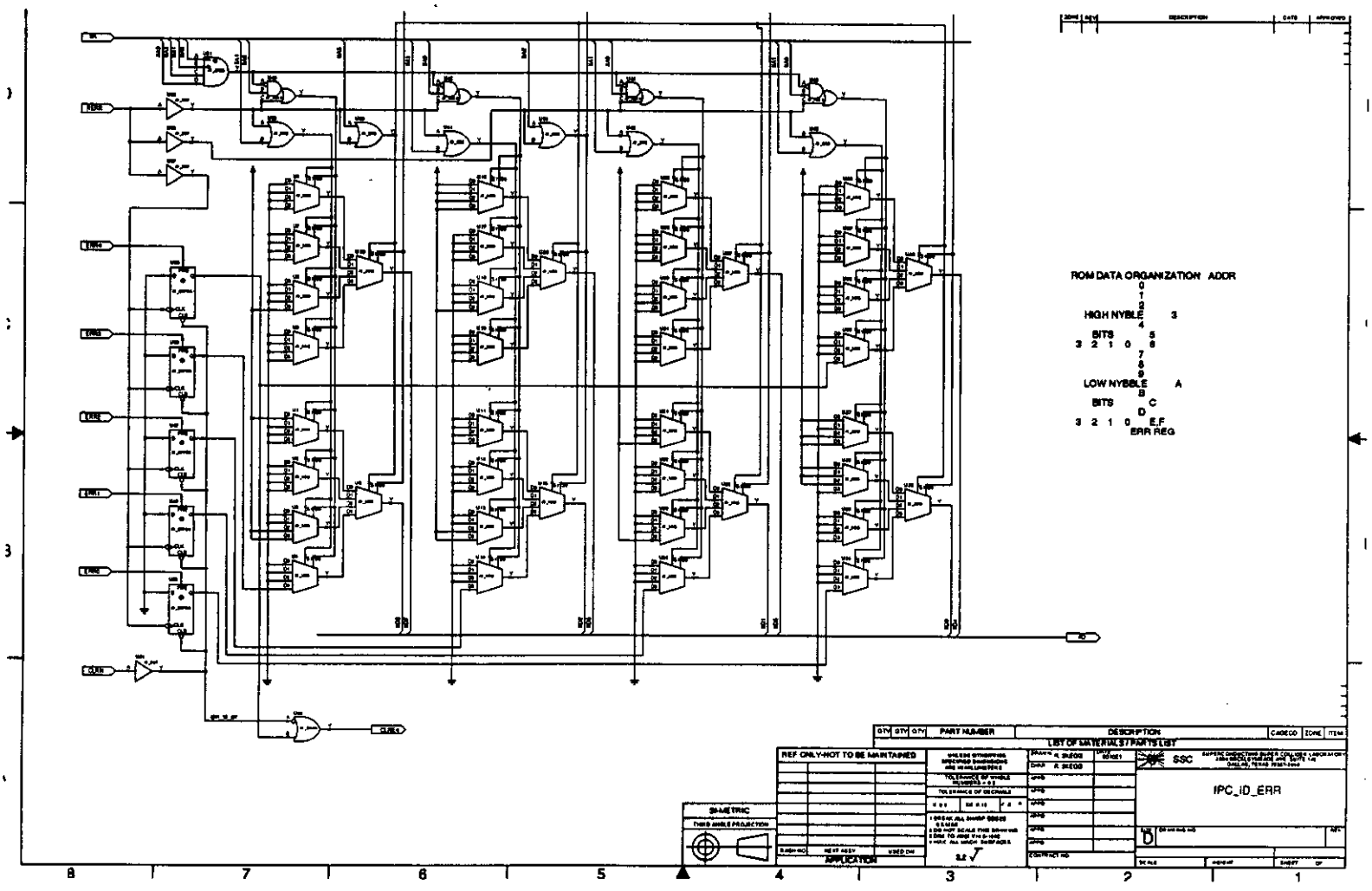
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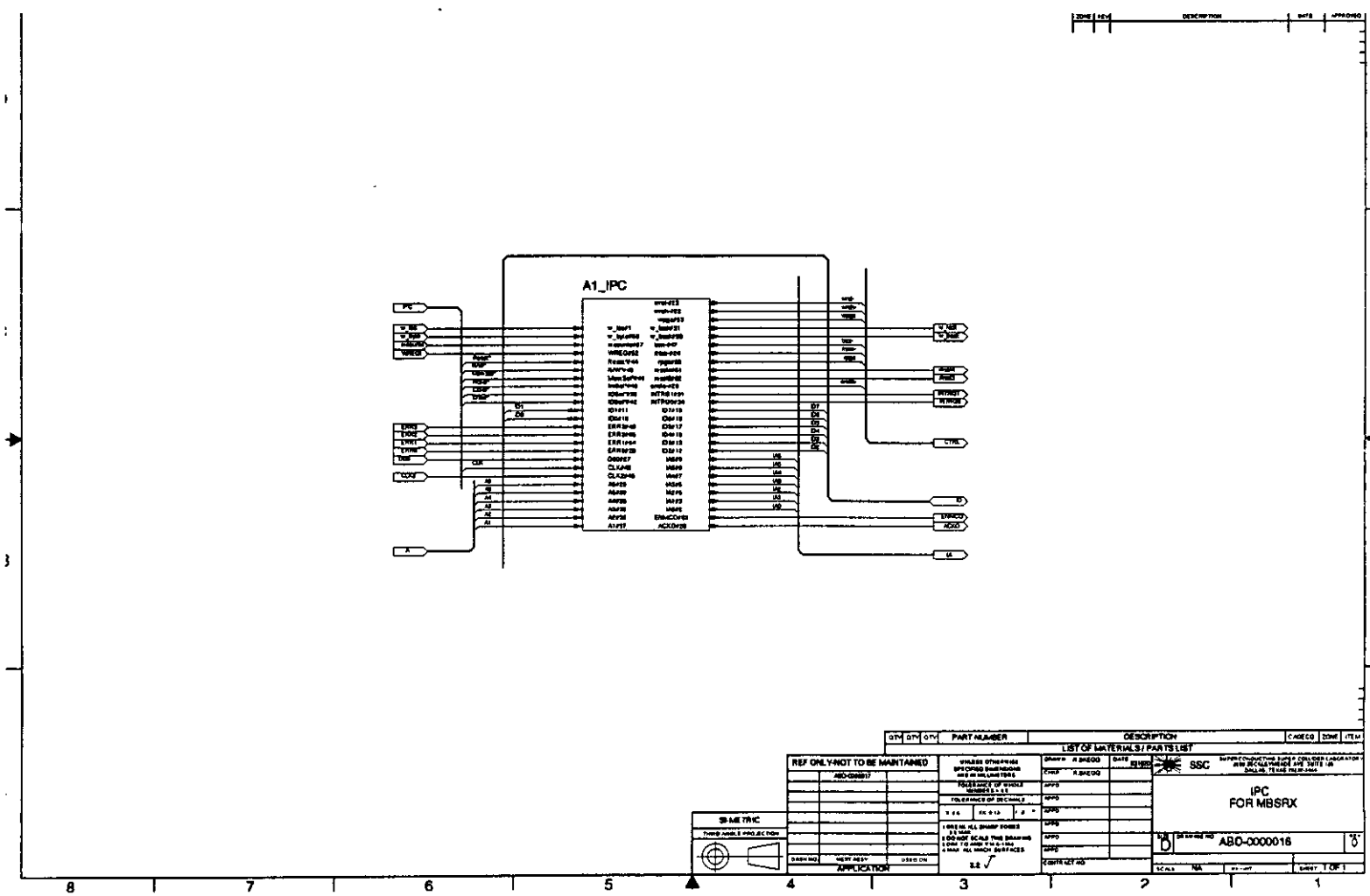
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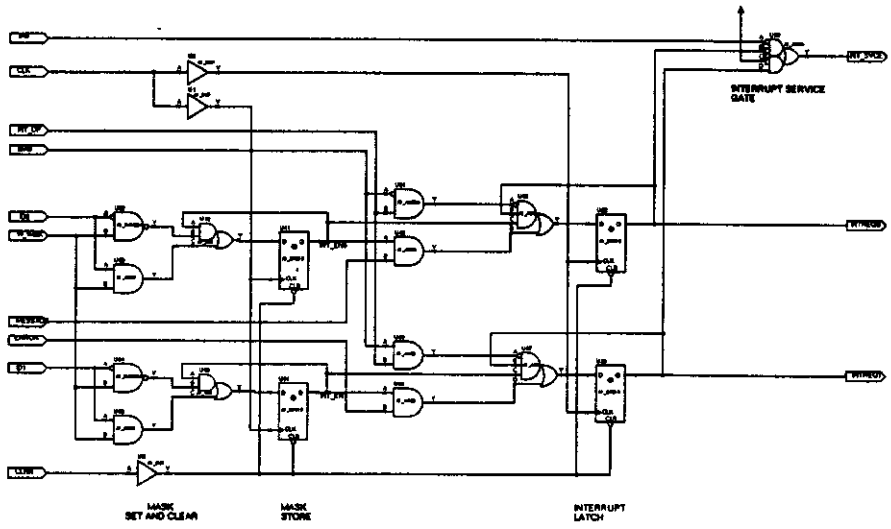

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APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

TOLERANCE OF WHOLE NUMBERS ± 0.5

TOLERANCE OF DECIMALS

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2 DO NOT SCALE THIS DRAWING
3 DIM. PD ARE TYP 3-1000
4 MAX. ALL MACH. SURFACES

3.2 √

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CHKD R.SIEGO
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SSC

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SCALE | WEIGHT | SHEET OF

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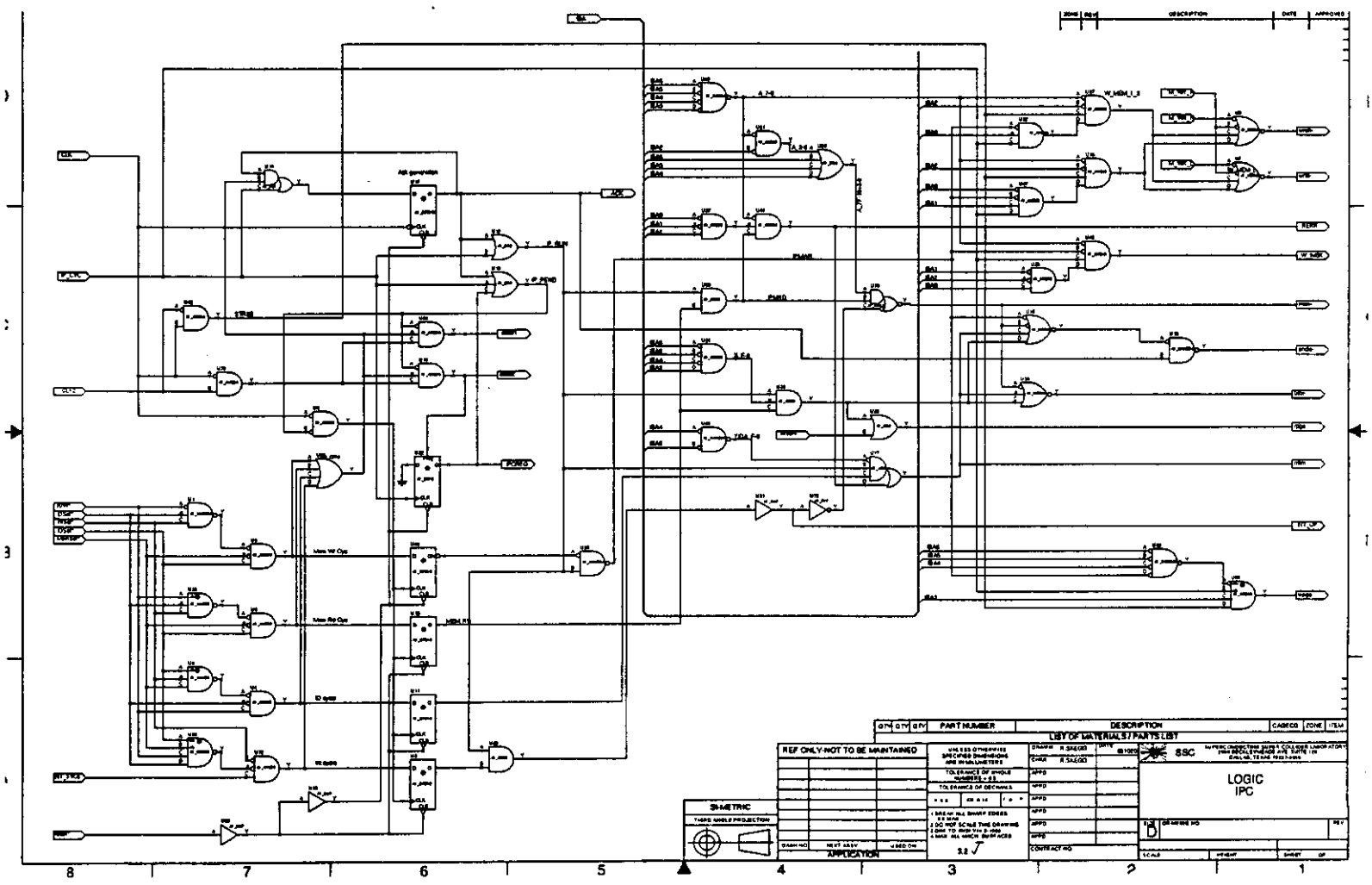
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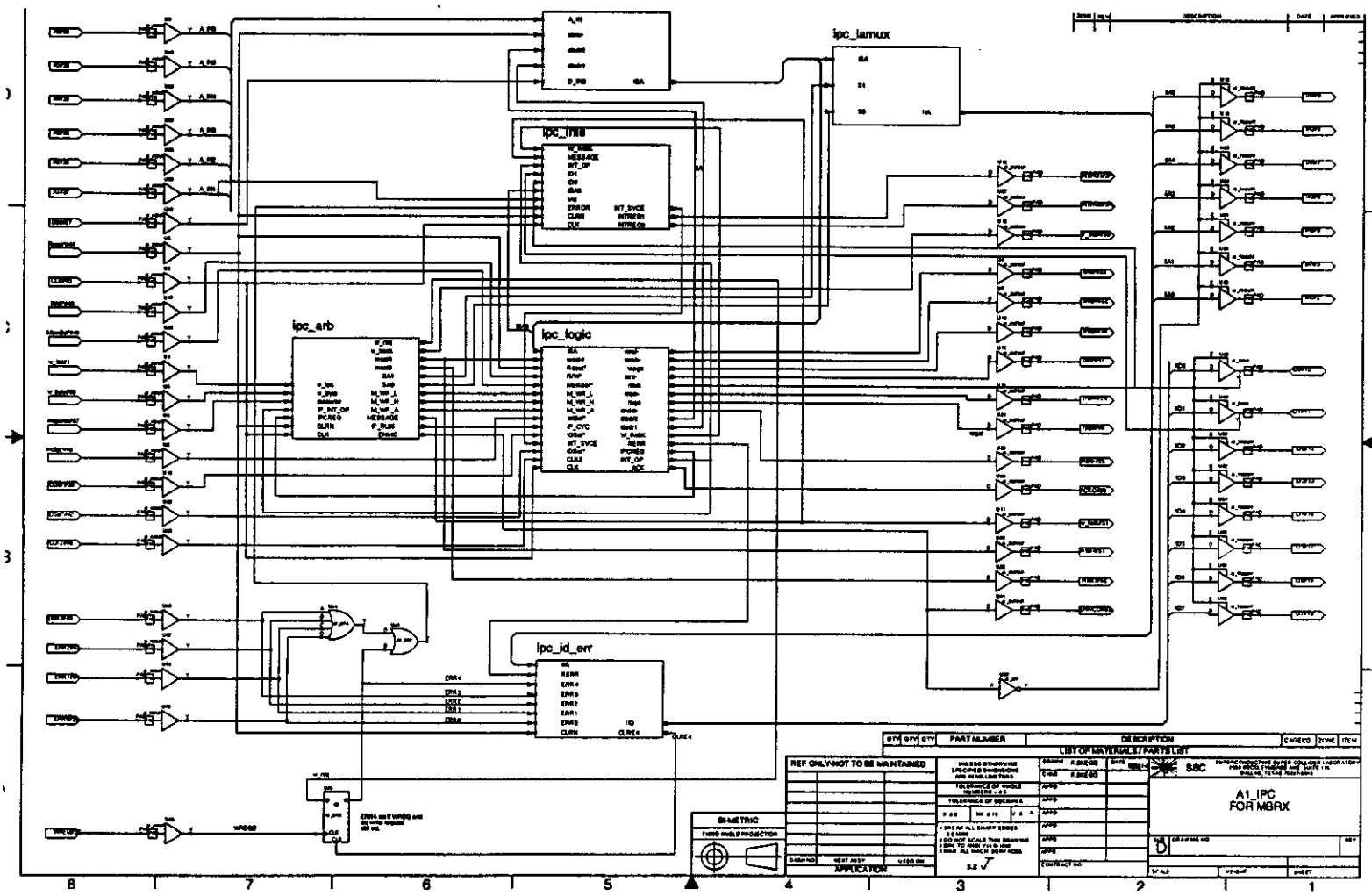
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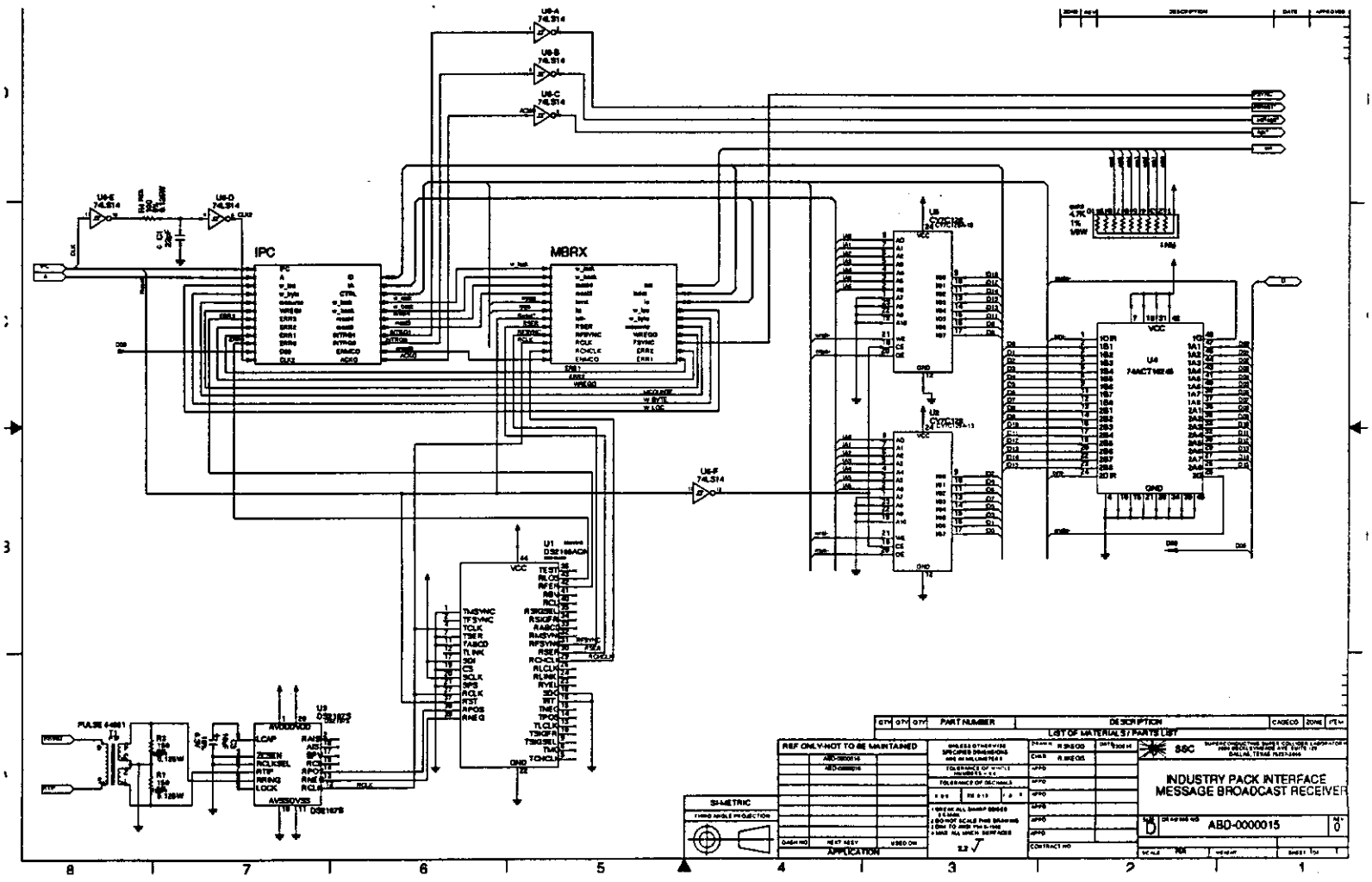
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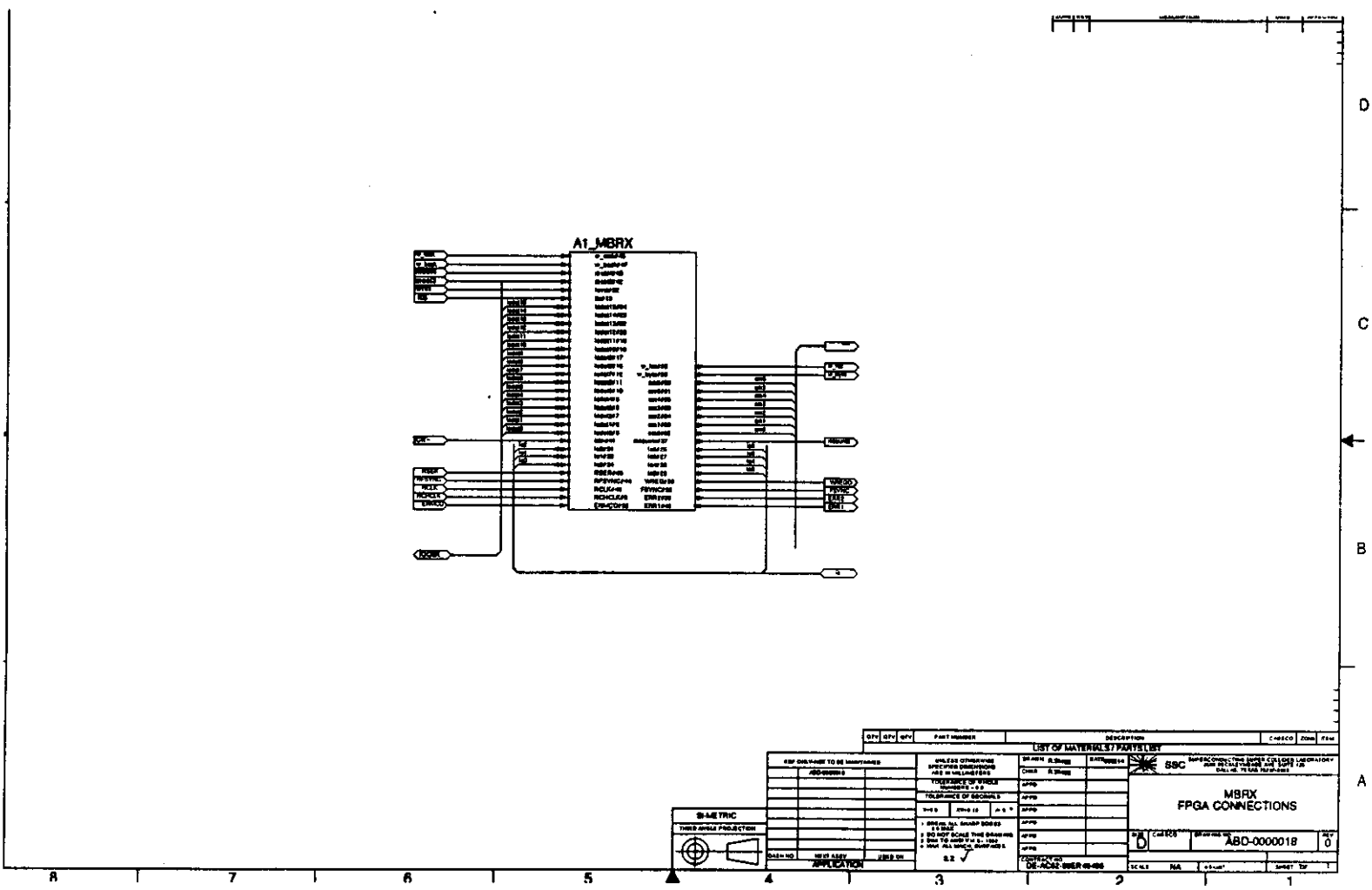
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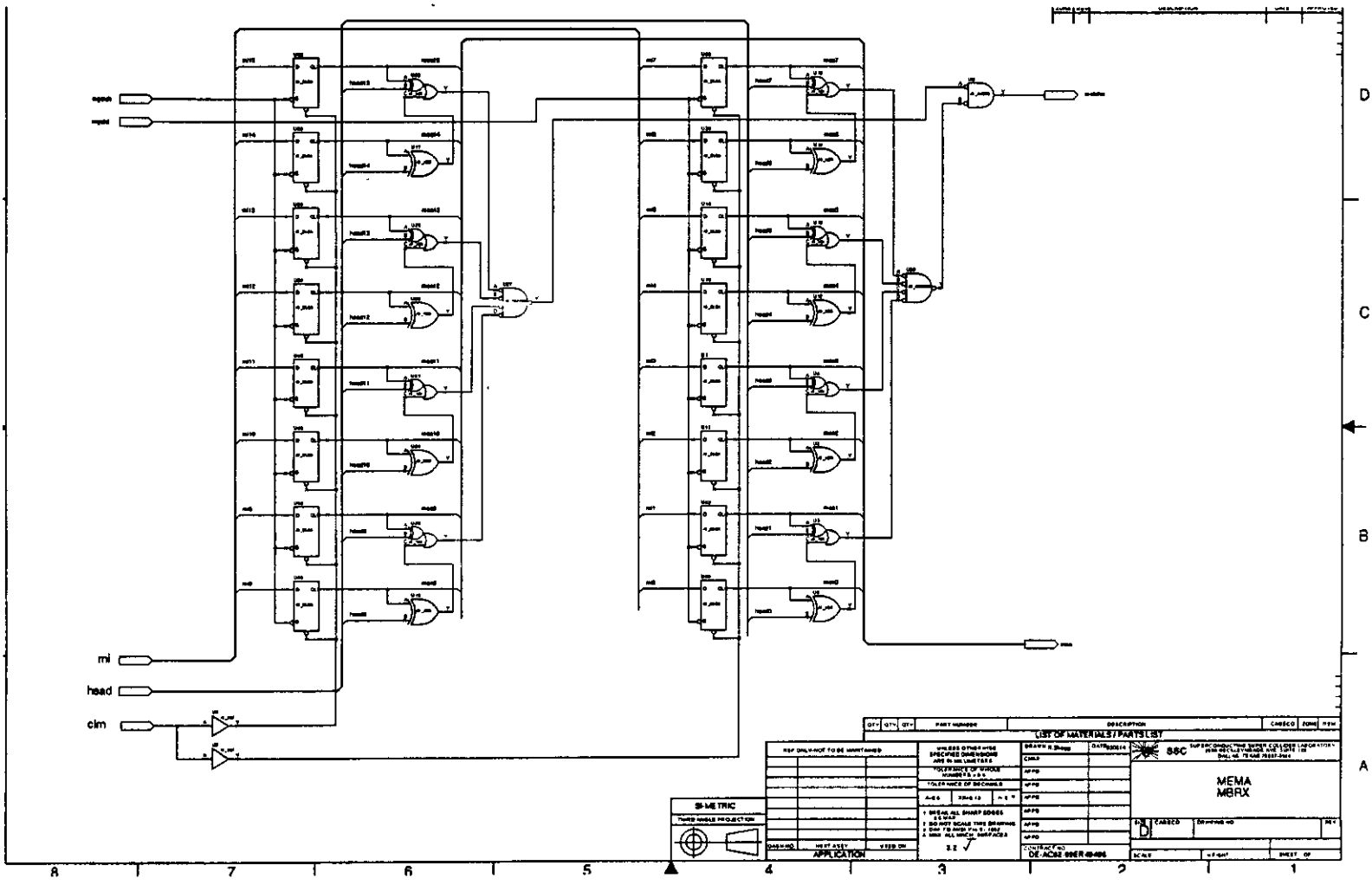

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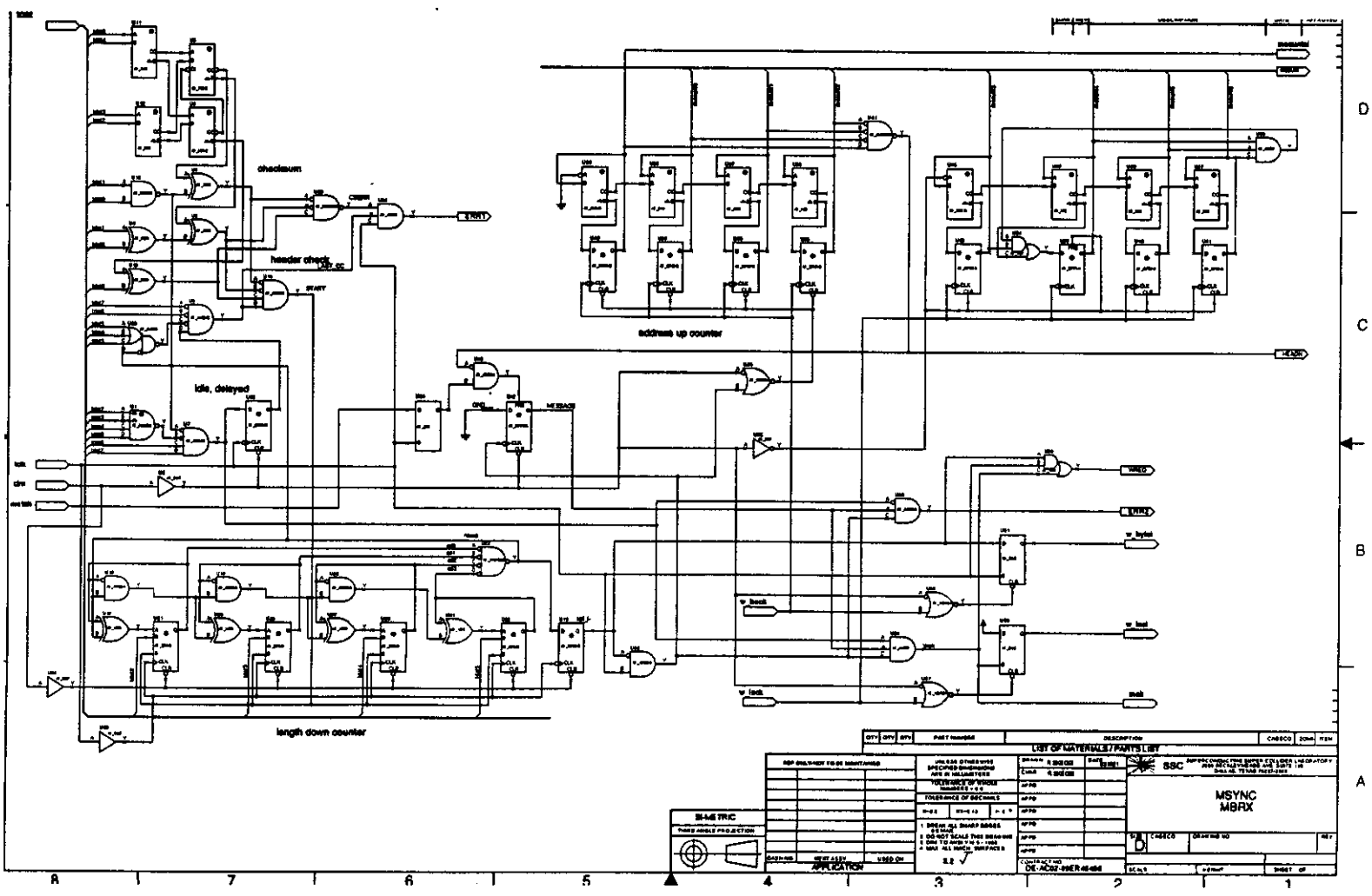
MEMA
MBRX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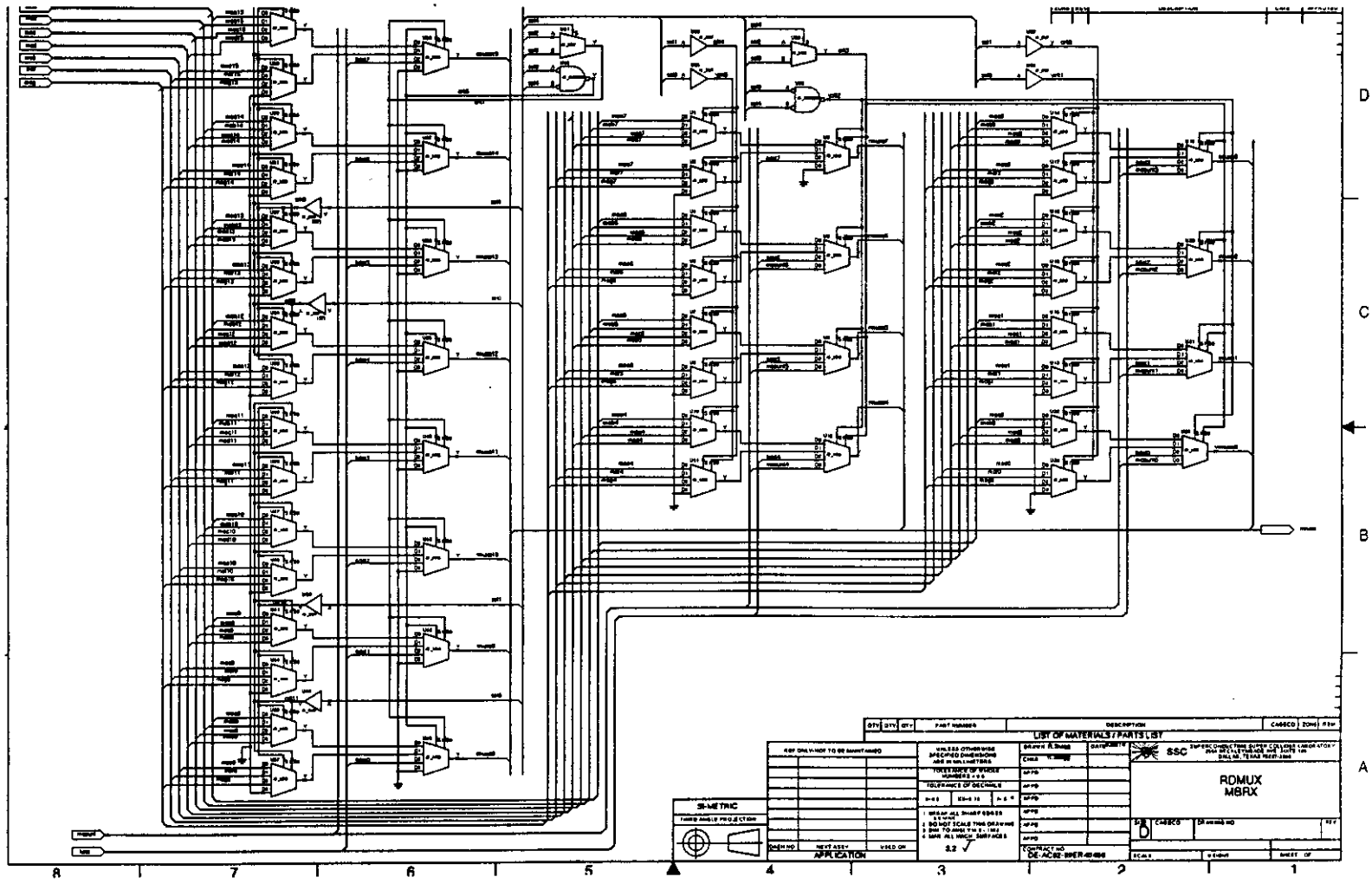
header check
idle, delayed
length down counter
address up counter
MESSAGE
HEADN
w_bytel
w_back
w_lock
w_lost
mak
LIST OF MATERIALS / PARTS LIST
SSC
MSYNC
MBRX
SI-METRIC
APPLICATION
D
C
B
A
8
7
6
5
4
3
2
1



LIST OF MATERIALS / PARTS LIST
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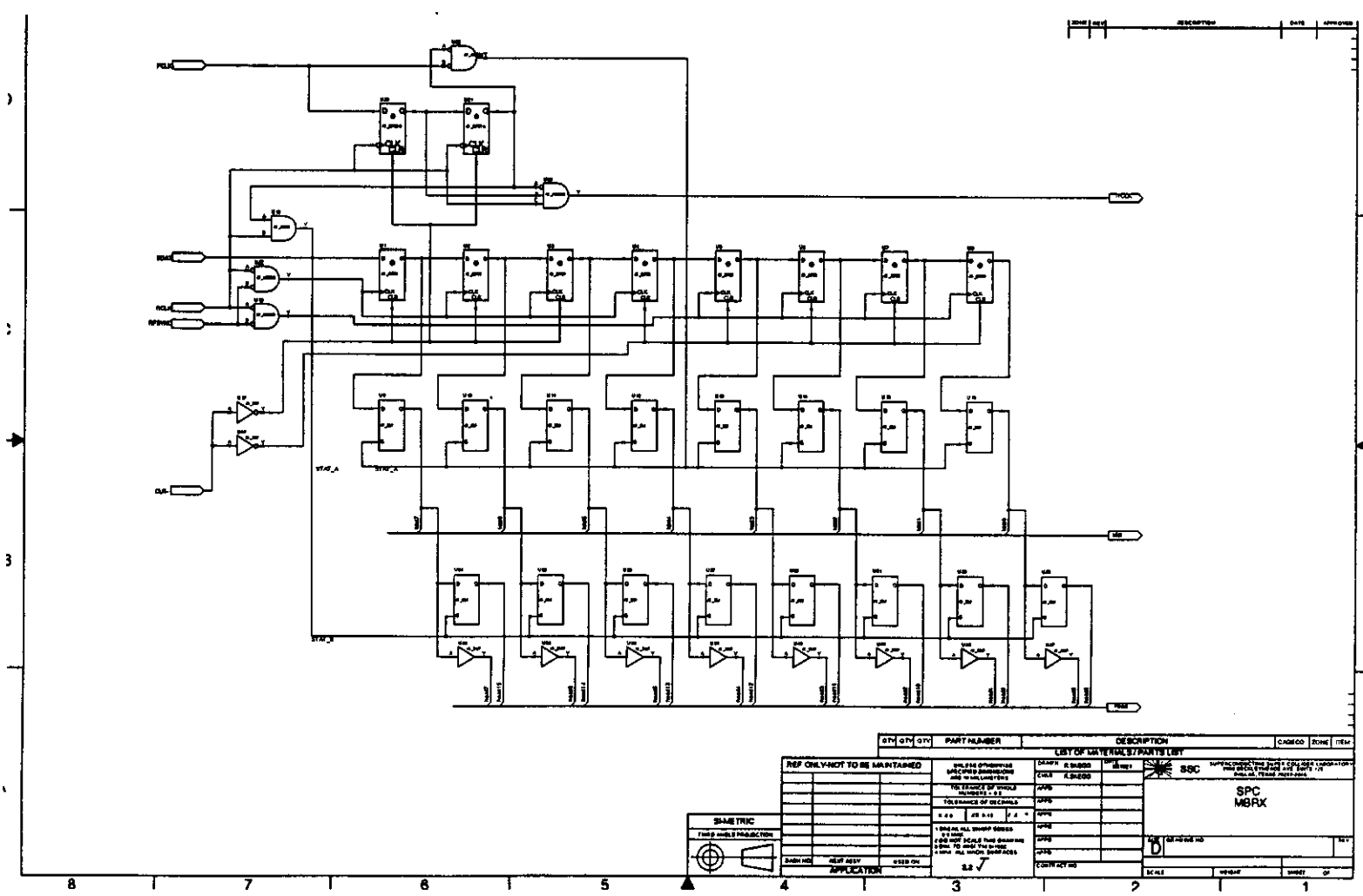
MBRX
D
SI-METRIC
APPLICATION



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QTY
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PART NUMBER
DESCRIPTION
CAGECO
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ITEM
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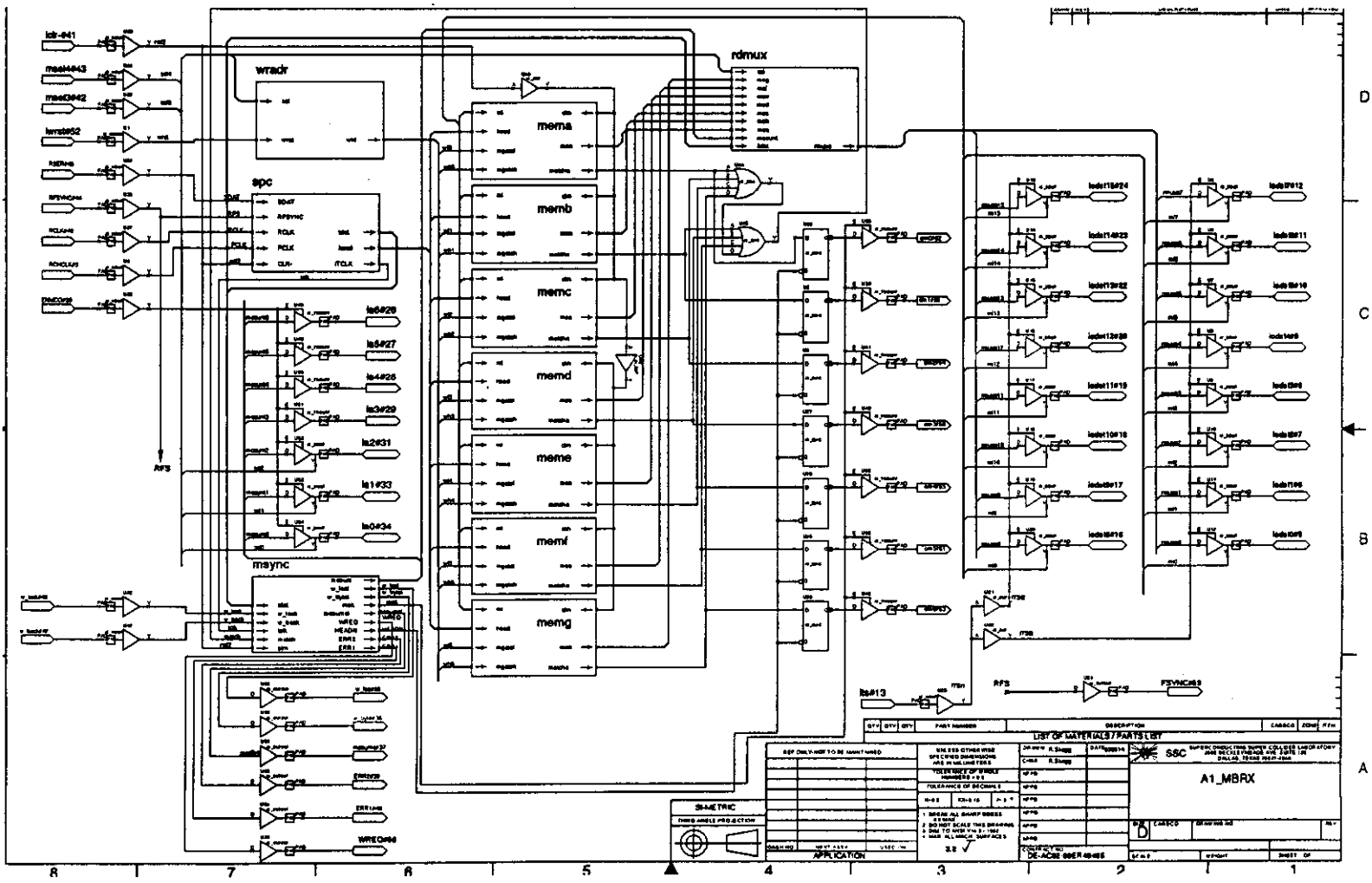
REF ONLY-NOT TO BE MAINTAINED
SSC
SPC
MBRX
D
SI-METRIC
APPLICATION



wradr
spc
msync
rdmux
mema
memb
memc
memd
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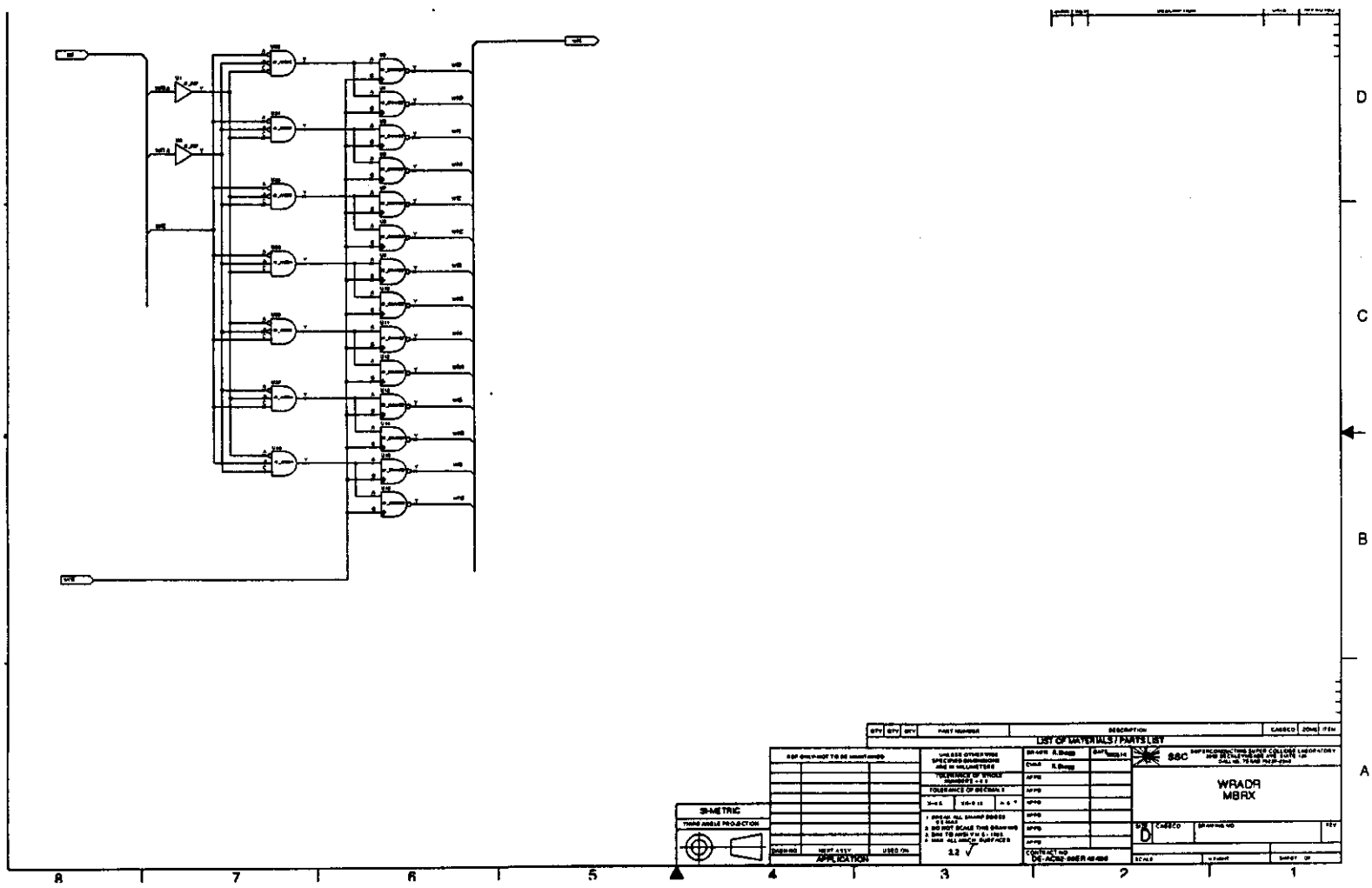
memf
memg
RFS
LIST OF MATERIALS / PARTS LIST
SSC
A1_MBRX
SI-METRIC
APPLICATION



LIST OF MATERIALS / PARTS LIST
SSC
WRADR
MBRX
SI-METRIC
APPLICATION