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CMOS Effective Channel Size Measurements

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Abstract

In general, the effective channel length and channel width of CMOS transistors differ slightly from the design values. This has implications on the characteristics of these devices. This paper presents measurements made of the effective length and width of transistors produced in a UTMC radiation hard process.

1.0 INTRODUCTION

The characteristics of CMOS transistors depend critically on the gate length and gate width of these devices. Length and width are specified at design and layout time. However the effective width of the actual transistors may differ slightly from the specified values. We have measured effective channel length and channel width for a number of n-Channel MOSFET test structures (drop-ins) designed at the Superconducting Super Collider. The drop-ins were designed at the Superconducting Super Collider Laboratory by Guy Vanstraelen. They were produced at UTMC using a radiation hard 1.2 μ process.

2.0 MEASUREMENT METHODS

Several methods exist to determine channel length.* They require a set of transistors that only differ in the length and the width of the gate area. It is possible to separate effects of effective length, width and parasitic series resistance. We used Whitefield's method to measure the effective channel length and checked it using Chern's method. We also successfully applied the same method to measure the effective channel width.

3.0 THRESHOLD VOLTAGE

Whitefield's method involves measurement of the threshold voltage. This is done by measuring the drain current I_D of a transistor operating in the saturation region. In this region the drain current has a square-law dependence.

$$\sqrt{I_D} = \sqrt{\frac{K}{2}}\,(V_{GS} - V_T)\,. \tag{1}$$

Where V_{GS} is the gate to source voltage, V_T is the threshold voltage, $K = \mu_0 C_{ox} W/L$, μo is the carrier mobility, C_{ox} is the gate capacitance per unit area, and W and L are the channel width and length of the device. The bias condition needed for the transistor to operate in saturation is $|V_{DS}| > |V_{GS} - V_T|$. A graphical approach is used to determine V_T. I_{DS} is measured for many values of V_{GS}. An illustration of this approach is shown in Figure 1. A straight line is drawn through the square-law region data and V_T is equal to the x-axis intercept. A numerical technique to determine V_T can be used by applying a linear regression to the data. This technique is more time consuming, but it is more accurate. The difference in these two methods has been reported to be less then 1%.† V_T can also be measured in the linear region, where $|V_{DS}| << |V_{GS} - V_T|$.‡ A straight line fit is made to I_{DS} as a function of V_{GS}. The point where the fitted line crosses the x-axis is $V_{T(LIN)}$. The threshold voltage is determined as:

$$V_T = V_{T(LIN)} - \frac{V_{DS}}{2}\,. \tag{2}$$

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*Colin C. McAndrew and Paul A. Layman, "MOSFET effective channel length, threshold voltage, and series resistance determination by Robust optimization," *IEEE Trans. Elect. Dev.*, Oct. 1992.

†Kwok K. Ng and John R. Brews, "Measuring the effective channel length of MOSFETs," *IEEE Trans. Elect. Dev.*, 1990.

‡Jhon Y. Chen, *CMOS devices and technology for VLSI.*

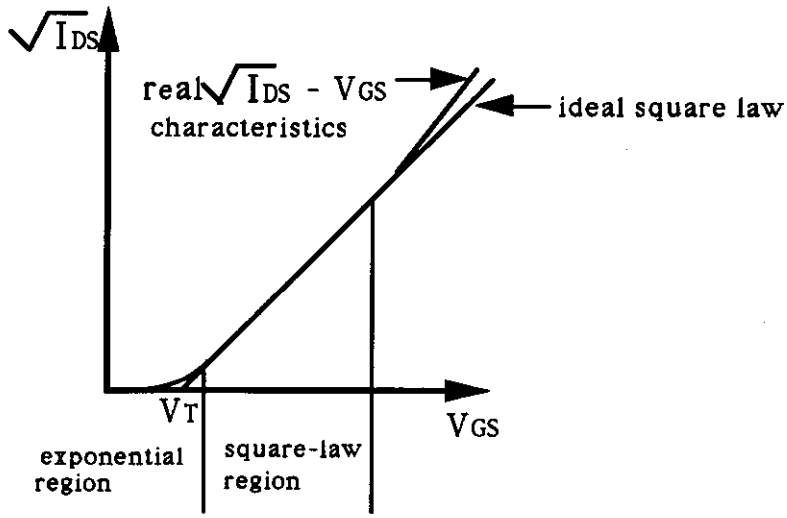

Figure 1. Graphical approach to extract V_T in the saturation region.

4.0 CHANNEL LENGTH

The equation for the channel current in the linear region ($|V_{DS}| << |V_{GS} - V_T|$) is,

$$I_{DS} = \mu_n C_{ox} W/L_{eff} (V_{GS} - V_T) V_{DS}, \tag{3}$$

where L_{eff} is the spacing between the metallurgical junctions of the source and drain. $L_{eff} = L_m - \Delta L$, and L_m is the mask length. The bias voltages seen by the intrinsic device differ from those actually applied. This is caused by the presence of series resistance from the source and drain side of the device, with total resistance $R_T = R_s + R_d$. The parasitic resistance can be included in the channel current Eq. (3) above which gives

$$I_{DS} = \mu_n C_{ox} W/(L_m - \Delta L) (V_{GS} - V_T) (V_{DS} - I_{DS}R_T). \tag{4}$$

For the Whitefield method, the equation used to determine ΔL is derived from Eq. (4). We define two different channel currents I_{DS1} and I_{DS2} for two different lengths L_{m1} and L_{m2}.

$$I_{DS1} = A(V_{DS} - I_{DS1}R_T)/(L_{m1} - \Delta L), \tag{5}$$

$$I_{DS2} = A(V_{DS} - I_{DS2}R_T)/(L_{m2} - \Delta L), \tag{6}$$

where $A = \mu_n C_{ox} W(V_{GS} - V_T)$.

Combination of Eqs. (5) and (6) gives,

$$I_{DS1}/I_{DS2} = (L_{m2} - \Delta L)/(L_{m1} - \Delta L)\ (V_{DS} - I_{DS1}R_T)/(V_{DS} - I_{DS2}R_T)\ . \tag{7}$$

The following parameters are defined:

$$I_{DS1} = V_{DS1}/R_{m1}\ , \tag{8}$$

$$I_{DS2} = V_{DS2}/R_{m2}\ , \tag{9}$$

where

$$V_{DS1} = V_{DS2} = V_{DS}\ . \tag{10}$$

Equations (8), (9), and (10) are substituted into Eq. (7) for I_{DS1}/I_{DS2} and the terms are rearranged.

$$R_{m2} - R_{m1} = (L_{m2} - L_{m1})/(L_{m1} - \Delta L)\ (R_{m1} - R_T)\ . \tag{11}$$

From the plot of $R_{m2} - R_{m1}$ vs. R_{m1}, we determine ΔL. The slope of $R_{m2} - R_{m1}$ is

$$m = (L_{m2} - L_{m1})/(L_{m1} - \Delta L)\ . \tag{12}$$

5.0 CHANNEL WIDTH

We start with the equation for the channel current in the linear region,

$$I_{DS} = \mu_n C_{ox} W_{eff}/L\ (V_{GS} - V_T)\ V_{DS}\ , \tag{13}$$

where $W_{eff} = Wm - \Delta W$ and Wm is the mask width.

$$I_{DS} = \mu_n C_{ox}\ (Wm - \Delta W)/L\ (V_{GS} - V_T)\ (V_{DS} - I_{DS}R_T)\ . \tag{14}$$

Assuming the same conditions as discussed in channel length, we obtain

$$I_{DS1}/I_{DS2} = (W_{m1} - \Delta W)/(W_{m2} - \Delta W)\ (V_{DS} - I_{DS1}R_T)/(V_{DS} - I_{DS2}R_T)\ . \tag{15}$$

By substituting Eqs. (8), (9), and (10) into Eq. (15), the above expression can be reduced to,

$$R_{m2} - R_{m1} = (W_{m1} - W_{m2})/(W_{m2} - \Delta W)\ (R_{m1} - R_T)\ . \tag{16}$$

From the plot $R_{m2} - R_{m1}$ vs. R_{m1}, we determine ΔW. The slope of $R_{m2} - R_{m1}$ is

$$m = (W_{m1} - W_{m2})/(W_{m2} - \Delta W) . \tag{17}$$

6.0 TEST SYSTEM

A HP4145B Semiconductor Parameter Analyzer is used to perform the measurements. It is a programmable test instrument designed to measure, analyze, and graphically display the DC characteristics of semiconductor devices. It simulates voltage and current sensitive devices, measures the resulting current and voltage responses, and displays the results in a user-selectable format on a CRT display. For all the measurements, a long integration time was used to reduce noise.

7.0 TEST RESULTS

To determine ΔL and ΔW, the n-channel device was configured as follows: In each case the drain voltage $V_{DS} = 1.5V$, the source and body were grounded and the gate voltage V_{GS} was swept from 0 to 4 volts in 0.5V increments. This bias condition operates the MOSFET in linear region. The drain current I_{DS} was measured for different channel lengths L while the width W was kept constant as shown in Table 1.

TABLE 1. DRAIN-SOURCE CURRENT, I_{DS}, FOR TEST STRUCTURES WITH DIFFERENT LENGTHS (W = 20 μm).

V_{GS} (V)	L = 1.2 μm (μA)	L = 1.4 μm (μA)	L = 1.7 μm (μA)	L = 3.0 μm (μA)	L = 5.0 μm (μA)
1.5	146.3	121.9	91.74	47.31	27.17
2.0	481.6	409.6	316.2	164.9	94.61
2.5	956.0	829.6	659.6	355.7	206.1
3.0	1507	1328	1082	606.4	357.0
3.5	2006	1782	1471	834.9	483.1
4.0	2348	2089	1723	955.3	511.0

From Table 1 we calculate the resistance $Rm = V_{DS}/I_{DS}$ for different channel lengths. Figure 2 shows a plot of $R_{m2} - R_{m1}$ vs. R_{m1} for channel lengths $L_{m1} = 3$ μm, and $L_{m2} = 5$ μm. From the slope $(L_{m2} - L_{m1})/(L_{m1} - \Delta L)$, ΔL is 0.3 μm. Other channel lengths combinations used are L = 1.2 μm & L = 1.4 μm, and L = 1.7 μm & L = 3.0 μm. The average value of ΔL for the three combinations is 0.29 μm.

Table 2 gives drain current for different channel widths. We calculate the resistances Rm, and plot $Rm_2 - Rm_1$ vs. Rm_1 for different channel widths combinations. Figure 3 shows the plot for channel width W = 4.5 μm & W = 6.0 μm combination. The slope of Figure 3 is 0.26, and ΔW is 0.23 μm. Other combinations used in determining ΔW are W = 3.6 μm & W = 6.0 μm, and W = 6.0 μm & W = 20.0 μm. The average value of ΔW for the given three combinations turns out to be 0.22 μm.

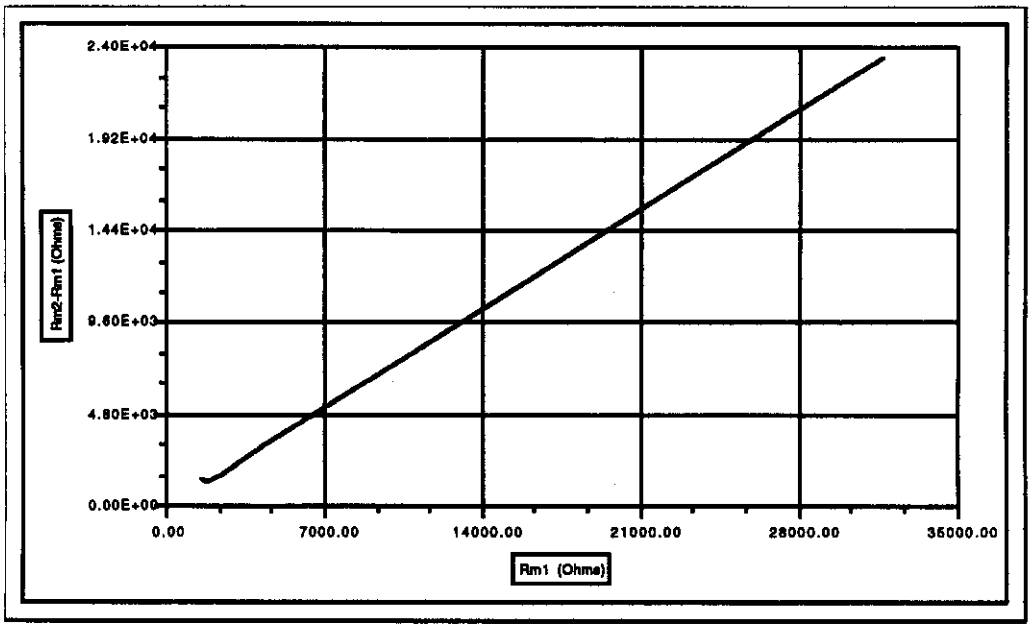

Figure 2. $R_{m2} - R_{m1}$ vs. R_{m1} for channel lengths $L_{m1} = 3\ \mu m$ and $Lm2 = 5\ \mu m$. The slope determines ΔL.

TABLE 2. DRAIN CURRENT FOR TEST STRUCTURES WITH DIFFERENT WIDTHS (L = 10 μm).

V_{GS} (V)	W = 3.6 μm (μA)	W = 4.5 μm (μA)	W = 5.0 μm (μA)	W = 6.0 μm (μA)	W = 20.0 μm (μA)
1.5	5.256	6.554	6.798	8.833	29.63
2.0	13.88	17.32	17.85	23.33	78.45
2.5	26.72	33.34	34.14	44.85	150.6
3.0	41.42	52.05	53.58	70.65	241.4
3.5	57.13	72.10	74.30	98.28	337.6
4.0	71.95	91.11	93.71	124.6	430.0

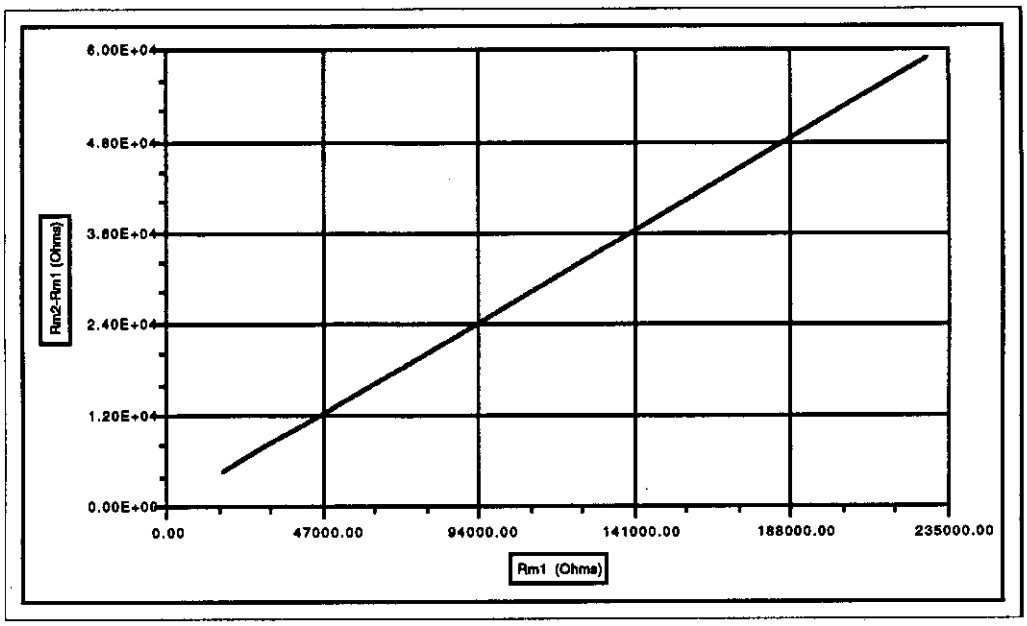

Figure 3. Rm2 – Rm1 vs. Rm1 for channel widths of 4.5 and 6.0 μm.

8.0 CONCLUSION

The values found for ΔL and ΔW, 0.3 μm and 0.2 μm, are well within the expected range. From the value of ΔL and ΔW, L_{eff} and W_{eff} can be calculated. This study provides us with the information how much the effective channel length and width differ from the designed values in the UTMC radiation hard process.